MICROWAVE CIRCUIT DESIGN USING LINEAR AND NONLINEAR TECHNIQUES

Second Edition

GEORGE D. VENDELIN
Vendelin Engineering

ANTHONY M. PAVIO
Rockwell Collins Phoenix Design Center

ULRICH L. ROHDE
Synergy Microwave Corporation

WILEY-INTERSCIENCE

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FOREWORD

Fifteen years have passed since I was asked to write the Foreword to the first edition of this book. Much has happened since that time in the fields of application addressed by this edition. For example, the design and technology of integrated microwave circuits (MMICs) have matured for both military applications and commercial applications such as found in communication systems. Wireless technology is now in full bloom. Silicon technology for active devices is complemented by gallium arsenide, SiGe, and MOS technologies for the microwave bands. Solid-state active devices are routinely being manufactured for higher power and frequency applications and for lower noise performance.

This second edition, a vastly expanded and revised version of the first edition, provides the engineer with the necessary additional data and design tools to best enable him or her to address the new requirements introduced by these technological developments. Five new chapters have added for this purpose.

The book begins with an introductory review chapter entitled "RF and Microwave Systems." It covers a variety of topics ranging from Maxwell's equations to RF wireless/microwave/millimeter-wave applications, analog and digital requirements, basic RF transmitters and receivers, and CAD for nonlinear circuit analysis, among others.

The next chapter, "Lumped and Distributed Elements" pertains to the frequency range from the RF band up through the millimeter bands. Over this huge frequency expanse, circuit elements exhibit a continuous transition in circuit behavior from that of lumped elements to that of distributed components. Understanding this behavior is of particular importance in broadband designs.

The third chapter, "Active Devices," is by far the largest chapter in the book. It covers in considerable detail all essential active microwave devices including diodes, bipolar transistors, field-effect transistors (FETs) and their variants such as MOSFETS and HEMTs. The small- and large-signal properties, modeling, and applications of these devices are addressed. More than 200 device-related equations are presented,

presumably enough to meet the needs of any designer. Also a subchapter on foundry requirements has been added.

It is safe to say that most applications of active devices consist of networks of two or more ports and their interconnections. Chapter 4, "Two-Port Networks," presents the tools needed for RF/microwave design based on two-port networks and, in addition, three- and four-port networks. Four-port parameters, for example, are necessary for the design and characterization of differential circuits that are common to communication circuits. Design considerations for power and current/voltage gain amplifiers, and their stability and noise performance also are addressed. Numerous examples are presented to demonstrate the utility of multiport parameters.

The next chapter entitled "Impedance Matching" complements Chapter 4 and follows, more or less, the traditional approach to impedance matching involving both lumped and distributed elements. Both analytic and graphical (Smith Chart) methods are illustrated. Many examples are chosen to illustrate the matching techniques.

Chapter 6, "Microwave Filters," is a welcome addition to the this text. Filters are crucial components of nearly every microwave system, whether it is a radar system or a cell phone transmitter. Much has been written about filter design in the literature harking back over nearly a century. Filters now are designed by a variety of methods ranging from the purely classical analytic approach, such as the Butterworth method, to techniques based on element optimization by computers. This chapter exploits the former approach. Low-pass, band-pass, and high-pass filter designs based on the Butterworth and Chebyshev response are described as are the Richards and Kuroda Transformations for transmission line filters. Numerous examples are used to illustrate these analytic approaches.

The next chapter addresses noise in linear two-ports and is a vastly enhanced version of the corresponding chapter in the first edition. One of the new features is a detailed treatment of the noise correlation matrix approach to noise analysis. This technique is particularly suited to computerization since noise matrices can be treated like two-port signal matrices, and can be intermixed with the latter. The noise matrix approach is a general scheme applicable to both linear passive and active devices. Examples of application to bipolar and field-effect transistors are included. An exhaustive set of equations is presented which should fulfill the needs of most designers.

Chapters 8 and 9, entitled "Small and Large-Signal Amplifier Design," and "Power Amplifier Design," respectively reflect the important advancements made in the wireless industry, both in circuit design and in circuit integration based on planar solid-state technology.

The next chapter on oscillators is a complete rewrite and expansion of the corresponding chapter in the previous edition. The most recent frequency and time domain analytic techniques have been applied. Strong emphasis is given to power optimization and noise analysis. To complement this chapter, an extensive bibliography of more than 180 references has been included.

Chapter 11, "Microwave Mixer Design" also has been broadened and now has a new subchapter that deals with the mathematics of mixer noise for two types of FETs. Also the use of CAD in mixer design is illustrated. The bibliography has been extended to reflect these additions.

Chapter 12 is a new chapter covering pin diodes and switches and attenuators based on them. FET switches also are covered. The final chapter on microwave CAD is essentially identical to the last chapter of the previous edition.

My objective has been to describe the salient features of this second edition. However, only a personal examination of the book will convey to the reader the broad scope of its coverage and how well it succeeds in addressing the changing needs of the microwave field and the communications industry.

The authors are to be commended for their efforts in this endeavor. This volume will be an asset to the designer's bookshelf.

ROBERT A. PUCEL, SC. D.
RCP Consultants

April, 2005

PREFACE

Approximately 15 years have passed since the first edition of this book, which was well received by both graduate schools and industry. While the basic principles of physics and mathematics have not changed, today's technology has provided us with huge opportunities to improve the circuit design for linear and nonlinear techniques. In addition, we felt it would be useful to streamline the book by following the concepts of systems and their requirements at microwave frequencies, showing the transition between lumped and distributed elements, and the new exciting devices, particularly the silicon-germanium transistors and the low-cost BiCMOS technology, which is competing heavily with gallium arsenide and seems to be winning in many wireless applications. The cutoff frequencies for modern transistors are in excess of 200 GHz, with low noise figures and low-voltage operation. Practical oscillators can now be made up to 70 GHz. For higher power applications gallium arsenide FETs are over 100 W, and LDMOS devices are also available for frequencies up to 3 GHz. The future looks very bright for lower noise, higher power, and higher frequencies as the technology continues to improve at a very rapid pace.

In streamlining the book, we now offer a separate chapter on two-port networks and all of their characteristics followed by two new chapters, one on matching networks and an extensive one on RF microwave filters, including silicon-based filters for cellular telephone applications.

The noise in the linear two-ports chapter has been extended by showing temperature-dependent noise and detailed derivations of noise figure for both bipolar and FETs. The small-signal amplifier and power amplifier chapters have incorporated the latest designs and circuit choices, including linearization.

The oscillator chapter has been extended to include BiCMOS and SiGe HBT oscillators suitable for high integration, and modern noise reduction circuits have been added. Also, time-domain analysis for startup conditions have been incorporated. The microwave mixer section has been extended with a wealth of new designs.

Consistent with the industry's needs, there is also a new chapter on RF switches and attenuators. As in the first edition, we close the book looking at and using modern

design software, realizing this field constantly changes by offering better and faster software tools, although the basic capabilities remain the same.

Most of the software tools in this book came from Ansoft. There are three student versions downloadable from their website. Other companies may also provide demonstration versions free of charge.

Of course, there have been numerous contributions by many people to this work, which took much longer than expected. Engineers from Synergy Microwave and Motorola have contributed generously. Professors from all over the world have given input, including Tim Healy, Robert Owens (who also wrote Chapter 6 on filters), Allen Sweet, and Martin Grace of Santa Clara University; G. R. Branner of UC Davis; Tom H. Lee of Stanford University; Ali Niknejad and Robert Broderson of UC Berkeley; Jose Carlos Pedro of University of Aveiro (Portugal); and Steve Long of University of California Santa Barbara (UCSB). Important inputs from industry were provided by Klaus Aufinger of Siemens (Germany); Steve Kovacic of SiGe (Canada); Rene Douville of CRC (Canada); Dipak Patel of Philips; Kirk Laursen of Oepic; Mike Zybura of RFMD; Jim Cochrane of Infineon; Jon Martens of Anritsu; Karl Niclas of Watkins Johnson; Paul Khanna of Agilent/Celeritek; Li-Wu Yang and Tanhua Wu of RFIC; Greg Zhou of MWT; Edison Fong of Motorola; Harpreet Randhawa and Pat Tesera of Ansoft; Peter Sturzu (consultant); Mike Bailey of Filtronics; Larry Dunleavy and Tom Weller of Modelithics; Al Ward, Biniam Ayele, and Rich Ruby of Agilent; and finally Ken Kawakami of Avnet (who wrote Appendix E). Several students assisted in putting the book and solution manual in final form, including Chi-Chung (Calvin) Chien, Hu-Sun (Luke) Huang, and Francisco Madriz.

The 13 chapters were written as follows: Vendelin—Chapters 1, 2, 4, 5, 6 (Owens), 8, and Appendices D and E (Kawakami); Pavio—Chapters 9, 11, and 12; Rohde—Chapters 3, 7, 10, Section 11.10, 13, and Appendices A, B, C, and F.

As always, Wiley has been a joy to work with through the leadership, patience, and understanding of George Telecki. Coordinating the efforts of three IEEE Fellows is a monumental task, fitting to the scope of this second edition.

Finally, we would like to thank Dr. Robert A. Pucel, one of the greatest pioneers in microwave circuit design and a good friend to have. He thoroughly reviewed both the first edition of this book and now 15 years later the second edition.

<div align="right">

GEORGE D. VENDELIN
ANTHONY M. PAVIO
ULRICH L. ROHDE

</div>

Saratoga, California
Phoenix, Arizona
Paterson, New Jersey
April, 2005

CHAPTER 1

RF/MICROWAVE SYSTEMS

1.1 INTRODUCTION

This book is similar to many well-known texts in the field [1.1–1.12]; they all have a different slant on the same engineering topics, that is, radio-frequency (RF) and microwave circuit design, from an intuitive and engineering point of view. This book was first written in 1982 [1.13] using only linear techniques, which is out of print, and was later augmented in 1990 [1.14] including both linear and nonlinear techniques. This second edition is an attempt to update the technology to include all of the very latest engineering tools, particularly the best of modern microwave computer-aided design (CAD), which is always in a state of rapid advancement.

The audience is both graduate students of RF/microwave courses and practicing engineers in this industry. We expect you have already mastered the fundamentals (component definitions for amplifiers, oscillators, and mixers; two-port network theory; power gains; Smith chart matching; direct current (dc) biasing; etc.), but these are also included in the text for careful review. Prior to using the CAD tools, the practicing engineer should be able to do general RF/microwave problems with a calculator and Smith chart. The CAD software is only a check on the engineer's design and in some cases an enhancement to the basic design. This entire process is only as good as the nonlinear models provided by the device manufacturers, which is a work in progress that improves every year.

This textbook is used in a four-quarter graduate sequence taught at Santa Clara University by one of the authors:

Fall: Fundamental Design—no CAD, Active Microwave Devices I (ELEN 711)

Winter: Linear Design (*S* Parameters with CAD), Active Microwave Devices II (ELEN 712)

Spring: Nonlinear Design (ELEN 714)

Summer: Advanced Nonlinear Design (ELEN 719)

This is often followed by thesis units, publications, papers, Ph.D. programs, and so on. The emphasis is always on understanding why CAD is working so well when the engineer understands the basic principles of circuit design with accurate nonlinear models. An excellent example of this will be shown in Chapter 8, where lossless feedback amplifiers are discussed, which was an extra credit problem in the spring quarter of 2002.

A book of this magnitude must begin with a brief history of the nineteenth- and twentieth-century communications achievements, which are tabulated in Table 1.1 [1.15]. While key scientific events occurred over a century ago, the present digital wireless era was demonstrated in 1962 and introduced commercially in 1988.

From a solid-state device perspective, the key events were the inventions of the bipolar junction transistor (BJT) and GaAs MESFET, which are even today the heart of electronics. The Ge BJT was quickly replaced by the Si BJT due to temperature considerations and the discovery of SiO_2 (the planar process). Bell Labs accidentally discovered the Ge BJT while attempting to build a variable resistor, or field-effect transistor (FET).

The first solid-state X-band radar was developed by Texas Instruments during the period 1966 to 1970 under contract to Wright Patterson Air Force Base [1.16]. This

TABLE 1.1   Historical Events in Communications

Event	Names	Year
Maxwell's equations	James Clerk Maxwell	1873
Invention of telephone	Alexander Graham Bell	1876
Validation of Maxwell's theory	Heinrich Hertz	1891
Transatlantic communications	Guglielmo Marconi	1901
Galena (lead sulfide) detector	J. C. Bose	1901 (Patent filed)
Superheterodyne receiver	Edwin H. Armstrong	1917
X-band radar	MIT Radiation Labs	1942
Invention of transistor	John Bardeen, William Brittain, and William Shockley, Bell Labs	1947
Digital voice transmission	ATT	1962
Invention of GaAs metal−semiconductor field-effect transistor (MESFET)	C.A. Mead Cal Tech	1965
First solid-state X-band radar	Texas Instruments	1970
First GaAs MESFETs in satellites	SPAR/CRC	1975
Analog cellular radio	ATT/Motorola	1983
Digital cellular radio	ATT	1988
Digital personal communication service (PCS) radio code division multiple access (GSM/CDMA)	Europe/Qualcomm	1993
WCDMA (wide-band CDMA) 4G CDMA Networks	Mobile Internet	2000

contract, which was called the MERA program (Microwave Electronics Radar Applications), revolutionized microwave engineering, providing new insights into the use of hybrid microwave integrated circuit (MIC) construction using microstrip transmission lines on alumina, after determining silicon would never succeed in this role. This is a phased array antenna which is pointed by the phase shifters preceding the 1-W transmitters, 640 of them. This was replaced in the 1990s by GaAs MESFET modules by Raytheon and Texas Instruments for the BMDO [Ballistic Missile Defense Operation for ground-based radar (GBR)] when 60,000 units were shipped about 1996 [1.17].

The first introduction of GaAs MESFETs into space deserves some comments. At this point in time (1973), two major companies were producing devices with about 2 μm gate lengths, Fairchild and Plessey, at a price of about $500 each. A satellite was about to be launched in 1975 by SPAR, which hired Communications Research Center CRC (Canada), which selected the new MESFETs from both suppliers, to design the low-noise amplifier (LNA). The first purchase of space-qualified GaAs MESFETs was 23 devices for $40,000 from Fairchild. These were all burned out in 2 months due largely to electro static discharge (ESD) problems, so they purchased an entire wafer next. To shorten the story, which is documented in Refs. 1.18 and 1.19, both suppliers provided transistors for five- or six-stage amplifiers (see Fig. 1.1) with 26 dB gain and 10 dB noise figure at 12 GHz [300 MHz bandwidth (BW)], and two satellites were launched in 1975; the project was a complete success, with a lifetime of about 3 years [1.20] for the Plessey amplifier; the Fairchild amplifier never turned on due to switching problems in the satellite. The circuits were made on 25-mil polished alumina with TiW/Au metal 6 μm thick. The resistance of the TiW was 50 Ω/square. Some photographs of these amplifiers, which were used in the world's first direct broadcast TV satellite, which was launched in Australia in late 1975, are shown in Figure 1.1.

Turning to cellular telephone, analog cellular systems introduced in 1984 are commonly referred to as first-generation systems. The digital systems currently in use, such as GSM, personal digital cellular (PDC), CDMAOne (IS-95), and US_TDMA (IS-136), are second-generation systems. These systems serve both voice communications and other services such as text messaging and access to data networks. Third-generation systems are designed for multimedia communication: With these person-to-person communication can be enhanced with high-quality images and video, and access to information and services on public and private networks will be enhanced by the higher data rates and new flexible communication capabilities of third-generation systems. WCDMA technology has emerged as the most widely adopted third-generation air interface. Its specification has been created in 3GPP (the Third Generation Partnership Project). Within 3GPP, WCDMA is called UTRA (Universal Terrestrial Radio Access), FDD (Frequency Division Duplex), and TDD (Time Division Duplex). The differences between WCDMA FDD and WCDMA TDD are explained in 1.21.

Consumer surveys have shown that extra features added to cell phones are secondary while voice performance and cost are primary. Secondary features include video, digital pictures, Internet browsing, and so on, which obviously add to the cost. Customers want "Zero-G," which could be defined as voice only, with minimum cost. Forget the bells and whistles; it is voice only, nothing else is of any interest to the average consumer at the time of this writing. New revolutions in cellular telephone are needed to bring the cost down, and these are in progress.

Another way of expressing the present state of complementary metal–oxide–semiconductor (CMOS) technology is the cost of a 40 × 40-mm silicon chip in
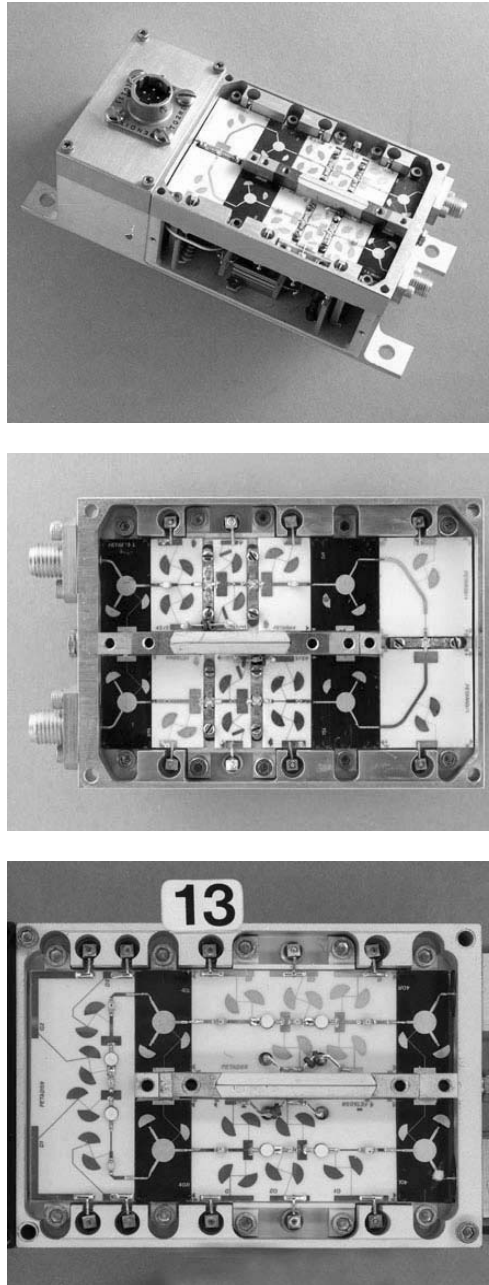
FIGURE 1.1 First GaAs MESFET amplifiers for 12-GHz satellite application for direct broadcast TV. (Courtesy of Rene Douville [1.18–1.20].)

high-volume production: 10 cents, insignificant for the RF portion. When the cellular RF analog transceiver has been reduced to this small size, the digital content, case, and antenna will become the virtual cost of the mobile telephone, which will be hopefully within the reach of most of the world.

Of course, there is also a great deal of RF/microwave engineering going on today for the entertainment industry, largely digital TV, the next consumer product. The integration of analog and digital functions on the same silicon chip is expected to significantly reduce costs for all consumer products.

Almost 100 years ago the simplest radio receiver was the crystal radio receiver shown in Figure 1.2, which uses no battery. The diode (or crystal) demodulates the amplitude-modulated (AM) carrier to excite the headphones into sound. This circuit is also called "the foxhole radio" because of its use during World War II. In this case the components were the antenna (a length of wire), the LC tank, the detector, which was made from pencil lead touching a Gillette razor blade, and a headphone set. The capacitor of 1000 pF in parallel with the headphones is an RF ground for the carrier frequency. The headphones detect the envelope of the received signal, which is the desired information. This type of receiver is the simplest of all, and there are numerous web sites which can sell you one for your evaluation.

A similar invention which also uses no battery is the telephone [1.22]. The detector is a diaphragm which transmits sound to the human ear drum, which has a threshold sensitivity of one hydrogen atom displacement [1.23], where the frequency is roughly 5 kHz.

The frequency spectrum of a receiver is shown in Figure 1.3, where the image signal may also produce an unwanted IF output, so the image should be filtered. The image signal is the mirror image of the desired RF signal.

The radio is a tuned resonant tank circuit at the carrier frequency, which maximizes the input voltage to the heterodyne receiver shown in Figure 1.4. The incoming signal is converted to a lower intermediate frequency (IF) by the local oscillator (LO), where the pertinent mathematics is

$$\cos \alpha \cos \beta = 0.5 \cos(\alpha - \beta) + 0.5 \cos(\alpha + \beta)$$
$$= 0.5 \cos(\omega_{IF} t) + 0.5 \cos(\omega_{RF} t + \omega_{LO} t) \tag{1.1}$$
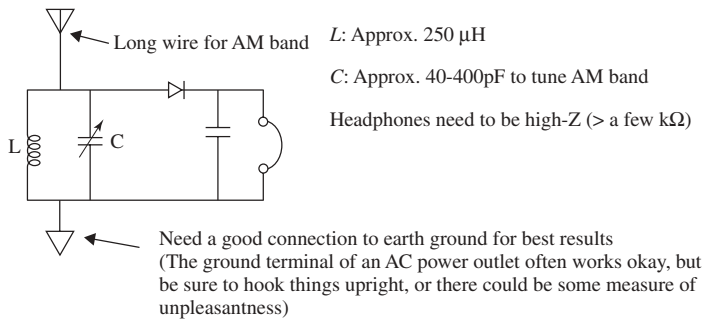
FIGURE 1.2 Crystal radio receiver or Foxhole Radio [1.12].
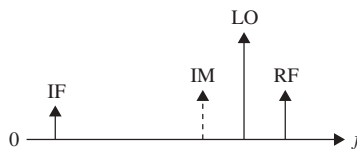
FIGURE 1.3 Frequency spectrum of radio receiver.

(*a*) Heterodyne receiver, if $f_{LO} = f_{RF}$, homodyne or direct-conversion receiver

(*b*) Superheterodyne receiver
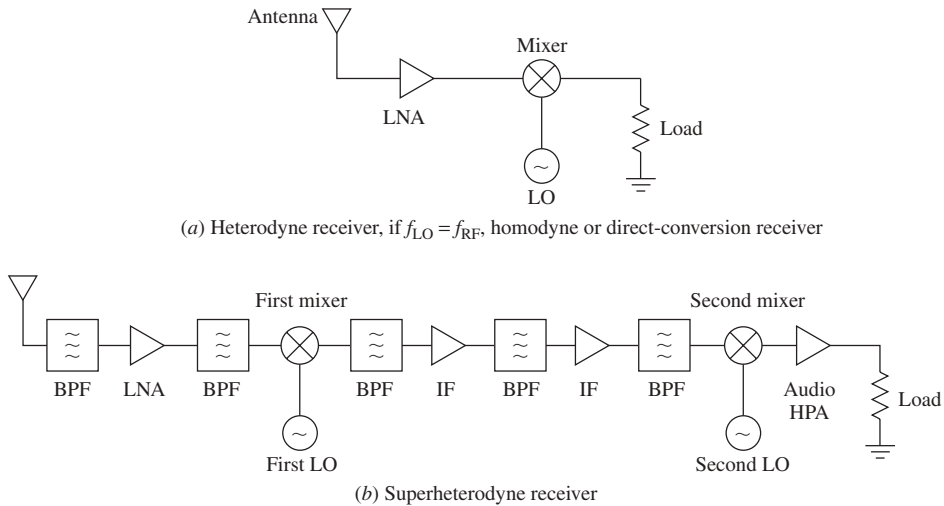
FIGURE 1.4   Heterodyne receiver, single-conversion superheterodyne receiver, double-conversion superheterodyne receiver [1.26].

where α and β are the RF and LO frequencies. The frequency spectrum is shown in Figure 1.3, where the image signal may also produce an unwanted IF output, so the image should be filtered. The image signal is the mirror image of the desired RF signal.

The basic heterodyne receiver invented by Armstrong in 1917 is given in Figure 1.4. The modulated carrier is amplified, converted to an IF, demodulated, and amplified at baseband (audio). This gives a single tuning control (the LO) and allows high gain and selectivity at the IF. A superheterodyne receiver has two (or more) mixers, so the frequency is converted once or twice to a lower frequency. Most of the gain is done at the first or second IF, where the cost is generally lower.

Most electrical engineers have worked in various aspects of RF or microwave design. This book is addressed to the designers of these circuits. The circuits are organized into three frequency ranges:

RF	1 MHz (or less) to 1 GHz
Microwave	1–30 GHz
Millimeter wave	30–300 GHz (or higher)

The word *wireless* was used by Marconi in 1901, and it reoccurred as a replacement for the word *radio* in about 1991. The design techniques tend to be different for these three groups, but there are many similarities. A single CAD package such as Ansoft Design Suite (which is provided in the jacket of this book), Agilent ADS (Advanced Design System), or Advanced Wave Research (AWR) Microwave Office (MWO) may be used for all three groups.

Another summary of wireless applications is given in Table 1.2 [1.24]. These applications include all three frequency groups as well as communications, radar, navigation, remote sensing, RF identification, broadcasting, automobiles and highways, sensors, surveillance, medical, and astronomy and space exploration.

TABLE 1.2   Wireless Applications [1.24]

1. *Wireless communications*: space, long-distance, cordless phones, cellular telephones, mobile, PCS, local-area networks (LANs), aircraft, marine, citizen's band (CB) radio, vehicle, satellite, global, etc.
2. *Radar (standing for radio detection and ranging)*: airborne, marine, vehicle, collision avoidance, weather, imaging, air defense, traffic control, police, intrusion detection, weapon guidance, surveillance, etc.
3. *Navigation*: microwave landing system (MLS), global positioning system (GPS), beacon, terrain avoidance, imaging radar, collision avoidance, auto-pilot, aircraft, marine, vehicle, etc.
4. *Remote sensing*: Earth monitoring, meteorology, pollution monitoring, forest, soil moisture, vegetation, agriculture, fisheries, mining, desert, ocean, land surface, clouds, precipitation, wind, flood, snow, iceberg, urban growth, aviation and marine traffic, surveillance, etc.
5. *RF identification*: security, antitheft, access control, product tracking, inventory control, keyless entry, animal tracking, toll collection, automatic checkout, asset management, etc.
6. *Broadcasting*: amplitude- and frequency-modulated (AM, FM) radio, TV, direct broadcast satellite (DBS), universal radio system, etc.
7. *Automobiles and highways*: collision warning and avoidance, GPS, blind-spot radar, adaptive cruise control, autonavigation, road-to-vehicle communications, automobile communications, near-obstacle detection, radar speed sensors, vehicle RF identification, intelligent vehicle and highway system (IVHS), automated highway, automatic toll collection, traffic control, ground penetration radar, structure inspection, road guidance, range and speed detection, vehicle detection, etc.
8. *Sensors*: moisture sensors, temperature sensors, robotics, buried-object detection, traffic monitoring, antitheft, intruder detection, industrial sensors, etc.
9. *Surveillance and electronic warfare*: spy satellites, signal or radiation monitoring, troop movement, jamming, antijamming, police radar detectors, intruder detection, etc.
10. *Medical*: magnetic resonance imaging, microwave imaging, patient monitoring, etc.
11. *Radio astronomy and space exploration*: radio telescopes, deep-space probes, space monitoring, etc.
12. *Wireless power transmission*: space-to-space, space-to-ground, ground-to-space, ground-to-ground power transmission.

At low frequency, we use lumped components with transistors and diodes as needed, that is, R, L, and C. When the components become about $\lambda/8$ long, about 500 MHz to 1 GHz, we may add transmission line components (usually microstripline) in addition to lumped components. The transition from lumped elements to distributed elements will be covered in Chapter 2. When the free-space wavelength becomes less than 1 mm (millimeter wave), the designers are usually forced to use distributed transmission line elements where possible. Other forms of transmission are also used due to the limitations of transverse-electromagnetic (TEM) stripline/microstripline transmission lines [1.25], such as waveguides, surface modes, slotline, coplanar waveguide, inverted microstripline, and suspended microstripline [1.26]. The geometry for these forms of TEM, transverse-electric (TE), and transverse-magnetic (TM) lines is given in Figure 1.5. It is useful to keep in mind that two wires (or conductors) are needed for TEM and only one conductor is required for TE and TM waves, which are generally at higher frequencies.

Transmission Lines
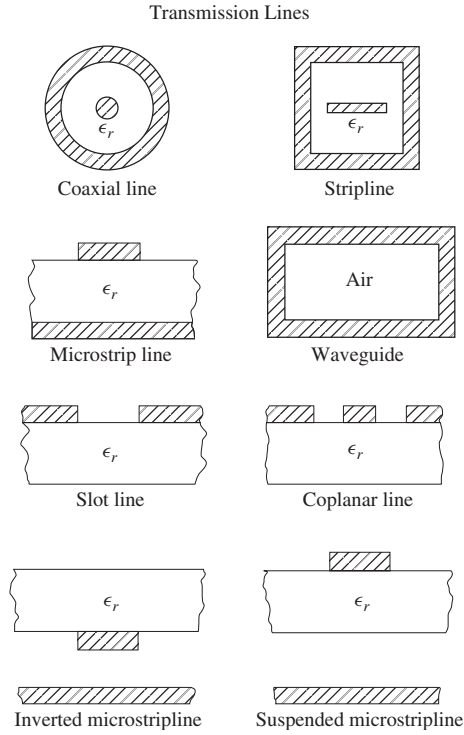
FIGURE 1.5 Geometry for microwave transmission.
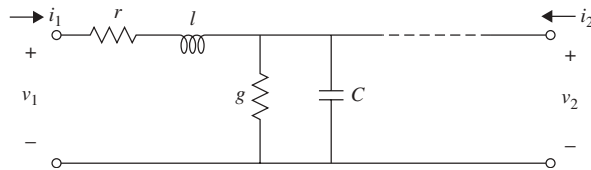
FIGURE 1.6 Lumped-element equivalent circuit of transmission line.

Transmission lines may be modeled as in Figure 1.6, which leads to the telegrapher equations, which are a time-domain description of the line:

$$\frac{\partial v(z,t)}{\partial z} = -RI(z,t) - L\frac{\partial I(z,t)}{\partial t} \tag{1.2}$$

$$\frac{\partial I(z,t)}{\partial z} = -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t} \tag{1.3}$$

For sinusoidal steady-state conditions, this may be simplified to

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{1.4}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{1.5}$$

which is noted to be very similar to Maxwell's curl equations:

$$\nabla \times E = -j\omega\mu H \tag{1.6}$$

$$\nabla \times H = j\omega\varepsilon E \tag{1.7}$$

Combining the telegrapher equations leads to

$$\frac{d^2 V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{1.8}$$

$$\frac{d^2 I(z)}{dz^2} - \gamma^2 I(z) = 0 \tag{1.9}$$

where

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{1.10}$$

is the complex propagation constant, which is a function of frequency. Traveling-wave solutions can be found as

$$V(z) = V_0^+ e^{-\gamma \cdot z} + V_0^- e^{\gamma \cdot z} \tag{1.11}$$

$$I(z) = I_0^+ e^{-\gamma \cdot z} + I_0^- e^{\gamma \cdot z} \tag{1.12}$$

With a few more steps, we may obtain the voltage waveform in the time domain as

$$V(z,t) = |V_0^+| \cos(\omega t - \beta z + \phi^+) e^{-\alpha z} + |V_0^-| \cos(\omega t + \beta z + \phi^-) e^{-\alpha z} \tag{1.13}$$

where $\phi^\pm$ is the phase angle of the complex voltage $V_0^\pm$. The wavelength on the line is

$$\lambda = \frac{2\pi}{\beta} \tag{1.14}$$

and the phase velocity is

$$v_p = \frac{\omega}{\beta} = \lambda f \tag{1.15}$$

where the actual time delay must be calculated using the group velocity, defined by

$$v_g = \frac{d\omega}{d\beta} \tag{1.16}$$

For a TEM wave, these two velocities are the same.

Some useful design aids for the microstripline case are given in Figures 1.7 and 1.8, which are the solutions provided by Wheeler in 1965 for wide and narrow lines [1.27]. These curves allow you to calculate the characteristic impedance and effective dielectric constant for the TEM mode and hence to draw the mask for your design. Many examples of this procedure will be given in this book.

There are many books which treat the solution to transmission line problems, but they all eventually lead to the Smith chart, which is the primary circuit design tool for these problems. The use and applications of the Smith chart will be described in
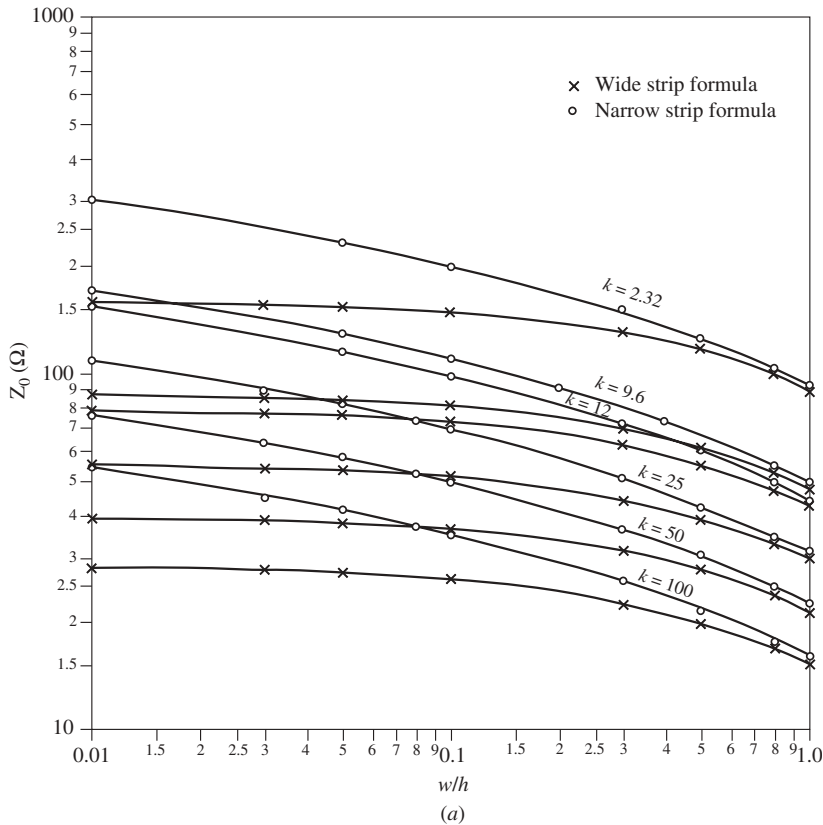
FIGURE 1.7   Characteristic impedance for (*a*) narrow and (*b*) wide microstripline [1.27].

detail in Chapter 5, where we find that graphical solutions provided by Smith charts are much more intuitive and faster than the analytic solutions provided from algebra.

Maxwell's equations become more useful as the frequency range exceeds 30 GHz, and the solutions to three-dimensional electromagnetic (3D EM) problems have now become a valuable engineering design tool, although improvements are needed in accuracy, speed, and cost. Examples of this software are Ansoft Maxwell and HFSS (High Frequency Solid Simulator), Sonnet, Zeland, and so on. Both $2\frac{1}{2}$D and 3D solutions are available from EM simulators, where $2\frac{1}{2}$D is faster but 3D is more accurate.

1.2   MAXWELL'S EQUATIONS

All forms of modern communications are based upon Maxwell's equations, which are treated in numerous textbooks [1.26–1.29]. These four equations are

$$\nabla \times E = -\frac{\partial B}{\partial t} \tag{1.17}$$

$$\nabla \times H = -\frac{\partial D}{\partial t} + J \tag{1.18}$$
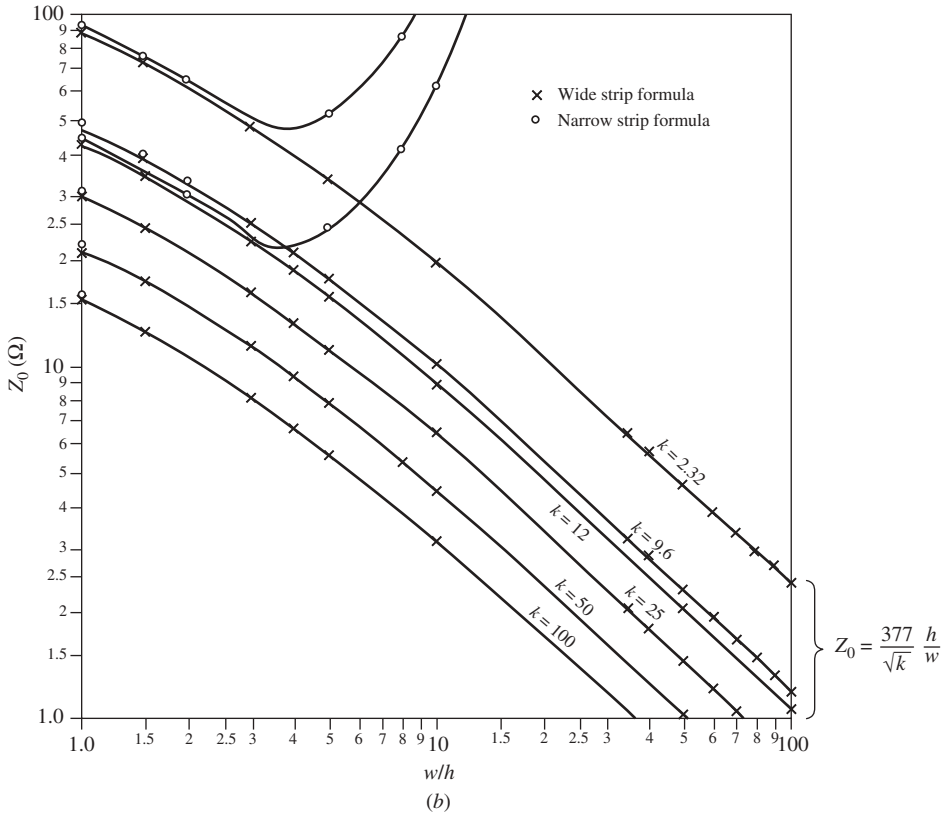
FIGURE 1.7   (*b*) Characteristic impedance for wide microstripline. (*continued*)

$$\nabla B = 0 \tag{1.19}$$

$$\nabla D = \frac{\rho}{\varepsilon} \tag{1.20}$$

These equations are also known as Faraday's law, Ampere's law, and Gauss's laws.

An interesting interpretation of these laws is shown in Figure 1.9, where physical examples of four antennas are shown to obey Maxwell's equations. The first equation is illustrated in Figure 1.9*a*, where a circular alternating current (ac) electric field requires an ac magnetic field. This is known as a loop antenna or electric antenna. The dual is shown in Figure 1.9*b*, which is a circular loop antenna or a magnetic antenna. Again, the circular ac magnetic field requires an ac electric field. The half-wavelength dipole antenna illustrates Gauss's law for electric charge, as given in Figure 1.9*c*. The electric fields terminate on charges only. The distribution of fields along the length of the dipole give a current, or H, maximum at the center and a voltage, or E, maximum at the open-circuited ends of the antenna. The final equation is illustrated in Figure 1.9*d* by a ferrite rod antenna. An air coil does not disturb the uniform H field, but a high micro ferrite inside the coil will attract the H fields inside the ferrite but there is no source of magnetic fields. Thus, the four Maxwell equations have been demonstrated by simple antenna examples.
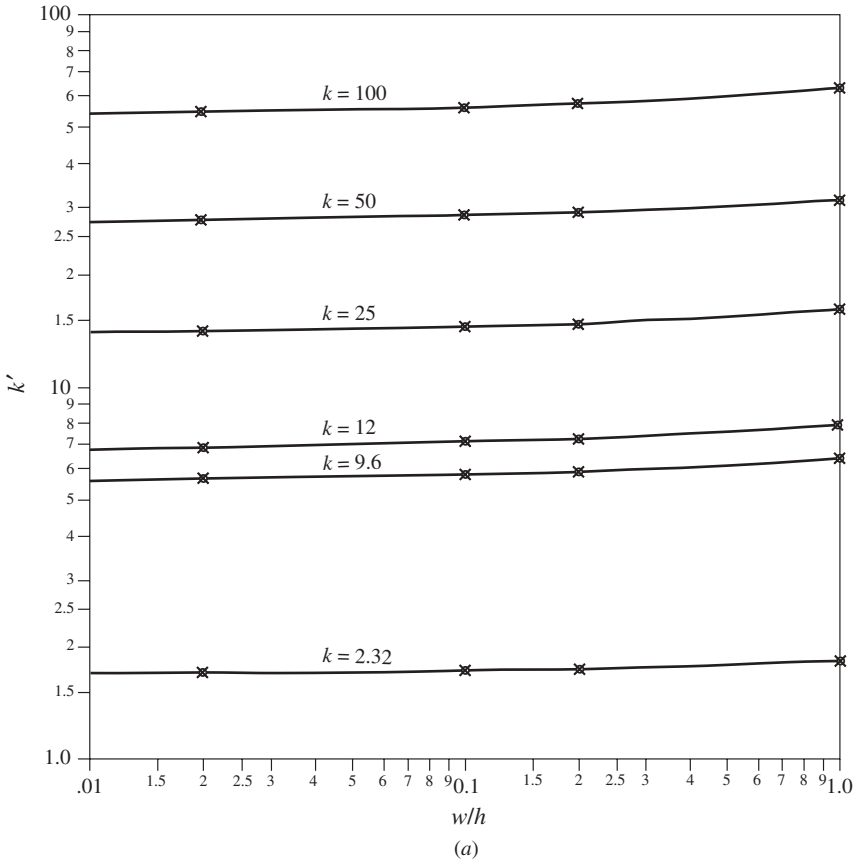
FIGURE 1.8 Effective dielectric constant for (*a*) narrow and (*b*) wide microstripline [1.27].

1.3 RF WIRELESS/MICROWAVE/MILLIMETER-WAVE APPLICATIONS

The primary applications of the three frequency groups are essentially the same: communications receivers and transmitters (or transceivers). The simplest example to envision is your cellular telephone at 850 MHz or 1.85 GHz. The essential components are the amplifiers, oscillators, and mixers, which will be covered in detail in this book. The complete derivations may be found in the references, but the necessary formulas are given in each chapter when appropriate.

The amplifier, oscillator, and mixer functions will use the lowest cost transistors which satisfy the specifications: including Si BJTs, GaAs MESFETs, AlGaAs PHEMTs, InGaP PHEMTs, SiGe HBTs, AlGaAs HBTs, InP HBTs, Si CMOS transistors, and Si LDMOS transistors, and the list continues to expand.

The oscillators use the same low-cost transistors with the additional requirement of low phase noise. The material properties and manufacturing methods presently favor silicon-based devices due to lower $1/f$ flicker noise, but this could change quickly. Designers of amplifiers and oscillators are usually the same engineers using the same software, transistors, and circuit technology; however, oscillator designers also need a high-Q resonator. These oscillator designs may also be approached from a linear
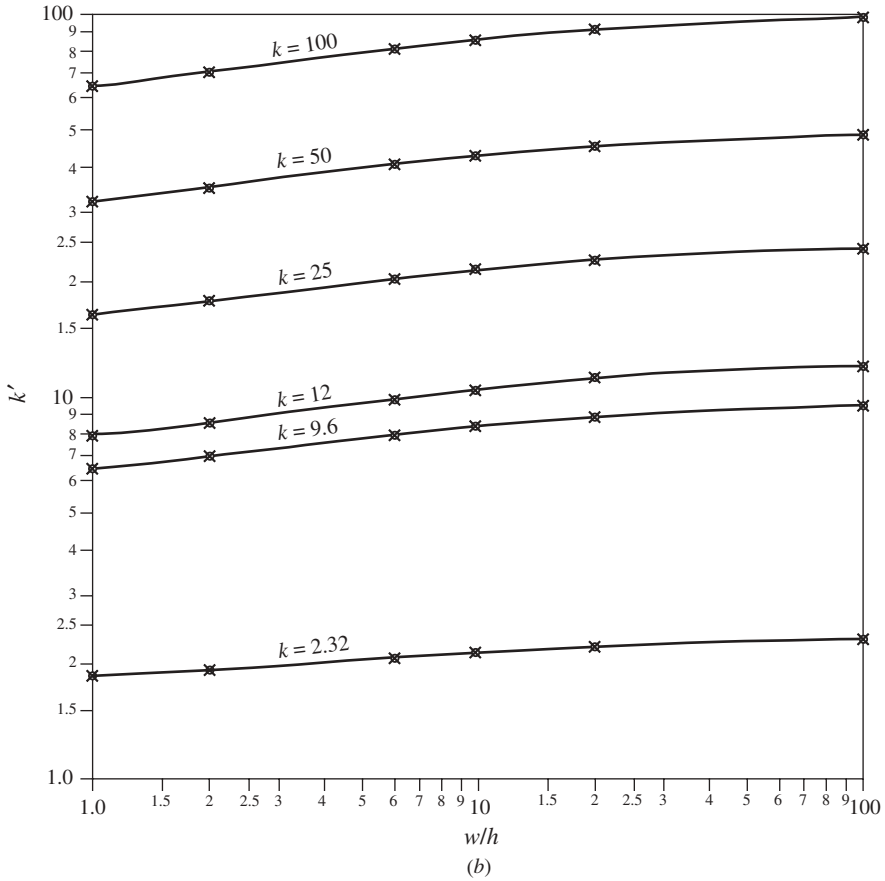
FIGURE 1.8 (*b*) Effective dielectric constant for a wide microstripline. (*continued*)
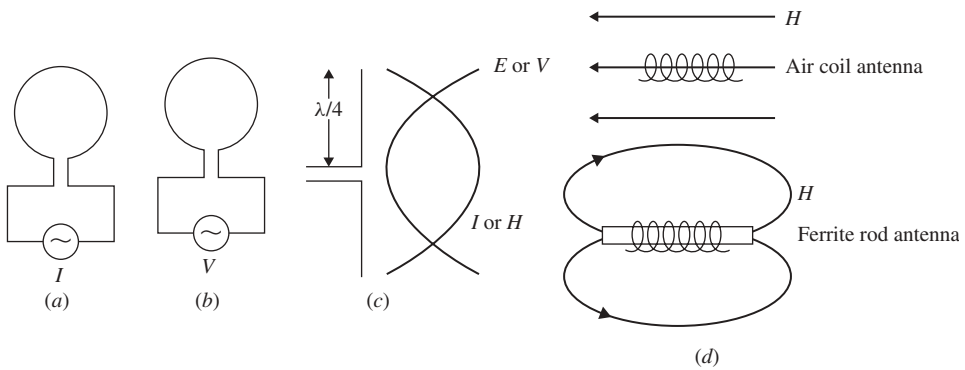
FIGURE 1.9   Four antennas illustrating Maxwell's four equations: (*a*) electric, (*b*) magnetic, (*c*) dipole, and (*d*) ferrite rod antennas.

S-parameter viewpoint; however, a more complete design requires a nonlinear CAD solution. This will be shown in Chapter 10.

The basic cellular RF wireless transceiver is shown in Figure 1.10 [1.30]. The circuits are basically the same for both analog and digital modulation, with most customers moving to digital modulation [time division multiple access (TDMA), frequency division multiple access (FDMA), and CDMA, which is explained later]. The transceiver is also the same in all frequency bands, even at 100 GHz [1.31].

The cellular telephone is a full duplex transceiver, meaning the send and receive functions are both on all of the time. Starting at the antenna, there is a duplex filter which feeds the receiver, which consists of a preamplifier, an additional filter, and a mixer. The duplexer is optimized more for separating transmit and receive signals, which are typically 50 MHz apart, rather than extreme selectivity. The front end is followed by a surface acoustic wave (SAW) filter which reduces the image frequency. These are high-impedance filters (about 150 Ω to 1 kΩ), not 50 Ω. Next is the demodulator and digital signal processing. The integrated circuits (ICs) are supplied by Philips and others. The four blocks on the right refer to the central processor, which handles display, power management, and information storage (such as frequently used telephone numbers).

The transmit portion consists of an independent synthesizer that is modulated. There are dual-synthesizer chips available to accommodate this. Both receive and transmit frequencies are controlled by a miniature temperature-compensated crystal oscillator (TCXO). One of its outputs is the system master clock for all digital activities. The output of the voltage-controlled oscillator (VCO) is then amplified and fed to the antenna through the same duplex filter as the receive portion.

A useful way to categorize the applications is to list some everyday products which the consumer uses (Table 1.3). Today there are very few applications in the millimeter-wave range, but the potential is obvious. All of these applications use transistors, passive components, duplexers, switches, attenuators, amplifiers, oscillators, mixers, and so on, which will be covered in detail in this book using the latest devices and modern CAD.

Another area of product development at the time of this writing (2003) is Bluetooth, a software-defined radio at the unlicensed frequency of 2.45 GHz which is governed
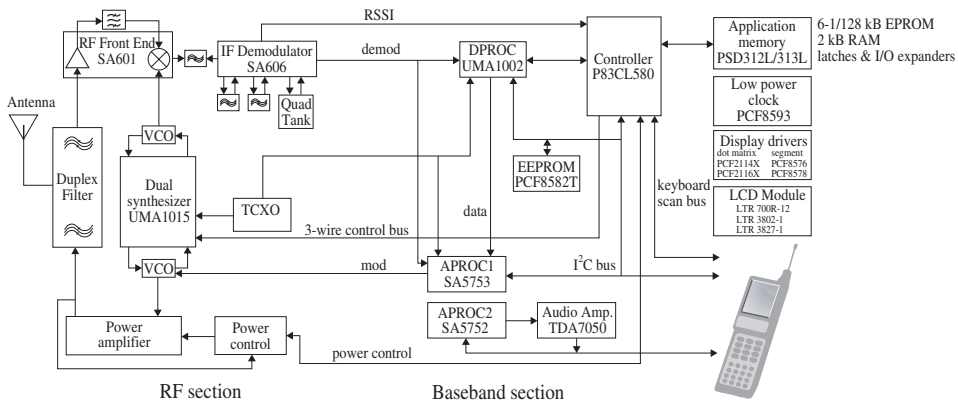
FIGURE 1.10 Cellular telephone [1.30].

TABLE 1.3   Applications

RF/Wireless	Microwave	Millimeter Wave
AM radio, 1 MHz	Ultrahigh frequency (UHF) TV, 300 MHz–1 GHz	LMDS (local multiple-distribution systems), 30 GHz
FM radio, 100 MHz	Microwave oven, 2.45 GHz	Communication at maximum attenuation, 60 GHz
Very high frequency (VHF) TV, 45–300 MHz	Cellular Telephone, 850 MHz and 1.85 GHz	Communication at minimum attenuation, 10 and 94 GHz
		Optical Communication at 40 GHz and above
	Bluetooth, 2.45 GHz	Laser frequency, typically 300,000 GHz
	Wireless Video, 2.45 GHz	Ultra wideband, 60–66 GHz
	COFDM (coherent orthogonal frequency division multiplexed), 5.25 GHz	
Cordless Telephone, 50 MHz	Ultra wideband, 3–10 GHz	
Garage/auto openers, 1–5 MHz		

by a simple protocol procedure, projected to sell at about \$5 per transceiver. This is a hand-held transceiver which is constantly looking for the user's new messages, for example, email, instant LAN, Internet access, remote synchronization of a personal digital assistant (PDA) and personal computer (PC), and printer cable replacement. It is low power (0 dBm transmit and −70 dBm receive) and thus short distance, less than 20 ft. This transceiver has a standby power of 100 μW. Data throughput is 721 kbps plus three voice channels. It uses FHSS with 1600 hops/s and includes forward error correction. The bandwidth is 1 MHz, and the frequency hopping is over the 2402- to 2480-MHz band. Clouds of Bluetooth transceivers are self-organized into piconets, which consist of up to eight Bluetooth devices. Adjacent piconets communicate to one another based upon received signal strength (nearest-neighbor) hierarchy. The system consists of one master transmitter and up to seven slaves, which form a piconet, each with a different frequency hopping pattern. One complete Bluetooth packet can be transmitted with each 625-μs hop slot. The receivers wake up every 1.28 s to listen for messages on 32 hop frequencies. To maintain synchronization, the master has to provide synchronization messages every 224 ms. A piconet is a TDD of one or more one-to-one links. The master transmits every other packet to a single slave; the slave responds immediately after being addressed. The slaves do not talk to each other, but anyone on the piconet may become the master. The piconet emphasizes flexibility, where members may join or leave at any time or they may form separate piconets if desired. Bluetooth is manufactured by over 200 registered companies worldwide, but this list is likely to reduce with time. Bluetooth solutions may consist of one to three

TABLE 1.4 Single-Chip Bluetooth System

RF 2.45 GHz; IF near zero
RSSI Measurement (Radiation Signal Strength Indicator)
8 Bit D/A and A/D Conversion, e.g., Power Amplifier Control
Power on Reset

Philips Electronics, Cambridge Silicon Radio, and Broadcom among others have announced the industry's first complete plug-and-play Bluetooth solution in a single low-cost chip package for applications such as mobile phones, headsets kits, and PDAs. The new Bluetooth semiconductor solution, the Philips BGB202 System-in-a-Package (SiP), represents a true breakthrough for designers of mobile devices through the integration of multiple technologies into one package, reducing the complete Bluetooth solution footprint to 56 mm^2.

The BGB102 RF SiP was announced in June 2003. It integrates everything needed for Bluetooth wireless technology functionality [radio, baseband, read-only memory (ROM), filters, and other discrete components] in one ultrasmall format. Housed in an HVQFN semiconductor package measuring only 7×8 mm, the BGB202 dramatically reduces the number of required components enabling quicker design cycles, lower risk, simplified manufacturing, and a reduced bill of materials (BOM).

The Philips BGB202 is currently being sampled by lead customer and will be available in production quantities early in the second quarter of 2004 at a cost of about $5 in large quantities.
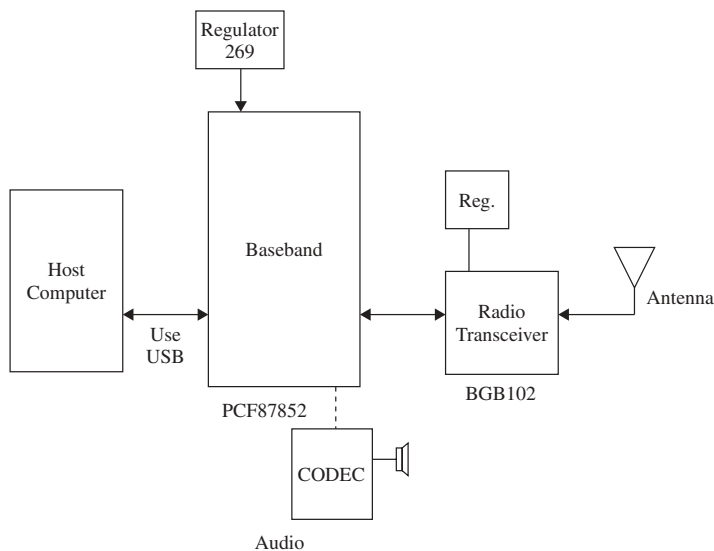
FIGURE 1.11 Bluetooth system using two Philips chips, BGB 101 transceiver chip and PCF87852 baseband chip, shown with external chips for audio processing, audio CODEC, flash memory, and external antenna.

chips at this time, where the single chip is an all-in-one, the 2 chip is RF and ASIC with microcontroller core, and the 3 chip is RF, ASIC, and microcontroller. A typical Bluetooth system from Philips is described in Table 1.4 and Figure 1.11.

Many other wireless applications are also under development at this time, including telematics at 2.4 GHz for automobile safety and entertainment and LMDS for home

entertainment (See Table 1.2) and the 802.11a and 802.11b unlicensed wireless bands (5.8 and 2.4 GHz) which are receiving a great deal of attention.

1.4   FREQUENCY BANDS, MODES, AND WAVEFORMS OF OPERATION

A useful list of the frequency bands is given in Table 1.5. As the frequency moves up, the wavelength of sinusoidal signals reduces and the bandwidth in hertz of the communications systems continues to increase, including optical circuits. The human eye operates at $\lambda = 5000$ Å, which is a frequency of

$$f = \frac{c}{\lambda_0} = \frac{3 \times 10^{10} \text{ cm/s}}{5000 \times 10^{-8}} = 0.6 \times 10^{15}$$
$$= 600,000 \text{ GHz} = 600 \text{ THz}$$

The carrier or unmodulated sinusoidal signal may propagate in several modes which satisfy Maxwell's equations. The simplest preferred mode is TEM, where there is no electric or magnetic field in the direction of propagation. This is the mode for low-frequency coaxial lines, low-frequency microstrip lines, and parallel-plate waveguides. When the parallel-plate waveguide is enclosed (see Fig. 1.5), the modes change to TE and TM, and the low-frequency propagation is not possible. The transmission medium has become a single piece of metal versus two pieces of metal for TEM modes. Another possible mode of propagation at microwave and millimeter-wave frequencies is a surface mode, TM or TE [1.25, 1.26]. Few applications have been found, but the very simplicity invites consideration. As the dielectric thickness approaches about $\lambda/4$ at high frequencies, the TE_1 surface mode is propagated with a cutoff frequency of

$$f_{c1} = \frac{c}{4 \, h(k-1)^{1/2}} \tag{1.21}$$

This mode is dispersive, that is, the velocity is increasing with frequency. When the TE mode begins, the velocity of the TM mode is close to the velocity of the microstrip TEM mode and the fields are very similar in nature, that is, well coupled. Does this

TABLE 1.5   Frequency Bands

Band	Frequency
RF	1–500 MHz
P	500 MHz–1 GHz
L	1–2 GHz
S	2–4 GHz
C	4–8 GHz
X	8–12 GHz
Ku	12–18 GHz
K	18–26 GHz
Ka	26–40 GHz
U	40–60 GHz
E	60–90 GHz

invite ideas? These concepts are only applicable when the frequency is high (millimeter wave) or the dielectric constant is high (100). For 25-mil alumina,

$$f_{c1} = \frac{3 \times 10^{10}}{4 \times 0.025 \times 2.54 \times 3} = 39.4 \text{ GHz}$$

But for 250-mil rutile ($k = 100$)

$$f_{c1} = \frac{3 \times 10^{10}}{4 \times 0.25 \times 2.54 \times 10} = 1.2 \text{ GHz}$$

and indeed effects of this were observed in the S band at Texas Instruments in 1967 [1.32].

When considering waveforms, we are thinking or calculating in the time domain instead of the more common frequency domain. The sinusoidal waveform is the basis of analog communications, and the reader should be familiar with AM and FM. The digital waveforms are more difficult to generate and visualize, especially when modulated, where the modulation is commonly PM. Fortunately, the actual circuits are essentially the same for both analog and digital, although some of the specifications will change and the methods of testing are obviously different. Modern CAD tools will give us the performance in the frequency and time domains, so the limitations may be studied in detail.

1.5   ANALOG AND DIGITAL REQUIREMENTS

Analog signals travel continuously in real time, so it is very difficult to multiplex signals to increase the number of customers on the frequency band. For digital signals, there are many ways of multiplexing the signals so several customers receive communications simultaneously over the same frequency band. This is one of the foremost advantages of digital communication systems. The process of converting analog signals to digital format uses high-speed sampling analog-to-digital converter (ADC) circuits. Once the signals are in the digital domain, it becomes very easy to multiplex the information. In addition, signal processing can be done using digital signal processing (DSP) circuits to perform filtering, interpolation, and so on. Once the above techniques are performed, high-speed digital-to-analog converter (DAC) circuits may be used to reconstitute the original analog signal.

Another feature of digital communications is error correction, which is not possible in analog communications. Analog signals may fade or become lost in the noise intermittently; with digital computer data, the digital format allows the information to be corrected for transmission errors, the accuracy is essentially 100%.

Analog signals are basically AM or FM (wider bandwidth). Digital signals are usually phase modulated (PM, which is also wide bandwidth). The phase of each digital carrier pulse contains the baseband information. PM and FM are both forms of angle modulation, where one is the derivative of the other,

$$f = \frac{d\phi}{dt} \tag{1.22}$$

The three most important forms of digital multiplexed signals are as follows:

TDMA means each user is sharing the same frequency with his or her own time slot, typically eight users on the same frequency (for GSM).

FDMA means the carrier frequency is hopping in a pattern known by the transmitter and receiver.

CDMA means the entire bandwidth is shared by all users, who have orthogonal signals which do not interfere with each other. The bandwidth for CDMA is 1.25 MHz, and it has increased to 5.0 MHz for WCDMA.

Presently the cellular telephone systems in the United States at 850 MHz and 1.85 GHz are roughly equally divided between TDMA and CDMA. Since both forms of multiplexing are constantly improving, the dominant choice has not been clearly found (if there is one).

The process of converting an analog signal to a digital bit stream is shown in Figure 1.12 [1.33]. The analog signal is sampled by an ADC, modulated to convert the digital bit stream into a transmittable form, typically pulses of current, and finally transmission or signal processing, which usually includes multiplexing, as shown in Figure 1.13. The sampling rate must be twice the period of the highest frequency due to the Nyquist sampling theorem.

For voice with an upper frequency of 4 kHz for telephones,

$$T = \frac{1}{f} = \frac{1}{4(10^3)} = 0.25 \text{ ms}$$

So the sampling rate must be faster than 0.125 ms. An excellent discussion of this process of quantization, coding, and transmission is found in Ref. 1.33.
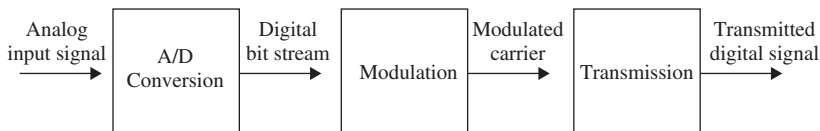
FIGURE 1.12   Block diagram of the digital communication process [1.33].
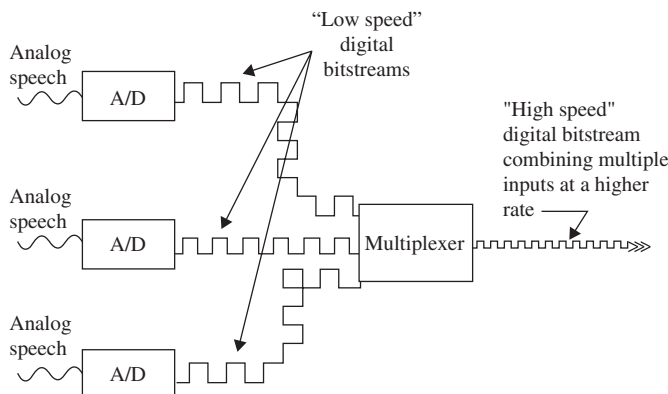
FIGURE 1.13   Multiplexing—TDMA [1.33].

TABLE 1.6   IEEE 802.11 Standards for Unlicensed Communications

Standard	Carrier	Modulation	Maximum Data Rate	Bandwidth	P_{max}
802.11b	2.4 GHz	CDMA	11 Mbps	83 MHz	1 W
802.11a	5.15–5.35 GHz	COFDM	54 Mbps	200 MHz	50 mW
	5.725–5.825 GHz	COFDM	54 Mbps	100 MHz	250 mW

Two relatively new standards generated in 1999 will be competing for the markets when this book is published: IEEE 802.11a at 5.5 GHz and IEEE 802.11b at 2.4 GHz. Some of the parameters for these bands are summarized in Table 1.6. The 2.4-GHz band is called the ISM band (industrial, scientific, and medical), but the higher frequency band has several distinct advantages if the cost can be competitive: greater range, smaller antennas, smaller circuits, and so on.

The 802.11b spectrum is plagued by saturation from wireless phones, microwave ovens, and other emerging technologies such as Bluetooth. In contrast, the 802.11a spectrum is relatively free of interference at the present time. The new technology for COFDM (coded orthogonal frequency division multiplexing) was developed for indoor wireless use and offers performance much superior to that of spread-spectrum solutions. It works by breaking one high-speed data carrier into several lower speed subcarriers, which are then transmitted in parallel. Each high-speed carrier is 20 MHz wide and is broken up into 52 subchannels approximately 300 kHz wide. COFDM uses 48 of these subchannels for data, while the remaining 4 are used for error correction.

Each subchannel in the COFDM implementation is about 300 kHz wide. At the low end of the speed gradient, binary phase shift keying (BPSK) is used to encode 125 kbps of data per channel, resulting in a 6-Mbps data rate. Using quadrature phase shift keying (QPSK), you can double the amount of data to 250 kbps per channel, yielding a 12-Mbps data rate. And by using a 16-level QAM encoding 4 bits/Hz, you achieve a data rate of 24 Mbps. The more bits per cycle (hertz) that are encoded, the more susceptible the signal will be to interference and fading. The de facto standard for 802.11a appears to be 54 Mbps, which is achieved by using 64 QAM, which yields 10 bits per cycle for a total of up to 1.125 Mbps per 300-kHz channel. With 48 channels, this results in a 54-Mbps data rate. Atheros Communications and Radiata Communications support these data rates, and Atheros also combines two carriers for a maximum theoretical data rate of 108 Mbps.

1.6   ELEMENTARY DEFINITIONS

Before concluding this chapter, a few elementary definitions are needed, including noise figure, minimum detectable signal (MDS), dynamic range (DR), spurious-free dynamic range (SFDR), P_1dBc, intermodulation distortion (IMD), third-order intermodulation (TOI), and so on. These definitions are used throughout the book.

The noise contributed by the receiver may be calculated from the noise figure, which is the ratio of S/N (signal-to-noise power) input to output:

$$\frac{(S/N)_{in}}{(S/N)_{out}} = F \geq 1 \tag{1.23}$$

or equivalently the noise temperature (in kelvin),

$$T_e = (F - 1) \ kTB \tag{1.24}$$

where k = Boltzmann's constant, $= 1.381 \times 10^{-23}$ J/K
    B = bandwidth, Hz
    T = ambient temperature (290 K is the IEEE standard for room temperature)

Since the receiver always adds additional noise while amplifying the input signal and noise, the input S/N is always greater than the output S/N. When we cascade components in a receiver, the total noise figure is calculated from Friis's noise figure equation:

$$F_{\text{tot}} = F_1 + \frac{F_2 - 1}{G_{A1}} + \frac{F_3 - 1}{G_{A1}G_{A2}} + \cdots \tag{1.25}$$

where F_N is the noise figure of the Nth component and G_{AN} is the available gain of that component, in ratio form (not decibels).

Before beginning the next section, one must realize the noise level of any resistor is kTB:

$$kTB = 1.38 \times 10^{-23} \times 290 \times 1 = -204 \text{ dBW/Hz} = -174 \text{ dBm/Hz} \tag{1.26}$$

where k = Boltzmann's constant
    T = 290 K degrees Kelvin by IEEE definition
    B = 1 Hz

This number is used constantly throughout engineering, and you must understand the meaning of this very important fundamental noise limit.

Another very important concept is the Friis transmission equation, which discusses the range of the communication system [1.34]. Consider the simplest communications system shown in Figure 1.14. The transmitter with a power of P_t is fed into a transmitting antenna with a gain of G_t. The received power is P_r at a distance of R. The received power density can be calculated assuming no atmospheric losses, mismatch losses, and so on, as

$$S_D = \frac{P_t}{4\pi R^2} G_t \qquad (\text{W/m}^2) \tag{1.27}$$

The received power is the power density multiplied by the effective area of the receiving antenna (which is related to the antenna gain)

$$P_r = \frac{P_t G_t}{4\pi R^2} A_{er} \qquad (\text{W}) \tag{1.28}$$
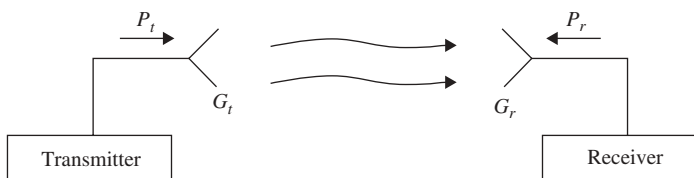
FIGURE 1.14   Simplified wireless communication system [1.34].

$$A_{er} = \frac{G_r \lambda_0^2}{4\pi} \tag{1.29}$$

Substituting gives the Friis power transmission equation:

$$P_r = \frac{P_t G_t G_r \lambda_0^2}{(4\pi R)^2} \tag{1.30}$$

which can also be put in the form [1.35]

$$\frac{P_L}{P_T} = \frac{k A_{et} A_{er}}{\lambda_0^2 R^2} \tag{1.31}$$

where k is an efficiency factor, generally 0.4 to 0.7, which accounts for factors such as misalignment, polarization mismatch, impedance mismatch, and atmospheric losses, and it is also called $1/L_{sys}$.

If $P_r = S_{i,\min}$, the minimum detectable signal required for the system, we have the maximum range

$$R_{\max} = \left[\frac{P_t G_t G_r \lambda_0^2}{(4\pi)^2 S_{i,\min} L_{sys}} \right]^{1/2} \tag{1.32}$$

This is a very important result for understanding the many components which constitute the communication system or wireless system.

An example will illustrate these concepts. Consider a transmitter at 2 GHz,

$$\lambda_0 = 15 \text{ cm} = 0.15 \text{ m} \qquad G_t = 10 \text{ dB} \qquad P_t = 1 \text{ W}$$

sending to a receiver with

$$G_r = 10 \text{ dB} \qquad S_{i\,\min} = -90 \text{ dBm} = -120 \text{ dBW} = 10^{-12} \text{ W} \qquad L_{sys} = 1$$

The maximum range is

$$R_{\max} = \left(\frac{1 \times 10 \times 10 \times (0.15)^2}{(4\pi)^2 \times 10^{-12}} \right)^{1/2}$$

$$= (1.42 \times 10^{10})^{1/2} = 119 \times 10^3 \text{ m}$$

which is about 75 miles. The range increases as the square root of the transmitted power increases. The frequency dependence indicates lower λ_0 or higher frequency will increase the maximum range [see Eq. (1.30)]. It is this property, more than any other, that makes microwaves and millimeter waves so important for communication and radar systems. To take it one step further, light is a much higher frequency which allows transmission over far greater distances; the communication part of this transmission has not yet been completed. If we increase the frequency in the previous example from 2 to 94 GHz [1.31], the $R_{\max}$ increases to 5.593×10^6 m, or approximately 3500 miles, about the length of the United States.

Another important observation is the difference between coaxial transmission and antenna-to-antenna transmission, shown in Figure 1.15 [1.35]. As the distance increases
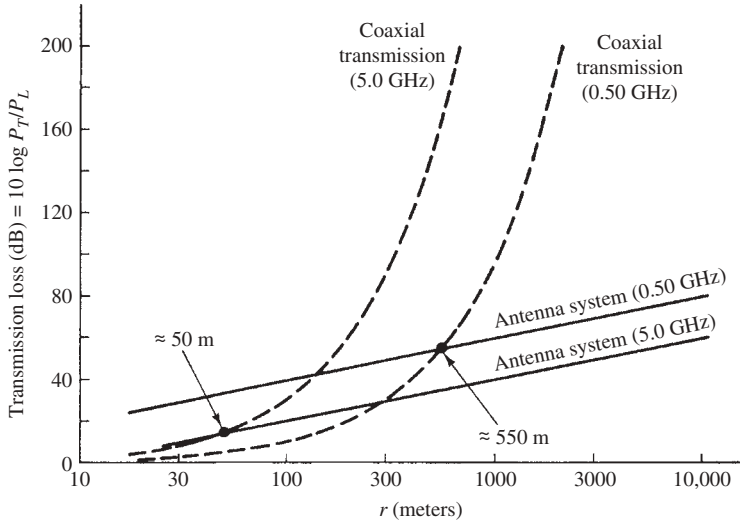
FIGURE 1.15 Attenuation for coaxial and antenna system communications [1.35].
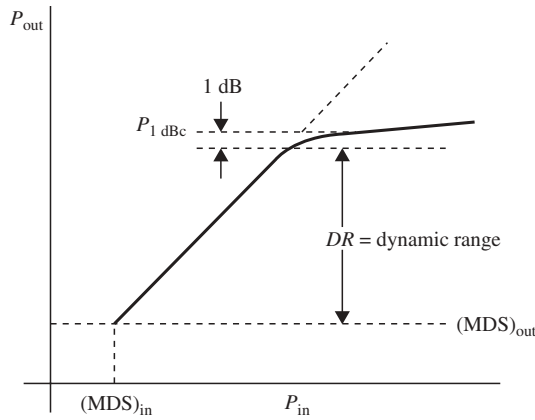
FIGURE 1.16 Dynamic range.

beyond 3000 m (1.86 miles), the coaxial system is impractical compared to antennas. Also, the losses reduce at higher frequencies for the antenna system, but the opposite is true for coaxial systems.

The dynamic range of the system is illustrated in Figure 1.16, which is a plot of P_{out} versus P_{in} at the carrier frequency, where power is always given in dBm, dB to 1 mW (e.g., 1 W is 30 dBm, 10 W is 40 dBm). Because of nonlinearities in every component, if two signals very close in frequency are introduced at the input, the output spectrum contains third-order intermodulation products which are impossible to filter at the output; the resulting power spectrum at the load is shown in Figure 1.17. The intercept of the extended linear gain and the extended third-order intermodulation products is a useful figure of merit called the TOI intercept point, or IP3, which is usually 10 dB or more above $P_{1\,dBc}$, the 1-dB compression point where the linear
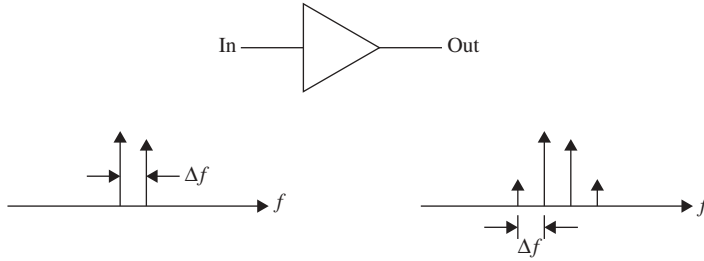
FIGURE 1.17 Output power spectrum for two input signals.
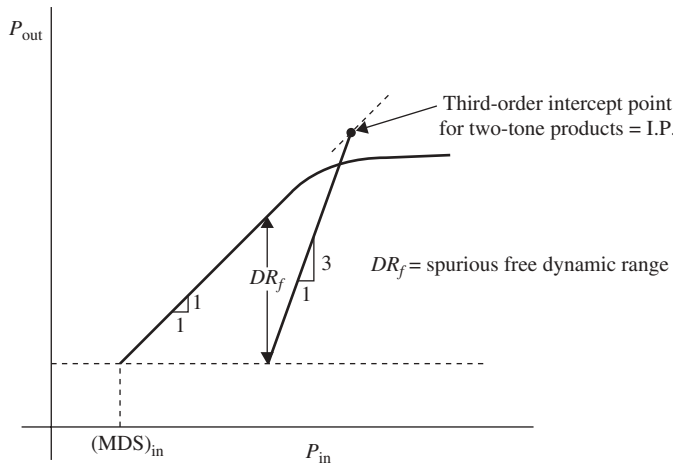
FIGURE 1.18 Spurious-free dynamic range.

gain has been reduced by 1 dB. The spurious-free dynamic range refers to the output power range where no third-order products are observed (Fig. 1.18). An example will illustrate these various definitions. Consider an amplifier with a bandwidth of 30 MHz, transducer gain of 30 dB, and noise figure of 6 dB, the minimum detectable signal is

$$\text{MDS}_{\text{in}} = -114 \text{ dBm} + 15 \text{ dB} + 6 \text{ dB} + 3 \text{ dB} = -90 \text{ dBm}$$

If the $P_{1\,\text{dBc}}$ is at +15 dBm, the linear dynamic range is

$$\text{DR} = P_{1\,\text{dBc}} - \text{MDS}_{\text{out}} = 15 \text{ dBm} + 60 \text{ dBm} = 75 \text{ dB}$$

And the spurious-free dynamic range is

$$\text{SFDR} = \tfrac{2}{3}(\text{TOI} - G - \text{MDS}_{\text{in}}) = \tfrac{2}{3}[25 - 30 - (-90)] = \tfrac{2}{3}[85] = 57 \text{ dB}$$

Which is 18 dB less that the linear dynamic range. All of these calculations pertain to analog signals.

For digital transmission, the equivalent way of expressing $P_{1\,\text{dBc}}$ is the ACPR (adjacent channel power ratio), which expresses the amount of signal "spilled over" to

the next channel at high output powers. Typical requirements are −55 dB (minimum) down for the measurement channel carrier power. An exceptionally good amplifier is given in Figure 1.19 using the MWT17 MESFET, which shows ACPR of 75 dBc at a low bias point, with the output power backed off from 1 W to 13 dBm. The equivalent TOI measurements for this amplifier are given in Figure 1.20 versus output power; again, this is an unusually high value for TOI for a 1200-μm MESFET.
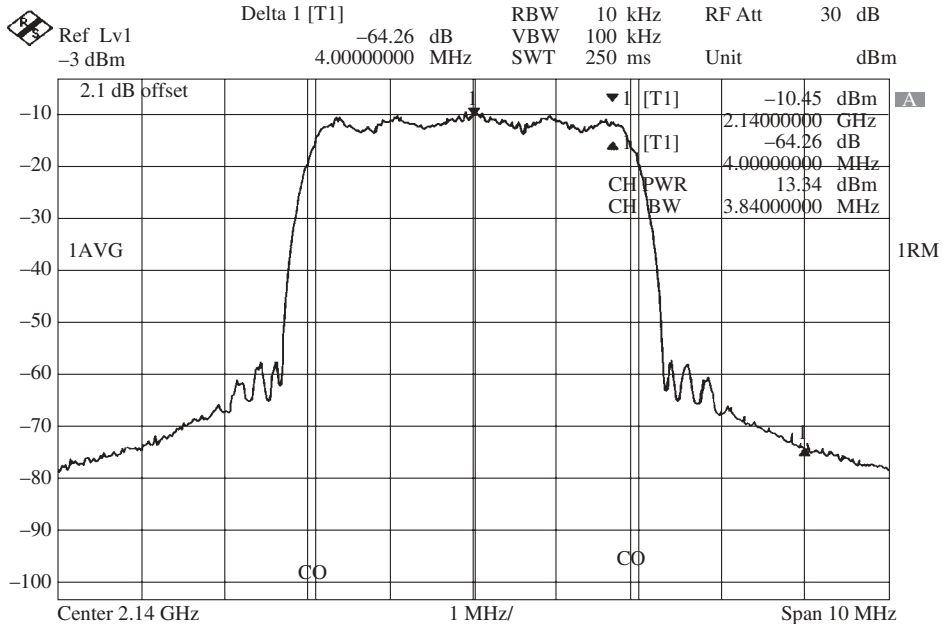
FIGURE 1.19   ACPR for a MWT-213011-82 amplifier. (Courtesy of Microwave Technology, Greg Zhou.)
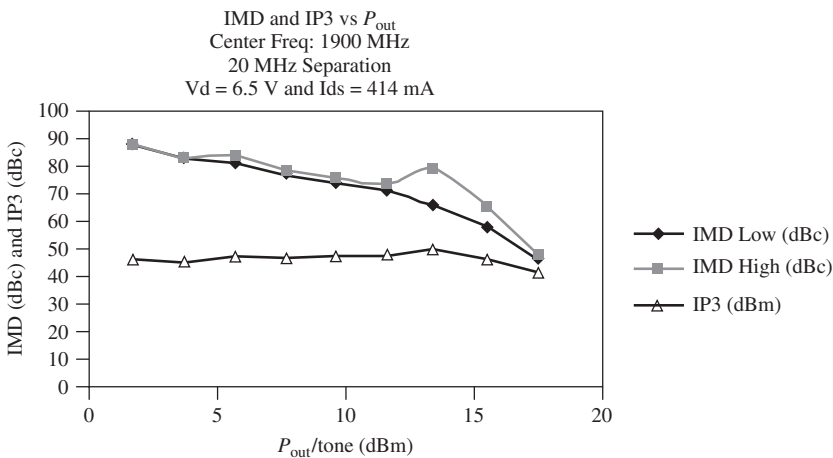
FIGURE 1.20   IP3 or TOI of MWT-213011-82 Amplifier versus P_{out}. (Courtesy of Microwave Technology, Greg Zhou.)

A new look at this subject has been published by Rohde [1.36]. He proposes the dynamic measure (DM), a new figure of merit for receivers. The equation for the DM is

$$DM = [(IP3_{in} + Att) - (NF_r + Att + NF_{ant})] \frac{NF_r}{NF_r + Att} \qquad (1.33)$$

where DM is a dimensionless number, $IP3_{in}$ is the receiver's third-order input intercept in dBμV (instead of dBm) without any added attenuation; NF_r is the receiver noise figure in dB without any added attenuation; NF_{ant} is the antenna-system noise figure in dB; and Att is the decibel value of any added attenuation, which is sometimes used to shift the upper and lower limits of a system's dynamic range to higher absolute signal levels. The Att will increase NF_r and increase $IP3_{in}$, but the dynamic measure will decrease, which is probably undesirable. The usefulness of the dynamic measure figure of merit is illustrated further in Ref. 1.36.

One final topic on definitions is the calculation of load power, which is usually a load of 50 Ω. However, if the load changes to 25 or 100 Ω due to load-pulling effects in the real world, the computer will not understand this change during harmonic balance calculations, so it incorrectly calculates the power as

$$P_L = \frac{V_L^2}{2R_L} = \frac{V_L^2}{100} \qquad (1.34)$$

This may be corrected by finding the V_L value and using (1.34) correctly with the intended load resistance. A correction formula is

$$P_L = P_L(50 \ \Omega) + 10 \ \log\left(\frac{50}{R_L}\right) \qquad (1.35)$$

Of course, the value of V_L is always the peak value unless otherwise stated.

1.7 BASIC RF TRANSMITTERS AND RECEIVERS

A typical RF receiver (based upon Armstrong's superheterodyne receiver; Fig. 1.4) is given in Figure 1.21 [1.37]. This could be an AM radio receiver for the commercial AM broadcast band. The signal is twice down-converted to the low-cost 10.7-MHz IF band, amplified, detected, and amplified again in the audio band (0 to 8 kHz).

The basic transmitter is given in Figure 1.22 [1.37]. The characteristics of interest include power output and operating frequency, efficiency, power output variation, frequency tuning range, stability, oscillator quality factor (Q_u), noise (AM, FM, and phase noise), spurious signals, frequency variations due to frequency jumping, frequency pulling (load variations), frequency pushing (DC supply variations), and posttuning drift (frequency and power variations due to heating of a solid-state device). The oscillator noise is discussed in great detail throughout the book and is defined by

$$\mathfrak{L}(f_m) = \frac{\text{noise power in 1-Hz bandwidth at } f_m \text{ offset from carrier}}{\text{carrier signal power}} = \frac{N}{C} \qquad (1.36)$$

$$= 10 \log\left(\frac{N}{C}\right) \qquad \text{dBc/Hz} \qquad (1.37)$$
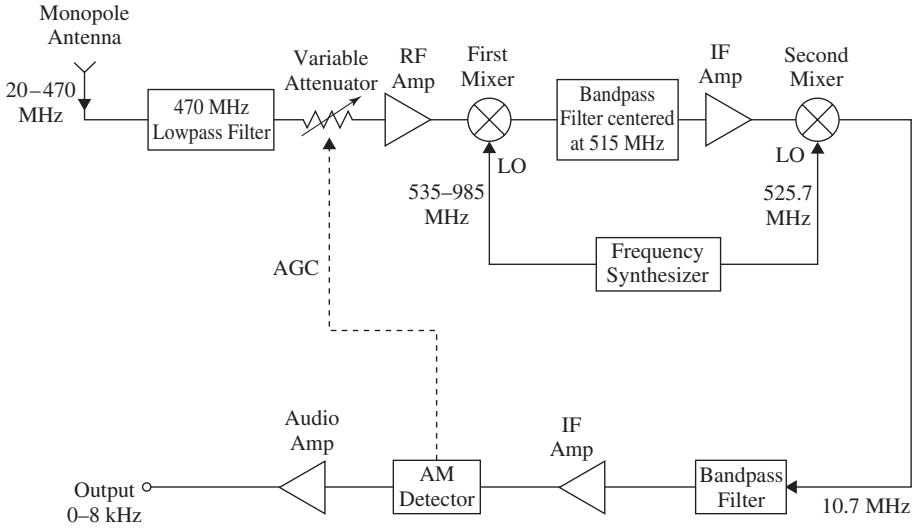
FIGURE 1.21 Typical radio receiver [1.37].
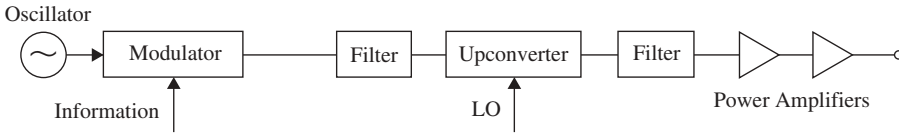
FIGURE 1.22 Transmitter system [1.37].

where the negative sign in the answer is usually omitted. For example, if the carrier is 1 mW (0 dBm) and the noise is -80 dBm at $f_m = 100$ kHz, the $\mathscr{L}(100$ kHz) is 80 dBc/Hz. Some more recent transceivers for wireless communications are given in Figure 1.23 [1.38]. This is a single-chip GSM transceiver which operates at 2.7 to 4.5 V, a typical mobile telephone.

The cascading of circuit components produces an increase in noise figure and a reduction of TOI (IP3). The total noise figure is given by

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_2 - 1}{G_1 G_2} + \cdots \tag{1.38}$$

and the total IP3 is given by

$$\frac{1}{\text{IP3}_{\text{tot}}} = \frac{1}{\text{IP3}_n} + \frac{1}{G_n \text{IP3}_{n-1}} + \cdots + \frac{1}{G_n} \cdots G_2 \ \text{IP3}_1 \tag{1.39}$$

Unless otherwise stated the TOI or IP3 usually refers to the output of the component, but it could also refer to the input. We also use the notation OIP3 for output and IIP3 for input to avoid confusion. Another way to express the total IP3 at the input is to
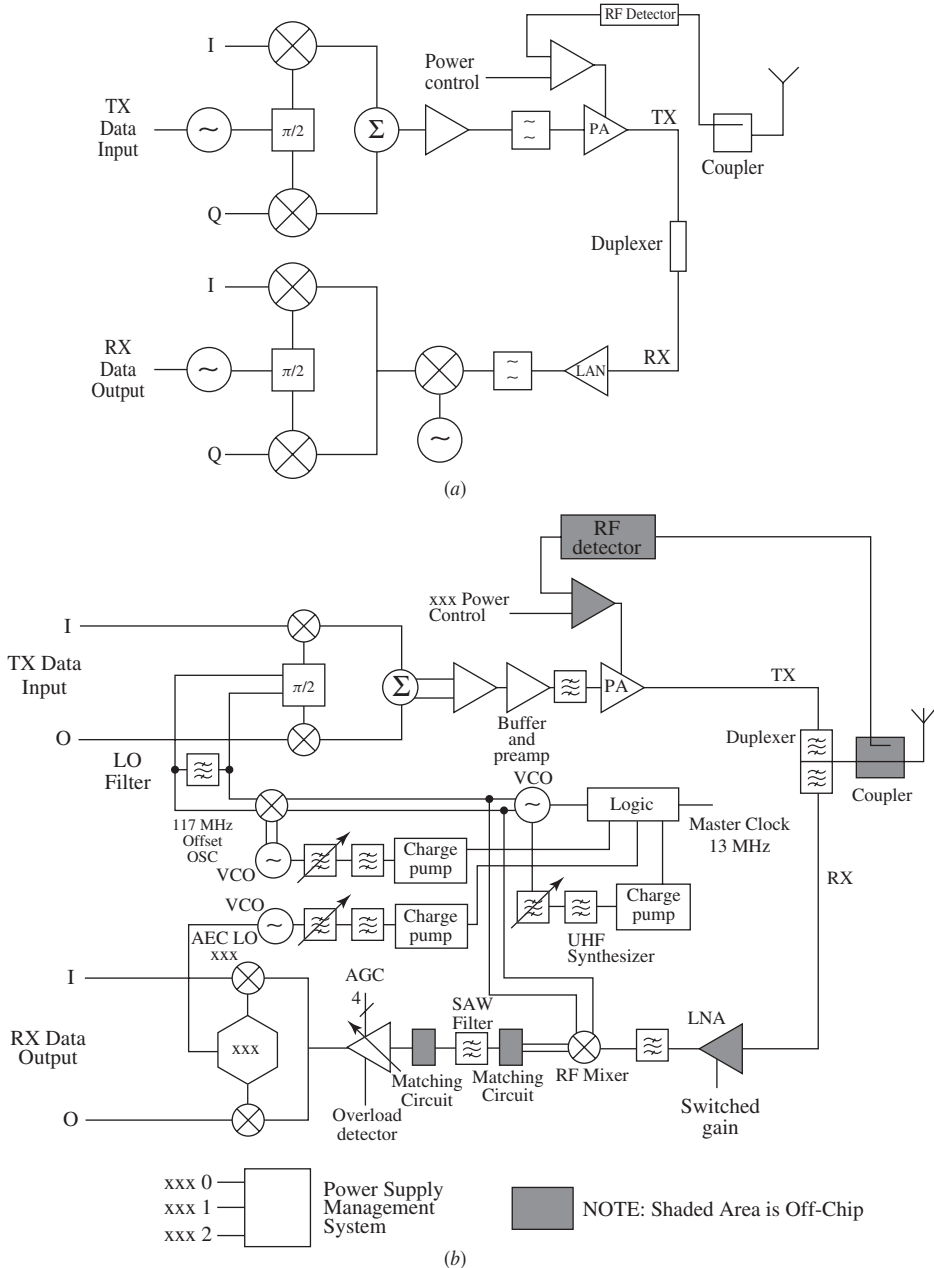
FIGURE 1.23 (*a*) Simplified transceiver block diagram for wireless communications. (*b*) Typical mobile phone systems. (From Ref. 1.38 © IEEE 1995.)

refer all of the IIP3 components to the input of the circuit, giving

$$\text{IIP3}_{\text{tot}} = 10 \log \left(\frac{1}{\text{IIP3}_1} + \frac{1}{\text{IIP3}_2} + \frac{1}{\text{IIP3}_3} + \cdots \right) \qquad (1.40)$$
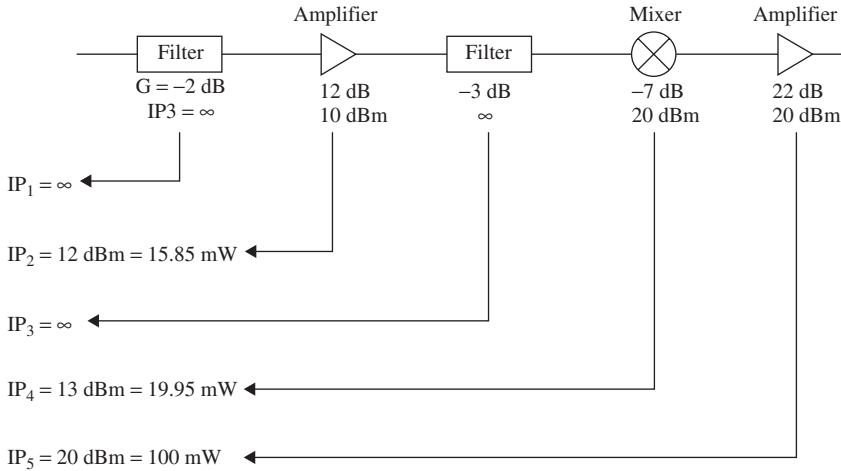
FIGURE 1.24   Receiver and its input intercept point.

An example of the total IP3 is calculated from Figure 1.24 [1.37]. For this circuit the total gain is 14 dB and the TOI is calculated for the input as

$$IIP3_{tot} = 10\log\left(\frac{1}{10} + \frac{1}{15.85} + \frac{1}{4}\right)^{-1}$$

$$= 10\log(0.10 + 0.0631 + 0.25)^{-1}$$

$$= 10\log(0.4131)^{-1} = 10\log(2.4208) = 3.84 \text{ dBm}$$

So the output TOI is

$$OIP3_{tot} = IIP3 + G_{tot} = 17.84 \text{ dBm}$$

1.8   MODERN CAD FOR NONLINEAR CIRCUIT ANALYSIS

In way of introductory material, the present-day nonlinear CAD for any circuit is available in at least three forms:

1. Transient time-domain form
2. Harmonic balance form
3. Envelope form (including modulation)

Each of these packages costs roughly $30,000 to $90,000, available from Ansoft, Agilent, Applied Wave Research, and others.

For circuits with no steady-state solution, transient time-domain solutions are found using some form of SPICE (which means Simulated Program with IC Emphasis). This can be the slowest form of the solution, but if needed, it is essential. SPICE

was developed by the University of California at Berkeley about 1965, and it was made available to the public at no charge. This sparked commercial development with improved graphics and frequency-domain solutions using the fast Fourier transform, but these solutions take great care since the minimum time step can change the answer dramatically. Many companies thrived on SPICE development, including HSPICE and PSPICE. The student version of PSPICE from Cadence is free, allowing nonlinear models of up to 15 devices, more than enough for most microwave circuits.

If there is a steady-state solution (e.g., an oscillator), the computation can be reduced dramatically by using harmonic balance techniques. This has become available since about 1980, and it is widely used. The number of harmonics is usually chosen between three and seven and the output power spectrum may be displayed at the load. In addition, the dynamic load line of the transistor may be displayed. The harmonic balance method is very valuable to the design of mixer circuits, where there are many frequencies to find the respective power levels.

The third form of calculation is Envelope, which is most suitable for carriers with modulation. This CAD can dramatically decrease the time of the calculations of complicated digital circuits with all kinds of phase modulation. The output baseband information may be displayed in many ways, including constellation diagrams and eye diagrams. This tool became available about 1995.

There are also linear CAD products at lower cost. These include Eagleware's Genesis and Optotek's MMICAD, among others. Of course, all nonlinear CAD may be used in the linear mode.

1.9 DYNAMIC LOAD LINE

Basic electronics teaches us that when two sinusoidal signals are applied to the vertical and horizontal inputs of an oscilloscope circles will occur known as Lissajous patterns when the load is a pure capacitor or inductor. This is important information related to the nature of the dynamic load line of a transistor amplifier. It can easily be shown
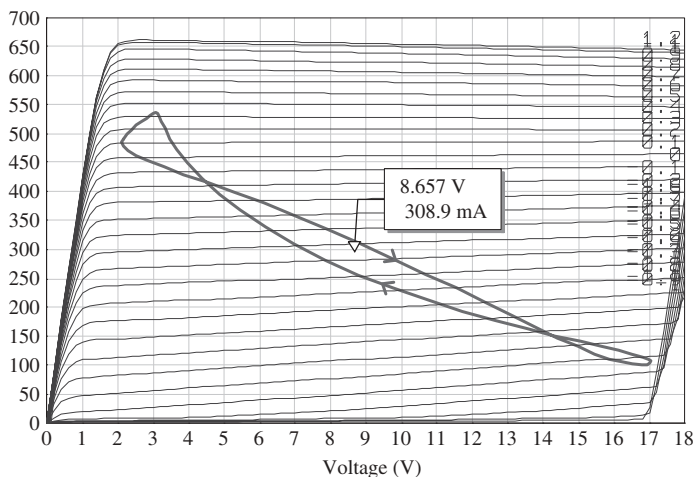
FIGURE 1.25 Dynamic load line of 2.4-GHz LP1500 PHEMT amplifier with $P_{\text{LOAD}} = 1$ W.

that a capacitor produces a clockwise (CW) pattern while an inductor produces a counterclockwise (CCW) pattern [1.39].

For a well-designed amplifier, both types of circles are frequently produced, that is, a figure-8 pattern, where part of the load line is capacitive (CW) and the other part is inductive (CCW). For most high-power amplifiers, the load line is an elliptical *RC* load (CW), where the closer this approaches a straight line, the higher the output power becomes (see Fig. 1.25).

A simple test for understanding the Lissajous pattern concept is to plot the time dependence of the input voltage and input current to a *L* or *C* element at a single frequency, then plot the input current versus the input voltage, also in the time domain. This gives a circle (or ellipse) which is CW for a capacitor and CCW for an inductor. This simple test will give an intuitive understanding of the nonlinear reactive impedance of the transistor in both amplifiers and oscillators. These techniques are especially applicable to high-power amplifiers and oscillators, where nonlinearities produce saturation effects of important significance. Several examples of this concept will occur throughout this book.

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PROBLEMS

1.1 Given a superheterodyne AM receiver for high fidelity (Fig. P1.1), design the gain of each stage for linear operation (multiple solutions are possible):

$$P_{in} = -90 \text{ dBm} \qquad f_{in} = 1 \text{ MHz} \quad \text{(FM radio)} \qquad P_{out} = 10 \text{ W}$$

The gain of each bandpass filter is −1 dB and of each mixer is −6 dB.
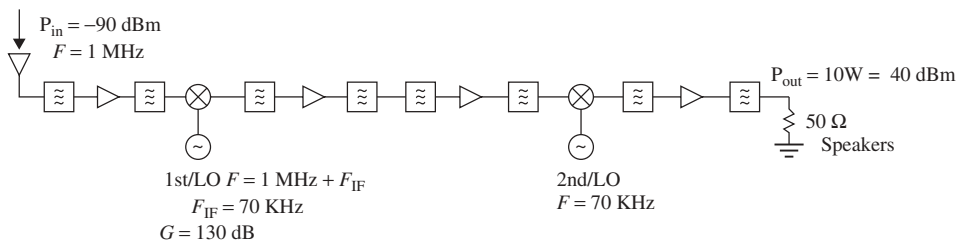
FIGURE P1.1   Superheterodyne receiver design.

1.2 For a high-power amplifier, the dynamic range is given below. Find the SFDR and the DR:

$$\text{MDS}_{\text{out}} = -60 \text{ dBm}$$

$$\text{BW} = 10 \text{ MHz}$$

$$\text{Transducer gain} = 30 \text{ dB}$$

$$P_{1\,\text{dBc}} = 40 \text{ dBm}$$

$$\text{TOI} = 50 \text{ dBm}$$

Refer to Figures 1.16 and 1.18.

1.3 Consider a substrate with $h = 10$ mils and $\varepsilon_r = 10$ (alumina). Find the f_{TE1} cutoff frequency and explain its significance. What thickness would you need for operation at 94 GHz with no effects from surface modes?

1.4 Explain why digital communications has finally overtaken analog communications in the modern world.

1.5 If a crystal radio receiver is designed for 1 MHz, what are some values for L and C (see Fig. 1.2)? Take L to be about 10 μH.

1.6 Given a three-stage LNA (low-noise amplifier) with

$$F_1 = 2.0 \text{ dB} \qquad \text{GA}_1 = 10 \text{ dB}$$

$$F_2 = 4.0 \text{ dB} \qquad \text{GA}_2 = 12 \text{ dB}$$

$$F_3 = 6.0 \text{ dB} \qquad \text{GA}_3 = 14 \text{ dB}$$

Find the total noise figure in dB and the T_e in kelvin.

1.7 Derive the SFDR from Figure 1.16 using simple geometry (similar triangles).

1.8 Given the modern 6-GHz heterodyne receiver shown in Figure P1.8, find the total TOI and the total NF of this receiver. For the total TOI use Eq. (1.39).
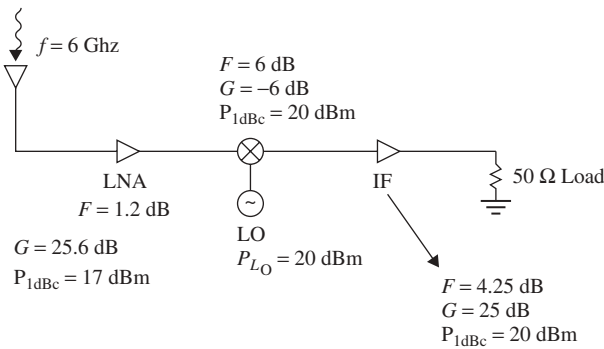
FIGURE P1.8   Modern 6-GHz heterodyne receiver.

CHAPTER 2

LUMPED AND DISTRIBUTED ELEMENTS

2.1 INTRODUCTION

Maxwell's equations govern all types of electromagnetic behavior at all frequencies. At lower frequencies (below about 500 MHz) where lumped components are less than $\lambda/8$ in length, it is convenient to define the component as a frequency-independent R, L, or C. As the frequency increases, the component will have distributed effects or added phase shift which must be accounted for in the analysis. These effects will be discussed in this chapter.

2.2 TRANSITION FROM RF TO MICROWAVE CIRCUITS

As electrical engineers, we first learn to analyze lumped-element circuits consisting of R, L, and C components, which are independent of frequency; the impedance or admittance of the components is linearly dependent on frequency. Then we learn that at high frequencies additional parasitic effects must be included in the model of the component. For lumped components at low frequencies signals travel at essentially the speed of light instantaneously through points in space where the component is located. At microwaves (defined as 300 MHz to 300 GHz, with above 30 GHz also called millimeter wave), the electrical component used to generate and process signals has a size similar to an eighth of a wavelength. Then we must back up to Maxwell's equations subject to the appropriate boundary conditions.

The RF range is generally defined as 30 to 300 MHz, but it should be a frequency where all of the lumped components are shorter than about $\lambda/8$ in length. In the 100 to 500-MHz range, we are in a grey area where the circuit might be treated as

either lumped or distributed provided the lumped equivalent circuit is accurate. The distributed transmission lines are very long in this frequency range and thus are not used very often. Even at 850 MHz lumped components are successfully used (e.g. cell phones). The distributed transmission line circuits would be very large for an 850-MHz cell phone but much more realistic at 5.8 GHz, a future band for cell phones and other nonlicensed products.

To illustrate this point, we calculate the λ/4 length on FR-4, a low-cost substrate at 850 MHz using an effective dielectric constant of 3:

$$\frac{\lambda}{4} = \frac{c}{4f\sqrt{\varepsilon_{\text{eff}}}} = \frac{7.5}{1.732 \cdot 0.85} = 5.09 \text{ cm} = 2.00 \text{ in.}$$

which is extremely large for a hand-held cellular phone circuit. A higher dielectric constant will reduce this dimension.

For transmission line circuits, we use TEM or quasi-TEM microstripline for the passive circuits, which became available in 1965 [2.1]. The impedance and phase velocity were given by Wheeler in this important paper. It was immediately applied to the design of an X-band solid-state radar at Texas Instruments [2.2] using hybrid technology based upon alumina substrates and millimeter-wave monolithic circuits using GaAs substrates at 94 GHz [2.3].

To understand this transition from RF to microwave or distributed elements, a plot of wavelength versus frequency is given in Figure 2.1 for various dielectric constants, where dielectrics effectively slow the velocity as ε_r increases. It is important for the
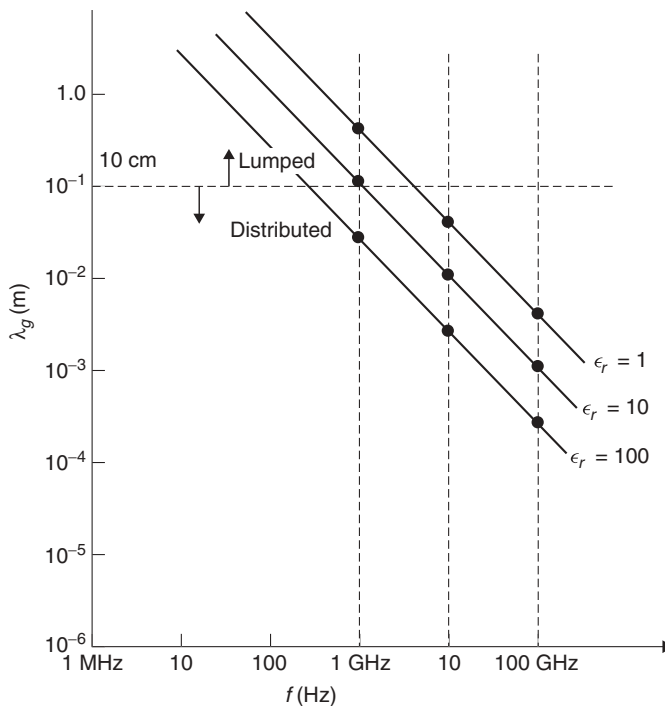
FIGURE 2.1 Guide wavelength versus frequency with dielectric constant as a variable.

loss tangent to be low, which is true for alumina and GaAs but not for silicon. With GaAs substrates, $\rho > 10^6$ Ω-cm is easily achieved and maintained throughout the processing cycle. With Si substrates of high resistivity (10^3 Ω-cm) the n-type may become p-type with processing, and the resistivity is likely to lower, which is unacceptable for monolithic circuits. One of the most challenging problems today is to achieve a high-Q inductor on silicon, where a Q above 10 at 2 GHz is about the best which can be achieved at the time of this writing, as shown later in this chapter.

Referring to Figure 2.1, the dielectric constant of most interesting dielectrics for MICs is of the order of 10, so the border between lumped and distributed may be estimated at $\lambda = 0.1$ m, or 10 cm, which coincides with the previous division at about 0.5 to 1 GHz. The calculation of the guide wavelength for an effective dielectric constant of 10 follows at 1 GHz:

$$\lambda_g = \frac{c}{f\sqrt{\varepsilon_{\text{eff}}}} = \frac{3 \times 10^{10}}{\sqrt{10} \times 10^9} = 10 \text{ cm} = 0.1 \text{ m} = 4 \text{ in.}$$

$$\frac{\lambda_g}{8} = 0.5 \text{ in.}$$

In other words, at frequencies above 1 GHz the circuit must be treated as distributed since a length of more than 0.5 in. will have distributed or phase properties which cannot be modeled by a simple R, L, C component.

Microwave transmission is often associated with waveguide transmission, which is a single metal conductor. This type of transmission is TM or TE, not TEM; therefore,
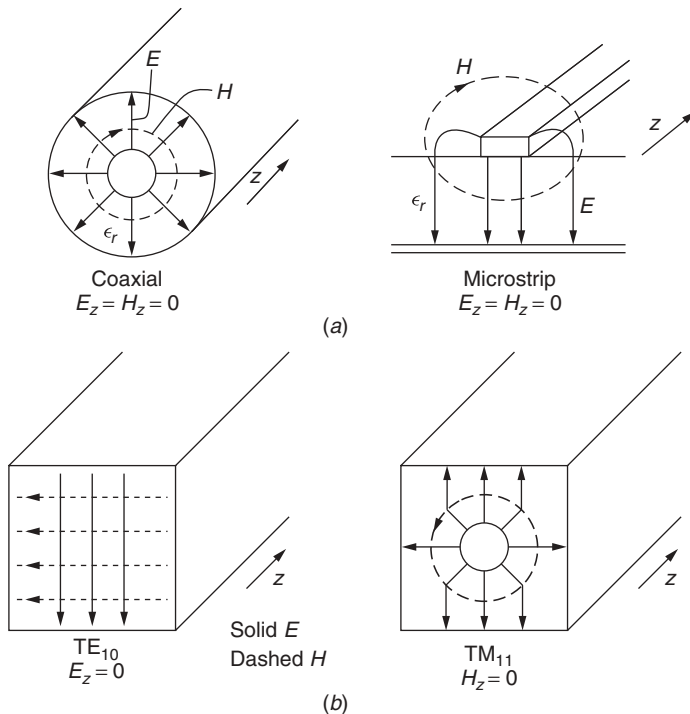
FIGURE 2.2 Examples of TEM, TE, and TM modes. (z is direction of propogation.)

it has little value in today's communications in the microwave region. The cost is high, and the performance is not comparable to planar microstrip technology for most applications, especially when we consider bandwidth. The TEM mode requires two conductors, but the TM and TE modes require only a single conductor or a single dielectric. Simple examples of these concepts are illustrated in Figure 2.2.

The passive components include all of the lumped transmission line elements needed for impedance matching and dc bias. The active components are the diodes and transistors needed for the circuits. Impedance matching may be accomplished with lumped inductors, lumped capacitors, transmission lines, shorted transmission line stubs, and open-circuited transmission line stubs, but usually not with resistors. There are at least two reasons for not using series transmission line stubs:

1. Series transmission line stubs are unrealizable in microstripline and therefore are a very poor choice, although many current books teach this type of impedance matching [2.4, 2.5].
2. This element offers no advantage in circuit design; it is unnecessary and simply a diversion from real circuit design.

Mathematically a series transmission line stub (either open or shorted) is possible, but practically this is unrealizable and therefore a waste of the designer's time. Some private communication sent by Pozar points out that CPW can be used, but no working circuits have yet appeared in the literature.

2.3   PARASITIC EFFECTS ON LUMPED ELEMENTS

Passive components may be purchased in various sizes as given in Table 2.1 [2.6]. The equivalent circuit of chip resistors is given in Figure 2.3, with the corresponding parasitic elements listed in Table 2.1. The equivalent circuit for chip capacitors is given in Figure 2.4.

The effect of the series inductance is plotted in Figure 2.5, where L_s is assumed to be 1 nH. The series resistance for the 1000-, 100-, and 10-pF capacitors is assumed to be 0.08, 0.2, and 0.5 Ω, respectively. The series resonant frequency versus capacitance is given in Figure 2.5b for three differing values of series inductance: 0.6, 1, and 1.5 nH. It is useful to know that an empirical rule of thumb for lead inductance on conventional components is around 1 nH/mm.

Alternative equivalent circuits of inductors and capacitors are given in Figure 2.6. Notice a capacitor becomes an inductor above the series resonant frequency and an

TABLE 2.1   Chip Resistor Versus Size and Typical Parasitic C and L

Resistor Size	Length (mm)	Width (mm)	Capacitance (pF)	Inductance (nH)
1206	3.2	1.6	0.05	2
0805	2.0	1.25	0.09	1
0603	1.6	0.8	0.05	0.4
0402	0.5	0.5		
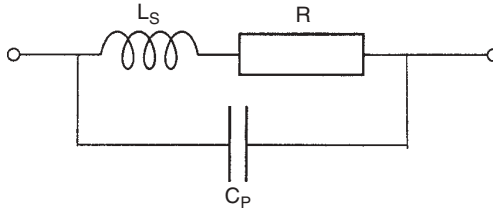
FIGURE 2.3   Equivalent circuit for a resistor.
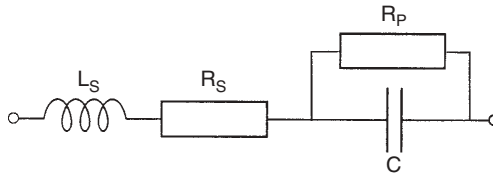
FIGURE 2.4   Equivalent circuit model for chip capacitors.

inductor becomes a capacitor above the parallel resonant frequency; thus, the choice of these components is crucial to finding realizable designs.

The frequency response of a typical chip inductor and chip capacitor has been plotted in Figure 2.7 for $\pm j50$ Ω at 10 GHz. For the inductor of 0.8 nH and a Q of 30 at 10 GHz, the parallel resonance is about 8 GHz, where the reactance changes from inductive to capacitive. For the capacitor of 0.3 pF and a similar Q of 30 at 10 GHz, a series resonance occurs at 16.5 GHz, where the component becomes inductive above this frequency. Notice the component is probably not useful below 5 GHz, where the insertion loss is greater than 2 dB. Modern CAD packages contain libraries of the lumped chip components (R, L, and C), which should be studied with great care if a chip or lumped-element approach is selected. The method of attachment must be repeated exactly if these libraries are to be useful.

Lumped elements may also be realized by direct deposit on the substrate using thick- or thin-film techniques [2.6]. This will often lead to much smaller designs with better performance, but the manufacturing cost is increased.

Amplifiers, oscillators, mixers, and other components may be designed with either lumped or distributed components (or a hybrid combination) with essentially the same performance, although lumped elements generally give the best performance, that is, the widest bandwidth. Since distributed transmission lines are more repeatable than lumped components, these elements are more commonly used [2.7–2.8].

A serious study into lumped components and the development of accurate lumped-component models will inevitably reveal that their performance is substantially dependent upon the surrounding circuit environment. Just as the properties of the microstrip line clearly depend on the substrate height and dielectric constant, and not just on the dimensions of the signal strip, lumped-element performance similarly depends on the substrate properties. As frequency increases and the physical dimensions of the lumped element attain greater electrical length, the isolation of lumped-component behavior from the substrate environment becomes increasingly improbable.
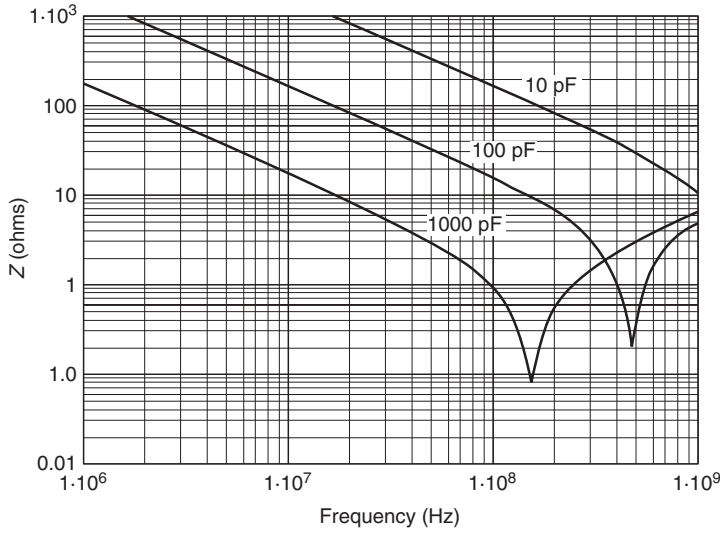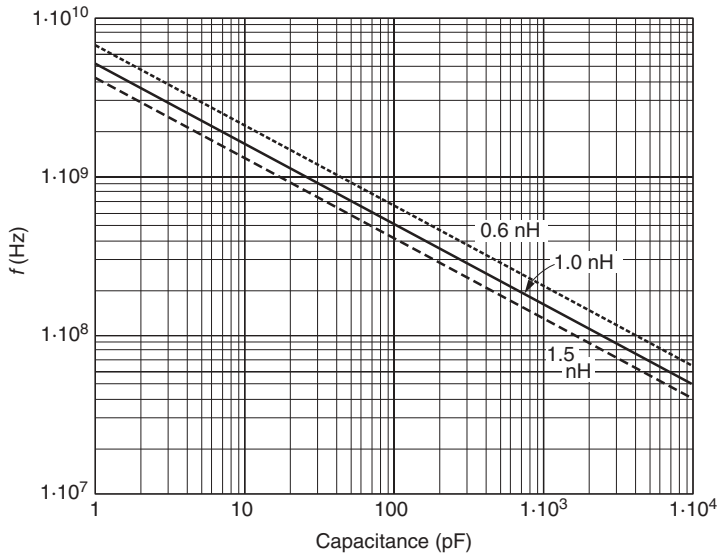
FIGURE 2.5   (*a*) Effect of series resonance on *Z*. (*b*) Series resonant frequency for *L* values of 0.6, 1.0, and 1.5 nH.

A lumped element can in fact be considered as a "signal strip," albeit of somewhat complex geometry. Chip resistors, of thick- or thin-film type, are very lossy strips that are deposited on top of a ceramic body with solder-attach pads. Multilayer ceramic capacitors, widely used in RF/microwave electronics, are comprised of several (up to 30 or more) metal electrodes that are closely stacked upon each other to realize *N* parallel capacitors. Finally, chip inductors are typically formed of wires either wrapped around a plastic core or embedded within a ceramic block. Regardless of the construction, the lumped component becomes a modified section of the signal line when mounted on

(a)

(b)
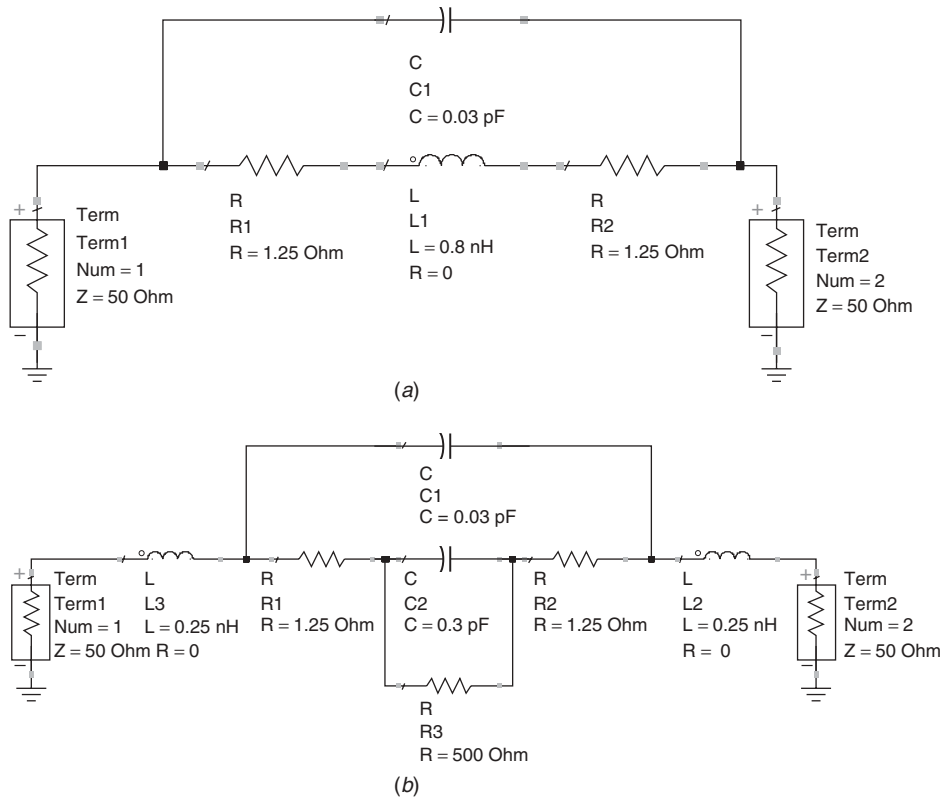
FIGURE 2.6 Equivalent circuits for a chip inductor and capacitor with a reactance of $\pm j50\ \Omega$ at 10 GHz for the ideal component.

a circuit board across a gap in the microstrip. At frequencies above 1 to 2 GHz it is important to consider this viewpoint.

Some recent modeling of lumped components performed by Modelithics [2.9–2.16] shows the effect of the substrate on the first resonant frequency for chip capacitors; see Figure 2.8. The figure shows that the resonant frequency decreases with increasing substrate height, a characteristic that is true of most types of surface-mount components. One expects that shunt capacitance will increase as the part nears the ground plane (Fig. 2.8b), but it is an accompanying decrease in the series inductance (Fig. 2.8c) that is needed to shift the resonance upward. At some point the ground effects become quite severe and there is no recognizable resonance.

The complexity of lumped-component behavior at high frequency presents significant challenges for the design engineer. To achieve high levels of miniaturization and keep costs low, lumped components are being used in many cases above 5 GHz [2.10, 2.14] and on substrates as thin as 1 to 2 mils [common in low-temperature cofired ceramic (LTCC) designs and in high-density interconnect (HDI) environments]. Knowledge of the component performance at multiple harmonics of the fundamental design frequency may even be needed when simulating nonlinear designs using the harmonic balance method [2.11]. In such demanding applications, accurate and broadband measurement data obtained using fixtures that are consistent with the intended application,
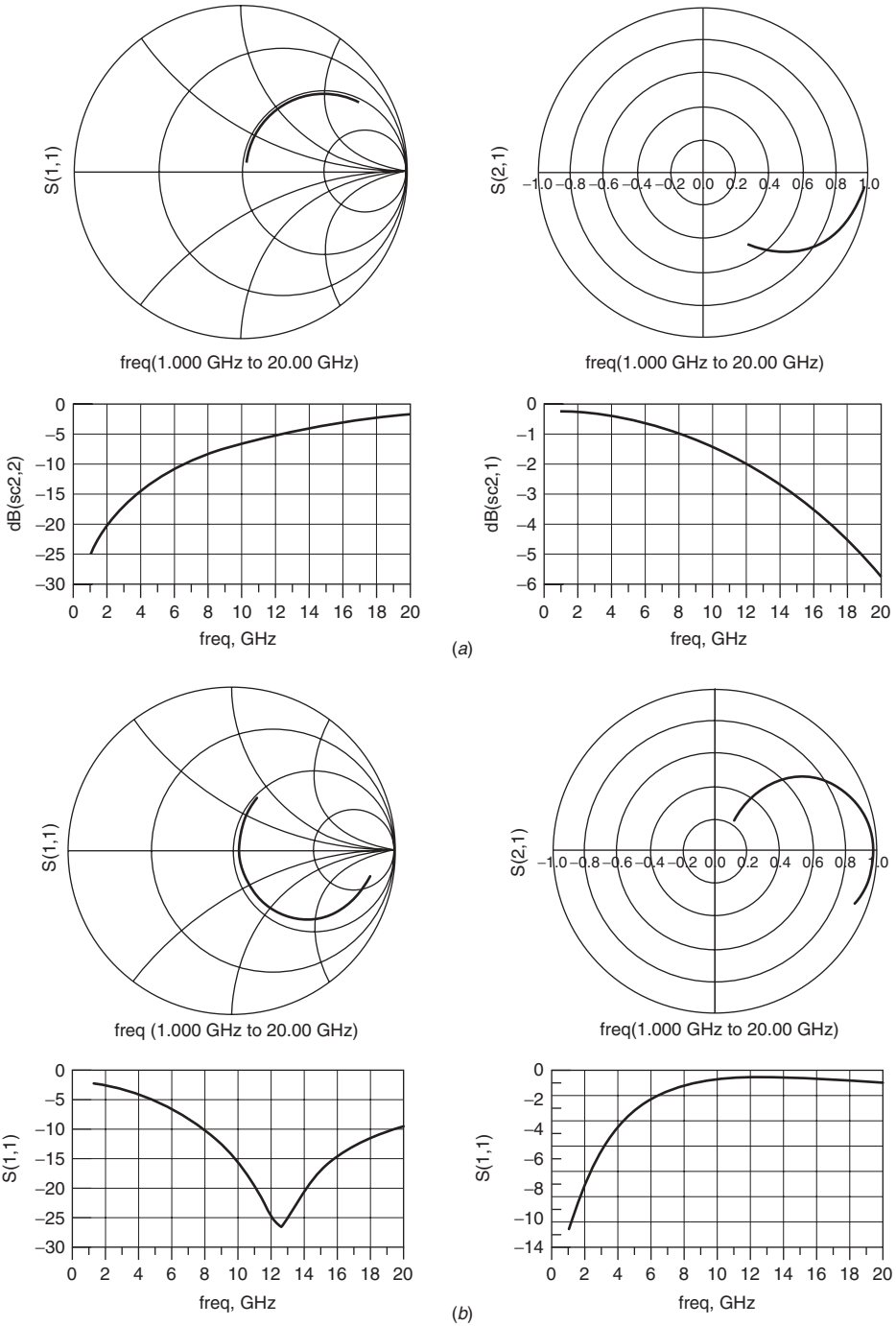
FIGURE 2.7   Frequency response of typical chip inductors and capacitors versus $Q = 30$ at 10 GHz: (*a*) 0.8-nH inductor; (*b*) 0.3-pF capacitor.
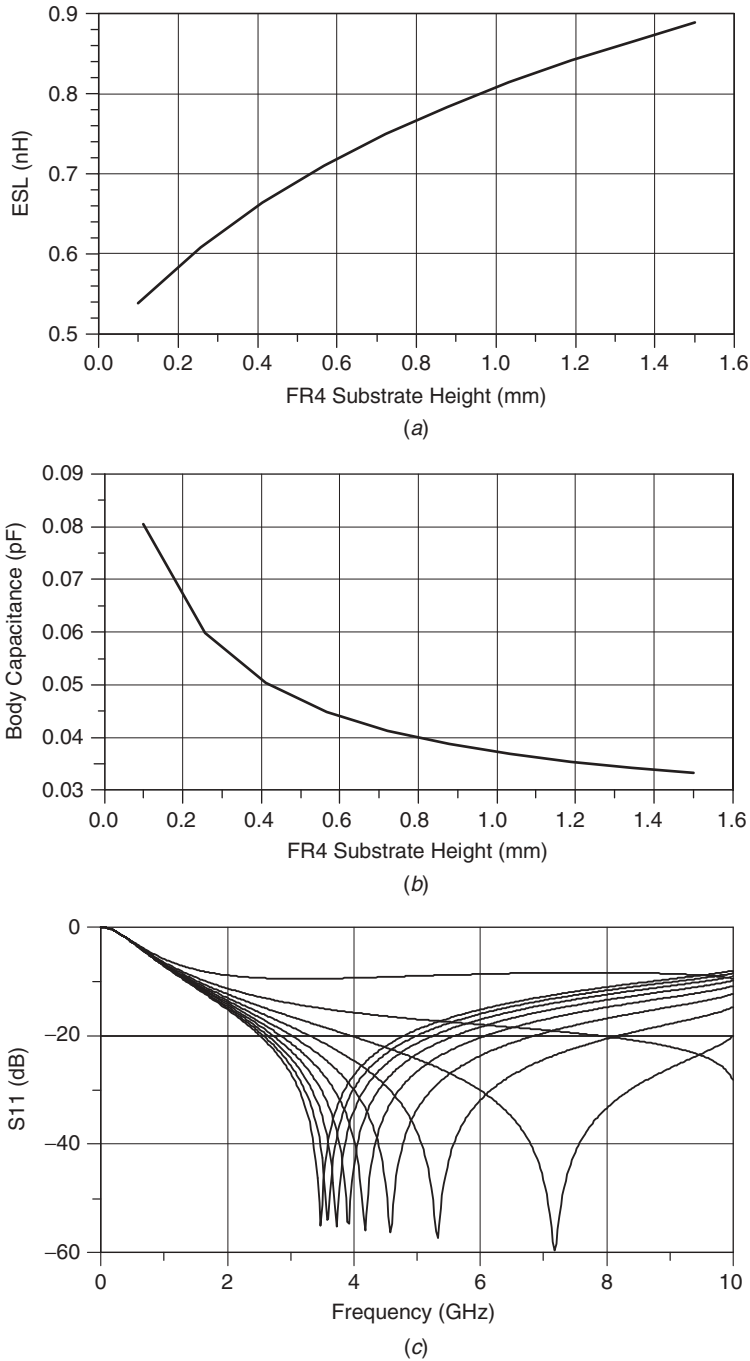
FIGURE 2.8   Frequency response of surface-mount chip capacitor versus substrate height: typical variation in (*a*) effective series inductance (ESL) and (*b*) body capacitance. (*c*) Typical variation in S_{11} for surface-mount capacitor in series two-port configuration: FR-4 heights from 0.1 mm (highest resonant frequency) to 1.5 mm (lowest resonant frequency).

or valid models of the same, are crucial to the design simulation process [2.12–2.15]. When predicting power dissipation characteristics is important, equivalent circuit models are far superior to data sets, as series resistance is not well represented with 50-Ω S parameters [2.16].

Another important area of research today is the development of high-Q inductors on silicon substrates [2.17–2.24]. Much effort has been applied to raise the Q above 10 at 2 GHz, as is discussed in these references. The losses of the inductor are due to skin effect metal losses in the inductor and ground return, dielectric losses in the silicon, eddy currents which are geometry dependent, possibly radiation, and surface roughness effects on metal losses. Several new innovative steps have reduced these losses, including patterned ground shields, square coils, CAD studies, and higher order modes (non-TEM); even conical designs with 3D effects are under consideration (e.g., LTCC).

Square inductors and spiral inductors give very similar performance; we often call square inductors *spiral* in the literature. Circular spirals have slightly higher Q than square inductors, on the order of 10%. A simple-minded explanation is that the circle is the shape of least perimeter for a fixed area. Therefore, for a fixed inductance (area) it has the lowest resistance (perimeter). An equivalent circuit for the spiral inductor on a silicon substrate is given in Figure 2.9. Frequency-dependent skin effect losses can be modeled with parallel-coupled inductors.

The loaded Q of a coil may be increased by increasing the strip width, decreasing the spacing between strips, increasing the substrate height, and increasing the metal thickness to at least five skin depths.

There are two cases to consider for the silicon loss:

1. 10 to 20 Ω-cm (moderate-resistivity bulk substrates)
2. 10 to 20 mΩ-cm (CMOS digital epitaxial process)

Most analog process technologies are closer to the first case where substrate losses are dominated by electrically induced losses. For the second case, the losses are much higher due to magnetically induced substrate eddy currents. We can somewhat improve the performance by the use of patterned ground shields, which prevent the electric field from entering the substrate silicon. The use of these patterned ground shields is illustrated in Figure 2.10. The ground shield is built with slots between the ground metal to give the best performance [2.18]. Patterned ground shields can only stop the electric field from penetrating the substrate and therefore cannot prevent eddy currents. But, precisely for the same reason, the shields do not significantly change the inductance of the device at lower frequency. The added capacitance of the shield reduces the
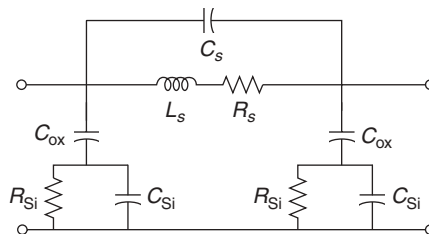
FIGURE 2.9   Lumped physical model of a spiral inductor on silicon.
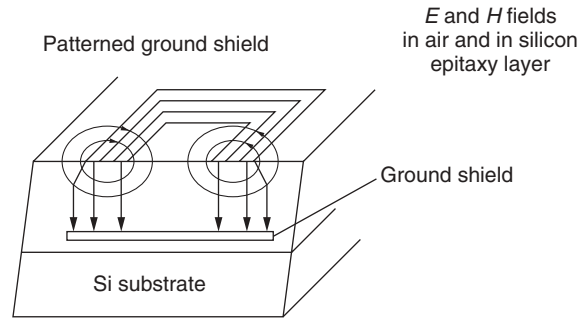
FIGURE 2.10   Electromagnetic fields for a spiral inductor using patterned ground shields [2.18].

self-resonant frequency and thus the magnetic energy storage of the device at high frequency. Halo substrate contacts have been shown to perform as well as patterned shields without the increase in capacitance. Also, the case for a shield is a difficult one to make and should be done on a case-by-case basis. The basic idea is to improve the Q factor of the parasitic capacitance of the spiral. The Q is determined largely by the substrate resistance, and the worse value of substrate resistance is a value equal to the substrate capacitance for a power match. Since a value of zero or infinity implies zero loss, it may be more practical to not shield the device at all to minimize losses. A shield tries to achieve zero resistance, but in practice, if the substrate resistivity is large enough, then the power loss without a shield may be lower than with a shield. But another added benefit of the shield is device isolation due to reduced parasitic substrate coupling between the devices. This of course requires a good on-chip bypass and low-inductance ground connections to the shield.

2.4   DISTRIBUTED ELEMENTS

The most common distributed elements are series transmission lines, shunt open stub transmission lines, and shunt shorted transmission lines. The transmission line was briefly covered in Chapter 1, where the telegrapher's equation was introduced and solved in the time domain.

The concepts associated with these impedance-matching elements will become clear when we discuss the Smith chart and matching techniques in Chapter 5. Consider these elements or components as nearly lossless reactive elements, very similar to inductors and capacitors. When properly applied to the circuit design, the distributed elements will give nearly equivalent performance compared to ideal lumped components, which always gives the greatest bandwidth.

The interconnection of transmission lines creates a new element in the circuit, a discontinuity [2.7, 2.8]. Examples are shown in Figure 2.11, including the open-circuit end effect, series coupling gaps, short circuits to ground plane (vias), right-angled corners or bends (unmitered and mitered), strip width changes, transverse slit, tee junction, and cross junction. These have been modeled in the CAD packages, and they simply shift reference planes and thus adjust the lengths of the connecting transmission lines. Higher order modes are also generated at discontinuities in order to satisfy Maxwell's equations, including surface modes (TM and TE) and radiation modes (from

Z_{02}

Z_{01}

Impedance step

Tee

(a)

Cross

(b)

Open-circuit end effect
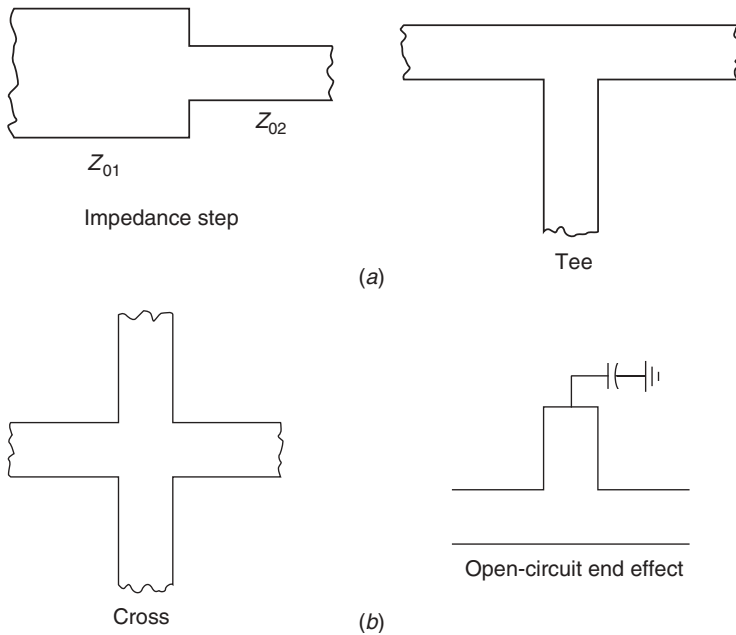
FIGURE 2.11   Transmission line discontinuities. (See Appendix F for more details.)

open-circuited stubs), which will cause a loss of power. An example of the effect of a microstrip cross junction (MCROS) can be found in Ref. 2.25, where a broadband amplifier is dramatically changed by the effect of the cross-parasitic element At higher frequencies, the model may not be sufficiently accurate, so we use 2D or 3D electromagnetic simulators to verify the performance of the circuit. This can be very time consuming and expensive, but it is necessary for accurate designs, especially at higher frequencies. The EM CAD packages are available from Ansoft, Sonnet, Zeland, and other software producers.

Since transmission lines have traveling waves in both directions over potentially many wavelengths, the time-domain transient solution may be expected to be very long. However, clever techniques using the propagation matrix $[W(\omega)$ matrix] have been found [2.26] which reduce the computation time and maintain good accuracy. When the skin effect losses are properly accounted for [2.27], the solution is even more accurate. These techniques continue to be an active research topic for transient solutions, but for most engineers it is the steady-state solution which is required, and this is most easily obtained in the frequency domain.

2.5   HYBRID ELEMENT: HELICAL COIL

Some circuit elements have the properties of both a lumped element (at low frequencies) and a distributed element at microwave frequencies. An example is the high-Q helical coil, which is an excellent resonator at certain frequencies, which are difficult to predict
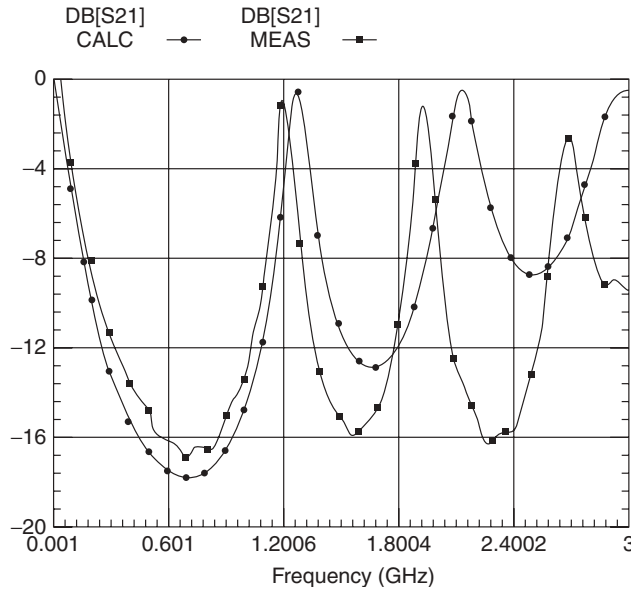
FIGURE 2.12 Frequency response of helical coil.

because of the use of second-order Bessel functions. An exact analysis of a helical coil has been published [2.28] and verified by 3D EM calculations using Ansoft Maxwell and laboratory measurements. A program is available to analyze a helical coil of any dimensions. The frequency response of a simple 2-GHz helical coil is shown in Figure 2.12, where it should be noted that the resonant frequencies are not related by integers, and the Q or bandwidth of the resonances is frequency dependent, a fact which is missing from other papers on this topic [2.29, 2.30]. Tapered or conical helical coils have been used for many years to achieve broadband performance in Hewlett-Packard bias tees. Since these products appeared in the early network analyzers (1965), this was obviously an empirical hand-made design. The coil was wound on a conical tapered dielectric of low dielectric constant, probably Teflon. Helical coils and also tapered helical coils are useful for filters, oscillators, bias tees, and other low-loss, high-Q applications.

Another form of a distributed-element transmission line is the twisted-wire transmission line, which is covered in Chapter 4, Figure 4.18. This form of transmission is used often in mixers below about 2 GHz.

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PROBLEMS

2.1   Calculate the guide wavelength for $\varepsilon_r = 10$ (alumina) at 100 MHz, 1 GHz, 10 GHz, and 100 GHz in mils (thousandths of an inch).

2.2   Find the S parameters versus frequency (0.1 to 20 GHz) using a CAD for a chip resistor with (Fig. 2.3)

$$R = 100 \ \Omega \qquad L_s = 1 \ \text{nH} \qquad C_p = 0.09 \ \text{pF}$$

2.3   Using a linear CAD tool, find the S parameters versus frequency (1 to 10 GHz) of the following circuit:

$w_1 = w_3 = 23.0$ mils

$w_2 = 5.0$ mils

$w_4 = 50.0$ mils
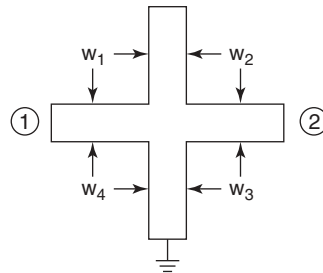
All lines are λ/8 at 5 GHz.   MCROS is the junction effect. Assume $\varepsilon_r = 10$ and $h = 25$ mils.

2.4   A 1-mil-diameter gold wire has an approximate inductance of 0.022 nH/mil. Calculate the bonding inductance if the length is 20 mils. Repeat the calculation for a high-impedance ideal transmission line ($Z_0 = 100 \ \Omega$ and $\varepsilon_r = 1$) and a microstrip line ($Z_0 = 100 \ \Omega$ and $\varepsilon_r = 6.7$) for a length of 20 mils. Assume $\varepsilon_r = 10$ for the microstrip line.

2.5   Design a bias tee for 6 to 18 GHz using a lumped L and C. Repeat for ideal transmission lines ($\varepsilon_r = 1$). Which gives the best performance over the greatest bandwidth?

CHAPTER 3

ACTIVE DEVICES

3.1 INTRODUCTION

In the previous chapter, we dealt only with passive devices, and it became apparent that the microwave frequencies had a drastic impact on the behavior of the components and structures when the electrical length of a component becomes of the order of $\lambda/8$ or longer. The majority of microwave circuits use active devices one way or another. While some applications operate the devices in a linear range, many applications need to understand the behavior under large-signal conditions. Typical examples for large-signal operations are mixer and oscillator circuits as well as power amplifiers. The basic nonlinearities are frequency independent, and yet because the nonlinear capacitance of the device starts playing a major role at higher frequencies, their effect has to be considered. Needless to say, this is a hot topic for CAD, specifically, nonlinear CAD. For small-signal operation, the semiconductor houses provide a set of bias-dependent S parameters, while for the large-signal operation the nonlinear models are only occasionally found on the data sheet or web site. Therefore, SPICE (the earliest nonlinear computer program developed at the University of California at Berkeley in the 1960s) has been used with simple diode models, Gummel–Poon BJT models, and simple Schichman–Hodges FET models at extended frequency ranges. The SPICE (Semiconductor Processing with Integrated Circuit Emphasis) program takes advantage of nonlinear parameters which describe the semiconductor under medium- to large-signal conditions based on a set of nonlinear parameters. These parameters will allow one to predict the bias point, time and frequency dependencies, and even temperature dependencies. Several companies have introduced microwave-capable SPICE programs and the latest CAD tools have these capabilities fully integrated. This chapter will

provide some high-frequency insight into the commonly used microwave active devices and prepare the reader for large-signal considerations.

This chapter begins with a detailed discussion of diode nonlinear performance, including: the *pn* junction, the Schottky diode, the *pin* diode, and the varactor diode (variable reactance). The basic nonlinearities are the capacitance and the forward bias current. Next the many forms of three-terminal transistors will be covered:

1. *BJT [3.1]* A current controlled transistor which is a minority-carrier device in the base region; this a bipolar device because there are two junctions, the emitter–base junction, which is forward biased to inject the minority carriers into the base, and the collector–base junction, which is reverse biased to collect all of the base minority carriers into the collector. The Gummel–Poon model is most commonly used, followed by the vertical bipolar integrated circuit (VBIC) model and MEXTRAM, the nonlinear bipolar model developed by Philips. The VBIC is an extension of the Gummel–Poon model, and the MEXTRAM model uses fewer nodes (five vs. seven) and therefore converges faster than other models in nonlinear situations (developed by Philips).

2. *MOSFET* Modern metal–oxide–semiconductor field-effect transistors (MOS-FETs) have become important at frequencies below 2.5 GHz. Some of the history includes double-diffused metal oxide semiconductor (DMOS) transistors which were developed at Signetics in the early 1970s [3.2, 3.3], the high-frequency performance of CMOS transistors, and the development of the high-power laterally diffused MOS (LDMOS) transistor which is discussed in the power amplifier chapter (Chapter 9). The nonlinear models come from SPICE developments, including bipolar CMOS nonlinear (Bi-CMOS) models among others. Bi-CMOS implies that BJTs, *n*-channel MOSFETs, and *p*-channel MOSFETs are on the same silicon chip [3.4, 3.5].

3. *MESFET* This transistor came about in 1965 with the development of Schottky diodes and ohmic contacts simultaneously on GaAs. It is a majority-carrier device which is voltage controlled at the gate. The name means metal–semiconductor field-effect transistor. The MESFET/HEMT models constitute a long list, including Curtice quadratic, Curtice cubic, Statz–Pucel, Materka and modified Materka (Raytheon/Ansoft), Tajima, Root (HP/Agilent), Angelov, Parker, EEFET3, EEHEMT1, and TOM3 (Triquent's own model), with more to come.

4. *HEMT (PHEMT and MHEMT)* This is replacing MESFETs in many applications due to superior performance. It is a high-electron-mobility transistor first introduced about 1980 by Fujitsu. It has progressed to PHEMT and MHEMT structures, with even better performance. A PHEMT is a lattice-matched pseudomorphic HEMT, while a MHEMT is a metamorphic HEMT, a newer development with great promise [3.6], where graded layers of doping are employed.

5. *HBT* The heterojunction bipolar transistor (HBT) was originally developed to improve emitter injection efficiency in GaAs BJTs, which has been a long-standing problem (since 1965). In addition, the SiGe HBT was added to the list about 1985 and offers a very low cost process with excellent microwave performance limited only by the low $T_{j,\max}$ value of 155°C.

The landscape has improved dramatically since the 1988 assessment of transistor performance given in the first edition of this book. The gains are higher, the noise

TABLE 3.1   Six Active Device Types [3.6]

BJT	MOSFET	MESFET	PHEMT	MHEMT	HBT
Ge	CMOS	Si	Al_2O_3GaAs	InAlAs/InGaAs	InGaP/InGaAs
Si	DMOS	GaAs	InGaAs		SiGe
	LDMOS				

figures are lower, the frequencies keep climbing, and, of course, the output powers continue to grow. Some recent developments include the enhancement- as well as depletion-mode PHEMTs, which are serious contenders for 2-GHz wireless amplifiers. The newer materials being developed today offer even further improvements in the near future, such as SiC and GaN, very promising high-power FETs. In addition n-channel MOSFETs have shown considerable promise at 60 GHz. A table of the six types of active devices is provided in Table 3.1.

3.2   DIODES†

The diode model [3.7] contains a nonlinear current source that follows the Shockley equation:

$$\text{Current} = I_S \left(e^{V_j/NV_t} - 1 \right) \tag{3.1}$$

where V_j = voltage across junction

$\quad V_t$ = thermal voltage $(= kT/q)$

$\quad N = 1.04–1.08$ (typical)

These values, with the model parameters I_S and N, are used to model the current–voltage effects of the semiconductor junction. This does not include the nonideal operation of real diodes. For example, at low currents (less than 1 nA), other semiconductor processes such as recombination increase the flow of current under forward bias.

By setting I_S to different values, we can obtain the characteristics of other devices, such as a Schottky barrier diode or a silicon diffused-junction diode. High-current effects are modeled, grossly, by including a series resistance that is intended to combine the effects of bulk resistance (the material on each side of the junction) and high-level injection. At high currents where the current density $J_{-S} \times A$ is of the order of the semiconductor doping, about 10^{16} cm^{-3}, the observed diode current stops following the Shockley form

$$I_{\text{forward}} = I_S e^{V_j/NV_t} \tag{3.2}$$

and approaches a modified form:

$$I_{\text{forward}} = I_S e^{V_j/2NV_t} \tag{3.3}$$

This equation is also used at low currents where recombination effects occur.

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† Portions of this chapter's diode coverage are based on material from the book *RF/Microwave Circuit Design for Wireless Applications* by Ulrich L. Rohde and David P. Newkirk, Wiley, New York, 2000.

3.2.1   Large-Signal Diode Model

Three diode models are used in the industry:

- Microwave diode model (including parasitics)
- The *pin* diode model
- Enhanced SPICE diode model

Figure 3.1 shows the large-signal microwave diode model. Its keywords appear in Table 3.2. This model can also be used to simulate varactor and Schottky diodes.

Table 3.3 lists SPICE parameters for a selection of Schottky mixer diodes by Alpha (Skyworks).

In most cases, the diode capacitance is modeled by a voltage-dependent capacitor, which is connected in parallel with the nonlinear current generator described previously, to represent the charge storage effects of the junction. There are two components to this charge:

- Reverse-voltage capacitive effect of the depletion region
- Forward-voltage charge represented by mobile carriers in the diode junction

Reverse-voltage capacitance follows the simple approximation that the depletion region (the area of the junction that is depleted of carriers) serves as the gap between the "plates" of a capacitor. This region varies in thickness, and therefore the capacitance varies with applied voltage. For a step (abrupt) junction or linearly graded junction, the capacitance approximation is

$$\text{Capacitance} = \frac{C_{J_0}}{(1 - V_j/\phi)^M} \tag{3.4}$$

where C_{J_0} is the zero-bias value, ϕ (phi) is the junction barrier potential, and M is the grading coefficient that varies ($\frac{1}{2}$ is used for step junctions and $\frac{1}{3}$ is used for linearly graded junctions, and most junctions are somewhere in between except the hyperabrupt junction, which can have M as high as 6 over a limited bias range).

There is often confusion about the barrier potential, which appears in the capacitance equation. From capacitance measurements, ϕ (model parameter V_I, not to be confused with V_j in the equations) takes on a value of nearly 0.7 V for regular (silicon) junction
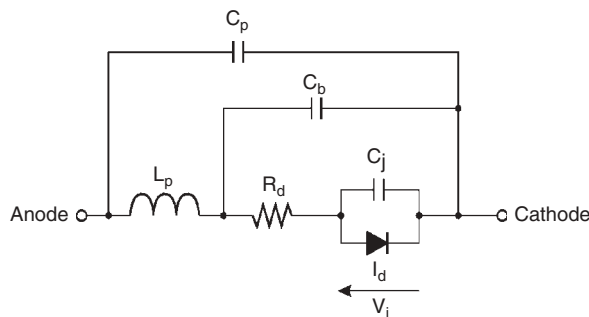
FIGURE 3.1   Large-signal microwave diode model. This model is temperature dependent.

TABLE 3.2   Nonlinear Diode Model

Keyword	Description	Unit	Default
	Intrinsic Model		
IS	Saturation current	A	0
ALFA	Slope factor of conduction current	V^{-1}	38.696
IB	Breakdown saturation current	A	10 mA
VB	Breakdown voltage	V	$-\infty$
E	Power law parameter of breakdown current	—	10.0
CT0	Zero-bias depletion capacitance	F	0
VJ	Built-in barrier potential	V	0.8
GAMA	Capacitance power law parameter	—	0.5
GC1	Varactor capacitance polynomial coefficient 1	V^{-1}	0.0
GC2	Varactor capacitance polynomial coefficient 2	V^{-2}	0.0
GC3	Varactor capacitance polynomial coefficient 3	V^{-3}	0.0
CD0	Zero-bias diffusion capacitance (*pn* diodes)	F	0
AFAC	Slope factor of diffusion capacitance	V^{-1}	38.696
R0	Bias-dependent part of series resistance in forward-bias condition	Ω	0
T	Intrinsic time constant of depletion layer for abrupt-junction diodes	s	0
KF	Flicker noise coefficient	—	0.0
AF	Flicker noise exponent	—	1.0
FCP	Flicker noise frequency shape factor	—	1.0
AREA	Area multiplier	—	1.0
	Extrinsic Model		
CP	Package parasitic capacitance	F	0.0
CB	Beam−lead parasitic capacitance	F	0.0
LP	Package parasitic inductance	H	0.0

TABLE 3.3   Diode SPICE Parameters for Alpha Diodes

Parameter	Unit	SMS1546	SMS3922	SMS3923	SMS3924	SMS3926	SMS3927	SMS3928	SMS7621	SMS7630
I_S	A	3E-7	3E-8	5E-9	2E-11	2.5E-07	1.3E-09	9E-13	4E-8	5E-06
R_S	Ω	4	9	11	11	4	4	4	12	30
n	—	1.04	1.08	1.05	1.08	1.04	1.04	1.04	1.05	1.05
T_d	sec.	1E-11	8E-11	8E-11	8E-11	1E-11	1E-11	1E-11	1E-11	1E-11
C_{J_0}	pF	0.38	0.9	0.93	1.6	0.42	0.39	0.39	0.1	0.14
m	—	0.36	0.26	0.24	0.4	0.32	0.37	0.42	0.35	0.4
E_G	eV	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.69
X_{ti}	—	2	2	2	2	2	2	2	2	2
F_C	—	0.5	0.5	0.5	0.5	0.5	0.5	0.5	5	0.5
B_V	V	3	20	46	100	2	3	4	3	2
I_{BV}	A	1E-5	1E-5	1E-5	1E-5	1.00E-5	1.00E-5	1.00E-5	1E-5	0.0001
V_J	—	0.51	0.65	0.15	0.84	0.495	0.595	0.800	0.51	0.34

diodes and a range of 0.58 to 0.85 volt for various Schottky barrier diodes. This value is sometimes confused with the forward-current voltage drop of the diode or the energy gap of the material; it is *neither* of these, but similar in value usually.

Varying *M* generates a variety of reverse-bias capacitance characteristics. Inspection of the capacitance formula reveals that it predicts infinite capacitance for a forward bias, which is not the case for a real junction. Several depletion−capacitance formulas

have been proposed that more correctly fit observed operation; however, SPICE uses a simple approach: for forward biases beyond some fraction (set by the parameter F_C) of the value for ϕ, the diode current is calculated as the linear extrapolation of the current at the departure. This provides a continuous numerical result and does not affect circuit operation significantly because, for forward bias, the device capacitance is normally dominated by diffusion capacitance.

Another useful form for the depletion capacitance is given by

$$C = C_{\min} \frac{(V_B + \phi)^{1/2}}{(V_R + \phi)^{1/2}} \tag{3.5}$$

where $C_{\min}$ is the capacitance at breakdown, V_R is the reverse-bias voltage, V_B is the breakdown voltage, and ϕ is the built-in potential.

The diffusion charge (and therefore the capacitance) varies with forward current and is simply modeled as a transit time (model parameter T_T) for the carriers to cross the diffusion region of the junction. The total charge is

$$\text{diffusion charge} = \text{device current} \times \text{transit time} \tag{3.6}$$

and capacitance is the derivative, with respect to bias, of this:

$$\text{Diffusion capacitance} = T_T \frac{I_S}{N V_t} \exp\left(\frac{V_j}{N V_t}\right) \tag{3.7}$$

Diffusion charge manifests itself as the *storage time* of a switching diode, which is the time required to discharge the diffusion charge in the junction, which must happen before the junction can be reverse biased (switched off). Storage time is normally specified as the time to discharge the junction so that it is supporting only a fraction (typically 10%) of the initial reverse current. First, a forward current is supplied to the device to charge the junction. Then, as quickly as possible, a reverse current is supplied to the device. Internally, the junction is still forward biased to a voltage nearly the same as before the switch in current; the junction is still conducting at the forward-current rate. This internal current adds to the external current as the total current discharging the junction. As the junction voltage decreases, the internal current falls off exponentially (according to the Shockley equation). This system is a relatively simple differential equation that can be solved to an explicit equation for the T_T parameter (assuming complete discharge) as follows:

$$\text{Transit time} = \frac{\text{storage time}}{\ln[(I_F - I_R)/ - I_R]} \tag{3.8}$$

The diffusion charge dominates the reverse-recovery characteristic of the diode. During the last part of the recovery, as the junction becomes reverse biased, the depletion capacitance dominates. This causes the small tail at the end of the discharge cycle. Total capacitance is taken to be the sum of these capacitances: The depletion approximation dominates for reverse bias as the device current is small, and the diffusion proximity dominates for forward bias as the device current is large.
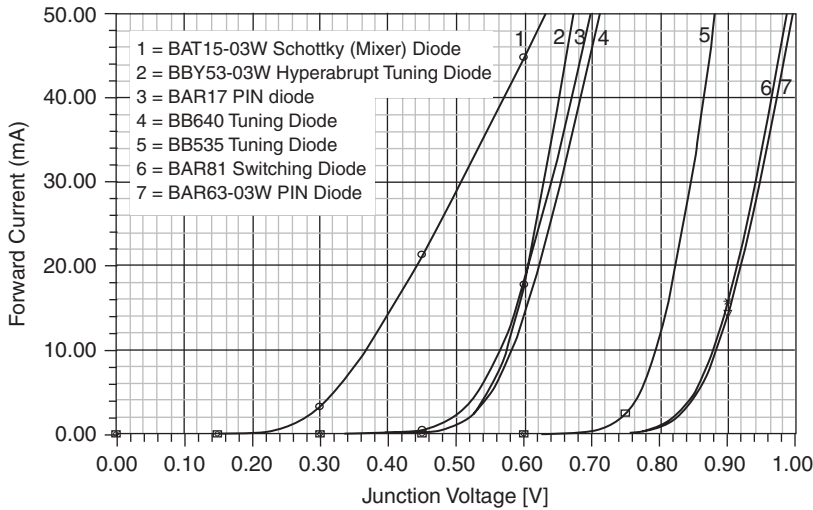
FIGURE 3.2   Direct-current $I-V$ curves for seven diodes, showing various barrier voltages that result from different doping profiles.

A special case for diode application is the switching diode, and its description and application will be part of a later chapter. Figure 3.2 shows the dc $I-V$ curves, which indicate the different voltage potential, that are a result of the different doping profiles.

3.2.2   Mixer and Detector Diodes

Electrical Characteristics and Physics of Schottky Barriers   Schottky barrier diodes differ from junction diodes in that current flow involves only one type of carrier instead of both types. That is, in n-type Schottky, the forward current consists of electrons flowing from the metal (anode) to the n-type material, which is the cathode. Since the number of holes flowing in the opposite direction (flowing from the n-type material into the metal) is negligible, we say the Schottky diode is a majority-carrier (electrons-only) device. Also $T_T = 0$ for Schottky diodes.

Diode action results from a contact potential set up between the metal and the semiconductor, similar to the voltage between the two metals in a thermocouple. When metal is brought into contact with an n-type semiconductor (during fabrication of the chip), electrons diffuse out of the semiconductor, into the metal, leaving a region under the contact that has no free electrons ("depletion layer"). This region contains donor atoms that are positively charged (because each lost its excess electron), and this charge makes the semiconductor positive with respect to the metal. Diffusion continues until the semiconductor is so positive with respect to the metal that no more electrons can go into the metal. The internal voltage difference between the metal and the semiconductor is called the contact potential and is usually in the range of 0.3 to 0.8 V for typical Schottky diodes. A cross section is shown in Figure 3.3.

When a positive voltage is applied to the metal, the internal voltage is reduced, and electrons can flow into the n-type cathode material. The process is similar to thermionic emission of electrons from the hot cathode of a vacuum tube, except that the electrons are "escaping" into the cathode material instead of into a vacuum. Unlike the vacuum
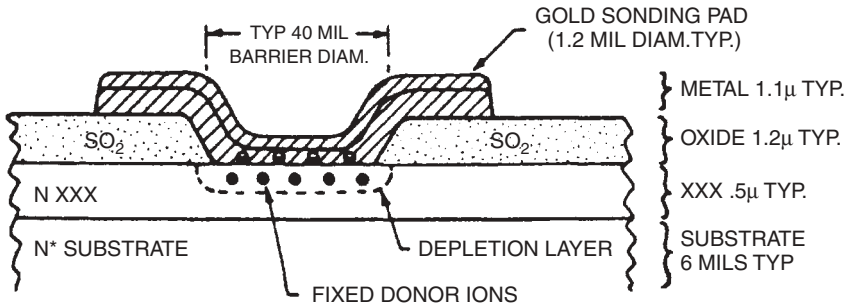
FIGURE 3.3   Schottky diode chip cross section.

tube case, room temperature is "hot" enough for this to happen if enough voltage is applied. However, only those electrons whose thermal energy happens to be many times the average can escape, and these "hot electrons" account for all the forward current from the semiconductor into the metal.

One important thing to note is that there is no flow of minority carriers from the metal into the semiconductor and thus no neutral plasma of holes and electrons is formed. Therefore, if the forward voltage is removed, current stops "instantly" and reverse voltage can be established in a few picoseconds. There is no delay effect to charge storage as in junction diodes. This accounts for the exclusive use of Schottky barrier diodes in microwave mixers, where the diode must switch conductance states at microwave oscillator rates.

The voltage–current relationship for a Schottky barrier diode is described by the Richardson equation (which also applies to thermionic emission from a cathode). The derivation is given in many textbooks:

$$I = A A_{\mathrm{RC}} T^2 \exp\left(-\frac{q\phi_B}{kT}\right)\left[\exp\left(\frac{qV_J}{kT}\right) - M\right] \tag{3.9}$$

where A = area (cm^2)

$\quad A_{\mathrm{RC}}$ = modified Richardson constant ($\mathrm{A/K^2/cm^2}$)

$\quad k$ = Boltzmann's constant

$\quad T$ = absolute temperature (K)

$\quad \phi_B$ = barrier height (V)

$\quad V_J$ = external voltage across depletion layer (positive for external voltage),

$\qquad = V - IR_S$

$\quad R_S$ = series resistance

$\quad M$ = avalanche multiplication factor

$\quad I$ = diode current (A) (positive forward current)

The barrier height ϕ_B is typically a few tenths of a volt higher than the contact potential ϕ_C (about 0.15 V higher than ϕ_C for silicon). This equation agrees well with experimental data for diodes without surface leakage but is difficult to use because A_{RC}, ϕ_B, and M are all dependent on applied voltage.

The major cause for variation in ϕ_B with voltage is the so-called image effect, in which the barrier height is lowered as the electric field near the metal is increased, especially at the edges.

A better equation for circuit designers to use is one in which all parameters are independent of voltage and current. The simplest one that agrees reasonably well with Richardson's equation is

$$I = I_S \left[\exp\left(\frac{V_J}{0.028} \right) - 1 + \frac{K}{1 - V_B/V} \right] \qquad (3.10)$$

where I_S = "saturation current" (a temperature-dependent quantity)

    $0.028 = nkT/q$ at room temperature ($n = 1.08$)

        n = forward slope factor (derived from the variation of ϕ_B with forward voltage)

        K = reverse slope factor (expressing the variation of ϕ_B with reverse voltage)

       V_B = breakdown voltage (the voltage at which $M = 1$)

As before, V and I are considered positive for forward bias and negative for reverse bias.

Typical ranges for these parameters for microwave Schottky and point-contact mixer diodes are as follows:

  I_S: 10^{-12} to 10^{-5} A

   n: 1.04 to 1.10

  R_S: 2 to 20 Ω

  K: 8 to 100

  V_B: 2 to 20 V

The quantities I_S and 0.028 are strongly temperature dependent, while both R_S and V_B increase with temperature to a slight degree. Series resistance R_S increases with current at high current levels (due to carrier velocity saturation) but is essentially independent of current at 10 mA and below for mixer diodes. Thus, for normal mixer and detector operation, R_S can be considered constant.

Agreement between Eqs. (3.9) and (3.10) is not perfect but (3.10) is much easier to use and is preferred by most circuit designers. A comparison of the two equations near zero bias gives the following relationship between zero-bias barrier height ϕ_0 and saturation current:

$$I_S = A A_{\mathrm{RC}} T^2 \exp -\frac{q\phi_0}{kT}$$

$$\cong \left(\frac{10^7 A}{\mathrm{cm}^2} \right) A \exp\left(-\frac{\phi_0}{0.026} \right) \quad \text{(for } n \text{ silicon at room temperature)} \quad (3.11)$$

Small-Signal Parameters By combining Eqs. (3.10) and (3.11), the values of the parameters in Eq. (3.9) can be derived from a few simple measurements. Many specific equations can be derived, but the following are commonly used for production measurements:

$$R_S = \frac{V_{F10} - V_{F1} - 0.065}{0.009} \qquad \text{(for } n = 1.08) \qquad (3.12)$$

$$\phi_0 = \frac{V_{F1} - 0.001 R_S + 0.28 + 0.12 \log_{10} D}{1.08} \qquad (3.13)$$

$$n = \frac{V_{F1} - V_{F0.1} - 0.0009 R_S}{0.060} \tag{3.14}$$

$$K = \left(\frac{I_{R1}}{I_S} - 1\right) V_B \tag{3.15}$$

$$I_S = \exp\left(-\frac{V_{F1}}{0.028} + \frac{R_S}{28}\right) \qquad \text{(mA)} \tag{3.16}$$

where $V_{F0.1}$, V_{F1}, and V_{F10} are the forward voltages at 0.1, 1, and 10 mA, respectively, and I_{R1} is the reverse current at 1 V. (The derivation of these equations requires that I_S be small compared to 0.1 mA.) The quantity D is the diameter of the metal–silicon contact in mils. Measuring V_{F1} at 1 and 10 mA instead of some other current levels leads to the best accuracy for typical mixer diodes.

The total dynamic resistance for a forward-biased diode is given by

$$R_T = \frac{dV}{dI} = R_S + \frac{nkT}{q(I + I_S)} = R_S + R_B \tag{3.17}$$

and

$$R_B = \frac{28}{I + I_S} \qquad \text{at room temperature (with } I \text{ and } I_S \text{ in mA, } n = 1.08) \tag{3.18}$$

This equation is also good at zero bias (unless K is very large or there is significant surface leakage). That is,

$$R_0 = R_S + \frac{28}{I_S} \tag{3.19}$$

For reverse voltages of a few volts, the dynamic resistance is dominated by the K term:

$$R_R = \text{reverse resistance} = \frac{dV}{dI} \cong \frac{V_B}{K I_S} \tag{3.20}$$

For typical values of I_S, R_0 is larger than 5000 Ω and R_R is larger than 100 kΩ. For some zero-bias Schottky applications, it is desirable for R_0 to be made smaller than this.

The factors that determine R_S are the thickness of the epitaxial layer, the epi doping level (N_D), the barrier diameter, the substrate resistivity ("spreading resistance"), the contact resistances of the metals used for the barrier and the substrate contact, and the resistance associated with the bonding wire or whisker. The barrier height is about 0.15 V higher that the contact potential between the barrier metal and the semiconductor and is influenced by the method used to apply the metal, conditions at the edge of the junction, and the doping level. Saturation current depends on barrier height, junction area, and temperature and the slope factors n and K depend on doping level, punchthrough voltage, and edge conditions.

Junction Capacitance   The capacitance of a Schottky barrier chip results mainly from two sources: the depletion layer under the metal–semiconductor contact and the

capacitance of the oxide layer under the bonding pad (the so-called overlay capacitance). The bonding pad is required because the typical Schottky barrier diameter is so small that it is impractical to bond directly to the metal on the junction. If the semiconductor epitaxial layer is uniformly doped, the capacitance–voltage characteristic is similar to that of a textbook "abrupt-junction" diode:

$$C_J = \frac{\varepsilon_S \varepsilon_0 A'}{X_D} + C_0 \tag{3.21}$$

$$X_D = \sqrt{\frac{2\varepsilon_S \varepsilon_0 (\phi_C - V)}{qN}} \tag{3.22}$$

where ϕ_C = contact potential
C_0 = overlay (bonding pad) capacitance
ε_S = dielectric constant of the semiconductor (11.7 for Si or 12.8 for GaAs)
N = doping level for the epitaxial layer
A' = effective contact area, including fringing corrections

In practical terms, the capacitance can be related to the 0-V barrier capacitance defined by

$$C_{B0} = \frac{\varepsilon_S \varepsilon_0 A'}{X_{D0}} \tag{3.23}$$

where

$$X_{D0} = \sqrt{\left(\frac{1.3 \times 10^{15}}{N_D}\right)\phi_C} \qquad (\mu m) \tag{3.24}$$

The resulting $C-V$ relationship can be written as

$$C_J = \frac{C_{B0}}{\sqrt{1 - V/\phi_C}} + C_0 \tag{3.25}$$

The contact potential ϕ_C is related to the barrier height as follows:

$$\phi_C = \phi_B - 0.026\left[1 + L_n\left(\frac{N_C}{N}\right)\right]$$

$$\cong \phi_B - 0.15 \qquad \text{(for silicon with } N = 10^{17}) \tag{3.26}$$

The theoretical meaning of these terms can be clarified by looking at Figure 3.4.

3.2.3 Parameter Trade-Offs

Barrier Height   The barrier height of a Schottky diode is important because it directly determines the forward voltage. To get a good noise figure, the LO drive voltage V_L must be large compared to V_T, which is essentially V_{F1}. Normally, it is best to have a low forward voltage (low V_{F1}), or low drive diode, to reduce the amount of LO power needed. However, if a high dynamic range is important, high LO power is needed, and the diode can have a higher V_F and should also have a high V_B (see Table 3.4).
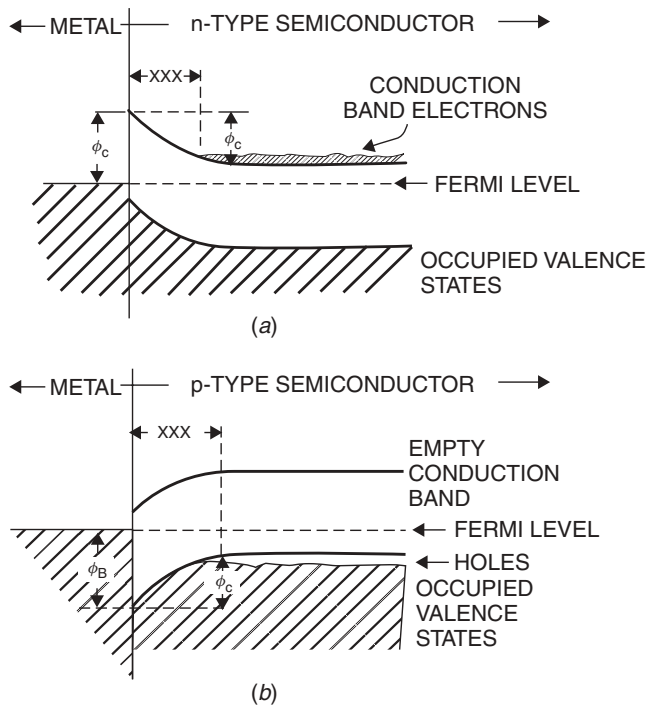
FIGURE 3.4 Schottky diode band diagrams: (*a*) forward bias; (*b*) reverse bias.

TABLE 3.4 Barrier Height Versus LO Power

Type	Typical V_{F1}	LO Power (mW)	Application
Zero bias	0.10–0.25	<0.1	Mainly for detectors
Low barrier	0.25–0.35	0.2–2	Low-drive mixers
Medium barrier	0.35–0.50	0.5–10	General purpose
High barrier	0.50–0.80	>10	High dynamic range

Noise Figure Versus LO Power At low LO drive levels, the noise figure is poor because of poor conversion loss, due to a too-low conduction angle. At very high LO drive levels, the noise figure again increases due to diode heating, excess noise, and reverse conduction.

If a high LO drive level is needed, for example, to get higher dynamic range, a high V_B (>5 V) should be specified. However, nature requires that you play for this with higher R_S (lower f_C), so the noise figure will be degraded compared to what could be obtained with diodes designed for lower LO drive. Forward voltage and breakdown are basically independent parameters, but high breakdown is not needed or desirable unless high LO power is used.

Such a high-breakdown diode will have low reverse current (which is important only if the diode has to run hot).

Silicon Versus GaAs   Typical silicon Schottky diodes have cutoff frequencies in the 800- to 2000-GHz range, which is good enough through the Ku band [3.8, 3.9].

At the Ku band and above or for image-enhanced mixers, higher f_C may be needed, which calls for the use of GaAs diodes. These have lower R_S due to higher mobility, which translates to cutoff frequencies in the 1000- to 4000-GHz range.

However, if intermediate frequency (IF) is low, be careful; GaAs diodes have high $1/f$ flicker noise. They also have high V_{F1}, so more LO power is required.

C_J Versus Frequency   There is a lot of latitude in choosing C_J. However, in general, the capacitive reactance should be a little lower than the transformed line impedance (Z_0). If Z_0 is not known, a good way to start is to use X_C values of 50–100 Ω. Experience has shown that most practical mixers use an X_C near this value (a little higher in the waveguide and lower in 50-Ω systems). This translates to the following rule of thumb for choosing the junction capacitance of a diode for operation at frequency f (in GHz):

$$C_{J0} \approx \frac{100}{\omega} \approx \frac{1.6}{f} \qquad \text{(pF)} \qquad (3.27)$$

To evaluate possible tolerances, we show the range of forward currents as a function of diode voltage (Fig. 3.5), the junction capacitance as a function of the bias voltage
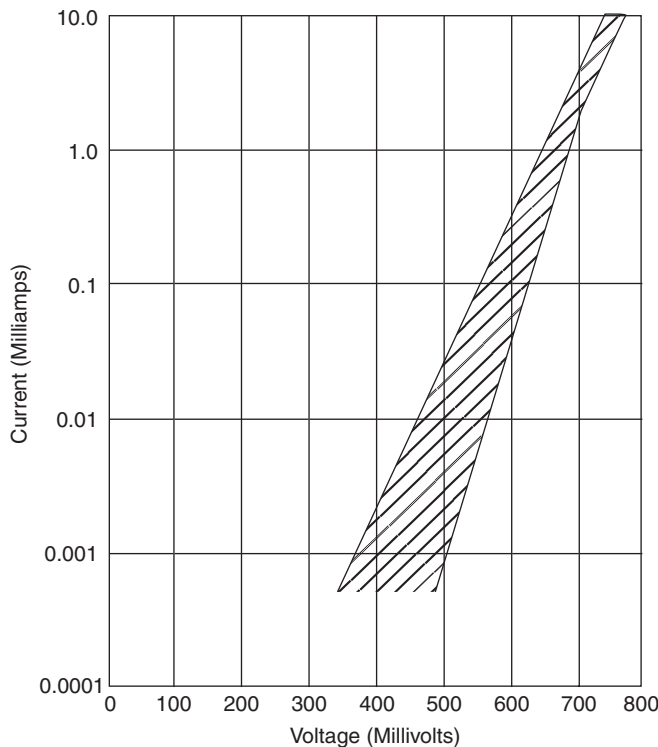
FIGURE 3.5   Forward dc characteristic curve range—voltage versus current.
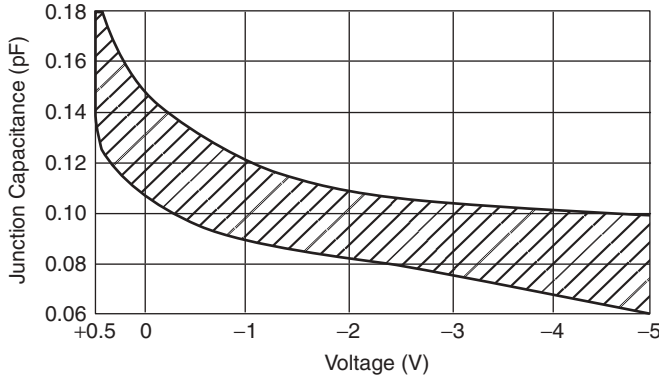
FIGURE 3.6   Junction capacitance range versus voltage.
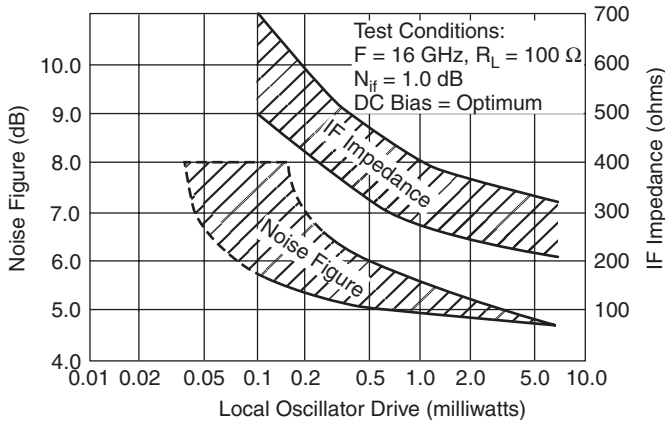
FIGURE 3.7   RF parameters versus LO drive level.

(Fig. 3.6), and finally some important RF parameters, such as noise figure and IF impedance, as a function of the LO drive (Fig. 3.7).

3.2.4 Mixer Diodes

As an example of some of the parameters for mixer diodes, Table 3.5 gives data on some of the X-band mixer diodes. The NF is measured at 9.375 GHz.

Linear Diode Model   Figure 3.8 shows the linear diode model. Its keywords appear in Table 3.6. Circuit simulators such as those supplied by Ansoft and Agilent provide a model library that has SPICE-type parameters for diodes (regular diodes, varactor diodes, and *pin* diodes) as well as bipolar transistors and FETs, which will be discussed later.

TABLE 3.5   X-Band Mixer Diodes

Material	Barrier	Typical V_F (at 1 mA)	Typical F_{C0} (GHz)	Typical R_S (Ω)	Typical C_{J0} (pF)	Maximum NF (dB)
n GaAs	high	.70	1000	—	0.15	5.0[a]
n GaAs (BL)	high	.70	500	—	0.15	6.0[a]
n GaAs (chip)	high	.70	1000	—	0.15	5.3[a]
n silicon (BL)	low	.28	150	6	0.20	6.5
n silicon (quad)	low	.28	150	6	0.20	6.5
p silicon (BL)	low	.28	150	12	0.20	6.5
n silicon (BL)	high	.60	100	8	0.20	6.5
n silicon (quad)	high	.60	100	8	0.20	6.5
n silicon	low	.28	200	6	0.15	5.5
p silicon	low	.28	200	18	0.14	6.0
p silicon	med	.40	150	12	0.12	6.5
n silicon	low	.28	150	8	0.18	6.5
p silicon	low	.28	150	12	0.18	6.5

[a] Specified for $N_{IF} = 1.0$ dB.
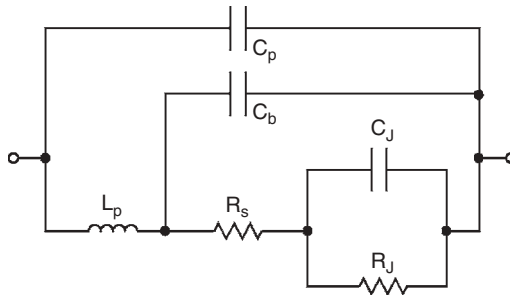
FIGURE 3.8   Linear diode model. This model is temperature dependent.

TABLE 3.6   Linear Diode Model

Keyword	Description	Unit	Default
LP	Package inductance	H	0.0
CB	Beam lead capacitance	F	0.0
CP	Package capacitance	F	0.0
RS	Contact resistance	Ω	0.0
RJ	Junction resistance	Ω	
CJ	Junction capacitance	F	

3.2.5 *pin* Diodes

Introduction   The *pin* diode [3.8], in comparison with other microwave semiconductor devices, is fairly easy to understand. This make it possible to reduce complex

behavior to simple terms and enables the microwave engineer to grasp the operating principles and design details of this family of devices.

We do not attempt to describe the many possible microwave circuits in which *pin* diodes are used. Rather, we attempt to explain the behavior of the diode in all aspects, giving the facts and some of the theory behind the facts. We offer the circuit designer the opportunity to understand the *pin*, so that he or she can understand its behavior in circuits. We assume the reader knows the circuit equations; to that knowledge we hope to add diode equations.

Most of the material presented consists of generalized data and explanations of the behavior of *pin* diodes; we conclude with a brief description of circuit performance, test methods, and some hints on proper *pin* specification writing.

The user can then evaluate the trade-offs involved in diode design and performance and be able to select the most nearly optimum diode from the wide range of diodes offered.

Large-Signal pin Diode Model   Figure 3.9 shows the large-signal model for a *pin* diode. Table 3.7 lists its keywords.

Notes on the pin Diode Model

1. The *pin* diode model is used to model a bias-dependent RF resistance for use in *pin* diode circuits such as attenuators and switches. The resistance varies from R_{max} to R_S using the R function above. A typical R-versus-I characteristic is shown in Figure 3.10 with parameters $I_S = 5.96$ nA, $R_S = 2.016$, $R_{max} = 6500$, $K_1 = 0.1272$, $K_2 = 1.0$, $N = 2.077$.

2. The transit time parameter T_T can also be used to approximately model a switching *pin* diode's reverse-recovery time—a value often provided by diode manufacturers.

3. Diode breakdown can be modeled by specifying IBV and BV parameters.

4. The reverse-bias capacitance characteristics can be more accurately modeled than the common expression derived from *pn* junction theory. The capacitance grading coefficient exponent can be expressed as a polynomial function of voltage by specifying values for GC1, GC2, and GC3.
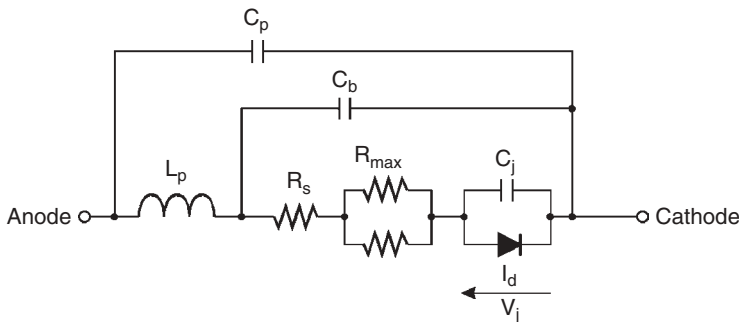
FIGURE 3.9   Large-signal *pin* diode model. This model is temperature dependent.

TABLE 3.7 *pin* **Diode Model**

Keyword	Description	Unit	Default
	Intrinsic Model		
IS	Saturation current	A	1.0×10^{-14}
N	Emission coefficient	—	1.0
IBV	Magnitude of current at reverse breakdown voltage	A	1.0×10^{-14}
BV	Magnitude of reverse breakdown voltage	V	∞
FC	Coefficient for forward-bias depletion capacitance	—	0.5
CJ0	Zero-bias *pn* junction capacitance	F	0.0
VJ	Built-in junction potential	V	1.0
M	*pn* Junction grading coefficient	—	0.5
GC1	Varactor capacitance polynomial coefficient 1	V^{-1}	0.0
GC2	Varactor capacitance polynomial coefficient 2	V^{-2}	0.0
GC3	Varactor capacitance polynomial coefficient 3	V^{-3}	0.0
TT	Transit time	s	0.0
K1	Variable resistance coefficient	V	0.0
K2	Variable resistance current exponent	—	1.0
RMAX	Maximum resistance of *pin* intrinsic region	Ω	0.0
KF	Flicker noise coefficient	—	0.0
AF	Flicker noise exponent	—	1.0
FCP	Flicker noise frequency shape factor	—	1.0
AREA	Area multiplier	—	1.0
	Extrinsic Model		
RS	Series resistance (minimum resistance of *pin* diode)	Ω	0.0
CP	Package parasitic capacitance	F	0.0
CB	Beam-lead parasitic capacitance	F	0.0
LP	Package parasitic inductance	H	0.0
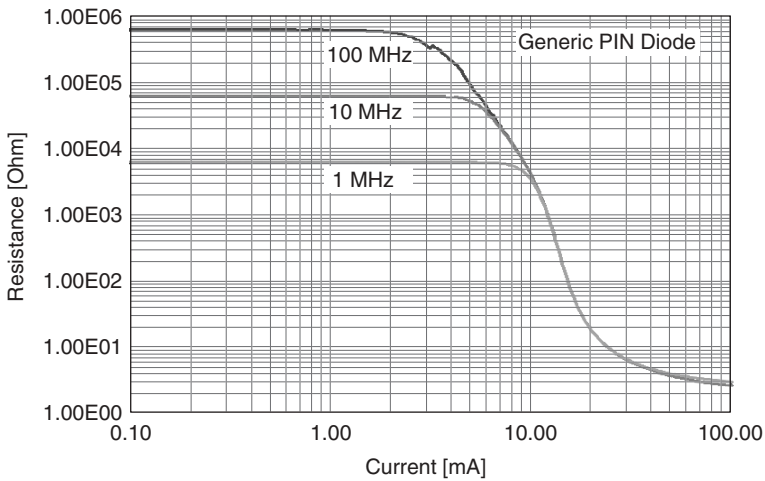
FIGURE 3.10   Simulated *pin* diode resistance as function of dc at 1, 10, and 100 MHz.

5. The *pin* diode model was derived from J Walston [3.10].

6. Following Sze [3.11], the variable resistance may be modeled by setting

$$R_i = \frac{3}{8} V_T \frac{W^2}{D_a \tau_a I_F} \tag{3.28}$$

where W = width of intrinsic region

   D_a = ambipolar diffusion coefficient

   τ_a = ambipolar lifetime

   V_T = thermal voltage

   I_F = forward current

Basic Theory: Variable Resistance   Intrinsic or "pure silicon" as it can be grown in a laboratory is an almost lossless dielectric. Some of its physical properties include the following:

Dielectric constant (relative)	11.7
Dielectric strength	400 V/mil (approximate)
Specific density	2.3
Specific heat	0.72 J/g/°C
Thermal conductivity	1.5 W/cm/°C
Resistivity	300,000 Ω-cm

Since a *pin* diode is valuable essentially because it is a variable resistor, let us concentrate initially on the resistivity. Consider a volume comparable to a typical *pin* diode chip, say 20 mils in diameter and 2 mils thick. This chip has a dc resistance of about 0.75 MΩ. High resistivity in any material indicates that most of the likely carriers of electric charge, electrons and holes, are tightly held in the crystal lattice and cannot "conduct."

In real life there are impurities (typically boron) that cannot be segregated out of the crystal. Such impurities contribute carriers, holes or electrons, that are not very tightly bound to the lattice and therefore lower the resistivity of the silicon.

Through various techniques we can adjust the level of impurities, called *dopants*, to produce resistivities ranging from 10 kΩ-cm (for good *pin* diodes) to 0.001 Ω-cm (for substrates).

If the impurity adds "electrons" to the crystal, it is called a *donor*; if it adds a hole, it is called an *acceptor*. Boron adds holes, hence it is an acceptor, and the silicon–boron combination is called *p*-type, or *positive*, because it has an excess of positive carriers. Phosphorus, on the other hand, is a *donor*, adding electrons, and the corresponding mix is *n*-type, or *negative*.

There are many concepts important to the physicist but not to the diode user that elaborate upon the impact of impurities on the behavior of silicon. The more carriers added, the lower the resistivity.

If one wished to vary the resistance of a given diode, in principle he or she could bring it into a semiconductor laboratory, add or subtract carriers as desired, and perhaps even make the process reversible. However, this is a slow, expensive, and impractical way to make a variable resistor; one would be better advised to take a wrench and a soldering iron and replace a component.

The *pin* diode derives its value from the fact that the free charge carrier concentration in silicon, and hence its resistance, can be varied electronically by means of current from a simple bias supply. This can be done rapidly (in nanoseconds in some cases), reversibly, repeatably, and accurately. The thing that makes this possible is called a *junction*, the interface between the relatively pure silicon in the middle of the *pin* diode (the *i* stands for *intrinsic*) and the heavily doped layers on either end, p^+ and n^+. The p^+ region is rich in holes; the n^+ region is rich in electrons. Both of these regions have low resistance. The *i* region is the variable resistive element in the diode (see Fig. 3.11). In the absence of any external bias, internal effects within the crystal keep the charges fixed; the resistance of the *i* region is high.

When the p^+ region (anode) is biased positively with respect to the n^+ region (cathode), the interface potential "barrier" is overcome. And direct current flows in the form of holes streaming from p^+ toward n^+, with electrons moving in the opposite direction; we say that free carriers have been injected into the *i* region. The resistance of the *i* region becomes low.

The number of free carriers within the *i* region determines the resistivity of the region and thus the resistance of the diode.

Consider "one hole" and "one electron" drifting in opposite directions in the *i* region under the impetus of the applied field. Under certain conditions, imperfections in the silicon may cause these carriers to recombine. They are no longer available to constitute current or to lower the resistivity of the *i* region.

It can be shown that the amount of "recombination" between holes and electrons that continuously takes place in a semiconductor is governed by a property of the lattice called *lifetime*. In fact, lifetime is defined as the reciprocal of recombination rate.

Thus $Q_S = Q_0 \exp(-t/T_L)$, where Q_S is the total amount of free charge "stored" in the *i* region and T_L is the lifetime, or the mean time between recombination events. In a steady-steady condition, the bias supply must deliver current to maintain constant Q_S. The required current is

$$I_{\text{dc}} = \frac{Q_S d}{dt} = -\frac{Q_S}{T_L} \tag{3.29}$$

or $Q_S = I_{\text{dc}} T_L$, dropping the minus sign.

Ignoring some details that are not crucial to this section, we can now calculate the resistance of a given diode of area A and thickness W (W stands for *base width*, the width or thickness of the intrinsic layer). The p^+ and n^+ regions have essentially zero resistance, as they are very heavily doped.
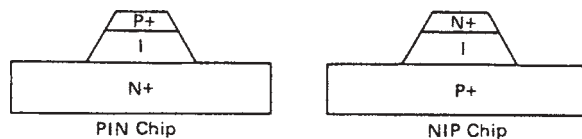
Note: Chips and diodes of either PIN or NIP polarity are generally available for any application. The only basic difference is the polarity of the heat sink end of the diode.

FIGURE 3.11   General outline of *pin* diode construction.

The resistivity of a given material is inversely proportional to the number of free carriers, N, and the mobility (not quite the same as velocity) of the carriers. Thus

$$\rho = \frac{1}{q(\mu_n N + \mu_p P)} \tag{3.30}$$

Both holes and electrons, μ_n, μ_p, are mobilities of electrons and holes and N, P are numbers of electrons and holes. Simplifying,

$$\rho = \frac{C}{Q_S d} \tag{3.31}$$

where C is a collection of constants and $Q_S d$ is the stored charge density (numbers per unit volume). For our piece of silicon, the volume is WA, and

$$Q_S d = \frac{Q_S}{WA} \tag{3.32}$$

The resistivity is

$$\rho = \frac{CWA}{Q_S} \tag{3.33}$$

and the resistance is

$$R_S = \rho\frac{W}{A} = \frac{CW^2}{I_{\text{dc}} T_L} \tag{3.34}$$

This is a fundamental equation in *pin* diode theory and design.

Rigorous analysis shows that

$$R = \frac{2Kt/q}{I_f} \sinh\left(\frac{W}{2\sqrt{DT_L}} \tan^{-1}\left[\sinh\frac{W}{2\sqrt{DT_L}}\right]\right) \tag{3.35}$$

where K = Boltzmann's constant

$\quad\ \ T$ = temperature (K)

$\quad\ \ D$ = diffusion coefficient, $= \mu KT/q$

For most *pin* diodes, W/DT_L is less than unity, and the equation simplifies to the simple equation above.

Typical data on R_S as a function of bias current are shown in Figure 3.12. A wide range of design choices are available, as the data indicate. Many combinations of W and T_L have been developed to satisfy the full range of applications.

Breakdown Voltage, Capacitance, and Q Factor   The previous section on R_S explained how a *pin* diode can become a low resistance, or a "short." This paragraph will describe the other state: a high impedance, or an "open." Clearly, the better *pin* diode is the one that has the better on–off ratio at the frequency and power level of interest.

If we return to the undoped, or intrinsic, i region, we note that it is an almost lossless dielectric. As such, it has a dielectric strength of about 400 V/mil, and all *pin* diodes have a parameter called V_b, breakdown voltage, which is a direct measure of the width of the i region. Voltage in excess of this parameter results in a rapid increase
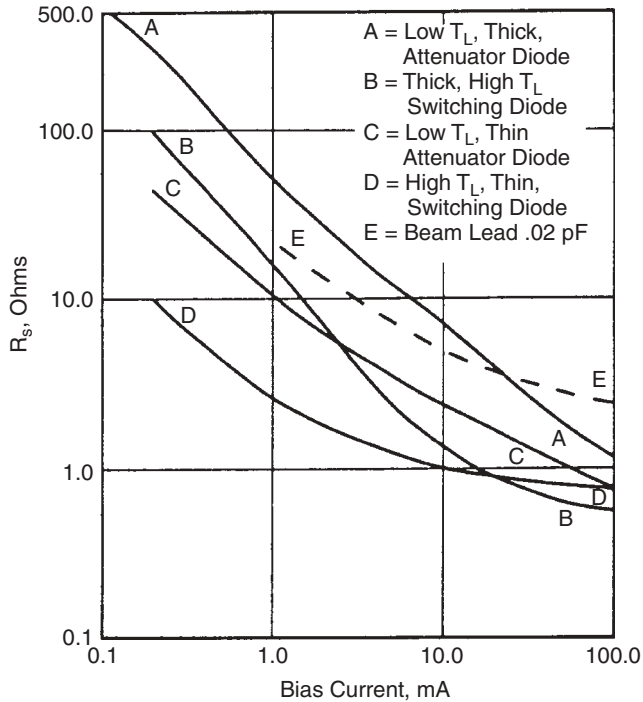
**FIGURE 3.12** Typical series resistance as function of bias (1 GHz).

in current flow (called avalanche current) (Fig. 3.13). When the negative bias voltage is below the bulk breakdown of the *i* region, a few nanoamperes will be drawn. As V_b is approached, the leakage current increases often gradually, as is exaggerated in the curve. This current is primarily caused by less-than-perfect diode fabrication, although there is some contribution from temperature. Typically, the leakage current occurs at the periphery of the *i* region. For this reason, various *passivation* materials (silicon dioxide, silicon nitride, hard glass) are grown or deposited to protect and stabilize this surface and minimize leakage. These techniques have been well advanced over the years, and *pin* diode reliability has improved as a result.

Most diodes are specified in terms of minimum V_b for a nominal leakage, usually 10 μA.

It will be noted later that RF voltage swings in excess of the rated V_b are permitted, for the mechanisms causing leakage current do not always respond at radio frequencies. However, bulk breakdown is effectively instantaneous, and that voltage should never be exceeded.

The next characteristic of our "open" circuit is the capacitance. In simplest form, the capacitance of a *pin* diode is determined by the area and width of the *i* region and the dielectric constant of silicon; however, we have discussed the fact that intrinsic material does contain some carriers and therefore has some conductivity. An *E* field could not exist unless all these carriers were swept out, or depleted.

Application of a reverse bias accomplishes this. At zero bias, the excess carriers on either side of the junction are separated, held apart, by "built-in" fields. This is the contact potential (about 0.5 V for silicon). If there are only a few excess carriers in the
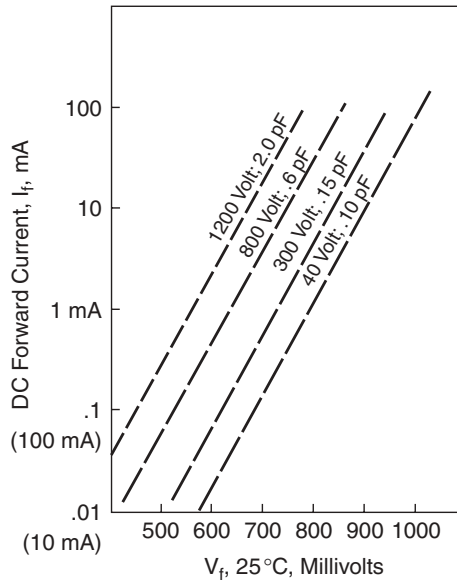
FIGURE 3.13   Voltage versus current for various *pin* diodes.

i region, this "potential" can separate the charges more easily. The junction "widens" in the sense that, starting at the p^+ and *i* interface, there is a region of no free carriers called the *depletion zone*. Beyond this depletion zone the *i* region still contains the free charges with which it started. With the application of reverse bias, the depletion zone widens. Eventually, at a bias equal to a so-called *punchthrough* voltage (V_{PT}), the depletion zone fills the entire *i* region. At this voltage, the 1-MHz capacitance bottoms out and the diode *Q* reaches its maximum. Figure 3.14 illustrates the equivalent circuit of the *i* region before punchthrough.

Some very interesting facts can be derived from this model. Consider the undepleted region; this is a lossy dielectric consisting of a volume (area *A*, length *l*) of silicon of permittivity 12 and resistivity ρ. The capacitance is

$$12\frac{\varepsilon_0 A}{l} \tag{3.36}$$
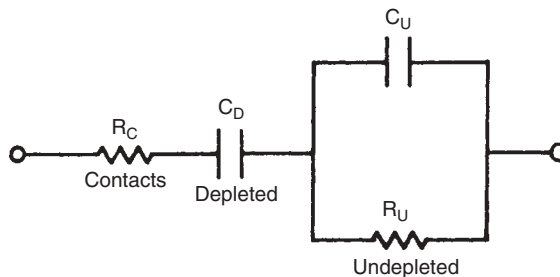
FIGURE 3.14   Equivalent circuit of *i* region before punchthrough.

and the admittance is

$$2\pi \frac{(12\varepsilon_0 A)}{l} f \qquad (3.37)$$

The resistance is $\rho l / A$ and the conductance is $A/\rho l$.

At very low frequencies, the undepleted zone looks like a pure resistor. At very high frequencies it looks like a lossy capacitor. The "crossover" frequency depends on the resistivity of the i region material. For ρ of 160 Ω-cm, the frequency is 1 GHz. Higher resistivity is generally used for *pin* diodes—say, 1000 Ω-cm—and the crossover frequency is 160 MHz.

Diode manufacturers measure junction capacitance at 1 MHz; clearly, what is measured is the depletion zone capacitance.

If the i region thickness is W and the depletion with X_d, the undepleted region is $W - X_d$.

The capacitance of the depleted zone is, proportionally,

$$\frac{1}{X_d} \qquad (3.38)$$

and that of the undepleted zone is

$$\frac{1}{W - X_d} \qquad (3.39)$$

The 1-MHz capacitance as a function of reverse bias is seen in Figure 3.15.

The 1-MHz capacitance decreases with bias until punchthrough, where $X_d = W$. However, at microwave frequencies well above the crossover, the junction looks like two capacitors in series:

$$C_T = \frac{C_d C_u}{C_d + C_u} \alpha \frac{1}{W} \qquad (3.40)$$

That is, the microwave capacitance tends to be constant, independent of X_d and bias voltage.
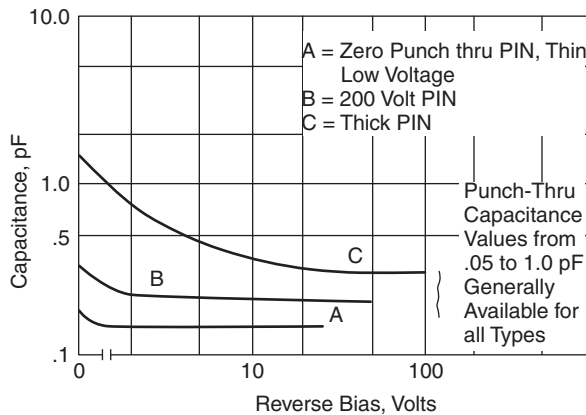
FIGURE 3.15   Typical 1-MHz capacitance.

However, since the undepleted zone is lossy, an increase in bias up to the punchthrough voltage reduces the loss.

At any given frequency, the equivalent network can now be drawn as Figure 3.16.

The equivalent series resistance of the undepleted region is now R_v. Typical R_v data are shown in Figure 3.17.

An alternate equivalent network is shown in Figure 3.18, and typical R shunt data are shown in Figure 3.19.

A good way to understand the effects of series resistance is to observe the insertion loss of a *pin* chip shunt mounted in a 50-Ω line, as shown in Figure 3.20.

An accepted way to include reverse loss in the figure of merit of a *pin* diode is to write

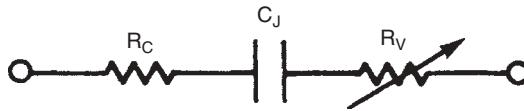$$Q = \frac{1}{2\pi C \sqrt{R_s R_v}} \tag{3.41}$$

FIGURE 3.16   Simplified equivalent circuit, series.
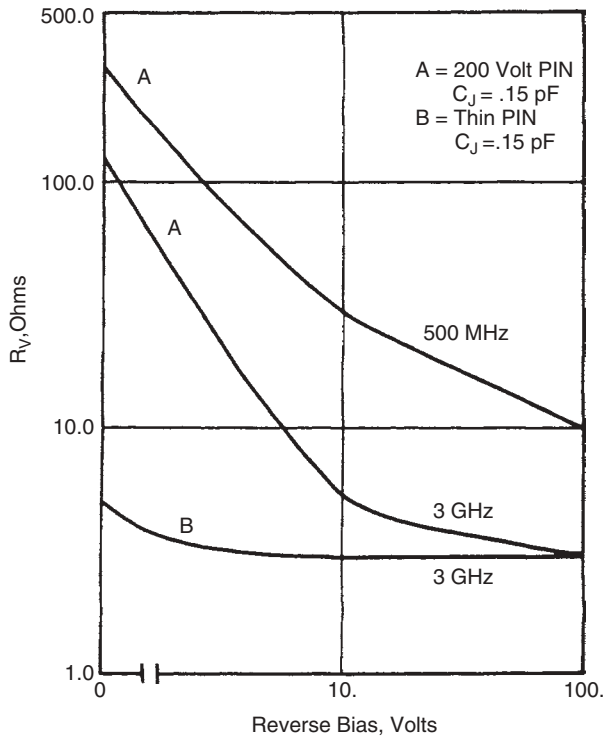
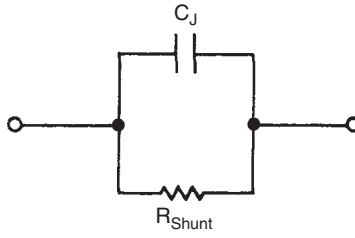

FIGURE 3.17   Reverse series resistance R_v.

FIGURE 3.18   Simplified equivalent circuit, shunt.
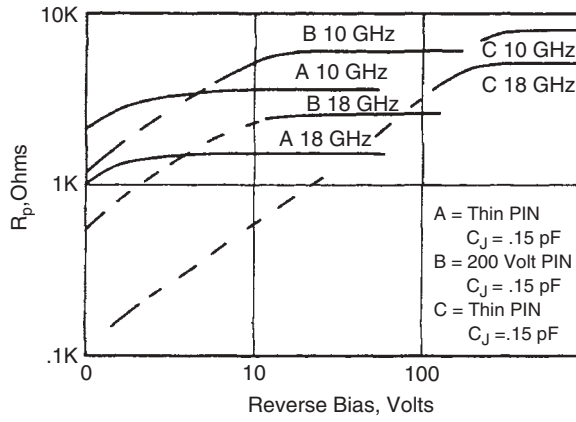

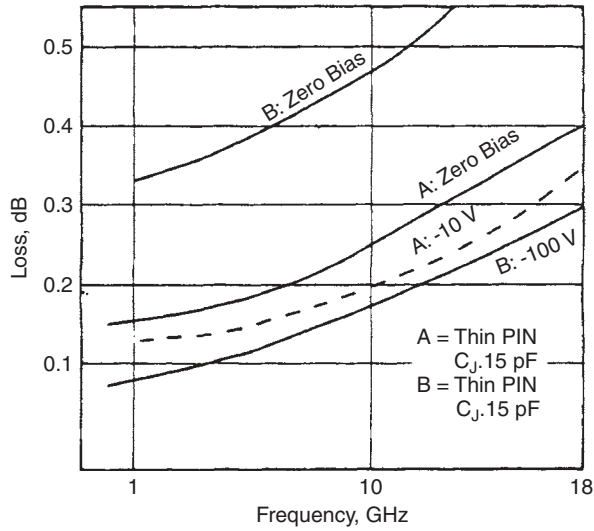**FIGURE 3.19**   Reverse shunt resistance R_p.

FIGURE 3.20   Insertion loss versus frequency.

where R_s and R_v are measured under the expected forward- and reverse-bias conditions at the frequency of interest.

The punchthrough voltage is a function of the resistivity and thickness of the i region. It is advisable to measure loss as a function of bias voltage and RF voltage to determine if the correct diode has been selected for your application. (*Note*: At frequencies below crossover and diodes with thin i regions, the effective junction capacitance can increase substantially at low forward bias, on the order of 1 to 200 μA.)

Incidentally, if you are working with *pin* or *nip* chips that do not have an opaque covering, note that *pin* diodes are photosensitive. Incident light causes photogeneration of carriers in the i region, increasing the chip's insertion loss.

pin Diode Applications   If the intrinsic zone is thick (10 to 100 μm), we then have a high-reverse-voltage rectifier with a low forward-voltage drop at high current or, in other words, a highly efficient rectifier. The low forward voltage results from the fact that the conductivity of the i zone can be modulated by large amounts of charge carriers injected from the p and the n zones.

Another application of *pin* diodes is the high-frequency (HF) field. Here, the fact is exploited that, due to the long carrier lifetime at frequencies beyond approximately 10 MHz, a rectifying effect will no longer occur and the *pin* diode rather behaves like a real resistance the magnitude of which depends on the forward direct current passed by the device and produces an equal effect on both half waves of the HF signal. In view of this behavior, the *pin* diode can be used as a switch or a variable resistor for HF signals. Thus it becomes possible, for example, to subject an HF signal to amplitude modulation by means of an amplitude-frequency (AF)-controlled *pin* diode.

An important application of *pin* diodes that has found favor in recent times is their application to dc-operated attenuators in TV tuners and antenna distribution amplifiers. Figure 3.21 shows the real HF forward resistance r_f as a function of the forward current I_f measured at 100 MHz. Figures 3.22 and 3.23 show second-order IMD and cross-modulation for *pin* diodes.
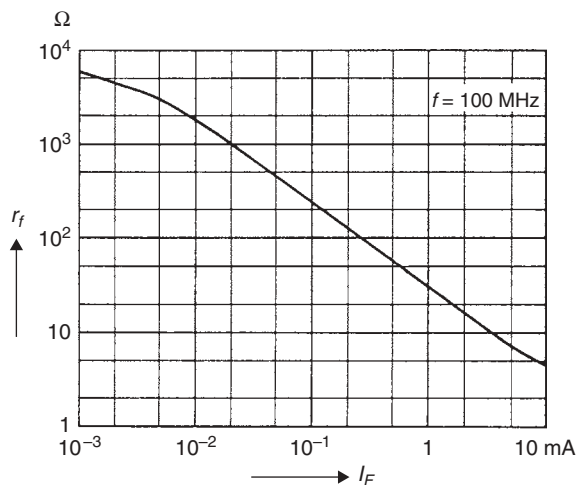
FIGURE 3.21   Forward resistance versus forward current.
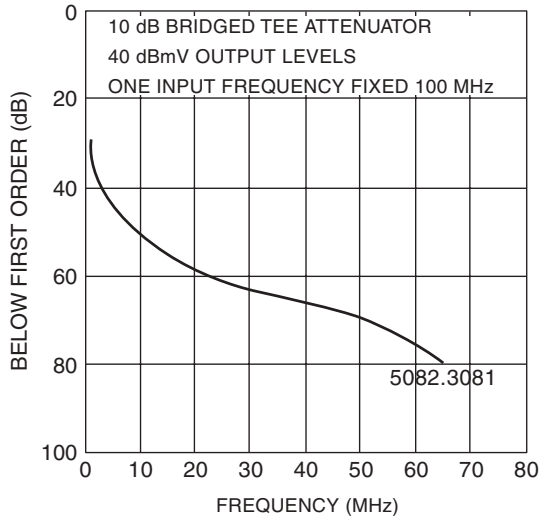
FIGURE 3.22 Second-order IMD in an Agilent *pin* diode.
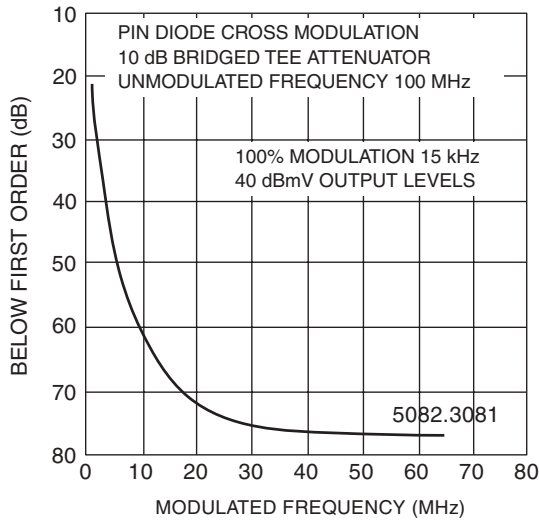
FIGURE 3.23 Cross-modulation in *pin* diode.

3.2.6 Tuning Diodes

Introduction In recent years, continuous development of tuning diodes—also known as *varactors* or *varicaps*—together with increased commercial and military use has led to substantial improvement in *Q*, reproducibility, and reliability. Concurrently, new techniques for producing and controlling a hyperabrupt dopant profile in the semi-conductor permit the capacitance–voltage law to be much faster than the classical square-root or cube-root behavior.

Current tuning diode materials include silicon and gallium arsenide; silicon is favored for low-cost and lower Q applications from HF through microwave frequencies. Hyperabrupt varactors, also of silicon, are finding large application in commercial television tuner applications, where their high tuning ratios, linear tuning, and low cost are needed. New developments include low-capacitance hyperabrupts for microwave and wireless applications.

Gallium arsenide used with high operating frequency dictates the highest Q possible, as in parametric amplifiers and millimeter multipliers.

This section will acquaint the reader with tuning diodes: how they work and what they can or cannot be expected to do in an electronic circuit. The basic properties of a tuning diode will be described in terms of the parameters that manufacturers use in characterizing them. The following topics will also be addressed:

- Capacitance ratio with respect to voltage and voltage breakdown
- Q as a function of design and operating conditions
- Stability—leakage current, temperature coefficient, and posttuning drift
- Distortion products
- Packaging parasitics
- Applications—suggestions on how to specify a varactor

Tuning Diode Physics All junction diodes are made up of the same physical parts: a *pn* junction, a carefully controlled epitaxial layer, and a very low resistance substrate. These parts are shown in Figure 3.24.

No matter what type of junction device we are discussing—a tuning diode, a step recovery diode, or a *pin* diode—these parts are all present; the main difference between these devices is the resistivity and thickness of the epitaxial layer. Tuning diodes and multiplier diodes need epitaxial layers where both the resistivity and thickness are carefully controlled.

3.2.7 Abrupt Junction

An abrupt-junction diode is one in which the p^+ (diffused) region of the diode is much more highly doped that the epitaxial layer. Also, the high doping drops to the doping level of the epitaxial layer in a distance that is short compared to the epitaxial layer thickness, and the doping level of the epitaxial layer is constant over its thickness. This is shown in Figure 3.25, with the corresponding $C-V$ curve shown in Figure 3.26. When these requirements are satisfied, the diode capacity, diode area, epitaxial layer doping level, and diode voltage are related by

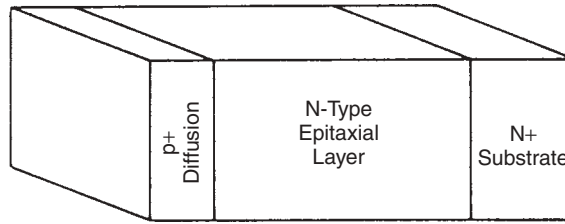$$\frac{C(V)}{A} = K\left(\frac{N}{V + \varphi}\right)^n \tag{3.42}$$

where $C(V)$ = capacitance of diode at voltage V
A = area of diode
N = doping level of epitaxial layer
V = voltage applied to diode
φ = built-in potential of diode (0.6–0.8 V)
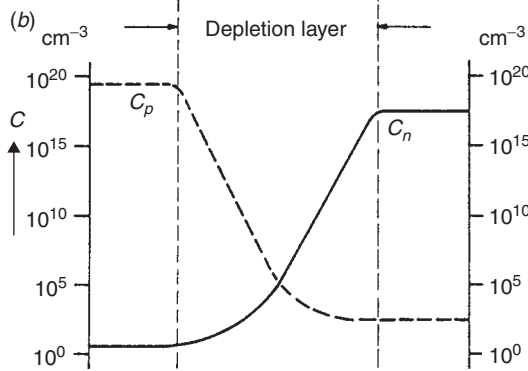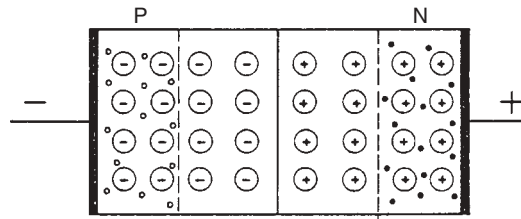
FIGURE 3.24 (*a*) Basic *pin* structure. (*b*) Cross section of reverse-biased *pn* junction. (*c*) Density distribution of free charge carriers.

$$n = \text{slope of diode } C\text{--}V \text{ curve}; n \approx 0.5 \text{ for an abrupt-junction diode}$$
$$K = \text{constant}$$

As a consequence of the physical properties of a *pn* junction, a depletion layer is formed between the *p* and *n* regions whose width depends on the voltage applied to the diode. The capacitance of the diode is inversely proportional to the width of the depletion layer. In addition, the series resistance of the diode is proportional to the width of the undepleted epitaxial layer. Thus, as diode reverse bias is increased, the depletion layer increases, causing a decrease in capacitance and an increase in series resistance. As the diode reverse bias is increased further, a point is reached where the electric field caused by the reverse bias reaches a critical level, and current through the diode increases rapidly; this is the breakdown voltage of the diode. If, at the breakdown voltage, the epitaxial layer is not completely depleted, the diode will have excessive
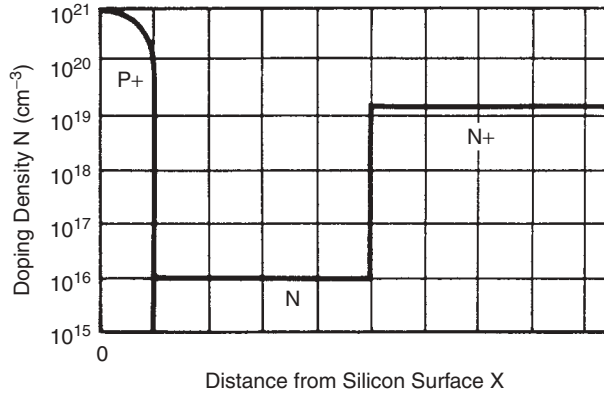
FIGURE 3.25 $N-X$ abrupt-junction diode.
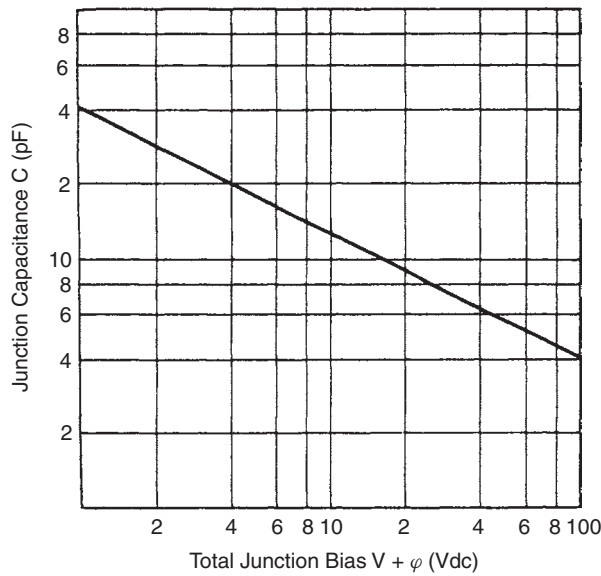
FIGURE 3.26   Capacitance versus total junction bias for abrupt diode.

series resistance. Conversely, if the epitaxial layer is depleted before the breakdown voltage is reached, no further capacitance decrease occurs after the total depletion, and a condition called *punchthrough* occurs [3.9].

While in the ideal case voltage breakdown will occur just as the epitaxial layer is totally depleted, this seldom occurs in practice, and we generally have a condition of either punchthrough or excess series resistance.

3.2.8   Linearly Graded Junction

If, instead of the junction profile shown in Figure 3.25, we have a p^+ region and an n region whose doping levels increase linearly with distance from the *pn* junction as
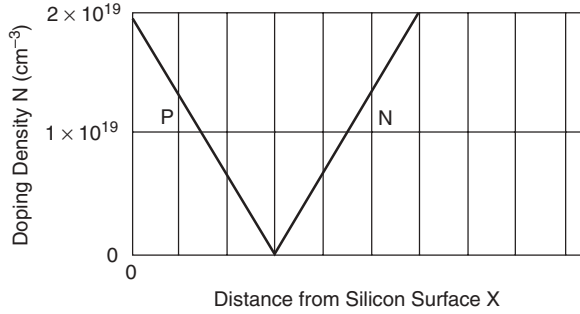
FIGURE 3.27 $N-X$ linearly graded junction.
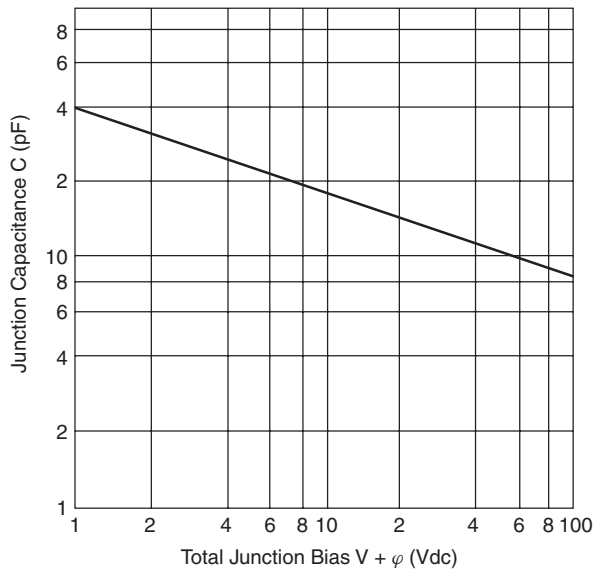
FIGURE 3.28 Capacitance versus total junction bias for linearly graded junction.

shown in Figure 3.27, with its corresponding $C-V$ curve in Figure 3.28, we then have what is called a linearly graded junction diode. This diode follows (3.42) with the exception that the exponent $n = \frac{1}{3}$. This means that, for a given voltage change, the linearly graded junction will have a smaller capacitance change than an abrupt-junction diode. Since, in most cases, the designer is looking for the maximum capacitance change obtainable, the linearly graded junction is not used as a tuning diode. This structure found its greatest use several years ago as a "cube-law" multiplier, but even this use has decreased as new structures have been developed.

3.2.9 Hyperabrupt Junction

The hyperabrupt diode provides a greater capacitance change than the abrupt-junction diode for a given voltage change as well as a linear frequency-versus-voltage characteristic over a limited voltage range. The structure of the hyperabrupt diode is shown

in Figure 3.29 and can be seen to be an abrupt-junction diode with an additional, increased doping level at the *pn* junction. This diode also follows Eq. (3.42) with the exception that *n* is not a function of voltage and is generally in the range of 0.5 to 2. A typical curve of *n* versus voltage is shown in Figure 3.30.

The $C-V$ curve in a hyperabrupt diode is shown in Figure 3.31 and is seen to start at a high value of capacitance per unit area at low bias (high epitaxial doping) and change to a lower value of capacitance per unit area (low epitaxial doping) at high bias. The details of the curve depend on details of the shape of the more highly doped region near the *pn* junction.

Unfortunately, with a hyperabrupt diode, you must settle for a lower Q than an abrupt-junction diode with the same breakdown voltage and same capacitance at 4 V.

It should be noted that any diode that has an *n* value that exceeds 0.5 at any bias voltage is, by definition, a hyperabrupt diode. Thus, the hyperabrupt diode family can
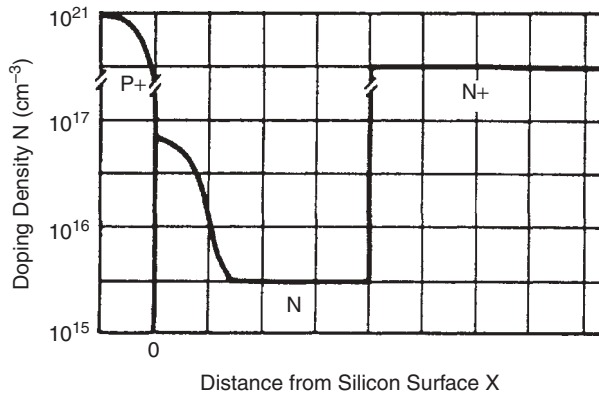
FIGURE 3.29 $N-X$ hyperabrupt junction.
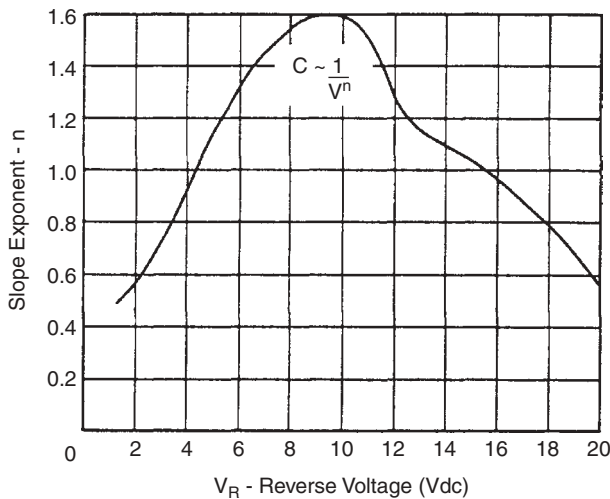
FIGURE 3.30   Typical *n* versus reverse voltage for hyperabrupt diode.
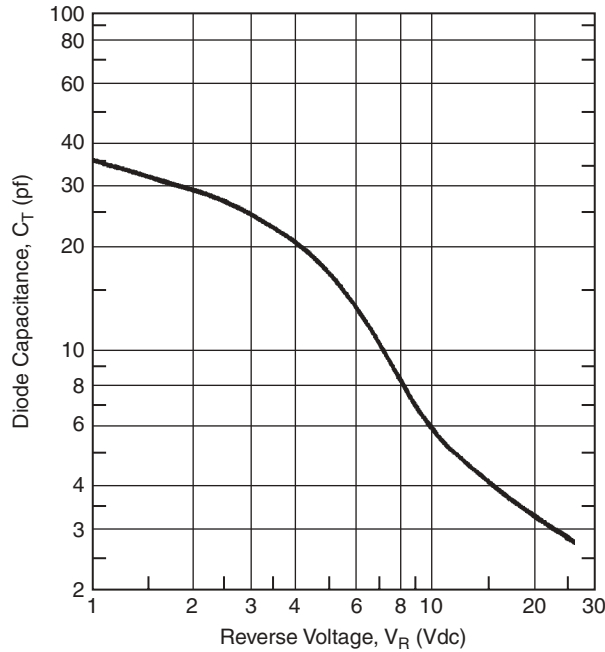
FIGURE 3.31   Capacitance versus junction bias for hyperabrupt diode.

have an infinite number of different $C-V$ curves. Since the abrupt-junction diode has a well-defined $C-V$ curve, the capacitance value at one voltage is sufficient to define the $C-V$ capacitance at any other voltage. This is not the case for the hyperabrupt diode. To adequately define the $C-V$ characteristics of a hyperabrupt diode, two and sometimes three points on the curve must be specified.

3.2.10   Silicon Versus Gallium Arsenide

Everything mentioned so far applies to both silicon and gallium arsenide (GaAs) diodes. The main difference between silicon and GaAs from a user's point of view is that higher Q can be obtained from GaAs devices. This is due to the lower resistivity of GaAs from a given doping level N. The resistivity of the epitaxial layer, or substrate, of a diode is given by

$$\rho = \frac{1}{Ne\mu} \tag{3.43}$$

where ρ = resistivity

N = doping level of layer

e = charge on electron

μ = mobility of charge carriers in layer

Gallium arsenide has a mobility about four times that of silicon and, thus, a lower resistivity and higher Q for a given doping level N. Since diode capacitance is proportional to $\sqrt{N}$, independent of resistivity, a silicon diode and a GaAs diode of equal area and doping will have a capacitance difference proportional to the square root of

the dielectric constant ratio. This gives the GaAs diode a 5% higher capacitance and is thus of little practical significance. The penalty paid for using GaAs is an unpassivated diode and a more expensive diode due to higher material and processing costs. If the higher Q of the GaAs device is not really needed, a substantial price saving will be obtained by using a silicon device.

Planar Versus Mesa Construction The three basic construction techniques used to manufacture tuning diodes are planar, ion implantation, and mesa; a cross section of each of these devices is shown in Figure 3.32. The planar process, which is the backbone of the integrated circuit industry, lends itself to large-volume production techniques and is the one use for the 1N series of tuning diodes. Ion implantation [3.12] gives more uniform doping and is therefore preferred in large-volume production. Mesa processing, on the other hand, requires more processing steps and is generally done on a wafer-by-wafer basis. This results in a more costly process and thus a more expensive diode. Most microwave tuning diodes are of mesa design because of greatly higher Q. Due to the relatively small radius of curvature at the junction edge of a planar diode, the electric field in this area is greater than the electric field in the center (flat) portions of the junction. As a result, the breakdown voltage of the diode is determined by both the epitaxial resistivity and the radius of curvature of the junction edge. Thus, for a given breakdown voltage, a planar or ion-implanted diode must use higher resistivity epitaxial material than a mesa diode, which has a completely flat junction. The end result is that the planar diode has a greater series resistance than a mesa diode for the same capacitance and breakdown voltage and thus lower Q.
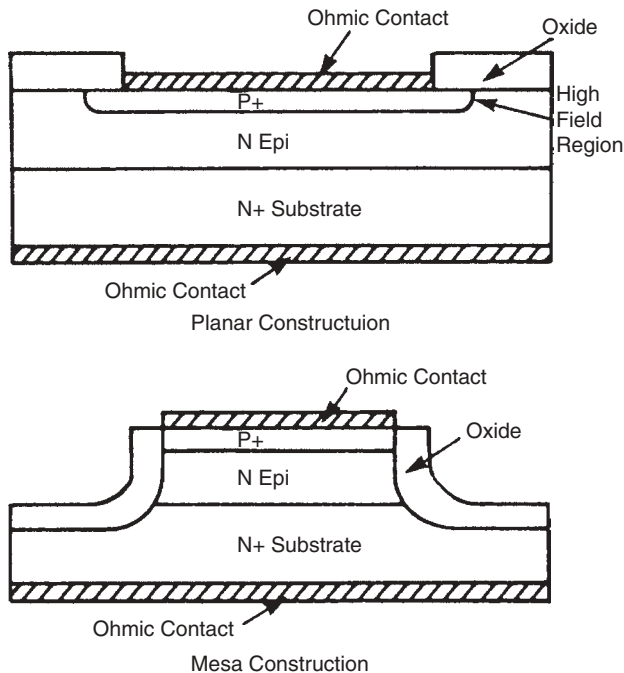

FIGURE 3.32 Cross sections of planar and mesa devices.

Capacitance Ratio   From the user's point of view, this ratio is simply the capacitance available in the circuit. Thus, a user tuning from, say, -4 to -45 V defines ratio as

$$R = \frac{C_T(-4)}{C_T(-45)} \tag{3.44}$$

where C_T includes $C_J + C_P + C_F$. The manufacturer, however, defines C_T as $C_J + C_P$.

To explore the significance of this difference, let us take two examples, a large C_J and a small C_J, in chip, package, and "typical" fringe situations. Both are 45-V tuning varactors.

Device	C_{J0}	C_{J45}	Ratio
A	0.6 pF	0.1 pF	6.0
B	15.0 pF	2.5 pF	6.0

Put both devices in a standard 023 package with C_P (strap and ceramic) of 0.18 pF:

Device	C_{T0}	C_{T45}	Ratio
C	0.78 pF	0.28 pF	2.75
D	15.18 pF	2.68 pF	5.67

Notice the drop in ratio, especially for the low-C_J diode. If we now add a typical 0.04 pF for external fringe capacitance, we get

Device	C_{T0}	C_{T45}	Ratio
C	0.82 pF	0.32 pF	2.56
D	15.22 pF	2.72 pF	5.6

The reduction in ratio, and thus the circuit-tuning capability, by the fringing fields is quite obvious and amounts to 7% in this example.

Because of the often stringent specifications on tuning ratio, it is mandatory that the manufacturer and customer clearly agree on the exact design of the holder used to measure the varactor in question.

Having described how to measure capacitance, it is relatively easy to describe the results. The section on diode physics described the various types of "laws," or $C-V$ curves, and we will not repeat them here. Nonetheless, several important points must be covered.

The first is "available capacitance swing." The laws indicate a steadily decreasing capacitance with voltage, which indicates that the epi region is widening and the electric field is increasing. (For an abrupt junction, since $C \propto 1/\sqrt{V}$, the depletion zone with W is increasing as $\sqrt{V}$ and the electric field V/W increases as $\sqrt{V}$.)

Two things can happen:

(a) The junction width widens so that the entire intrinsic region is depleted. The capacitance bottoms out, resulting in voltage punchthrough.

(b) The electric field exceeds the dielectric strength of silicon (or GaAs), and "solid-state discharge" or "avalanche" current is drawn.

The diode impedance drops, the varactor no longer "varacts," and circuit operation ceases. Moreover, if more than a few milliamperes of current is drawn, localized overheating may destroy the diode, resulting in breakdown voltage. All varactors are characterized for breakdown voltage—for example, 45 V minimum.

The theoretical tuning varactor is designed so that the punchthrough occurs at a voltage equal to the voltage breakdown of the diode. Logically, then, this means that, to obtain greater tuning ratios, it is necessary to be able to increase the depletion layer width without reaching punchthrough or breakdown. You must have a thicker epi region to make this possible.

Figure 3.33 shows catalog ratio values, from zero bias to breakdown, as a function of breakdown voltage necessary. In the next section, on Q, we will discuss other elements in your choice of V_B.

To complete this section, we should mention that semiconductor processing control has been refined so well that capacitance tracking to within $\pm 1\%$ over the full range from zero to breakdown is now readily obtainable in production quantities.

Temperature Coefficient of Capacitance (T_{CC})   Unfortunately, since most data-sheets give the value of T_{CC} at 4 V, it is sometimes assumed that this value applies at all bias voltages. This is not the case. Consider Eq. (3.45a), a rewritten form of Eq. (3.42):

$$C(V) = \frac{C(O)}{(V + \varphi)^n} \tag{3.45a}$$
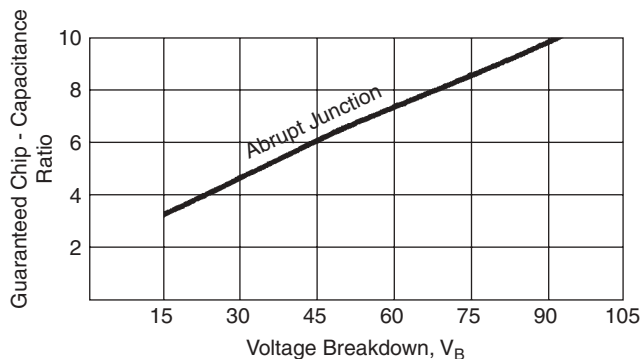
Taking the derivative of this with respect to temperature T, we have

$$\frac{dC(V)}{dT} = \frac{+nC(O)}{(v + \varphi)(v + \varphi)^n} \frac{d\varphi}{dT} \tag{3.45b}$$

or, after substituting Eq. (3.45a),

$$T_{CC} = \frac{1}{C(V)} \frac{dC(V)}{dT} = \frac{-n}{V + \varphi} \frac{d\varphi}{dT} \tag{3.46}$$

FIGURE 3.33   Capacitance ratio versus breakdown voltage.

As a first approximation, we can say that $d\varphi/dT = -2.3$ mV/°C over the temperature range of interest.

From Eq. (3.46) we can draw the following conclusions:

1. The temperature coefficient is inversely proportional to the applied voltage.
2. The temperature coefficient is directly proportional to the diode slope, n.

For an abrupt-junction diode that has a constant value of n (0.5), the temperature coefficient has a smooth curve in the form $K/(v + \varphi)$. However, in the case of hyperabrupt diodes, n is a function of voltage, and the shape of the T_{CC} curve depends on the details of the $n(V)$ curve. A typical T_{CC} curve for an abrupt-junction diode is shown in Figure 3.34 and for an Alpha DKV6520 series hyperabrupt diode in Figure 3.35. The inflection in the hyperabrupt T_{CC} is due to the fact that in this voltage range $n(V)$ is increasing faster than $1/V$, giving an increase in T_{CC}. It should also be noted, however, that over the range of the T_{CC} minimum the temperature coefficient is relatively constant, and operation in this area may be advantageous in some applications where a restricted tuning range can be used.

3.2.11 *Q* Factor or Diode Loss

Definitions The classical definition of the Q of any device or circuit is

$$Q = \frac{2\pi \text{ energy stored}}{\text{energy dissipated per cycle}} \tag{3.47}$$
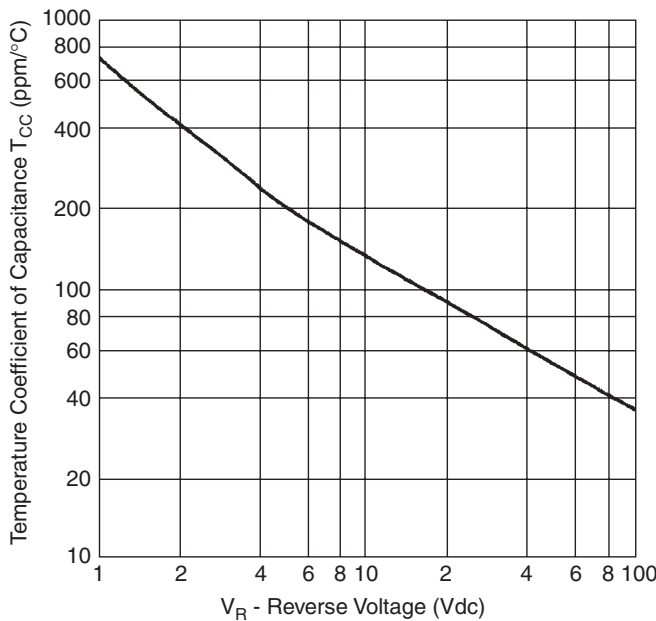
FIGURE 3.34 Temperature coefficient of capacitance versus tuning voltage—abrupt-junction diode.
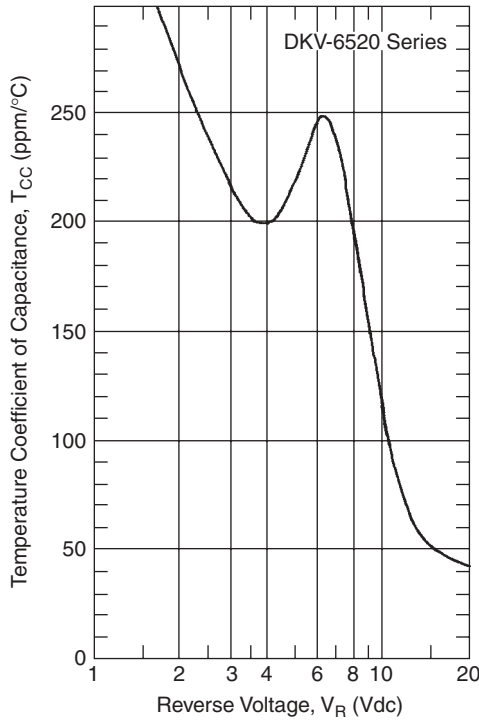
FIGURE 3.35 Temperature coefficient of capacitance versus tuning voltage ($T_A = 25°C$)—hyperabrupt-junction diode.
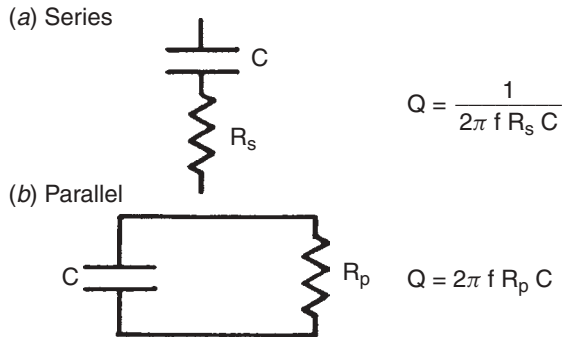
FIGURE 3.36 Two formulations of Q for a capacitor.

The equivalent circuit of a lossy capacitor can be given in two forms, as shown in Figure 3.36.

For a capacitor, two formulations are possible as shown in Figure 3.36.

Clearly, the two definitions must be equal at any frequency, which establishes

$$R_P = \frac{1}{(2\pi f)^2 C^2 R_S} \tag{3.48}$$

In the case of a high-Q tuning diode, the proper physical model is the series configuration, for the depleted region is almost perfectly pure capacitance, and the undepleted region, due to its relatively low resistivity, is almost a pure resistor in series with the capacitance. Further, the contact resistances are also clearly in series. Then, for a tuning diode Q is given by

$$Q_{(-v)} = \frac{1}{2\pi f_0 R_{(-v)} C_{(-v)}} \tag{3.49}$$

where f_0 is the operating frequency, $C_{(-v)}$ is the junction capacitance, and $R_{(-v)} = R(\text{epi}) + R_{C'}$, the sum of the resistance of the undepleted epi and the fixed contact resistance.

Cutoff frequency f_c is defined as that frequency at which Q equals unity. Thus,

$$f_{c_{(-v)}} = \frac{1}{2\pi R_{(-v)} C_{(-v)}} \tag{3.50}$$

It has been shown that the highest cutoff frequencies will be obtained from linearly graded junctions with low-breakdown diodes (<10 V), approaching 10,000 GHz for silicon [3.8].

Historically, the tuning diode business has a habit of specifying Q at 50 MHz, despite the fact that Q values of microwave diodes are so high that it is almost impossible to measure them at 50 MHz. Instead, as discussed below, Q is measured at microwave frequencies (e.g., 1 to 3 GHz) and related to 50 MHz by the relationship

$$Q_{(f1)} = Q_{(f2)} \frac{f_2}{f_1} \tag{3.51}$$

which derives quickly from the assumption that f_c is independent of the measuring frequency.

Since both junction capacitance and epi resistance are functions of the applied bias, it is not possible to calculated Q as a function of bias from a measurement of capacitance alone. Catalog specifications typically show Q at -4 V together with the capacitance at two or more voltages.

Relative to $Q_{(-4)}$, Q increases faster than the reduction in capacitance for bias greater than 4 V and, conversely, decreases faster for bias less than 4 V.

In the following section, we will discuss the diode design parameters that determine Q. Following this, we will describe some elementary Q measurement techniques.

Causes   In the discussion of device physics, the resistivity of the epi region was discussed together with its impact on punchthrough and breakdown. For example, Table 3.8 supplies typical resistivity and relative parameters of 0.6-pF ($C_{J_{-4}}$) diodes of different breakdowns. If we remember that at any bias lower than breakdown the epi region is not completely depleted, it follows that the undepleted portion presents a resistance in series with the pure capacitance of the depleted zone. The magnitude of this "undepleted" resistance is also shown in the table.

The entry "R_{sp}" ($R_{\text{spreading}}$) is the series resistance between the epi region and the low-resistivity substrate. The calculations are for idealized cylindrical epi regions of

TABLE 3.8 Parameters for 0.6-pF Diode

Breakdown Voltage V_B	Resistivity (Ω-cm)	Junction Diameter (mils)	epi Region (μm)	Depleted epi, $V = -4$ V (μm)	Undepleted epi, $V = -4$ V (μm)	R Undepleted (Ω)	R_{sp} (Ω)	Q_4
30	.31	2.4	1.37	.54	.83	.81	.18	5200
45	.52	2.8	2.25	.73	1.52	1.86	.15	2600
60	.74	3.2	3.20	.90	2.30	3.24	.13	1500
90	1.25	3.7	5.27	1.21	4.06	7.17	.10	700

uniform resistivity, low-resistivity contact on the anode (top), and low-resistivity substrate on the cathode. This resistance is constant, independent of bias; also shown are epi thickness and width of the depletion zone at -4 V bias.

Note the substantial reduction in Q for high-voltage diodes caused by the increased epi resistance; this is true for any value of capacitance or any type of junction. For greater voltage breakdown, the epi thickness must be increased, which requires an increase in epi layer resistivity; the higher resistivity of the undepleted zone multiplied by the fact that it is much wider for high-voltage diodes means the resistance increases substantially.

Consequently, a rule of thumb emerges: For maximum Q, never choose a tuning diode with a voltage breakdown in excess of what is needed for the necessary tuning range. If the required tuning range is an octave, requiring a 4:1 ratio, the selection of a 30-V diode will result in diode losses half those of a 60-V diode.

Table 3.9 lists capacitance and Q for each of these chips as a function of bias. Remember that Q is calculated at 50 MHz.

Table 3.10 rewrites the data of Table 3.9 to show available capacitance ratios between zero bias and breakdown. The first column is the theoretical optimum, as tabulated. The second column is the typical catalog specification. The reduction in tuning ratio below theoretical optima is caused by nonideal junction fabrication. The junctions are never perfectly abrupt.

Although the tables and numbers given refer to abrupt-junction silicon devices, the principle applies without exception to all types of tuning diodes. For comparison, Table 3.11 lists available ratios and Q values for a number of different varactors. The high Q values for GaAs and the low values for hyperabrupts are apparent.

One last point: The Q values and series resistance refer to chips only. The effects of package parasitics will be discussed later, but it is important to consider circuit contact losses here. For low-capacitance diodes—for example $C_{J4} = 0.6$ pF—the epi region

TABLE 3.9 Q Versus Bias for 0.6-pF Diode

Breakdown Voltage V_B	C_{J0}	Q (0)	C_J (-4)	Q (-4)	C_J (-10)	Q (-10)	C_J (-30)	Q (-30)	C_J (-45)	Q (-45)	C_J (-60)	Q (-60)	C_J (-90)	Q (-90)
30	1.43	1,700	0.6	5,200	0.4	10,000	0.23	64,000						
45	1.43	850	0.6	2,600	0.4	5,000	0.23	20,000	0.19	90,000				
60	1.43	550	0.6	1,500	0.4	3,000	0.23	9,000	0.19	23,000	0.17	170,000		
90	1.43	270	0.6	700	0.4	1,300	0.23	3,500	0.19	6,000	0.17	10,000	0.14	220,000

TABLE 3.10   Capacitance Ratios ($C_{J0}/C_J V_B$)

Breakdown Voltage V_B	Optimum Ratio	Minimum Guaranteed Ratio	Typical Q_{-4}
30	6.2	4.5	3000
45	7.5	6.0	2500
60	8.4	7.5	1400
90	10.2	8.7	650

TABLE 3.11   Comparative Tuning Diodes

Type	C_{J0}	Breakdown Voltage V_B	Q_{-4}[a]	Ratio $C_{J0}/C_J V_B$[a]
Silicon abrupt	1.0	30	5,000	4.5
Silicon abrupt	2.5	30	4,600	4.5
Silicon abrupt	5.0	30	3,800	4.5
Gallium arsenide abrupt	1.0	25	10,000	3.6
Gallium arsenide abrupt	0.5	10	17,000	2.5
Silicon hyperabrupt	50.0	22	300	17.0
Silicon hyperabrupt	2.5	22	500	14

[a] Minimum guaranteed.

contributes a high value of resistance and dominates Q except at punchthrough. Diode contact losses are less significant.

3.2.12   Diode Problems

Posttuning Drift   Posttuning drift (PTD) is the change in oscillator frequency with time after the tuning voltage has stabilized. The minimization of PTD has assumed greater importance with the design of more sophisticated electronic countermeasure systems, where rapid, accurate frequency changes are required.

Posttuning drift can be characterized as short term and long term. Short-term PTD occurs in the time range of tens of nanoseconds to a few seconds, while long-term PTD is in the time range of seconds to minutes, hours, or days.

Short-term PTD is mainly dependent on the thermal properties of the diode and is improved by high-Q (low-power-loss) and flip-chip construction. Long-term PTD depends on oxide stability and freedom of mobile charge in the oxide. It should be noted that actual oscillation frequency change may occur even with a perfect tuning diode because of variation with frequency in the power dissipated by the diode, changes in the diode heat-sink temperature, and frequency changes due to other circuit elements. Less than 0.01% short- and long-term PTD can be obtained.

Distortion Products   Inasmuch as nonlinear components generate harmonics and other distortion products, an understanding of this mechanism is of prime interest to the circuit designer. In some instances, the distortion products are the desired end result of the circuit design, as in frequency multipliers, where harmonics of the input

signal frequency are the required output signal. For other applications, such as tuning-diode-tuned linear circuits, distortion products are extremely undesirable, and in some instances the end-product specification may set a maximum limit to the distortion products allowed.

Cross-Modulation   Cross-modulation is the transfer of the modulation on one signal to another signal and is caused by third-order and higher odd-order nonlinearities in the behavior of the device. Rewriting Eq. (3.42), we have

$$C(V) = \frac{C_0}{(1 + V/\varphi)^n} \tag{3.52}$$

where C_0 = capacitance
$\quad\quad V$ = applied voltage, $= V_0 + v$
$\quad\quad V_0$ = dc applied voltage
$\quad\quad v$ = ac applied voltage

Then, for a desired signal of
$$S_1 = v_1 \sin \omega_1 t \tag{3.53}$$

and a second, amplitude-modulated signal of

$$S_2 = v_2(1 + m \cos \omega_m t) \sin \omega_2 t \tag{3.54}$$

it can be shown that the cross-modulation γ defined by

$$\text{Ouput Signal} \sim v_1 \sin \omega_1 t + \gamma \sin(\omega_1 \pm \omega_m)t \tag{3.55}$$

is found to be
$$\gamma = \frac{n(n+1)mv_2^2}{4(V_0 + \varphi)^2} \tag{3.56}$$

From this equation cross-modulation can be defined as follows:

- Proportional to the square of the interfering signal
- Directly proportional to the interfering signal's modulation index, m
- Independent of the strength of the desired signal
- Independent of the frequencies of the desired and interfering signals (assuming that the nonlinearity to which both signals are subjected is sufficiently frequency indiscriminate so this is the case)
- Present for all values of n; that is, no value of n gives zero cross-modulation

Solving Eq. (3.56) for the signal level v_2 required to produce cross-modulation of value γ, we have
$$v_2 = \frac{2(V_0 + \phi)\gamma}{n(n+1)^m} \tag{3.57}$$
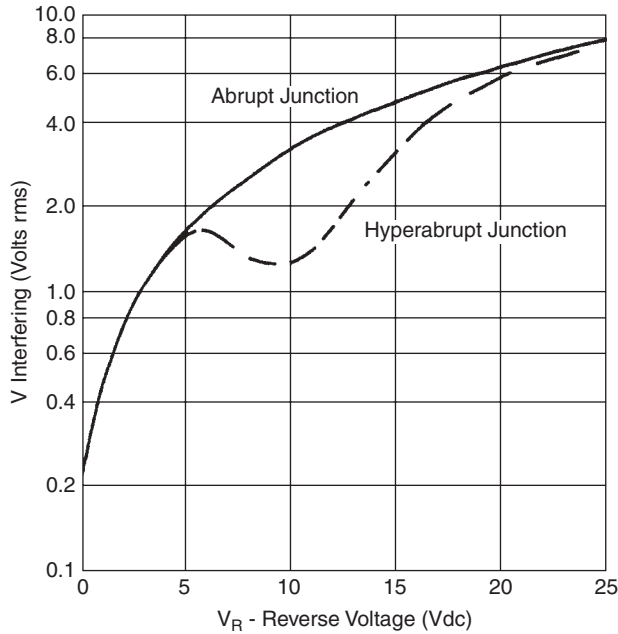
FIGURE 3.37 Interfering signal (30% amplitude modulated) level versus bias for 1% cross-modulation—abrupt and hyperabrupt junctions.

The interfering signal levels required to produce 1% cross-modulation from a 30% modulated interfering signal applied to an abrupt-junction diode and a hyperabrupt-junction diode are shown in Figure 3.37.

From this figure, it can be seen that the hyperabrupt diode is more susceptible to cross-modulation than the abrupt-junction diode in the region of maximum slope of the hyperabrupt diode. For many applications, however, distortion products will be generated by other devices, such as transistors, at signal levels considerably below those given in Figure 3.37.

Intermodulation   Intermodulation is the production of undesired frequencies in the form

$$\sin(2\omega_1 t - \omega_2 t) \qquad \text{and} \qquad \sin(\omega_1 t - 2\omega_2 t) \tag{3.58}$$

from an input signal in the form of

$$v(\cos \omega_1 t + \cos \omega_2 t) \tag{3.59}$$

From an analysis similar to that done for cross-modulation, it can be shown that

$$\text{Intermodulation} = \frac{n(n+1)v^2}{8(V_0 + \varphi)^2} \tag{3.60}$$

or

$$\text{Cross-modulation} = 2m \times \text{intermodulation} \tag{3.61}$$

Harmonic Distortion   Harmonic distortion products are integral multiples of the signal frequencies and decrease in amplitude as the harmonic number decreases. Due to passband considerations and amplitude decrease with harmonic number, the second harmonic is the one of prime concern. Again, it can be shown that the second harmonic, v_2, of a signal of amplitude v_1 is

$$v_2 = \frac{n}{3(V_0 + \phi)} v_1^2 \qquad (3.62)$$

Figure 3.38 shows the signal level required to produce 10% second-harmonic distortion in an abrupt-junction and a hyperabrupt-junction diode. Again, as in the case of cross-modulation, the hyperabrupt diode is slight worse than the abrupt-junction diode in the region of maximum slope of the hyperabrupt diode.

Reduction of Distortion Products   In some cases, the signal levels applied to the diode generate distortion products larger than desirable for the circuit application. In this case, significant reduction in the distortion products can be achieved by using two diodes in a back-to-back configuration, as shown in Figure 3.39. Analysis shows that the fundamental signal components through the diodes are in phase and add, while some distortion products are out of phase and cancel, thus improving distortion performance.

Since the gradient of the electrical field produced in the depletion layer by a reverse bias applied to the device is proportional to the space charge density, the following equations can be written for the junction width W as a function of the reverse bias V_R:
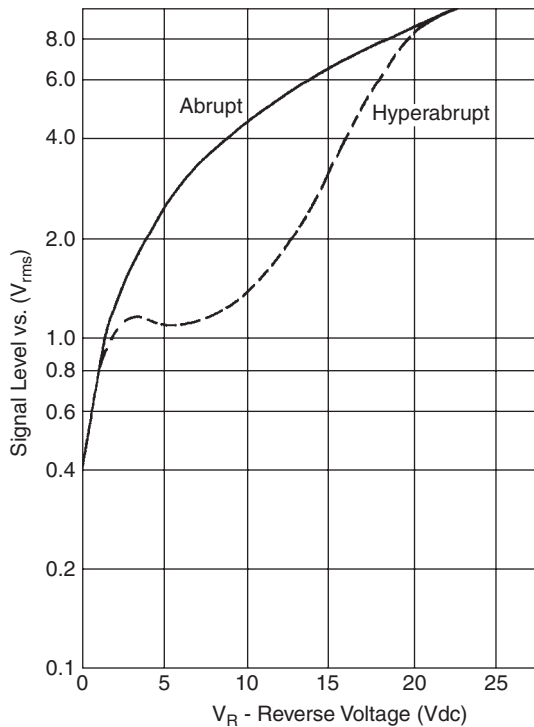
FIGURE 3.38   Signal level versus reverse voltage for 10% harmonic distortion.
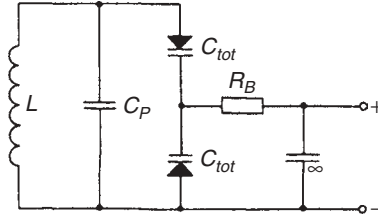
FIGURE 3.39 Back-to-back diodes: C_P = fixed parallel capacitance, R_B = bias decoupling resistor, and capacitor marked ∞ is a low-impedance bypass.

For an abrupt *pn* junction (alloyed diodes)

$$W = \sqrt[2]{2\frac{\varepsilon_r \varepsilon_0}{q}\left(\frac{1}{C_p} + \frac{1}{C_n}\right)(V_R + V_D)} \qquad (3.63)$$

For linear *pn* junctions (single-diffused diodes, such as BA110 to BA112)

$$W = \sqrt[3]{12\frac{\varepsilon_r \varepsilon_0}{aq}(V_R + V_D)} \qquad (3.64)$$

where a is the impurity gradient within the depletion layer, ε_0 is the absolute dielectric constant ($8.85 \times 10^{-14}\,A_s/V_{cm}$), and $\varepsilon_r \approx 12$, the relative dielectric constant of silicon.

The junction capacitance, which is inversely proportional to the junction width, therefore varies in alloyed diodes with the square root, and in single-diffused diodes with the cube root of the externally applied reverse bias, and can be calculated from the general equation

$$C = \frac{\varepsilon_r \varepsilon_0 S}{W} \qquad (3.65)$$

where in S is the surface area of the *pn* junction. By way of approximation, we can also use the equation

$$C = \frac{K}{(V_R + V_D)^n} \qquad (3.66)$$

where all constants and all parameters determined by the manufacturing process are contained in K. The exponent n is a measure of the slope of the capacitance–voltage characteristics and is 0.5 for alloyed diodes, 0.33 for single-diffused diodes, and (on average) 0.75 for tuner diodes with a hyperabrupt *pn* junction. Figure 3.40 shows the capacitance–voltage characteristics of an alloyed, a diffused, and a tuner diode.

Recently, an equation is indicated which, although purely formal, describes the practical characteristics better than (3.66):

$$C = C_0\left(\frac{A}{A + V_R}\right)^m \qquad (3.67)$$

where C_0 is the capacitance at $V_R = 0$ and A is a constant whose dimension is a voltage. The exponent m is much less dependent on voltage that the exponent n in (3.66).
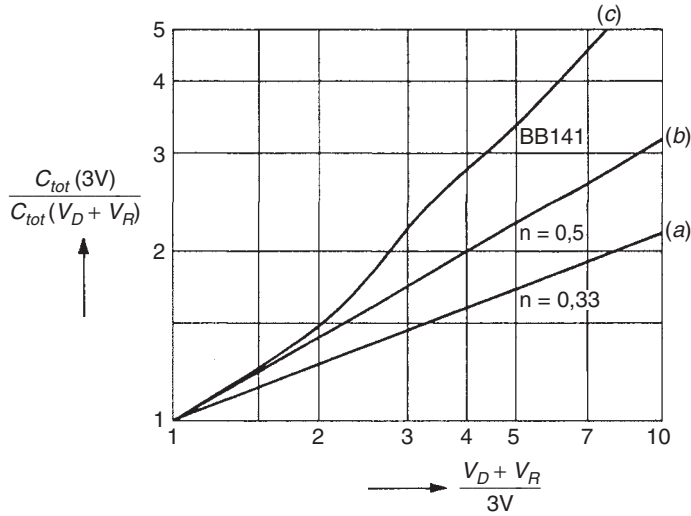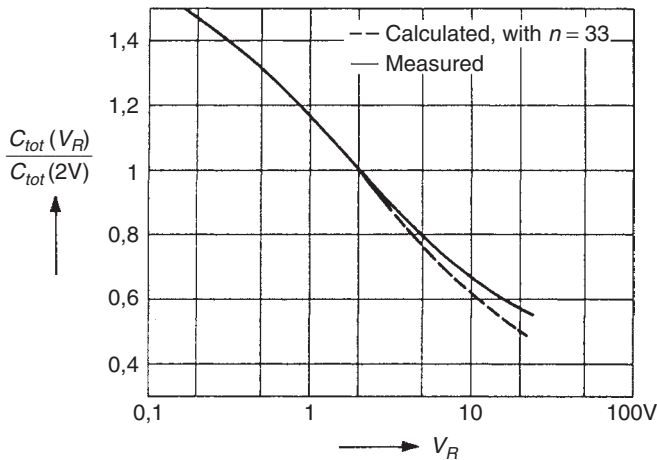
FIGURE 3.40 Capacitance–voltage characteristic: (*a*) alloyed capacitance diode; (*b*) diffused capacitance diode; (*c*) wide-range tuner diode (BB141).

Equations (3.63) through (3.67) express the pure junction capacitance of the capacitance diode, but to this must still be added a constant capacitance, determined by structure parameters, in order to obtain the diode capacitance C_{tot}, which interests the user. With high inverse voltages—that is, low junction capacitance—a difference will therefore arise between the theoretical capacitance–voltage characteristic according to (3.66) and the practical characteristic, as shown in Figure 3.41.

The operating range of a capacitance diode or its useful capacitance ratio

$$\frac{C_{\max}}{C_{\min}} = \frac{C_{tot}(V_{R,\min})}{C_{tot}(V_{R,\max})} \tag{3.68}$$

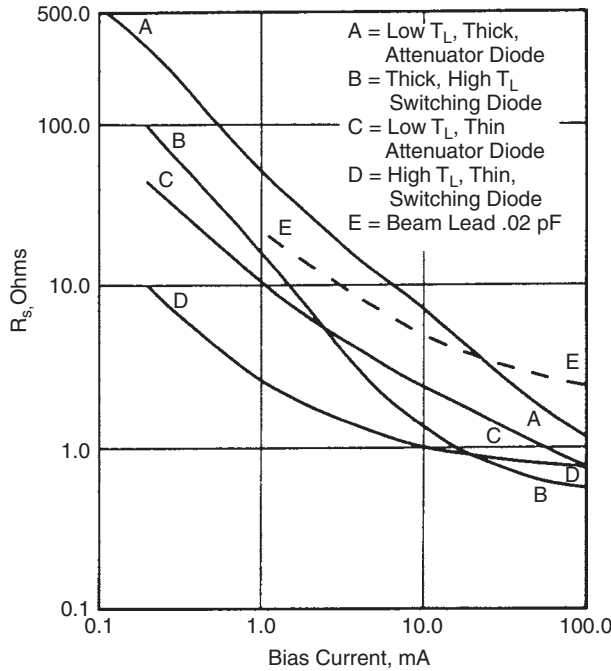**FIGURE 3.41** Capacitance–voltage characteristic of BA110 diode.

FIGURE 3.42   Basic current–voltage and capacitance–voltage characteristics.

is limited by the fact that the diode must not be driven by the alternating voltage superimposed on the tuning voltage into either the forward mode or the breakdown mode. Otherwise, rectification, which would shift the diode's bias and considerably affect its figure of merit, would take place. Figure 3.42 plots the capacitance–voltage characteristics of a capacitance diode to clarify the relationship. The useful operating range lies between the voltages

$$V_{\min} > \hat{V} - V_F \tag{3.69}$$

and

$$V_{\max} < V_{(BR)R} - \hat{V} \tag{3.70}$$

As has already been indicated, the exponent n for large-capacitance-ratio or tuning diodes in current use for TV tuners is not constant but is voltage dependent and subject to manufacturing tolerances. This means that the capacitance–voltage characteristic of these diodes is likewise subject to manufacturing tolerances. Since, in a TV tuner, it is necessary for two or three circuits to be tuned uniformly, tuner diodes must be selected empirically for identical characteristics and supplied in equipment lots.

3.2.13   Diode-Tuned Resonant Circuits

Tuner Diode in Parallel Resonant Circuit   Figures 3.43, 3.44, and 3.45 illustrate three basic circuits for the tuning of parallel resonant circuits by means of capacitance diodes.
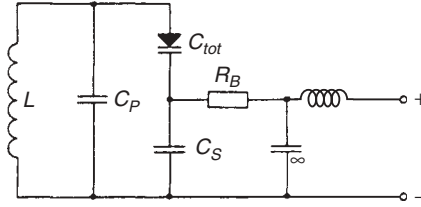
FIGURE 3.43 Parallel resonant circuit with tuner diode and bias resistor parallel to series capacitor.
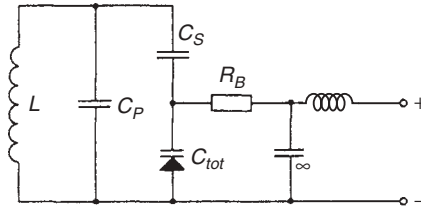
FIGURE 3.44 Parallel resonant circuit with tuner diode and bias resistor parallel to the diode.
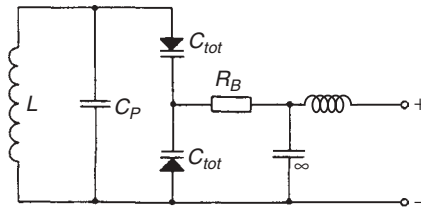
FIGURE 3.45 Parallel resonant circuit with two tuner diodes.

In the circuit diagram of Figure 3.43, the tuning voltage is applied to the tuner diode via the input coil and the bias resistor R_B. Series connected to the tuner diode is the series capacitor C_S, which completes the circuit for ac but isolates the cathode of the tuner diode from the coil and thus from the negative terminal of the tuning voltage. Moreover, a fixed parallel capacitance C_P is provided. The decoupling capacitor preceding the bias resistor is large enough for its value to be disregarded in the following discussion. Since for high-frequency purposes the biasing resistor is connected in parallel with the series capacitor, it is transformed into the circuit as an additional equivalent shunt resistance R_c. We have the equation

$$R_c = R_B \left(1 + \frac{C_S}{C_{\text{tot}}}\right)^2 \tag{3.71}$$

If in this equation the diode capacitance is substituted by the resonant circuit frequency ω, we obtain

$$R_c = R_B \left(\frac{\omega^2 L C_S}{1 - \omega^2 L C_P}\right)^2 \tag{3.72}$$

The resistive loss R_c caused by the bias resistor R_B is seen to be highly frequency dependent, and this may result in the bandwidth of the tuned circuit being independent of frequency if the capacitance of the series capacitor C_S is not chosen sufficiently high.

Figure 3.44 shows that that the tuning voltage can also be applied directly and in parallel to the tuner diode. For the parallel loss resistance transformed into the circuit, we have the expression

$$R_c = R_B \left(1 + \frac{C_{\text{tot}}}{C_S} \right)^2 \tag{3.73}$$

and

$$R_c = R_B \left(\frac{\omega^2 L C_S}{\omega^2 L (C_S + C_P) - 1} \right)^2 \tag{3.74}$$

The influence of the bias resistor R_B in this case is larger than in the circuit of Figure 3.43 provided that

$$C_S^2 > C_S(C_{\text{tot}} + C_P) + C_{\text{tot}} C_P \tag{3.75}$$

This is usually the case because the largest possible capacitance will be preferred for the series capacitor C_S and the smallest for the shunt capacitance C_P. The circuit of Figure 3.43 is therefore normally preferred to that of Figure 3.44. An exception would be the case in which the resonant circuit is meant to be additionally damped by means of the bias resistor at higher frequencies.

In the circuit of Figure 3.45, the resonant circuit is tuned by two tuner diodes that are connected in parallel via the coil for tuning purpose but series connected in opposition for high-frequency signals. This arrangement has the advantage that the capacitance shift caused by the ac modulation (see Section E, Modulating Diode Capacitance by Applied ac Voltage) takes effect in opposite directions in these diodes and therefore cancels itself. The bias resistor R_B, which applies the tuning voltage to the tuner diodes, is transformed into the circuit at a constant ratio throughout the whole tuning range. Given two identical, loss-free tuner diodes, we obtain the expression

$$R_c = 4 R_B \tag{3.76}$$

Capacitances Connected in Parallel or Series with Tuner Diode   Figures 3.43 and 3.44 show that a capacitor is usually in series with the tuner diode in order to close the circuit for alternating current and, at the same time, to isolate one terminal of the tuner diode from the rest of the circuit with respect to direct current, so as to enable the tuning voltage to be applied to the diode. As far as possible, the value of the series capacitor C_S will be chosen such that the effective capacitance variation is not restricted. However, in some cases, as for example in the oscillator circuit of receivers whose intermediate frequency is of the order of magnitude of the reception frequency, this is not possible and the influence of the series capacitance will then have to be taken into account. By connecting the capacitor C_S, assumed to be lossless, in series with the diode capacitance C_{tot}, the tuning capacitance is reduced to the value

$$C^* = C_{\text{tot}} \frac{1}{1 + C_{\text{tot}}/C_S} \tag{3.77}$$

The Q of the effective tuning capacitance, taking into account the Q of the tuner diode, increases to

$$Q^* = Q(1 + C_{\text{tot}}/C_S) \tag{3.78}$$

The useful capacitance ratio is reduced to the value

$$\frac{C_{\text{max}}^*}{C_{\text{min}}^*} = \frac{C_{\text{max}}}{C_{\text{min}}} \frac{1 + C_{\text{min}}/C_S}{1 + C_{\text{max}}/C_S} \tag{3.79}$$

where C_{max} and C_{min} are the maximum and minimum capacitances of the tuner diode.

On the other hand, the advantage is gained that, due to capacitive potential division, the amplitude of the alternating voltage applied to the tuning diode is reduced to

$$\hat{v}^* = \hat{v} \frac{1}{1 + C_{\text{tot}}/C} \tag{3.80}$$

so that the lower value of the tuning voltage can be smaller, and this results in a higher maximum capacitance C_{max} of the tuner diode and a higher useful capacitance ratio. The influence exerted by the series capacitor, then, can actually be kept lower than (3.78) would suggest.

The parallel capacitance C_P that appears in Figures 3.43 to 3.45 is always present, since wiring capacitances are inevitable and every coil has its self-capacitance. By treating the capacitance C_P, assumed to be lossless, as a shunt capacitance, the total tuning capacitance rises in value and, if C_S is assumed to be large enough to be disregarded, we obtain

$$C^* = C_{\text{tot}} \left(1 + \frac{C_P}{C_{\text{tot}}} \right) \tag{3.81}$$

The Q of the effective tuning capacitance, as derived from the Q of the tuner diode, is

$$Q^* = Q \left(1 + \frac{C_P}{C_{\text{tot}}} \right) \tag{3.82}$$

or, in other words, it rises with the magnitude of the parallel capacitance. The useful capacitance ratio is reduced:

$$\frac{C_{\text{max}}^*}{C_{\text{min}}^*} = \frac{C_{\text{max}}}{C_{\text{min}}} \frac{1 + C_P/C_{\text{max}}}{1 + C_P/C_{\text{min}}} \tag{3.83}$$

In view of the fact that even a comparatively small shunt capacitance reduces the capacitance ratio considerably, it is necessary to ensure low wiring and coil capacitances in the circuit design stage.

Tuning Range

The frequency range over which a parallel resonant circuit according to Figure 3.46 can be tuned by means of the tuner diode depends upon the useful capacitance ratio of the diode and on the parallel and series capacitances present in the circuit.
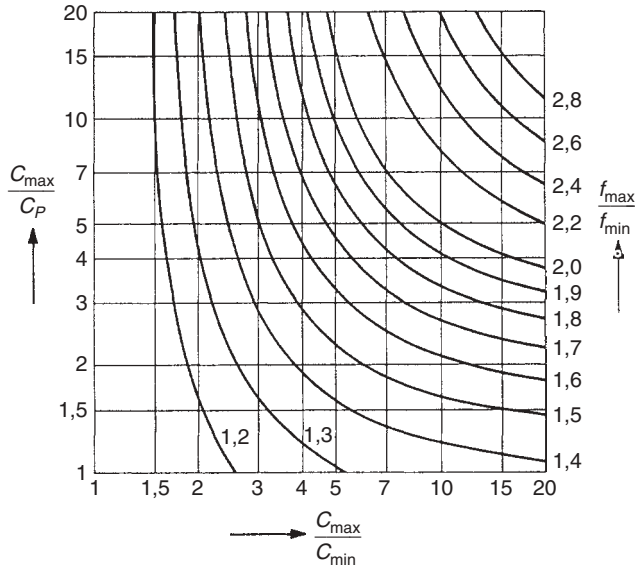
FIGURE 3.46   Diagram for determining capacitance ratio and minimum capacitance.

The ratio can be found from

$$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{1 + C_{\max}/[C_P(1 + C_{\max}/C_S)]}{1 + C_{\max}/[C_P(C_{\max}/C_{\min} + C_{\max}/C_S)]}} \qquad (3.84)$$

In many cases, the series capacitor can be chosen large enough for its effect to be negligible. In that case, (3.84) is simplified as follows:

$$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{1 + C_{\max}/C_P}{1 + C_{\min}/C_P}} \qquad (3.85)$$

From this equation, the diagram shown in Figure 3.46 is computed. With the aid of this diagram, the tuner diode parameters required for tuning a resonant circuit over a stipulated frequency range—that is, the maximum capacitance and the capacitance ratio—can be determined. Whenever the series capacitance C_S cannot be disregarded, the effective capacitance ratio is reduced according to (3.79).

Tracking   Some applications require the maintenance of a fixed frequency relationship between two or more tuned circuits as their tuning is simultaneously adjusted. Referred to as *tracking*, this technique requires narrow tolerances of capacitance versus tuning voltage. Minimizing tracking error requires special care if the tracking circuits must cover the same frequency span beginning at different start and end frequencies, as is necessary when simultaneously tuning oscillator and mixer/RF circuitry in a superheterodyne receiver. Then, tracking error must be minimized by means of series and shunt capacitances in accordance with methods known from variable capacitors. The

frequency deviations that must be anticipated are summarized in the equation

$$\frac{df}{f} = -\frac{1}{2}\frac{dC_0}{C_0} - \frac{1}{2}\frac{d(L - L_0)}{L} - \frac{1}{2}\frac{dL_0}{L_0} + \frac{n}{2}\frac{dV_R}{V_R + V_D} \tag{3.86}$$

The spread of parameters dC_0/C_0 and dL_0/L_0 can only be compensated by varying the circuit inductances $d(L - L_0)/L$ or the bias $dV_R/(V_R + V_D)$.

Modulating Diode Capacitance by Applied ac Voltage   In normal operation, the sum of the tuning voltage and the alternating signal voltage of the resonant circuits is applied to the tuner diode. The bias, and thus the capacitance, of the tuner diode therefore varies at the rhythm of the alternating voltage. Due the nonlinear character of the capacitance-versus-voltage curve, voltage distortions and capacitance shifts are inevitable, and these must be kept within adequate limits. This is done by maintaining the ac applied to the diode(s) at sufficiently low ac amplitude and by choosing an adequate minimum value for the tuning voltage. In the resonant circuit, a tuner diode is modulated predominantly by a current free from harmonics, according to the equation

$$i = \hat{i}\cos\omega t \tag{3.87}$$

The alternating voltage across the diode is

$$v = (V_R + V_D)\left[\left(1 + \frac{\hat{i}(1 - n)}{\omega C_{\text{tot}}V_R}\sin\omega t\right)^{1/(1-n)} - 1\right] \tag{3.88}$$

An evaluation of this equation shows that especially the first harmonic makes its appearance. The capacitance shift caused by the alternating voltage superimposed on the tuning voltage is shown in Figure 3.47. However, the voltage distortion, and thus the capacitance shift, can be largely avoided if two tuner diodes are used, as in Figure 3.45.
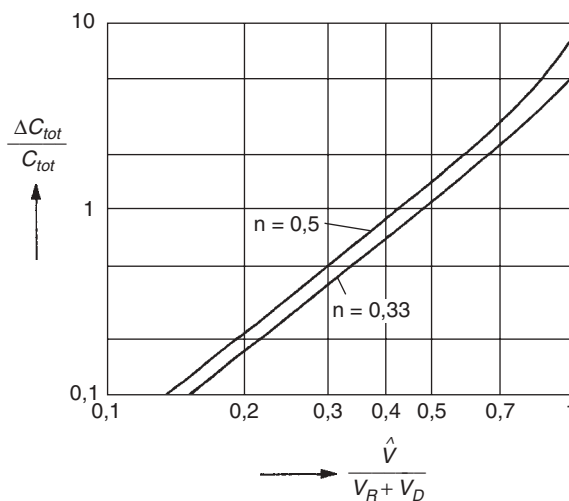

FIGURE 3.47   Capacitance increase as function of ac voltage drop across tuner diode.

3.3 MICROWAVE TRANSISTORS

3.3.1 Transistor Classification

Microwave transistors can be presently classified into five groups:

Silicon BJTs
Silicon MOSFETs
Gallium arsenide MESFETs
InGaAs/InP PHEMTs
InAlAs/InGaAs MHEMTs
InGaP/InGaAs and SiGe HBTs

The first transistors used germanium in 1947 [3.13], but the maximum junction temperature was too low, so it was quickly replaced by the silicon BJT, for a T_{max} of 200°C compared to 100°C for germanium. The silicon MOSFET has been very popular for digital circuits, but it became a competitive analog microwave transistor as early as 1972 with the disclosure of the DMOS transistor, which has many attributes, including high breakdown voltage and high f_t (4–7 GHz typical) [3.2], and it has many applications up to 2.5 GHz today. The GaAs MESFET was developed about 1965 at Cal Tech, Fairchild, and IBM (Switzerland) [3.14–3.16]. These transistors have been replaced by HEMTs of various types (PHEMT and MHEMT) because of their superior performance. The PHEMT is a pseudomorphic high-electron-mobility transistor, meaning the channel material is lattice matched to the adjoining layers. The MHEMT is a metamorphic high-electron-mobility transistor, where graded doping can be used to change the breakdown voltage depending on the application [3.17]. The final category is the HBT (heterojunction bipolar transistor), which was developed to have a GaAs bipolar with high emitter efficiency. The most useful forms of this device are the InGaP/InGaAs and SiGe HBTs, which are having a strong impact on today's technology.

Compounds of groups III to V have inherent advantages over silicon, including higher T_{max} in theory. GaAs, InGaAs, and InP are a few of these materials [3.11]. The Compounds of groups II to VI have similar advantages, including SiC (4 W/mm) and GaN (10 W/mm). Some of these physical parameters are compared in Table 3.12, where the main advantage of silicon is lower cost.

It is also important to note that Agilent has discontinued MESFETs in favor of HEMTs, which are superior in nearly every way, except possibly third-order inter-modulation products. The possible exception to this rule is the enhancement PHEMT, which is very new. Even newer is the MHEMT, discussed later in this chapter.

For the first edition of this book, the choice of transistors was usually between the silicon BJT and the gallium arsenide MESFET. A comparison of these devices in 2005 is given in Table 3.13. Silicon has another important advantage, a lower flicker corner frequency, which is important for oscillator applications.

The higher output power of the GaAs MESFET, PHEMT, and HBT is a direct result of the higher critical field and higher saturated drift velocity for *n*-type material (electrons). The approximate power–frequency squared limit is given by [3.38]

$$Pf^2 = \left(\frac{E_c v_s}{2\pi} \right)^2 \frac{1}{X_c} \tag{3.89}$$

TABLE 3.12   Semiconductor Parameters at $T = 25°C$ [3.11, 3.18–3.29]

Parameter	Ge	Si	GaAs	InGaAs 2 DEG[a]	Si_(1-x)Ge_x 2 DEG[a]	InP
Electron mobility (cm^2/V s)	3900	1500	8500	6000	$1450 - 4325x$ $0 < x < 0.3$	5400
Hole mobility (cm^2/V s)	1900	450	400	200	$450 - 865x$	200
Saturated drift velocity, $\times 10^7$ (cm/s) electrons	0.6	0.7	2.0	2.7	0.65	2.0
Band gap (eV)	0.66	1.12	1.42	0.78	$1.12 - 0.41x + 0.088x^{\wedge 2}$, $x < 0.85$ $1.86 - 1.2x$, $x > 0.85$	1.35
Avalanche field, $\times 10^5$ (V/cm)	2.3	3.8	4.2	—	3.0	5.0
T_{max} (°C)	100	270	300	300	225	400
T_{max} practical (°C)	75	200	175	175	155	300
Thermal conductivity at 150°C (W/cm°C)	0.4	1.0	0.3	—		
Thermal conductivity at 25°C (W/cm°C)	0.6	1.4	0.45	—	$0.46 + 0.084x$	0.68

[a]DEG = Two dimensional electron gas.

where E_c = effective electric field before avalanche breakdown

$\qquad v_s$ = drift velocity of carriers (electrons)

$\qquad X_c$ = device impedance level

Since the parameters E_c and v_s are higher for GaAs and other compound semiconductors of groups III to V, the GaAs MESFET is intrinsically a higher power device.

If we include a correction factor for the geometry of the transistor, the effective values for GaAs are

$$X_c \simeq 1 \ \Omega$$

$$E_c \simeq \tfrac{1}{4} E_{max} \simeq 10^5 \ \text{V/cm}$$

$$v_s \simeq \tfrac{1}{5} v_{sat} \simeq 4 \times 10^6 \ \text{cm/s}$$

$$Pf^2 \simeq 5 \times 10^{21} \ \text{W/s}^2$$

TABLE 3.13   2002 Comparison of Microwave Transistors [3.30–3.37]

Parameter	Silicon BJT[a] ($f_t = 10$ GHz)					GaAs MESFET[b] ($f_t = 25$ GHz)				
	1 GHz	2 GHz	4 GHz	8 GHz	12 GHz	4 GHz	8 GHz	12 GHz	18 GHz	26 GHz
Gain (dB)	18	14	16	10	7	22	20	24	10	8
F_{min} (dB)	0.6	1.3	2.5	4.5	8	0.5	0.7	1.0	1.2	1.6
Power (W)	–	>100	8	3	0.5	40	20	10	3	1

Parameter	PHEMT (AlGaAs/InGaAs)[c] ($f_t = 50$ GHz)				HBT (InGaP/InGaAs)/SiGe[d] ($f_t = 40$ GHz)		
	2 GHz	12 GHz	36 GHz	60 GHz	12 GHz	36 GHz	60 GHz
Gain (dB)	17	24	15	9	22/7	11	8
F_{min} (dB)	0.3	0.5	3	5	2/3	5	8
Power (W)	25	20	2	0.25	15/1	1	–
Power-added efficiency (%)	90	65	55	42	60	40	20

Note: $1/f_c$ = oscillator noise flicker corner frequency; Pf^2 = theoretical limit; L_G = emitter width.
[a] $1/f_c = 5$ kHz; $Pf^2 = 5 \times 10^{20}$ W/s^2.
[b] $1/f_c = 3$ MHz; $Pf^2 = 5 \times 10^{21}$ W/s^2
[c] $1/f_c = 3$ MHz; $L_G = 0.15$–0.30; power density = 2 W/mm.
[d] $1/f_c = 100$ kHz/ 20 kHz; $L_c = 0.25$–2.0; power density = 4/0.8 W/mm.

In 1980, the continuous-wave performance of 10 W at 10 GHz had already been achieved, giving

$$Pf^2 = 10 \times 10^{10} \times 10^{10} = 10^{21} \text{ W/s}^2$$

In 1988, the class A continuous-wave performance of 8 W at 15 GHz had been reached [3.39], which is $Pf^2 = 1.8 \times 10^{21}$ W/s^2. In 1978, the continuous-wave silicon bipolar transistor had reached 1.5 W at 10 GHz [3.40]:

$$Pf^2 = 1.5 \times 10^{10} \times 10^{10} = 1.5 \times 10^{20} \text{ W/s}^2$$

with a theoretical limit of S 5×10^{20} W/s^2, an order of magnitude lower than GaAs. This was a Texas Instruments research contract with the Air Force, at Wright Patterson Air Force Base, and the process was deemed impractical for production in the early 1980s.

The measured Pf^2 product improves by about a factor of 2 under pulsed conditions [3.41]. The advantages of silicon are lower cost, higher thermal conductivity, and lower $1/f$ noise. The device limitations on frequency response are the transit time of electrical charge and the rate of change of electrical charge. These limitations are discussed in this chapter. For completeness, the heterojunction transistors have been included in the tables. These transistors will become the microwave transistors of the future.

3.3.2   Transistor Structure Types

All current RF silicon transistors are of the bipolar *npn* planar epitaxial type or the *n*-channel MOS or DMOS epitaxial type. Briefly, the significance of each of these terms is as follows:

Bipolar In its broadest sense, the basic structure shown schematically in Figure 3.48, that is, the familiar three-semiconductor-region structure. *Bipolar* specifically means that there are two *pn* junctions used in the transistor structure. The high-frequency bipolar has an "*npin*" structure, where the thickness of the *i* layer determines the collector–base breakdown voltage. In contrast, unipolar types include the junction-gate and insulated-gate FETs, which are basically one- or two-semiconductor-region structures in which carriers of a single polarity (usually electrons because of the higher mobility) dominate.

npn An abbreviation for *n*-type, *p*-type, *n*-type that identifies the regions of the structure as to polarity of the dominant or majority carrier in each region. The other polarity type is *pnp* (see Fig. 3.48).

Planar A term that denotes that both emitter–base and base–collector junctions of the transistor intersect the device surface in a common plane (hence, a better term might be *coplanar*). However, the real significance of the so-called planar structure is that the technique of diffusing dopants through an oxide mask, used in fabricating such a structure, results in junctions being formed beneath a protective oxide layer. These protected junctions are less prone to the surface problems sometimes associated with other types of structures, such as the mesa.

Epitaxial This term, as it is commonly used, is actually a shortening of the term *epitaxial-collector*. That is, the collector region of the transistor is formed by the epitaxial technique, rather than by diffusion, which is commonly used to form the base and emitter regions. The epitaxial layer is formed by condensing a single-crystal film of semiconductor material upon a wafer or substrate that is usually of the same material. Thus, an epitaxial (collector) transistor is one in which the collector region is formed upon a low-resistivity substrate. Subsequently, the base and emitter regions are diffused into the "epi" layer. The epitaxial technique lends itself to precise tailoring of collector region thickness and resistivity with consequent improved device performance and uniformity.

Ion Implantation A newer form of doping semiconductors which is much more repeatable (higher yield) is the ion implantation process developed in the early 1970s [3.12]. This technique is used widely with excellent uniform yields, which is needed in production.

Cross–Section of a Simplified Bipolar Transistor (Not to Scale)
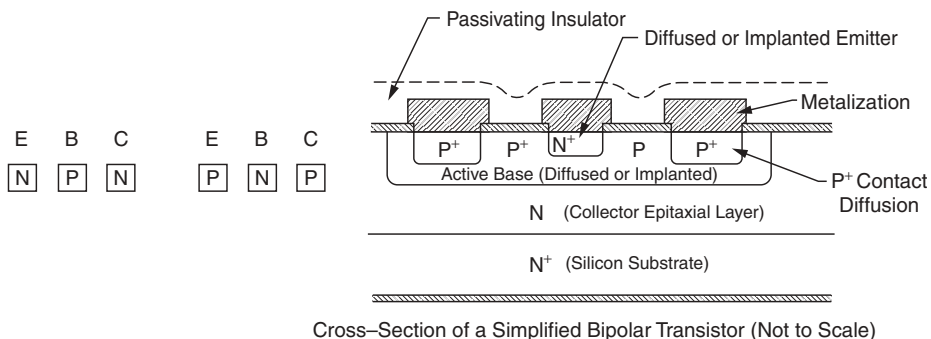
**FIGURE 3.48** Transistor structure schematic.

DMOS (double - diffused MOS)
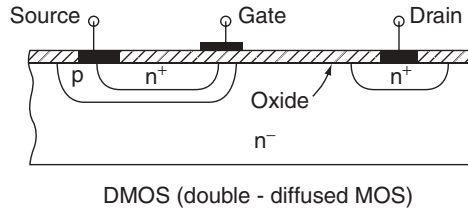
FIGURE 3.49 Cross section of D-MOS transistor on epitaxial material. (From Ref. 3.2 ©
IEEE 1972.)

MOSFET It has been known for many years that majority-carrier devices such
as the MOSFET should have higher cutoff frequencies than the minority-carrier
devices such as the BJT. This was demonstrated in 1969 with the disclosure
of the D-MOS transistor [3.2] (see Fig. 3.49). In this structure, one can make
an analogy to the microwave *npin* BJT structure. The forward-biased emitter
emits electrons into the base, which diffuse and drift as minority carriers to the
reverse-biased collector–base *i* region, where they are swept to the collector at
the v_{sat} velocity. In the DMOS structure, we also have an *npin* structure, where
the source of electrons is the ohmic source region, the gate makes a surface
inversion layer of electrons in a *p*-type region, and the electrons are swept to
the ohmic drain region at the v_{sat} velocity by a high positive bias V_{ds}, where
the source is considered grounded. The flow of electrons in the channel beneath
the gate is controlled by the bias voltage V_{gs}, which is normally negative for
a depletion-mode FET. The f_{max} can be shown to be proportional to $(1/L_{base})^2$
in the BJT, but if the carriers quickly reach v_{sat} in the channel, the f_{max} is
proportional to $1/L_{channel}$ in the D-MOS and MESFET devices [3.2].

3.3.3   dc Model of BJT

dc Model   The basic dc model used in SPICE and the harmonic balance simulator
to describe the BJT [3.42] is the Ebers–Moll model (Fig. 3.50). The model shown
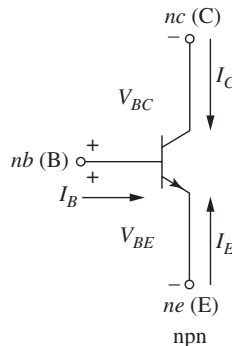
FIGURE 3.50   The *npn* bipolar transistor elements.
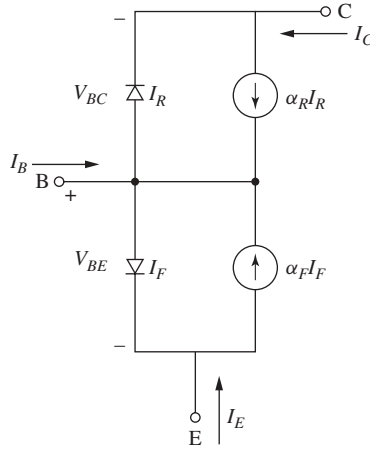
FIGURE 3.51   Ebers–Moll injection model of *npn* transistor.

in Figure 3.51 is the *injection version* of the Ebers–Moll model, which uses diode currents I_F and I_R as reference:

$$I_F = I_{ES}(e^{qV_{BE}/kT} - 1) \qquad I_R = I_{CS}(e^{qV_{BC}/kT} - 1) \qquad (3.90)$$

Where the emission coefficients have been assumed to equal 1. The three terminal currents of the transistor, I_C, I_E, and I_B, can be expressed as functions of the two reference currents and the forward- and reverse-current gains, a_F and a_R, of the common-base (CB) connected BJT:

$$I_C = a_F I_F - I_R \qquad I_E = I_F + a_R I_R \qquad I_B = (1 - a_F)I_F + (1 - a_R)I_R \qquad (3.91)$$

where I_{ES} and I_{CS} are the saturation currents of the *BE* and *BC* junctions, respectively. These two currents satisfy the reciprocity equation

$$a_F I_{ES} = a_R I_{CS} = I_S \qquad (3.92)$$

where I_S, a SPICE BJT model parameter, is the saturation current of the transistor.

The SPICE implementation of the Ebers–Moll model is a variant known as the *transport version* and is shown in Figure 3.52. The injection version is commonly documented in textbooks and has been repeated above for comparison with the transport version. The currents flowing through the two sources, which represent the transistor effect of the two back-to-back *pn* junctions, are chosen as reference:

$$I_{CC} = I_S(e^{qV_{BE}/N_F \cdot kT} - 1) \qquad I_{CE} = I_S(e^{qV_{BC}/N_R \cdot kT} - 1) \qquad (3.93)$$

The three terminal currents assume the following expressions:

$$I_C = I_{CC} - \frac{\beta_R + 1}{\beta_R}I_{CE} = I_{CT} - \frac{1}{\beta_R}I_{CE} \qquad (3.94)$$
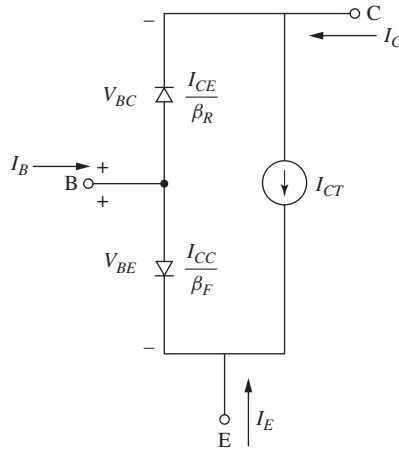
FIGURE 3.52   Ebers–Moll transport model of *npn* transistor.

$$I_E = I_{CE} - \frac{\beta_F + 1}{\beta_F} I_{CC} = -I_{CT} - \frac{1}{\beta_F} I_{CC} \qquad (3.95)$$

$$I_B = \frac{1}{\beta_F} I_{CC} + \frac{1}{\beta_R} I_{CE} = I_{BC} + I_{BE} \qquad (3.96)$$

where

$$I_{CT} = I_{CC} - I_{CE} \qquad (3.97)$$

β_F and β_R in the above equations are the forward- and reverse-current gains, SPICE parameters BF and BR, of a bipolar transistor in the common-emitter (CE) configuration.

Depending on the values of the two controlling voltages, V_{BE} and V_{BC}, the transistor can operate in the following four modes:

Forward active	$V_{BE} > 0$ and $V_{BC} < 0$
Reverse active	$V_{BE} < 0$ and $V_{BC} > 0$
Saturation	$V_{BE} > 0$ and $V_{BC} > 0$
Cutoff	$V_{BE} < 0$ and $V_{BC} > 0$

In most applications, the transistor is operated in the forward active, or linear, region and in some situations in the saturation region. The suffixes F and R in many SPICE parameter names indicate the region of operation.

The $I-V$ characteristics described by Eqs. (3.10) are shown in Figure 3.53 for positive values of V_{BE} and V_{CE}. These characteristics are ideal, ignoring the effects of finite output conductance in the forward and reverse regions and the parasitic series resistances associated with the collector, base, and emitter regions; these resistances are modeled by parameters RC, RB, and RE, respectively.

The finite output conductance of a BJT is modeled in SPICE by the Early effect implemented by two parameters, VAF and VAR. The *Early voltage* is the point on the V_{BC} axis in the (I_C, V_{BC}) plane where the extrapolations of the linear portions
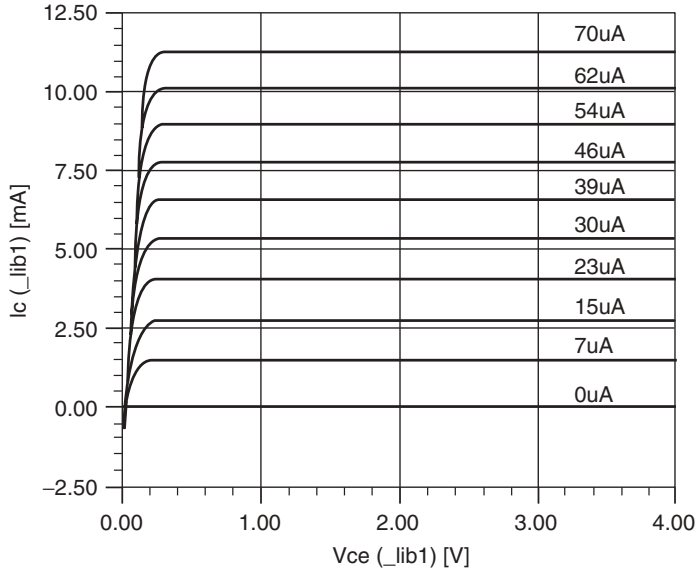
FIGURE 3.53   Ideal $I-V$ curves of *npn* transistor.
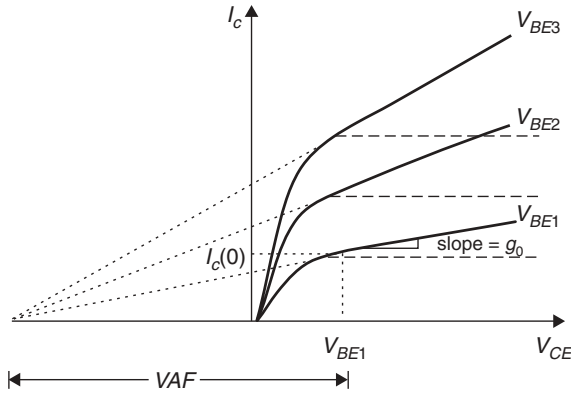
FIGURE 3.54 $I-V$ curves showing Early voltage of *npn* transistor.

of all I_C characteristics meet. This geometric interpretation of the Early effect and its SPICE implementation are shown in Figure 3.54 for the $I_C = f(V_{CE})$ characteristics: $V_{CE} = V_{BE} - V_{BC}$. The reverse Early voltage, VAR (sometimes called the late voltage), has a similar interpretation for the reverse region. For most practical applications VAF is important and VAR can be neglected.

With the addition of the Early voltage, I_C and I_{CT} in Eqs. (3.94) are modified as follows:

$$I_C = (I_{CC} - I_{CE}) \left(1 - \frac{V_{BC}}{\text{VAF}} - \frac{V_{BE}}{\text{VAR}} \right) - \frac{1}{\beta_R} I_{CE} = I_{CT} - I_{BC} \qquad (3.98)$$

Dynamic Models   The dynamic behavior of a BJT is modeled by five different charges [3.42]. Two charges, Q_{DE} and Q_{DC}, are associated with the mobile carriers. These are the diffusion charges represented by the current sources I_{CC} and I_{CE} in the Ebers–Moll model. The other three charges model the fixed charges in the depletion regions of the three junctions: base–emitter, Q_{JE}; base–collector, Q_{JC}; and collector–substrate, Q_{JS}.

The diffusion charges are modeled by the following equations in the large-signal transient analysis:

$$Q_{DE} = T_F I_{CC} \tag{3.99}$$

$$Q_{DC} = T_R I_{CE} \tag{3.100}$$

where T_F and T_R are the forward and reverse transit times, respectively, of the injected minority carriers through the neutral base.

The depletion charges can be derived using the nonlinear equation that defines the depletion capacitance, C_J, of a *pn* junction. The SPICE large-signal implementation of the three depletion charges defines the charge Q_J. The three voltage-dependent junction capacitances are described by the following functions:

$$C_{JE} = \frac{C_{JE}}{(1 - V_{BE}/V_{JE})^{M_{JE}}} \tag{3.101}$$

$$C_{JC} = \frac{C_{JC}}{(1 - V_{BC}/V_{JC})^{M_{JC}}} \tag{3.102}$$

$$C_{JS} = \frac{C_{JS}}{(1 - V_{CS}/V_{JS})^{M_{JS}}} \tag{3.103}$$

Each junction can be characterized in SPICE by up to three parameters: C_{JX}, the zero-bias junction capacitance; V_{JX}, the built-in potential; and M_{JX}, the grading coefficient. The symbol X stands for E, C, or S, denoting the emitter, collector, or substrate junction, respectively.

The nonlinear BJT model in SPICE, including charge storage and parasitic terminal resistances, is depicted in Figure 3.55. The five charges are consolidated into three: Q_{BE}, which includes Q_{DE} and Q_{JE}; Q_{BC}, which includes Q_{DC} and Q_{JC}; and Q_{CS}, modeled by C_{CS}, the collector–substrate capacitance. Figure 3.55 is a first-order representation of the complete Gummel–Poon BJT model available in SPICE and is sufficiently accurate for many applications. The complete model includes second-order effects, such as β_F and τ_F dependency and I_C, base push-out, and temperature effects. The complete equations and model parameters are summarized in Appendix A.

The linearized small-signal model of a BJT, also known as the hybrid-π model, is shown in Figure 3.56. The nonlinear diodes and the current generator I_{CT} in Figure 3.52 are replaced by the following linear resistances (conductances) and transconductances:

$$g_\pi = \frac{1}{r_\pi} = \frac{\partial I_B}{\partial V_{BE}} = \frac{1}{\beta_F}\frac{dI_{CC}}{dV_{BE}} \tag{3.104}$$

$$g_\mu = \frac{1}{r_\mu} = \frac{\partial I_B}{\partial V_{BC}} = \frac{1}{\beta_R}\frac{dI_{CE}}{dV_{BC}} \tag{3.105}$$
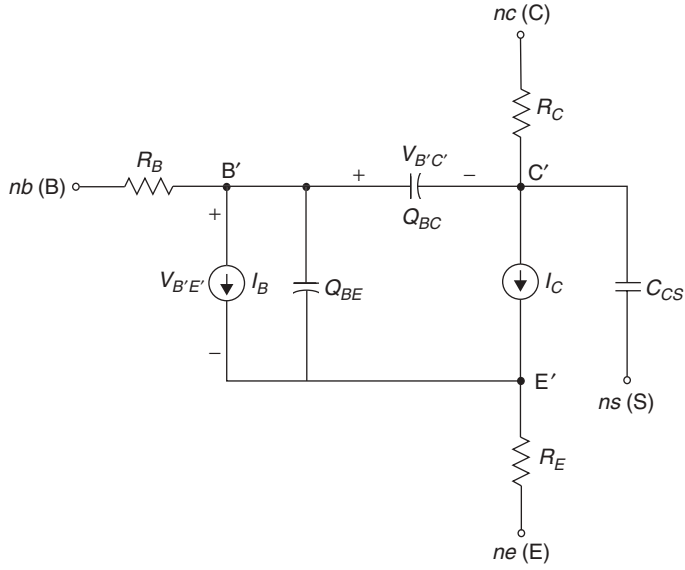
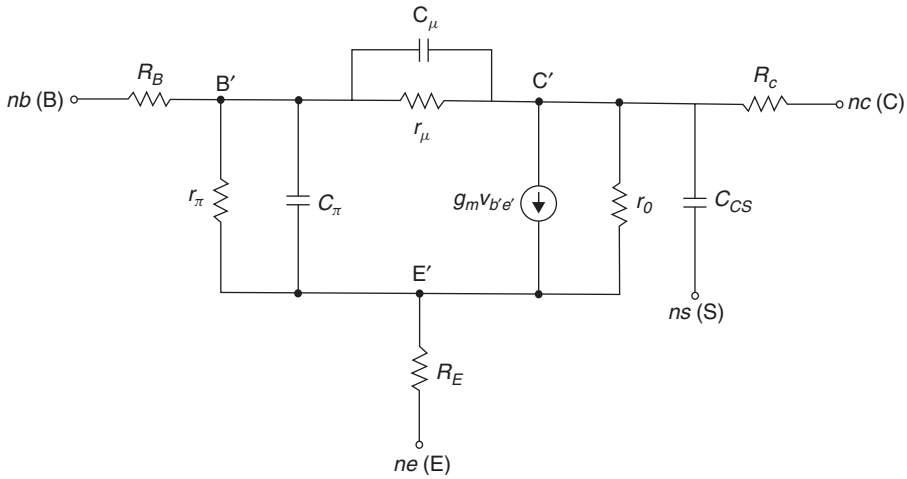**FIGURE 3.55**   Large-signal SPICE BJT model.

FIGURE 3.56   Small-signal SPICE BJT model.

$$g_{mF} = \frac{\partial I_{CT}}{\partial V_{BE}} \tag{3.106}$$

$$g_{mR} = g_0 = \frac{1}{r_0} = -\frac{\partial I_{CT}}{\partial V_{BC}} = -\frac{\partial I_C}{\partial V_{BC}} - \frac{\partial I_B}{\partial V_{BC}} = -\frac{\partial I_C}{\partial V_{BC}} - g_\mu \tag{3.107}$$

$$g_m = g_{mF} - g_{mR} = \frac{\partial I_C}{\partial V_{BE}} - g_0 \tag{3.108}$$

The above small-signal parameters have been derived assuming no parasitic terminal resistances R_C, R_B, and R_E; if these resistances are present, terminal voltages $V_{B'E'}$ and $V_{B'C'}$ replace V_{BE} and V_{BC}.

The small-signal ac collector current i_c can be expressed using the hybrid-π model (Fig. 3.56) as

$$i_c = \frac{\partial I_{CT}}{\partial V_{BE}} v_{be} + \frac{\partial I_{CT}}{\partial V_{BC}} v_{bc} - \frac{\partial I_{BC}}{\partial V_{BC}} v_{bc} = g_m v_{be} + g_0 v_{ce} - g_\mu v_{bc} \qquad (3.109)$$

where v_{bc} has been replaced by $v_{be} - b_{ce}$ in the second term. In the forward active region, the small-signal equations assume the more commonly known expressions [3.42]

$$i_c = g_m v_{be} = g_{mF} v_{be} \qquad (3.110)$$

$$g_m = g_{mF} = \beta_F g_\pi = \frac{q I_C}{N_F \cdot kT} \qquad (3.111)$$

$$r_\pi = \frac{1}{g_\pi} = \frac{\beta_F}{g_m} \qquad (3.112)$$

$$r_\mu \to \infty, \qquad q_\mu \approx 0 \qquad (3.113)$$

$$r_0 = \frac{1}{g_0} = \frac{V_{AF}}{I_C} = \frac{V_{AF}}{g_m V_{th}} \qquad (3.114)$$

In small-signal ac analysis, charge storage effects are modeled by nonlinear capacitances. The diffusion charges are modeled by two diffusion capacitances, C_{DE} and C_{DC}:

$$C_{DE} = \frac{dQ_{DE}}{dV_{BE}} = T_F \frac{\partial I_{CT}}{\partial V_{BE}} = T_F g_{mF} \qquad (3.115)$$

$$C_{DC} = \frac{dQ_{DC}}{dV_{BC}} = T_R \frac{\partial I_{CT}}{\partial V_{BC}} = T_R g_{mR} \qquad (3.116)$$

Where g_{mF} and g_{mR} are the forward and reverse transconductances of the BJT. The junction capacitances are defined by Eqs. (3.115) and (3.116). In the small-signal BJT model (Fig. 3.52) the two types of capacitances for the *BE* and *BC* regions are consolidated in C_π and C_μ, corresponding to Q_{BE} and Q_{BC}, respectively:

$$C_\pi = C_{DE} - C_{JE} \qquad (3.117)$$

$$C_\mu = C_{DC} + C_{JC} \qquad (3.118)$$

An important characteristic of a BJT is the cutoff frequency f_T, where the current gain drops to unity; f_T can be expressed as a function of the small-signal parameters:

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)} \qquad (3.119)$$

Large-Signal Bipolar Transistor Model   The previous introduction to the nonlinear bipolar transistor gave a simplified overview. The transport equations refer to the Gummel–Poon transistor model, which is the one implemented in all modern harmonic balance and RF-SPICE programs, including its package parameters and splitting up the

base spreading resistor. Appendix A shows the implementation of the Gummel–Poon model, including the equations applicable for the model.

A good example of the SiGe microwave bipolar transistor is the Infineon model BFP620 transistor with a cutoff frequency of 65 GHz (Table 3.14).

We now take the SPICE parameters given in Table 3.14 and use a simulator to generate S parameters at a given dc bias point of 2 V and 10 mA. At the same time, we plot the published S parameters at the same bias point. This gives a good feeling for the accuracy of the simulation and SPICE parameters. The circuit diagram in Figure 3.57a showing the transistor and its parasitics also uses published values. Figures 3.57a to 3.57d show the tracking of measured versus simulated parameters from 500 MHz to 6 GHz.

TABLE 3.14   BFP620 SiGe Transistor

Description

- High-gain, low-noise RF transistor
- Provides outstanding performance for a wide range of wireless applications
- Ideal for CDMA and WLAN applications
- Outstanding noise figure $F = 0.7$ dB at 1.8 GHz; Outstanding noise figure
   $F = 1.4$ dB at 6 GHz
- High maximum stable gain, $G_{ms} = 21.5$ dB at 1.8 GHz

Parameter	Symbol	Value	Unit
Maximum Ratings			
Collector–emitter voltage	V_{CEO}	2.3	V
Collector–base voltage	V_{CBO}	7.5	V
Emitter–base voltage	V_{EBO}	1.2	V
Collector current	I_C	80	mA
Base current	I_B	3	mA
Total power dissipation, $T_S \leq 95^a$	P_{tot}	185	mW
Junction temperature	T_j	150	°C
Ambient temperature	T_A	$-65 \ldots 150$	°C
Storage temperature	T_{stg}	$-65 \ldots 150$	°C
Thermal Resistance			
Junction-soldering point[b]	R_{thJS}	≤ 300	K/W

Parameter	Symbol	Values			Unit
		Minimum	Typical	Maximum	
Electrical Characteristics at $T_A = 25°C$ (unless otherwise specified)					
DC CHARACTERISTICS					
Collector–emitter breakdown voltage: $I_C = 1$ mA, $I_B = 0$	$V_{(BR)CEO}$	2.3	2.8	—	V
Collector–base cutoff current: $V_{CB} = 5$ V, $I_F = 0$	I_{CBO}	—	—	200	nA

TABLE 3.14   BFP620 SiGe Transistor (*continued*)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
			Values		Unit
Emitter–base cutoff current: $V_{EB} = 1$ V, $I_C = 0$	I_{EBO}	—	—	10	μA
dc Current gain: $I_C = 20$ mA, $V_{CE} = 1.5$ V	h_{FE}	100	180	250	—
AC CHARACTERISTICS (VERIFIED BY RANDOM SAMPLING)					
Transition frequency: $I_C = 60$ mA, $V_{CE} = 1.5$ V, $f = 1$ GHz	f_T	—	65	—	GHz
Collector–base capacitance: $V_{CB} = 2$ V, $f = 1$ MHz	C_{cb}	—	0.12	0.2	pF
Collector–emitter capacitance: $V_{CE} = 2$ V, $f = 1$ MHz	C_{ce}	—	0.22	—	pF
Emitter–base capacitance: $V_{EB} = 0.5$ V, $f = 1$ MHz	C_{eb}	—	0.5	—	pF
Noise figure: $I_C = 5$ mA, $V_{CE} = 2$ V, $Z_S = Z_{S,\mathrm{opt}}$, $Z_L = Z_{L,\mathrm{opt}}$, $f = 1.8$ GHz	F	—	0.7	—	dB
Power gain, maximum stable[c]: $I_C = 20$ mA, $V_{CE} = 2$ V, $Z_S = Z_{S,\mathrm{opt}}$, $Z_L = Z_{L,\mathrm{opt}}$, $f = 1.8$ GHz	G_{ms}	—	21.5	—	dB
Insertion power gain: $I_C = 20$ mA, $V_{CE} = 2$ V, $f = 1.8$ GHz, $Z_S = Z_I = 50$ Ω	$|S_{21}|^2$	—	19	—	dB
Third-order intercept point at output[d]: $V_{CE} = 2$ V, $f = 1.8$ GHz, $Z_S = Z_L = 50$ Ω, $I_C = 20$ mA	IP3	—	25	—	dBm
1 dB Compression point at output: $V_{CE} = 2$ V, $f = 1.8$ GHz, $Z_S = Z_L = 50$ Ω, $I_C = 20$ mA	$P_{-1\ \mathrm{dB}}$	—	11	—	dBm

SPICE Parameters (Gummel–Poon Model, Berkley-SPICE
2G6 Syntax):Transistor Chip Data

IS = 354 aA	BF = 557.1	NF = 1.021
VAF = 1000 V	IKF = 2.262 A	ISE = 2.978 pA
NE = 3.355	BR = 100	NR = 1
VAR = 1.2 V	IKR = 6.31 mA	ISC = 19.23 fA
NC = 2.179	RB = 2.674 Ω	IRB = 18 μA

TABLE 3.14   (*continued*)

RBM = 2.506 Ω	RE = 0.472 Ω	RC = 2.105 Ω
CJE = 371.6 fF	VJE = 0.898 V	MJE = 0.315
TF = 1.306 ps	XTF = 2.71	VTF = 0.492 V
ITF = 2.444 A	PTF = 0 deg	CJC = 225.6 fF
VJC = 0.739 V	MJC = 0.3926	XCJC = 1
TR = 0.3884 ns	CJS = 60 fF	VJS = 0.5 V
MJS = 0.5	XTB = −0.9	EG = 1.114 eV
XTI = 3.43	FC = 0.821	TNOM = 298 K

Package Equivalent Circuit
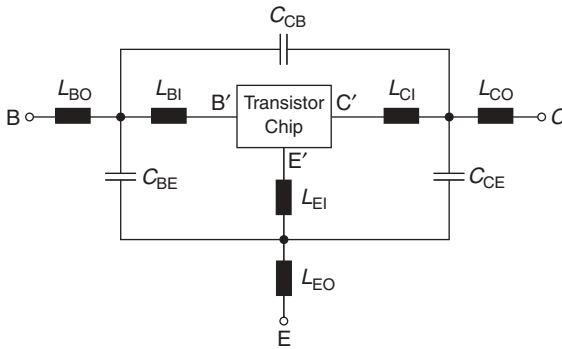
L_{BI} = 0.47 nH
L_{BO} = 0.53 nH
L_{EI} = 0.23 nH
L_{EO} = 0.05 nH
L_{CI} = 0.56 nH
L_{CO} = 0.58 nH
C_{BE} = 136 fF
C_{CB} = 6.9 fF
C_{CE} = 134 fF
Valid up to 6 GHz.

Transition frequency $f_T = f(I_C)$
f = 1 GHz
V_{CE} = parameter in V
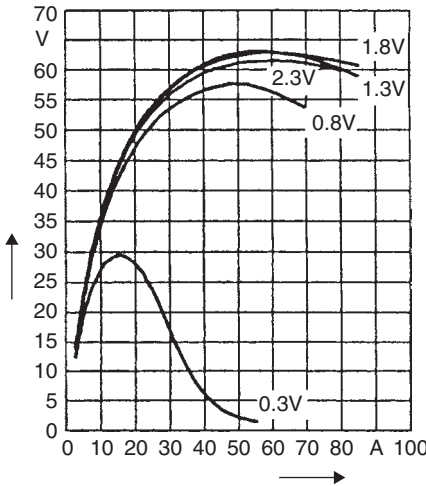
Power gain G_{ma}, $G_{ms} = f(I_C)$
V_{CE} = 2 V
f = parameter in GHz
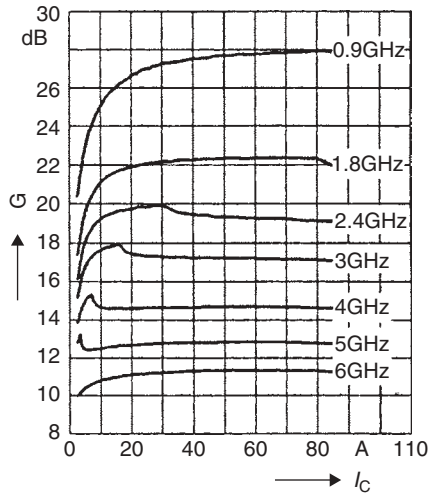
TABLE 3.14   BFP620 SiGe Transistor (*continued*)

Power gain $G_{ma}, G_{ma} = f(V_{CE})$
$I_C = 20$ mA
f = parameter in GHz

BFP620 die
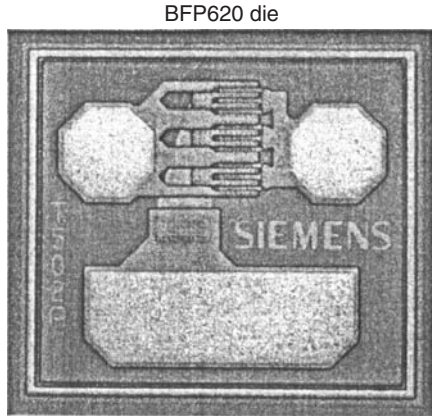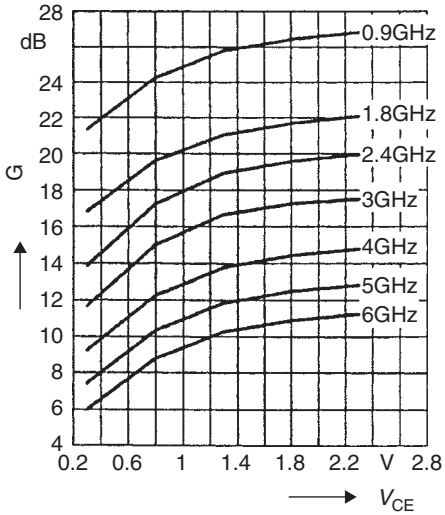
Picture of the Infineon BFP620
microwave transistor die.

Noise figure $F = f(I_C)$
$V_{CE} = 2$ V, $Z_S = Z_{Sopt}$
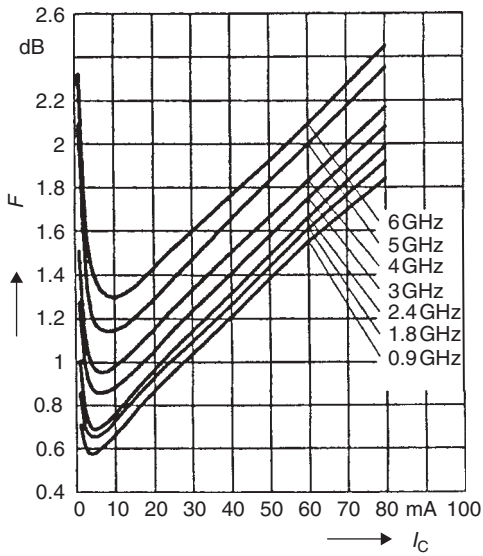
Noise figure $F = f(I_C)$
$V_{CE} = 2$ V, $f = 1.8$ GHZ

TABLE 3.14   (*continued*)

Noise figure $F = f(f)$
$V_{CE} = 2$ V, $Z_S = Z_{Sopt}$

Source impedance for min. noise figure vs. Frequency
$V_{CE} = 2$ V, $I_C = 5$ mA / 20 mA
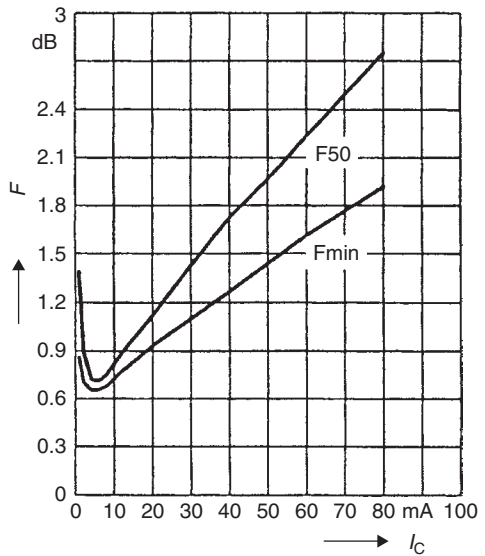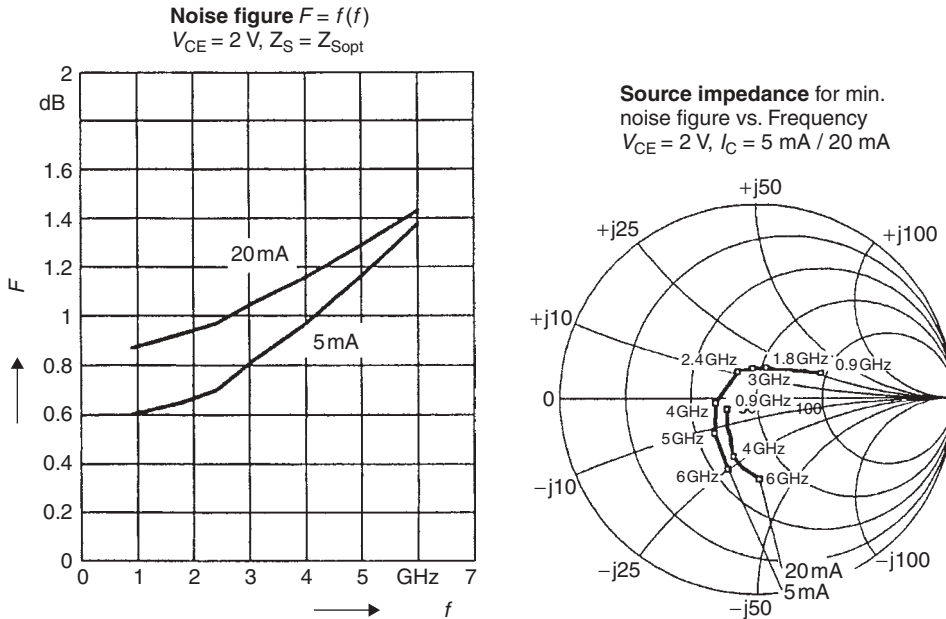
[a] T_S is measured on the emitter lead at the soldering point to the printed circuit board.
[b] For calculation of R_{thJA} refer to Application Note Thermal Resistance.
[c] $G_{ms} = |S_{21}/S_{12}|$.
[d] IP3 value depends on termination of all intermodulation frequency components. Termination used for this measurement is 50 Ω from 0.1 MHz to 6 GHz.
All parameters are ready to use, no scaling is necessary.
The SOT-343 package has two emitter leads. To avoid high complexity of the package equivalent circuit, both leads are combined in one electrical connection.

Silicon Bipolar Small-Signal Model   The small-signal equivalent circuit of the silicon bipolar transistor can be derived from the physical cross section of the device given in Figure 3.58. For this device structure, the distributed T-equivalent circuit of Figure 3.59 has been found to be an effective small-signal model at fixed-bias conditions. The parameter values for this equivalent circuit are given in Table 3.15 for three modern microwave transistors at the bias for a low noise figure and at the bias for high gain. The emitter pitch and emitter periphery for these transistors will determine the optimum frequency range of operation. These parameters are also given in Table 3.15.

Other bipolar transistor equivalent circuits are given in Figure 3.60, including the distributed hybrid-Π, the simplified hybrid-Π, and the simplified T-equivalent circuit. The simplified circuits are less accurate in broadband device simulations. The hybrid-Π is popular because of its similarity to the GaAs MESFET equivalent circuit described later. The bonding inductances to the base and emitter must also be included in the RF design, usually about 0.5 nH for the base and 0.2 nH for the emitter. Typical circuit values are given for a modern silicon bipolar transistor (Agilent/Avantek AT-41400)

Model−BFP620 (Spice Parameters)
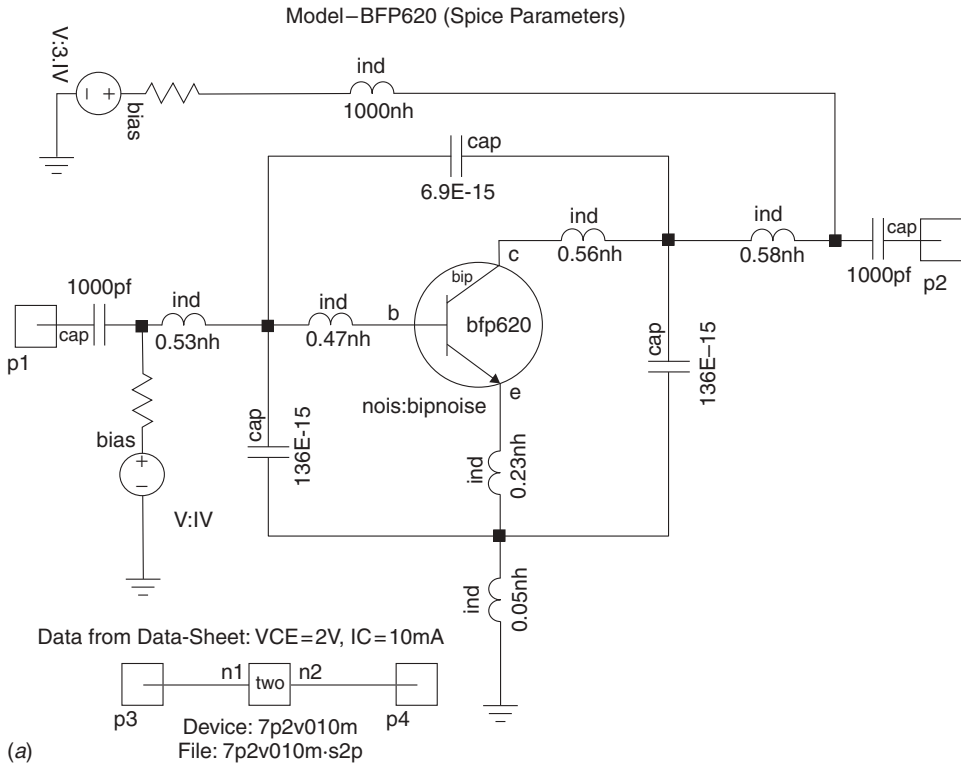
(a)
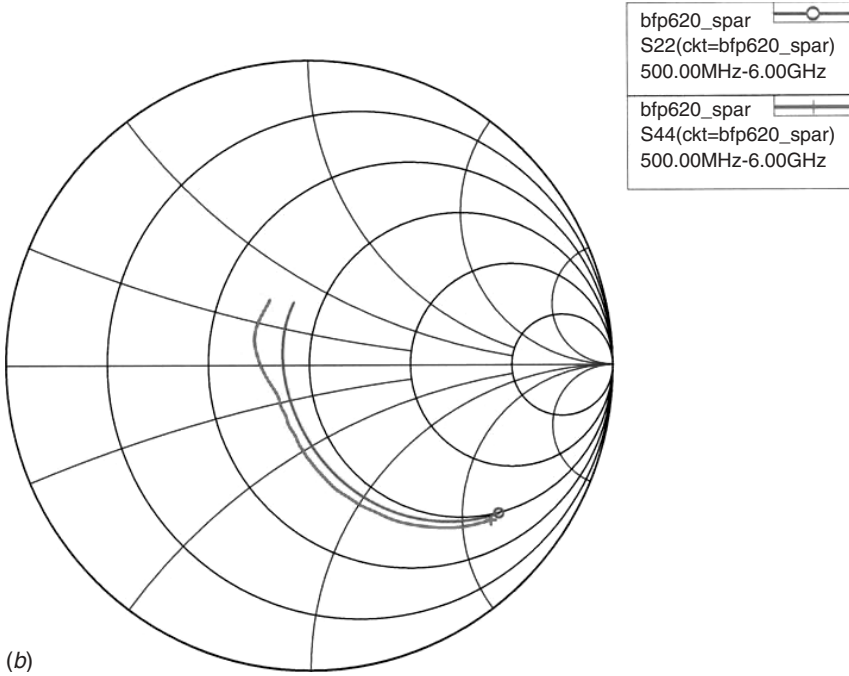
(b)

FIGURE 3.57   (*a*) Chip model of BFP 620. (*b*) S_{22} fit. (*c*) S_{11} fit. (*d*) S_{21} fit. (*e*) S_{12} fit.
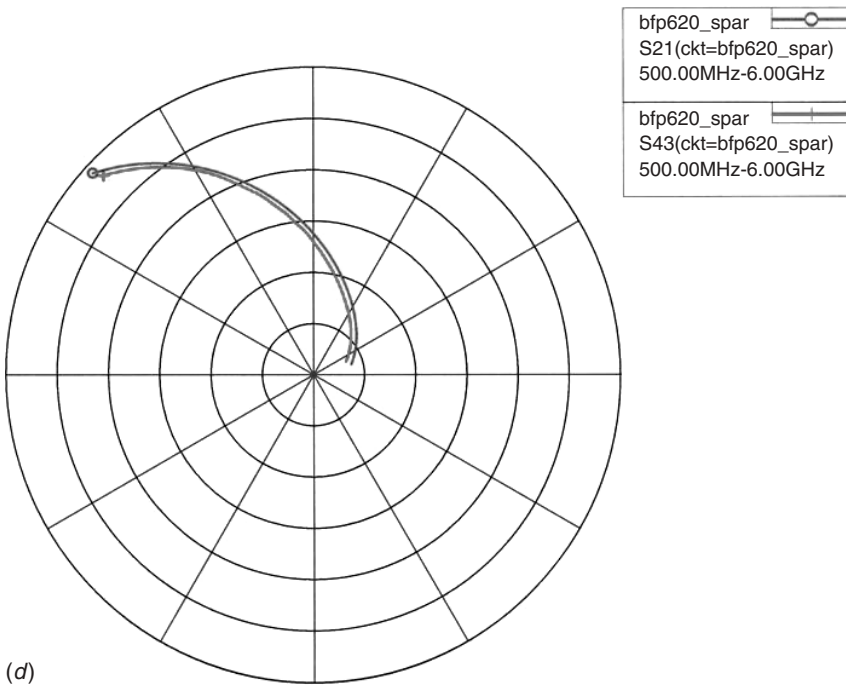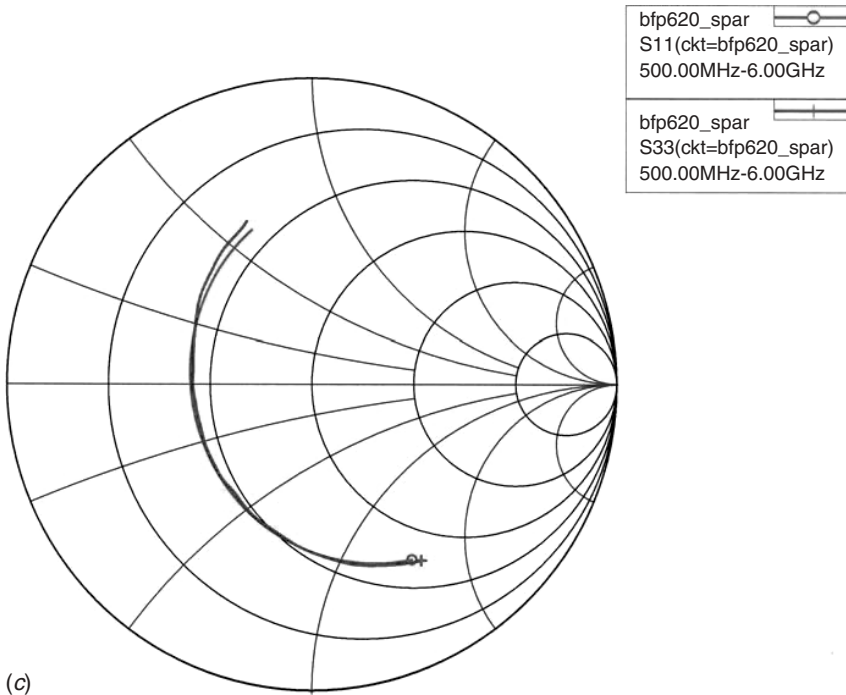
(c)

(d)

FIGURE 3.57   (*continued*)
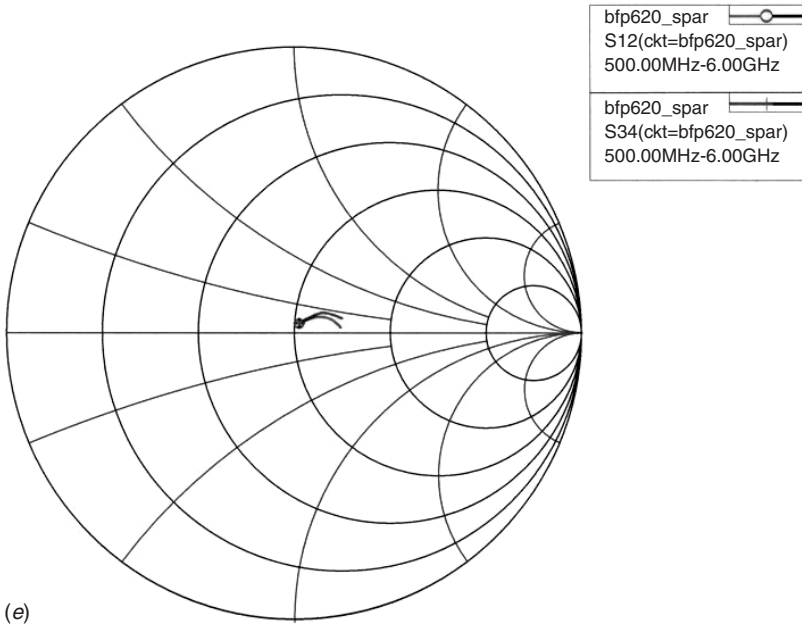
(e)

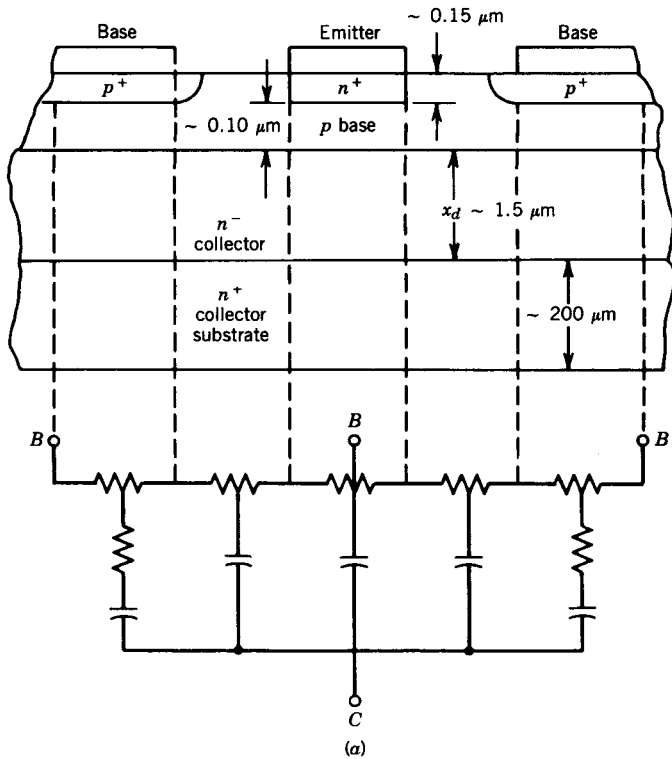**FIGURE 3.57**   (*continued*)

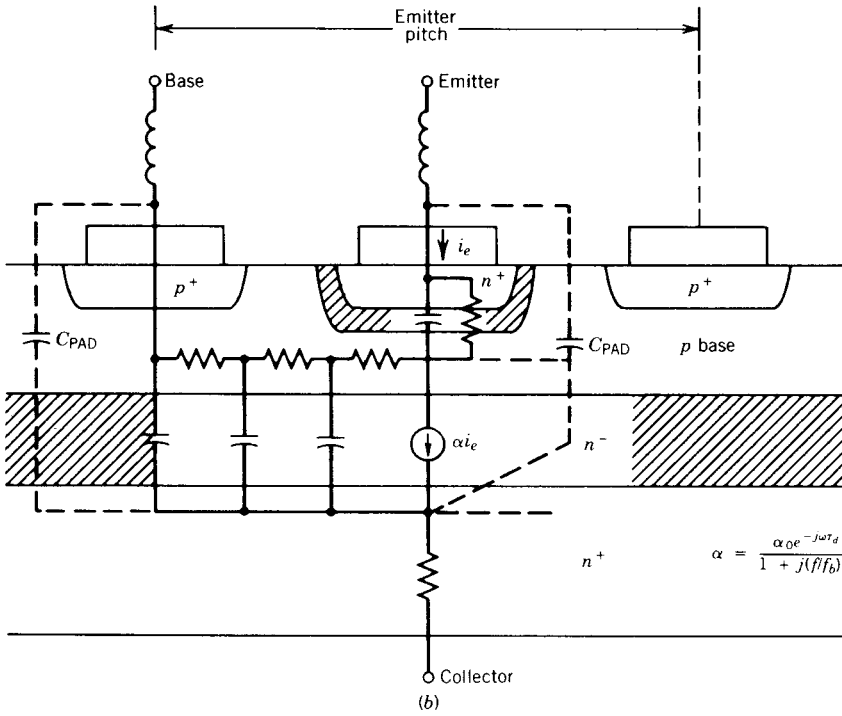**FIGURE 3.58**   (*a*) Bipolar transistor cross section (*npin*). (*b*) Bipolar T-equivalent circuit.
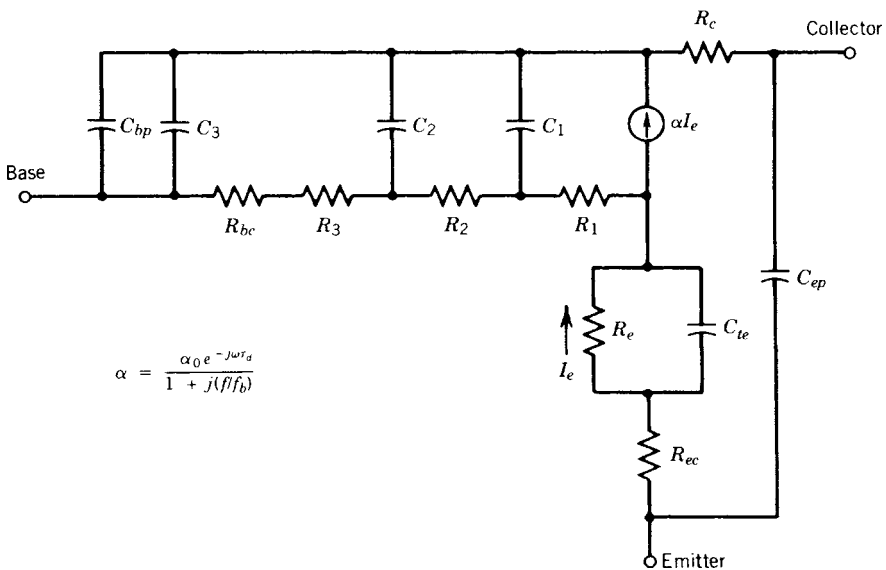
FIGURE 3.58   (*continued*)

FIGURE 3.59   Small-signal equivalent circuit of microwave bipolar transistor chip excluding bondwire inductances and package parasitics.

TABLE 3.15   Small-Signal Equivalent-Circuit Elements for Microwave Bipolar Transistors

	Silicon Bipolar Transistors from Avantek				
	AT-60500		AT-41400		AT-22000
Parameter	$V_{CE} = 8$ V, $I_C = 2$ mA	$V_{CE} = 8$ V, $I_C = 10$ mA	$V_{CE} = 8$ V, $I_C = 10$ mA	$V_{CE} = 8$ V, $I_C = 25$ mA	$V_{CE} = 8$ V, $I_C = 18$ mA
C_{ep}	0.026 pF	0.026 pF	0.032 pF	0.032 pF	0.020 pF
$C_{bp} + C_3$	0.055 pF	0.055 pF	0.091 pF	0.091 pF	0.040 pF
R_{ec}	0.66 Ω	0.66 Ω	0.24 Ω	0.24 Ω	0.2 Ω
$R_{bc} + R_3$	4.2 Ω	4.2 Ω	1.0 Ω	1.0 Ω	0.4 Ω
R_c	5.0 Ω	5.0 Ω	5.0 Ω	5.0 Ω	5.0 Ω
R_1	7.5 Ω	7.5 Ω	2.7 Ω	2.7 Ω	1.8 Ω
R_2	10.3 Ω	10.3 Ω	3.1 Ω	3.1 Ω	2.0 Ω
C_1	0.010 pF	0.010 pF	0.023 pF	0.023 pF	0.020 pF
C_2	0.039 pF	0.039 pF	0.048 pF	0.048 pF	0.015 pF
R_e	12.9 Ω	2.6 Ω	2.6 Ω	1.1 Ω	1.6 Ω
C_{te}	0.75 pF	0.75 pF	2.1 pF	2.1 pF	1.5 pF
α_0	0.99	0.99	0.99	0.99	0.99
τ_d	6.9 ps	7.3 ps	6.9 ps	7.3 ps	8 ps
f_b	22.7 GHz	22.7 GHz	22.7 GHz	22.7 GHz	25 GHz
Emitter pitch	6 μm		4 μm		2 μm
Emitter length (Z)	125 μm		350 μm		300 μm
Die size	0.3 mm × 0.3 mm × 0.1 mm		0.3 mm × 0.3 mm × 0.1 mm		0.3 mm × 0.3 mm × 0.1 mm

Symbol	Definition	Symbol	Definition
C_{ep}	Emitter bond pad capacitance	C_{te}	Emitter–base junction capacitance
C_{bp}	Base bond pad capacitance	α	Common-base current gain: $\alpha = \dfrac{\alpha_0 e^{-j\omega\tau d}}{1 + jf/f_b}$
R_{ec}	Emitter contact resistance	α_0	Low-frequency common-base current gain
R_{bc}	Base contact resistance	τ_d	Collector depletion region delay time
R_c	Collector resistance	τ_b	Base region delay time
$\left.\begin{array}{l}R_1\\R_2\\R_3\end{array}\right\}$	Distributed base resistance	f_b	Base cutoff frequency: $f_b = \dfrac{1}{2\pi\tau_b}$
$\left.\begin{array}{l}C_1\\C_2\\C_3\end{array}\right\}$	Distributed collector-base capacitance	r_b'	Base resistance: $r_b' = R_{bc} + R_1 + R_2 + R_3$
R_e	Emitter resistance, $R_e = kT/qI_e = r_e'$	C_c	Collector–base capacitance: $C_c = C_{bp} + C_1 + C_2 + C_3$

at $V_{CE} = 8$ V, $I_{CE} = 25$ mA. The complete Gummel–Poon model for the AT-41400 is found in Table 9.1.

Although the distributed nature of the bipolar transistor requires an effective value of r_b and C_c, the figure of merit for the bipolar is

$$f_{max}^2 = \frac{f_t}{8\pi r_b' C_c} \tag{3.120}$$
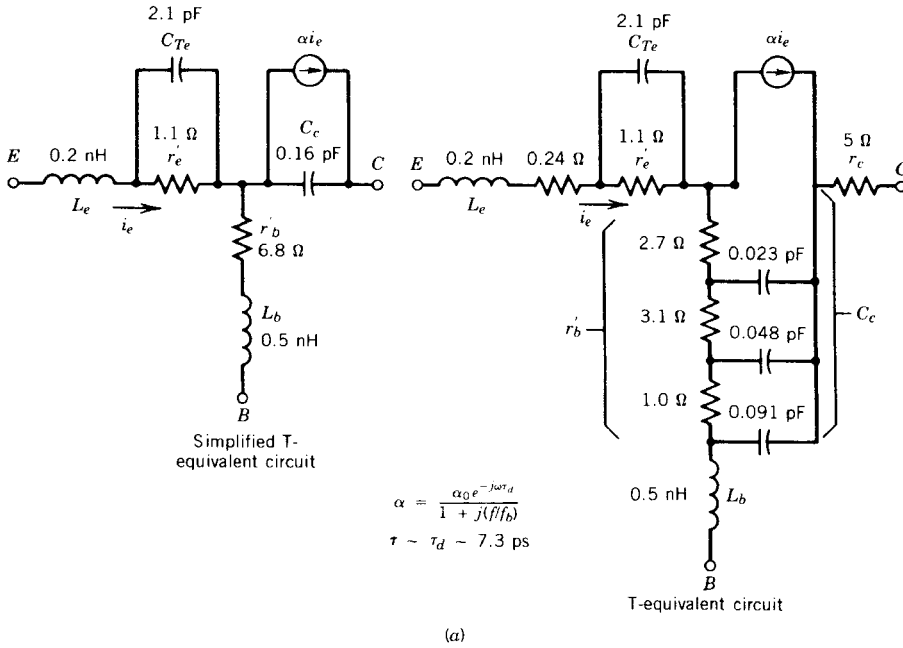
FIGURE 3.60 (*a*) T-equivalent circuit for AT-41400 at $V_{CE} = 8$ V, $I_{CE} = 25$ mA.

where $f_{\max}$ is the frequency at which unilateral gain becomes unity and f_t represents the delay time from emitter to collector (i.e., the transit time). The transit time is given by

$$\tau_{ec} = \tau_e + \tau_{eb} + \tau_{bc} + \tau_b + \tau_d + \tau_c \tag{3.121}$$

where τ_e = emitter delay due to excess holes in emitter

τ_{eb} = emitter–base capacitance charging time through emitter,
$\quad = r_e' C_{Te} = (kT/qI_E)C_{Te}$

τ_{bc} = base–collector capacitance charging time through emitter, $= r_e' C_c$

τ_b = base transit time

τ_d = collector depletion layer delay time, $= X_d/2v_s$

τ_c = base–collector capacitance charging time through collector

The frequency at which the common-emitter current gain ($|h_{21e}|$) reduces to unity is defined by f_t and is determined by the delay time from emitter to collector τ_{ec} according to the equation

$$f_t = \frac{1}{2\pi\,\tau_{ec}} \tag{3.122}$$

The calculation for the transit time of the Agilent/Avantek AT-41400 transistor chip at $V_{CE} = 8$ V, $I_{CE} = 25$ mA follows:

$$\tau_e = \frac{X_{jeb}^2}{2D_{pe}\beta_0} = \frac{(0.15)^2(10^{-8})}{(2)(2)(100)} = 0.56 \text{ ps}$$
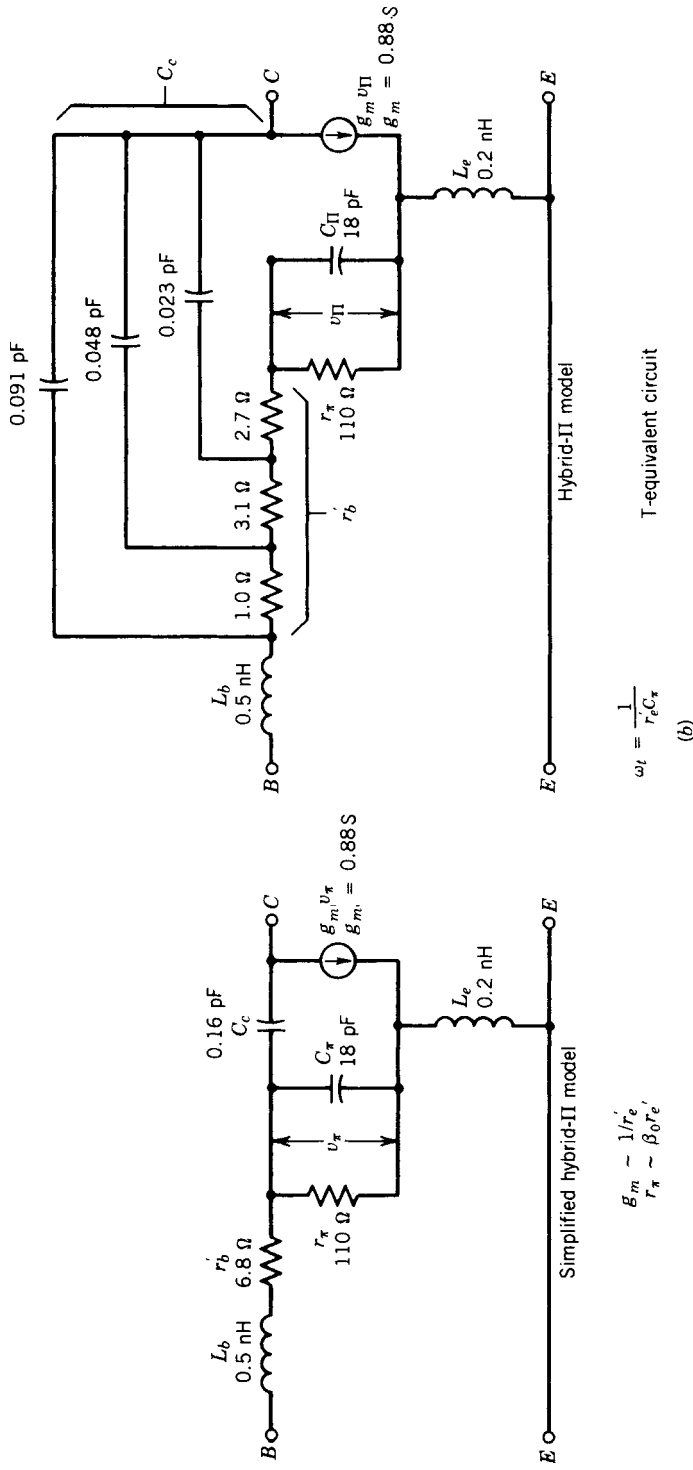
FIGURE 3.60 (b) Hybrid-π equivalent circuit for AT-41400 at $V_{CE} = 8$ V, $I_{CE} = 25$ mA.

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where $\beta_0 = 100 =$ low-frequency or dc value of current gain, h_{FE}

$\quad D_{pe} = 2 \text{ cm}^2/\text{s} =$ hole diffusion coefficient in emitter

$\quad X_{jeb} = 0.15 \ \mu\text{m} =$ depth of emitter–base junction

$$\tau_{eb} = r'_e C_{Te} = (1.1)(2.1) = 2.31 \text{ ps}$$

$$\tau_{bc} = r'_e C_c = (1.1)(0.16) = 0.18 \text{ ps}$$

$$\tau_b = \frac{W^2}{n D_{nb}} = \frac{10^{-5} \times 10^{-5}}{(2.2)(8)} = 5.68 \text{ ps}$$

where $W =$ base length, $= 0.10 \ \mu\text{m}$

$\quad D_{nb} =$ electron diffusion coefficient in base, $= 8 \text{ cm}^2/\text{s}$

$\quad\quad n =$ empirical factor to account for built-in aiding electric field due to base impurity gradient, $= 2.2$

$$\tau_d = \frac{X_d}{2v_s} = \frac{1.1 \times 10^{-4}}{1.6 \times 10^7} = 6.88 \text{ ps}$$

where $X_d =$ depletion width of collector, $= 1.1 \ \mu\text{m}$

$\quad v_s =$ saturated drift velocity for silicon, $= 0.8 \times 10^7 \text{cm/s}$

$$\tau_c = r_c C_c = (5)(0.16) = 0.80 \text{ ps}$$

$$\tau_{ec} = 16.4 \text{ ps}$$

$$f_t = \frac{1}{2\pi(16.4) \times 10^{-12}} = 9.7 \text{ GHz}$$

$$r'_b C_c \simeq \frac{(6.8)(0.16)}{2} = 0.54 \text{ ps}$$

$$f_{\max} = \sqrt{\frac{9.7 \times 10^9}{8\pi(0.54)(10^{-12})}} = 26.7 \text{ GHz}$$

A fair approximation for the bipolar is

$$U \simeq G_{ma} \simeq \left(\frac{f_{\max}}{f}\right)^2 \tag{3.123}$$

which gives an estimate of the transistor gain. The G_{ma} is usually 2 to 5 dB lower than U in practice. The S parameters of the transistor should be used to give a more accurate calculation of G_{ma} using the equations in Chapter 1.

For optimum design of silicon bipolar transistors, the parasitic resistances and capacitances must be minimized. In addition, (3.120) to (3.122) show that the minimum values of r'_b, C_c, and τ_{ec} will give the maximum frequency of operation and therefore the maximum gain.

An important observation for the bipolar transistor is the large transconductance, which can be shown to follow from the forward-biased emitter–base junction. Since the emitter current is given by

$$I_E = I_s \left[\exp\left(\frac{q V_{\text{in}}}{kT} \right) - 1 \right] \tag{3.124}$$

the transconductance is

$$g_m = \frac{\partial I_c}{\partial V_{\text{in}}} = \frac{\alpha_0 I_E q}{kT} = \frac{I_E(\text{mA})}{26} \tag{3.125}$$

Since this will scale with size, the transistor gain parameter at high gain bias is

$$\frac{g_m}{Z} = \frac{I_E(\text{mA})}{26 \ Z} \simeq \frac{1 \ \text{S}}{0.35 \ \text{mm}} \simeq 3 \ \text{S/mm}$$

$$\frac{I_E}{Z} = \frac{25 \ \text{mA}}{0.35 \ \text{mm}} \simeq 70 \ \text{mA/mm}$$

where Z is the emitter length or periphery. These are the values reported in Table 3.15 and achieved from the microwave silicon bipolar structure used at Agilent/Avantek.

The superior microwave performance of the AT-220 bipolar transistor is a result of the reduction of the emitter pitch to 2 μm. The proportional increases in the ratio of the emitter periphery to base area lead to increase in f_{max} and reduction in noise figure. The curves of gain versus frequency for the modeled transistor are given in Figure 3.61. The f_{max} is extrapolated to 50 GHz, and further improvements will be obtained when another reduction in emitter pitch can be achieved [3.43].

Using the familiar T-equivalent circuit for the bipolar transistor, we are now trying to obtain a linear model for the SiGe HBT BFP620 from Infineon. This is done by optimizing the linear equivalent circuit and obtaining S parameters and optimizing them against the same set of measured data. For the package model, the manufacturer's data are being used. Figure 3.62a shows the equivalent circuit used for this and Table 3.16 explains the meaning of different parameters.

Figures 3.62b to 3.62e show the matching between the datasheet published S parameters versus the modeled S parameters.

The amplifier illustrated in Figure 3.63, built around BFP620, is an example of how powerful these silicon germanium transistors are. Based on the large-signal parameters, we used the Ansoft Designer to design a 7-GHz amplifier to build a low-noise, high-gain, stable 7-GHz amplifier. While the topic of matching has not been introduced (see Chapter 5), this circuit shows a necessary network at the input and output to provide selectivity, good input and output matching, and a good noise figure at the same time. Figure 3.64 shows the circuit and the simulated response. A noise figure of approximately 1 dB was obtained with 14 dB gain. There will be other silicon transistors on the market, but it appears that Infineon has one of the best selections at the moment of such discrete transistors.

Figures 3.65 to 3.70, pictures from an Infineon presentation, show some exciting applications based around silicon germanium HBTs.
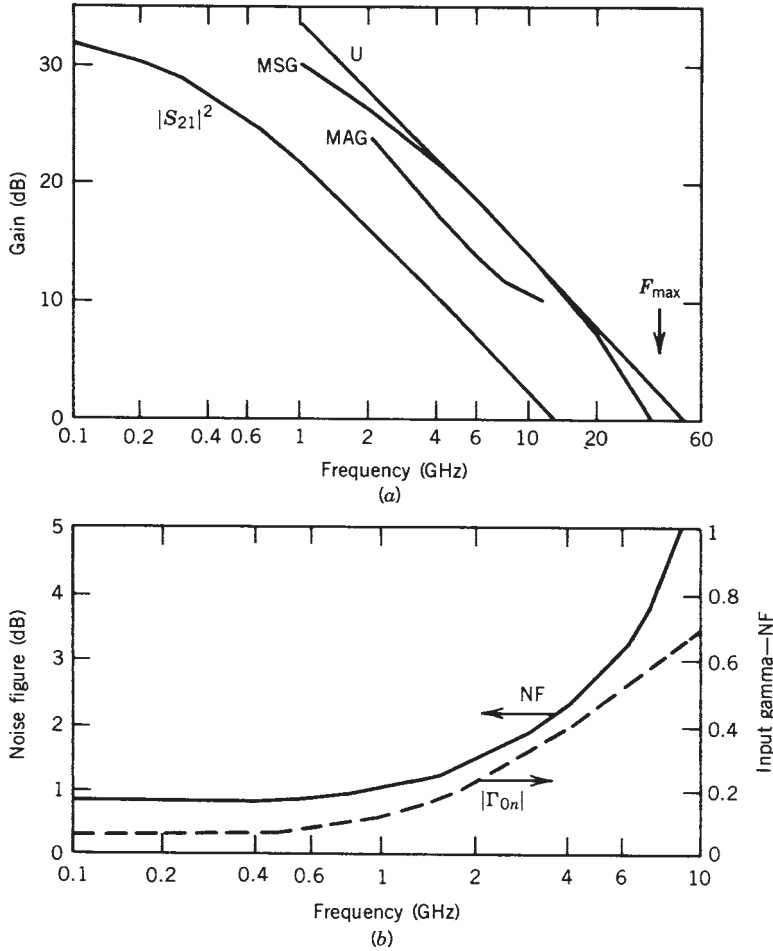
FIGURE 3.61 Common-emitter performance of 2-μm-pitch silicon bipolar transistor chip (AT-22000): (a) S_{21} gain, maximum available gain G_{ma}, maximum stable gain G_{ms}, and unilateral gain U versus frequency; (b) minimum noise figure and associated input reflection coefficient versus frequency [3.43].

Silicon Bipolar Noise Model T Configuration The noise of a silicon bipolar transistor can be modeled by the three noise sources

$$\overline{e_g e_g^*} = \overline{e_g^2} = 4KTR_g \ \Delta f \tag{3.126}$$

$$\overline{e_b e_b^*} = \overline{e_b^2} = 4KTr_b \ \Delta f \tag{3.127}$$

$$\overline{e_e e_e^*} = \overline{e_e^2} = 2KTr_e \ \Delta f \tag{3.128}$$

$$\overline{i_{cp} i_{cp}^*} = \overline{i_{cp}^2} = \frac{2KT(\alpha_0 - |\alpha|^2)}{r_e} \Delta f = 2KTg_e(\alpha_0 - |\alpha|^2) \ \Delta f \tag{3.129}$$

$$\overline{i_{cp} e_e^*} = 0 \tag{3.130}$$
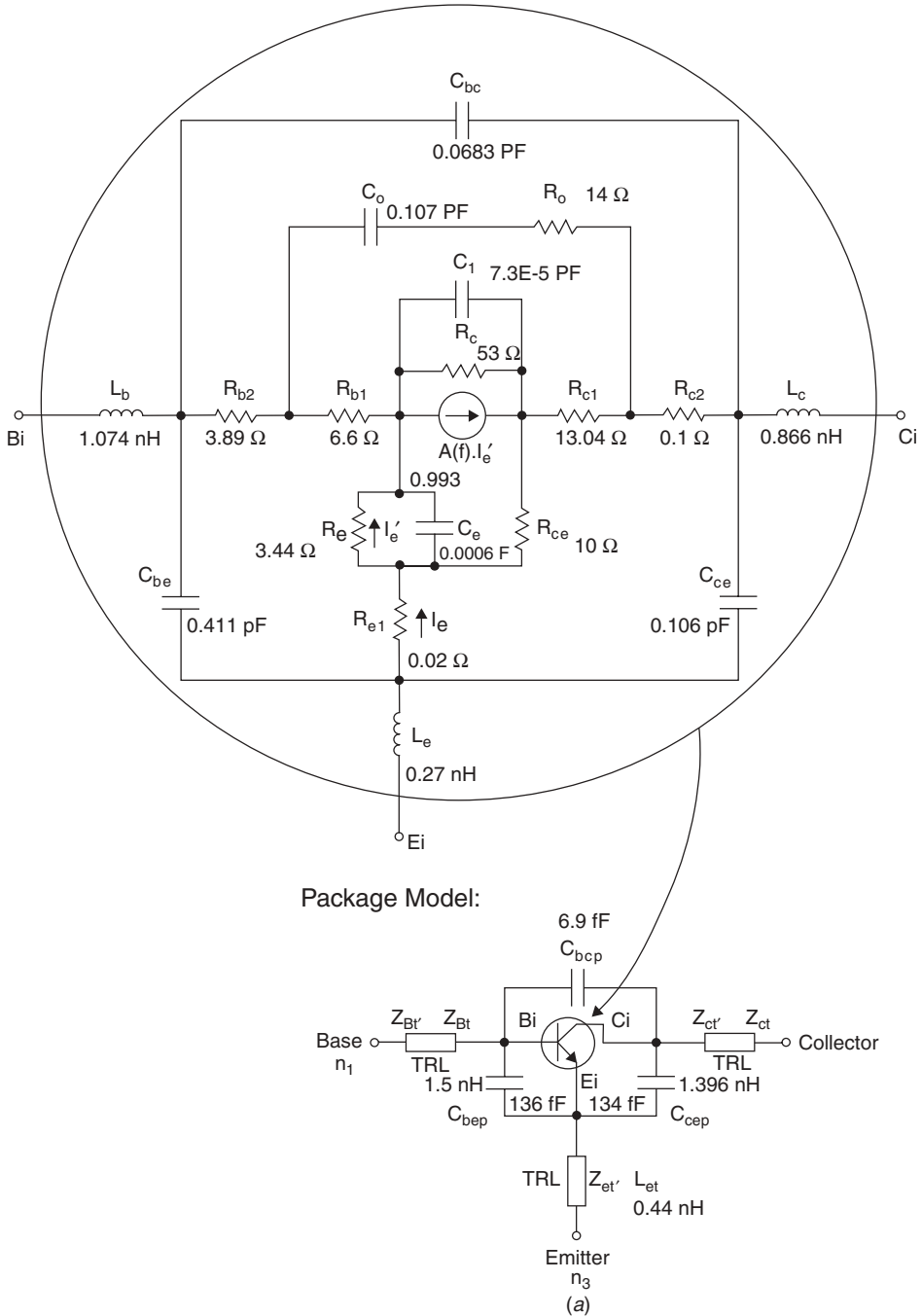
FIGURE 3.62 (*a*) BFP620 Chip Model. (*b*) S_{22} fit. (*c*) S_{21} fit. (*d*) S_{11} fit. (*e*) S_{12} fit.

(b)

(c)

FIGURE 3.62 (*continued*)

(d)

(e)
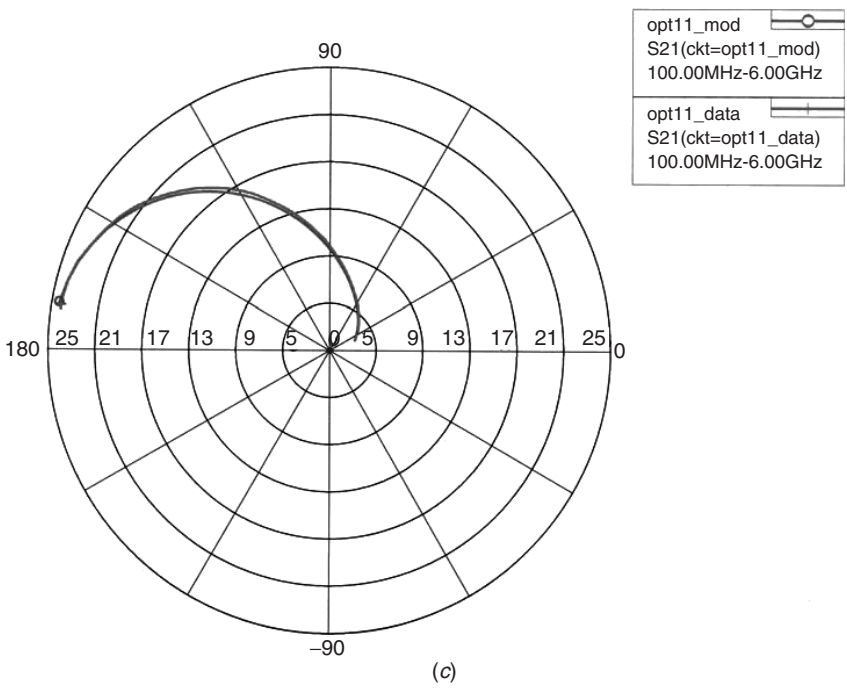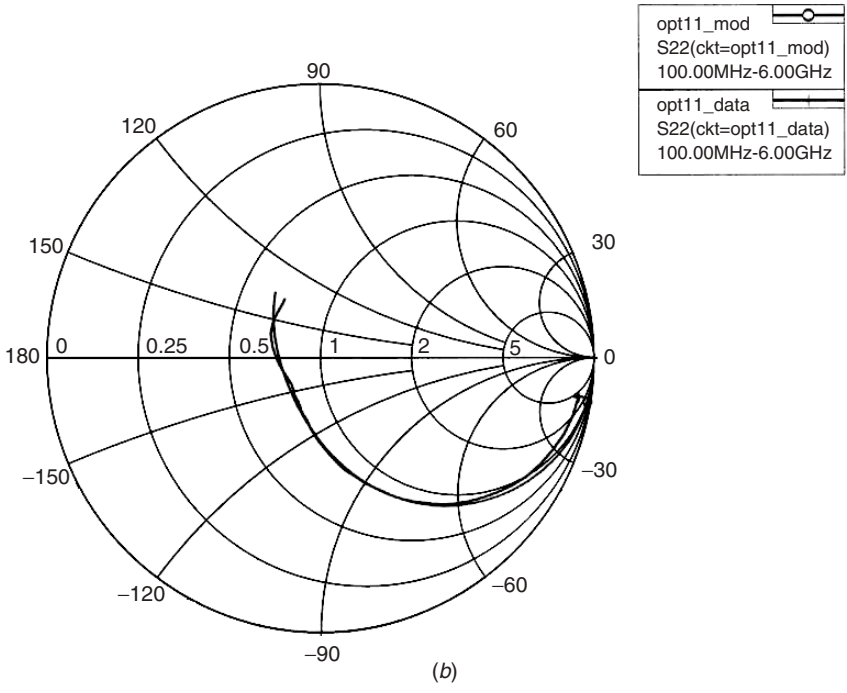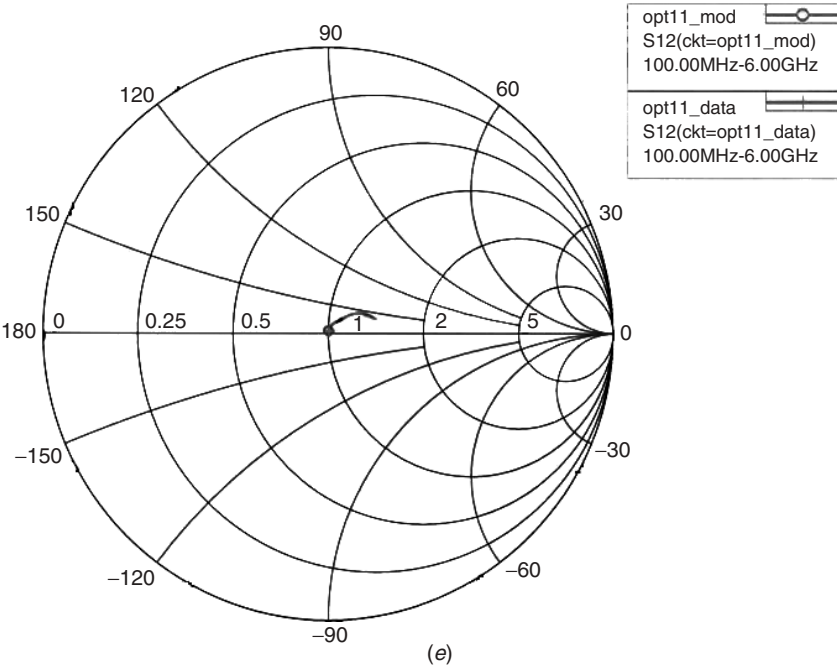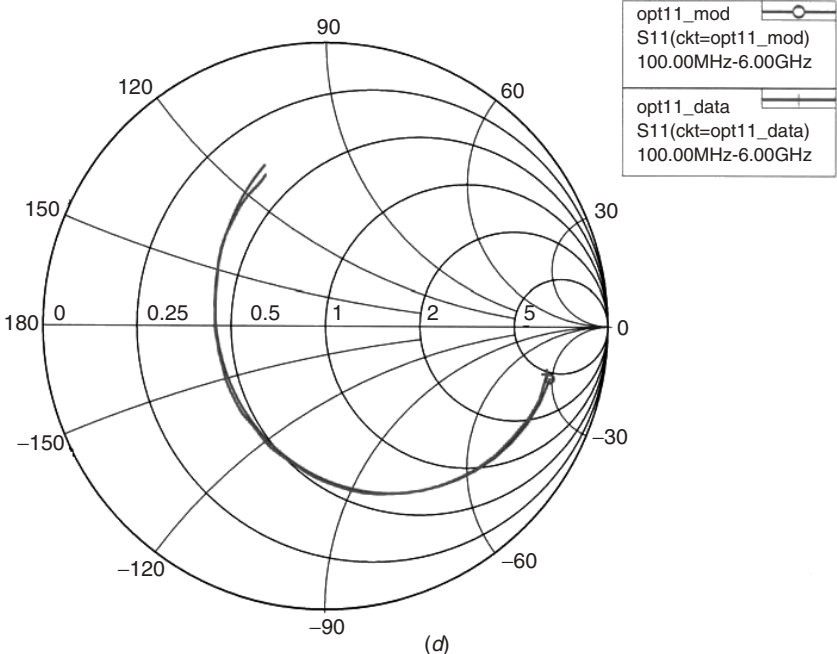
FIGURE 3.62   (*continued*)

TABLE 3.16 BFP620 SiGe HBT

Keyword	Description	Unit	Parameter Value
	Intrinsic Model		
A	Ratio of I_C to I_E at dc		0.993
RE	Emitter resistance	Ω	3.44
F	Current generator roll-off frequency	Hz	7.7×10^{12}
T	Time delay	s	0
CE	Emitter capacitance	F	0.6×10^{-15}
CI	Collector capacitance	F	7.3×10^{-17}
RCE	Collector emitter resistance	Ω	10×10^3
RC	Collector resistance	Ω	53×10^3
RO	Extrinsic base collector resistance	Ω	14
CO	Extrinsic base collector capacitance	F	0.107×10^{-12}
RB1	Intrinsic base resistance (R_{bb})	Ω	6.6
RC1	Parasitic collector resistance	Ω	13.09
RE1	Parasitic emitter resistance	Ω	0.02
RB2	Parasitic base resistance	Ω	3.89
RC2	Parasitic collector resistance	Ω	0.10
CBE	Base-to-emitter package capacitance	F	136×10^{-15}
CBC	Base-to-collector package capacitance	F	6.9×10^{-15}
CCE	Collector-to-emitter package capacitance	F	134×10^{-15}
LB	Base lead inductance	H	1.047×10^{-9}
LC	Collector lead inductance	H	0.866×10^{-9}
LE	Emitter lead inductance	H	0.27×10^{-9}
TJ	Chip temperature	K	298
NFAC	Noise factor proportional to drive		1.0
FC	Flicker noise (1/f noise) corner frequency	Hz	20e3
	Package Model		
CBCP	Base-to-collector package capacitance	F	6.9×10^{-15}
CBEP	Base-to-emitter package capacitance	F	136×10^{-15}
CCEP	Collector-to-emitter package capacitance	F	134×10^{-15}
ZBT	Base transmission line impedance	Ω	50
ZCT	Collector transmission line impedance	Ω	50
ZET	Emitter transmission line impedance	Ω	50
LBT	Base transmission line length $@\varepsilon_r = 1$	m	1.5×10^{-9}
LCT	Collector transmission line length $@\varepsilon_r = 1$	m	1.396×10^{-15}
LET	Emitter transmission line length $@\varepsilon_r = 1$	m	0.44e-9

Note:

1. $A \equiv \alpha = I_c/I_e$; $\beta = $ dc current gain $= \alpha(1 - \alpha)$.
2. The bipolar current gain in this model is described by

$$A = A(0) = \frac{e^{-j\omega T}}{1 + jf/F}$$

where $\omega = 2\pi f$ and $f = $ frequency.

3. The current source is controlled by the current through R_e. The current generator has a cutoff frequency with respect to the total emitter current I_E:

$$F = \frac{g_m}{2\pi C_e}$$

where $g_m = 1/R_e$. This frequency becomes infinity for the default value for C_e (0.0). The parameter F specifies the frequency roll-off for the current generator with respect to the current through R_e. Effectively, this frequency parameter may be used to model additional delays in the device.
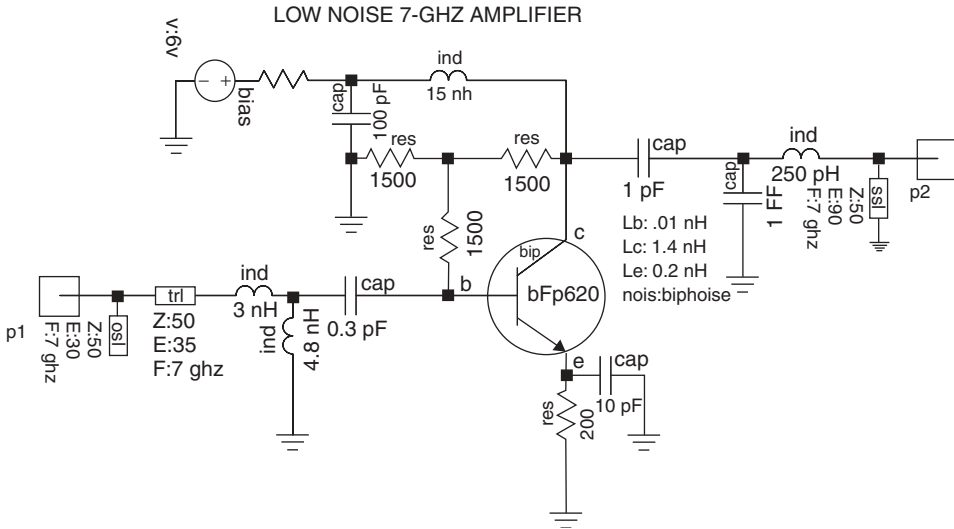
FIGURE 3.63   Low noise amplifier (LNA) at 7 GHz using BFP620.
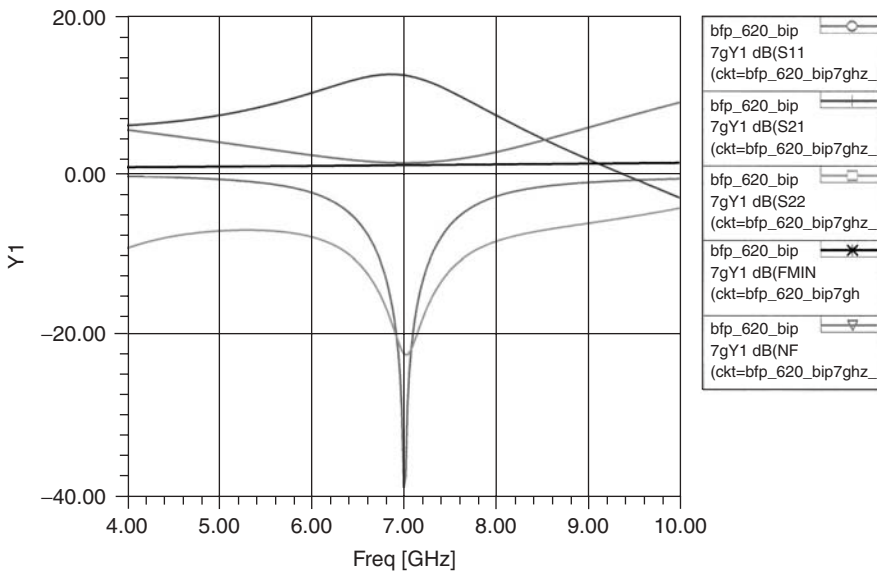
FIGURE 3.64   LNA performance.

$$\alpha = \frac{\alpha_0}{1 + j\dfrac{f}{f_b}} \qquad \beta = \frac{\alpha}{1 - \alpha} \qquad r_e = \frac{KT}{qI_e} \qquad g_e = \frac{1}{r_e} \qquad (3.131)$$

which are shown in Figures 3.71 and 3.72. The base thermal noise e_b due to r_b, the shot noise of the forward-biased emitter–base junction e_e, and the collector partition noise i_{cp}, which is strongly correlated to the emitter–base shot noise, are the noise sources.
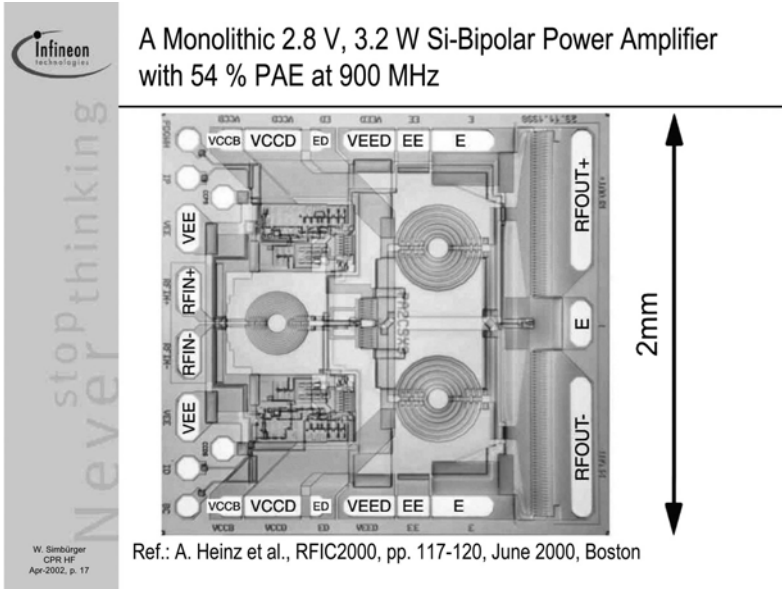
FIGURE 3.65   High-efficiency 900-MHz amplifier.
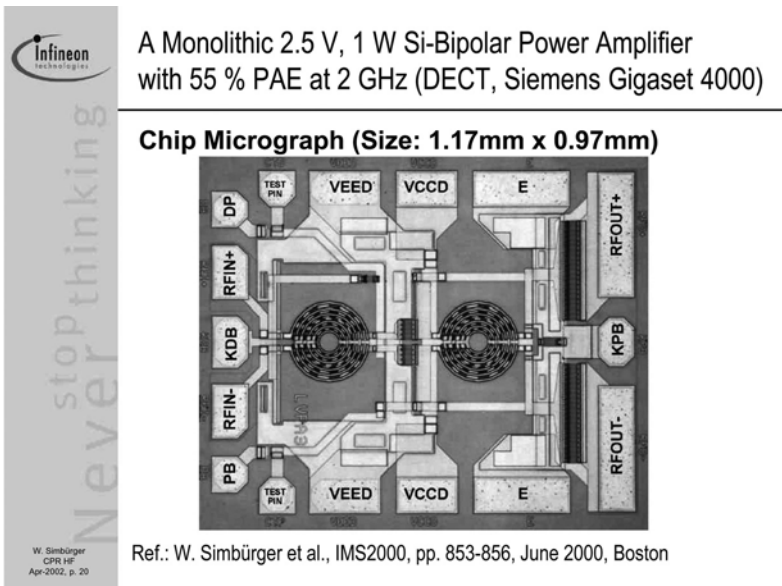
FIGURE 3.66   High-efficiency 2-GHz amplifier.

Figure 3.71 shows the T-equivalent circuit of bipolar transistor in which C_{Te} is emitter junction capacitance and Z_g is complex source impedance. For calculation of minimum noise figure, the T configuration is simpler than the hybrid-Π, whereas for formation of the noise correlation matrix with base–collector capacitance C_{bc}, the hybrid-Π topology is the better approach for analysis [3.44].
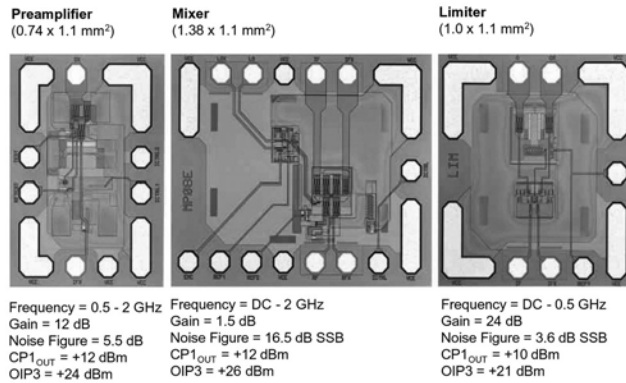
FIGURE 3.67   High IP3 receiver for 0.5 to 2 GHz.

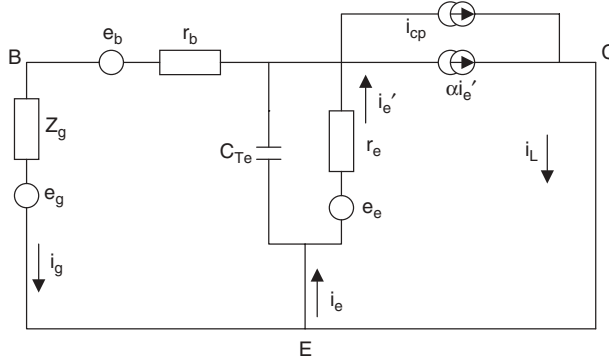**FIGURE 3.68**   A 7.35-GHz frequency synthesizer.
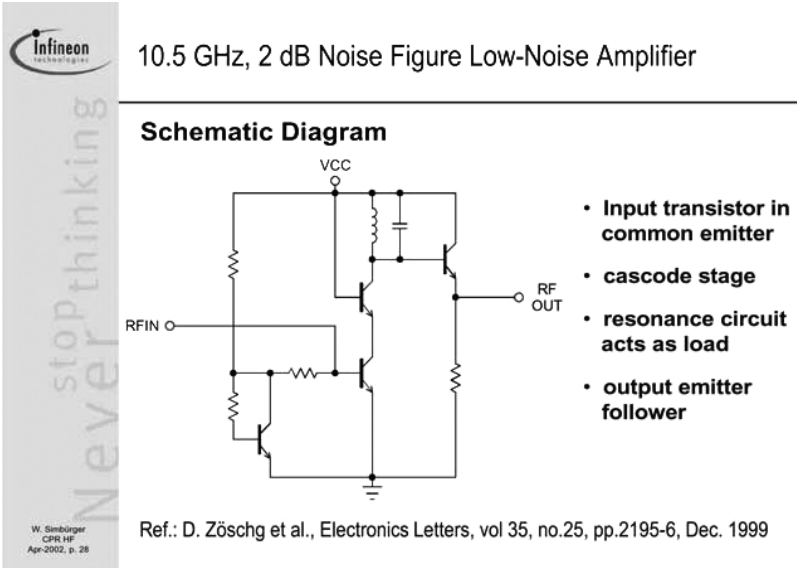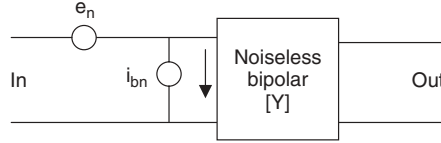
FIGURE 3.69 A 10.5-GHz LNA.
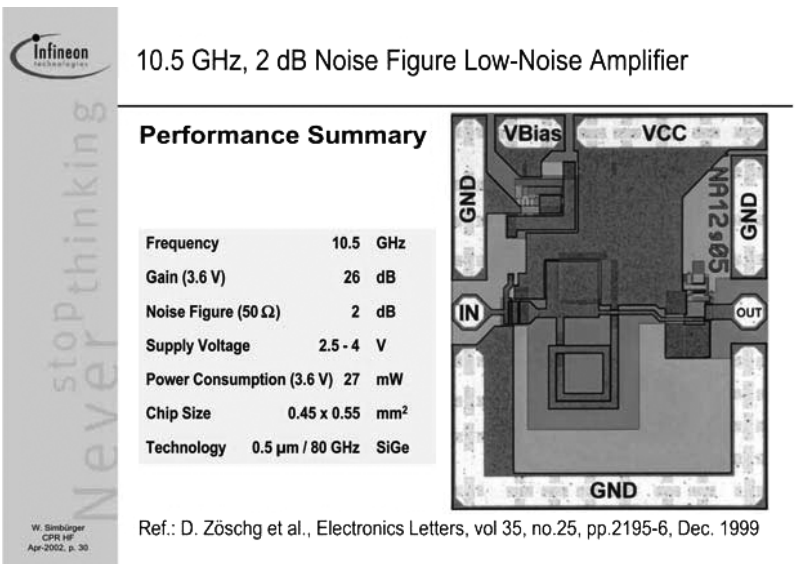
FIGURE 3.70 Performance of 10.5-GHz LNA.

The definition we use as the noise figure is defined as the ratio of the output noise power to that from a noiseless but otherwise identical device: Noise figure F is given by

$$F = \frac{\overline{i_L^2}}{\overline{i_{L0}^2}} \tag{3.132}$$

FIGURE 3.71   T-equivalent circuit of bipolar transistor.

FIGURE 3.72   Noise sources transformed to input.

Where i_{L0} is the value of i_L due to the source generator e_g alone. From Kirchhoff's voltage law (KVL), for the loop containing Z_g, r_b, and r_e the loop equation can be written as

$$i_g(Z_g + r_b) + i'_e r_e = e_g + e_b + e_e \tag{3.133}$$

$$i_L = \alpha i'_e + i_{cp} \tag{3.134}$$

$$i'_e = \frac{i_L - i_{cp}}{\alpha} \tag{3.135}$$

$$i_e = i'_e(1 + jwC_{Te}) - jwC_{Te}e_e \tag{3.136}$$

$$i_g = i_e - i_L \tag{3.137}$$

$$= i'_e(1 + jwC_{Te}r_e) - jwC_{Te}e_e - i_L \tag{3.138}$$

$$= \frac{i_L - i_{cp}}{\alpha}(1 + jwC_{Te}r_e) - jwC_{Te}e_e - i_L \tag{3.139}$$

$$i_g(Z_g + r_b) + i'_e r_e = e_g + e_b + e_e \tag{3.140}$$

$$\left[\left(\frac{i_L - i_{cp}}{\alpha}(1 + jwC_{Te}r_e) - jwC_{Te}e_e - i_L\right)(Z_g + r_b)\right] + \left(\frac{i_L - i_{cp}}{\alpha}\right)r_e$$

$$= e_g + e_b + e_e \tag{3.141}$$

$$\frac{i_L}{\alpha}[(1 - \alpha + jwC_{Te}r_e)(Z_g + r_b) + r_e]$$

$$= e_g + e_b + e_e[1 + jwC_{Te}(Z_g + r_b)]$$

$$+ \frac{i_{cp}}{\alpha}[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e] \tag{3.142}$$

$$i_L = \alpha \left[\frac{\begin{array}{c} e_g + e_b + e_e[1 + jwC_{Te}(Z_g + r_b)] \\ + (i_{cp}/\alpha)[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e] \end{array}}{(1 - \alpha + jwC_{Te}r_e)(Z_g + r_b) + r_e} \right] \quad (3.143)$$

where i_L is the total load current or collector current (ac short-circuited current) due to all the generators such as e_e, e_b, e_g, and i_{cp}. Assume i_{L0} is the value of i_L due to source generator e_g alone and other noise generators (e_e, e_b, e_g, and i_{cp}) are zero:

$$i_{L0} = \alpha \left[\frac{e_g}{(1 - \alpha + jwC_{Te}r_e)(Z_g + r_b) + r_e} \right] \quad (3.144)$$

$$F = \frac{\overline{i_L^2}}{\overline{i_{L0}^2}} = \frac{\overline{\{e_g + e_b + e_e[1 + jwC_{Te}(Z_g + r_b)]} \; \overline{+ (i_{cp}/\alpha)[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e]\}^2}}{\overline{e_g^2}} \quad (3.145)$$

$$= \frac{\begin{array}{c} \overline{e_g^2} + \overline{e_b^2} + \overline{e_e^2[1 + jwC_{Te}(Z_g + r_b)]^2} \\ + (i_{cp}^2/|\alpha|^2)[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e]^2 \end{array}}{\overline{e_g^2}} \quad (3.146)$$

$$= \frac{\begin{array}{c} 4KTR_g + 4KTr_b + 2KTr_e\overline{[1 + jwC_{Te}(Z_g + r_b)]^2} \\ + [2KT(\alpha_0 - |\alpha|^2)/|\alpha|^2r_e]\overline{[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e]^2} \end{array}}{4KTR_g} \quad (3.147)$$

$$= 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}\overline{[1 + jwC_{Te}(Z_g + r_b)]^2}$$
$$+ \frac{(\alpha_0 - |\alpha|^2)}{2R_g|\alpha|^2r_e}\overline{[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e]^2} \quad (3.148)$$

$$= 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}|1 + jwC_{Te}(R_g + r_b + jX_g)|^2$$
$$+ \left(\frac{\alpha_0}{|\alpha|^2} - 1 \right) \frac{|(1 + jwC_{Te}r_e)(R_g + r_b + jX_g) + r_e|^2}{2R_gr_e} \quad (3.149)$$

$$= 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}|1 + jwC_{Te}(R_g + r_b) - wC_{Te}X_g|^2 + \left(\frac{\alpha_0}{|\alpha|^2} - 1 \right)$$
$$\times \frac{|R_g + r_b + r_e - wC_{Te}X_gr_e + jwC_{Te}r_e(R_g + r_b + X_g)|^2}{2R_gr_e} \quad (3.150)$$

$$= 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}\{(1 - wC_{Te}X_g)^2$$
$$\times + w^2C_{Te}^2(R_g + r_b)^2\} + \left(\frac{\alpha_0}{|\alpha|^2} - 1 \right)$$
$$\times \frac{[R_g + r_b + r_e(1 - wC_{Te}X_g)]^2 + [X_g + wC_{Te}e_e(R_g + r_b)]^2}{2R_gr_e} \quad (3.151)$$

$$= 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g} + \left(\frac{\alpha_0}{|\alpha|^2} - 1 \right) \frac{(R_g + r_b + r_e)^2 + X_g{}^2}{2R_g r_e}$$

$$+ \left(\frac{\alpha_0}{|\alpha|^2} \right) \left(\frac{r_e}{2R_g} \right) [w^2 C_{Te}^2 X_g{}^2 - 2w C_{Te} X_g + w^2 C_{Te}^2 (R_g + r_b)^2] \quad (3.152)$$

where noise terms and the generator thermal noise are given as ($\Delta f = 1$ Hz).

$$\overline{e_g^2} = 4KTR_g \tag{3.153}$$

$$= 4KTR_b \tag{3.154}$$

$$= 2KTr_e \tag{3.155}$$

$$\overline{i_{cp}^2} = \frac{2KT(\alpha_0 - |\alpha|^2)}{r_e} \tag{3.156}$$

Real Source Impedance   In the case of a real source impedance, for example, $R_g = 50\ \Omega$, $X_g = 0$, the above equation of noise figure becomes

$$F = 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g} + \left(\frac{\alpha_0}{|\alpha|^2} - 1 \right) \frac{(R_g + r_b + r_e)^2}{2R_g r_e} + \frac{\alpha_0}{|\alpha|^2} w^2 C_{Te}^2 r_e{}^2 \frac{(R_g + r_b)^2}{2R_g r_e} \tag{3.157}$$

Substituting the value of α where f_b is the cutoff frequency of the base alone and introducing an emitter cutoff frequency $f_e = 1/2\pi C_{Te} r_e$,

$$F = 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g} + \left(1 - \alpha_0 + \frac{f^2}{f_b^2} \right) \frac{(R_g + r_b + r_e)^2}{2R_g r_e \alpha_0} + \left(1 + \frac{f^2}{f_b^2} \right) \frac{f^2}{f_e^2} \frac{(R_g + r_b)^2}{2R_g r_e \alpha_0} \tag{3.158}$$

Simplifying the preceding equation by f_e',

$$f_e' = f_e \frac{R_g + r_b + r_e}{R_g + r_b} = \frac{R_g + r_b + r_e}{2\pi C_{Te} r_e (R_g + r_b)} \tag{3.159}$$

The simplified equation of the noise figure for a real source impedance is given by

$$F = 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g} + \left[\left(1 + \frac{f^2}{f_b^2} \right) \left(1 + \frac{f^2}{f_e'^2} \right) - \alpha_0 \right] \frac{(R_g + r_b + r_e)^2}{2R_g r_e \alpha_0} \tag{3.160}$$

Minimum Noise Figure   The minimum noise figure $F_{\min}$ and the corresponding optimum source impedance $Z_{\mathrm{opt}} = R_{\mathrm{opt}} + j X_{\mathrm{opt}}$ are found by differentiating the general equation of the noise figure with respect to X_g and then R_g.

The noise figure can be represented as

$$F = A + B X_g + C X_g^2 \tag{3.161}$$

where, by introducing the form factor,

$$a = \left(1 - \frac{|\alpha|^2}{\alpha_0} + w^2 C_{Te}^2 r_e^2 \right) \frac{\alpha_0}{|\alpha|^2} \tag{3.162}$$

The coefficients A, B, and C can be written as

$$A = a\frac{(R_g + r_b)^2}{2R_g r_e} + \frac{\alpha_0}{|\alpha|^2}\left(1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}\right) \tag{3.163}$$

$$B = -\frac{\alpha_0}{|\alpha|^2}\frac{wC_{Te}r_e}{R_g} \tag{3.164}$$

$$C = \frac{a}{2r_e R_g} \tag{3.165}$$

Differentiating with respect to X_g and setting dF/dX_g to zero for the optimum source reactance,

$$\left.\frac{dF}{dX_g}\right|_{X_{opt}} = 0 = B + 2CX_{opt} \tag{3.166}$$

$$X_{opt} = \frac{-B}{2C} = \frac{\alpha_0}{|\alpha|^2}\frac{wC_{Te}r_e}{a} \tag{3.167}$$

The corresponding noise figure is

$$F_{X_{opt}} = A - CX_{opt}^2 \tag{3.168}$$

$$= a\frac{(R_g + r_b)^2}{2R_g r_e} + \frac{\alpha_0}{|\alpha|^2}\left(1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}\right) - \frac{aX_{opt}^2}{2r_e R_g} \tag{3.169}$$

This must be further optimized with respect to the source resistance to give F_{min} by differentiating $F_{X_{opt}}$ with respect to the source resistance:

$$F_{X_{opt}} = a\frac{(R_g + r_b)^2}{2R_g r_e} + \frac{\alpha_0}{|\alpha|^2}\left(1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}\right) - \frac{aX_{opt}^2}{2r_e R_g} \tag{3.170}$$

$$= A_1 + \frac{B_1}{R_g} + C_1 R_g \tag{3.171}$$

$$A_1 = a\frac{r_b}{r_e} + \frac{\alpha_0}{|\alpha|^2} \tag{3.172}$$

$$B_1 = a\frac{r_b^2 - X_{opt}^2}{2r_e} + \frac{\alpha_0}{|\alpha|^2}\left(r_b + \frac{r_e}{2}\right) \tag{3.173}$$

$$C_1 = \frac{a}{2r_e} \tag{3.174}$$

Differentiating the noise figure with respect to R_g to get the minimum noise figure,

$$\left.\frac{dF}{dR_g}\right|_{R_{opt}} = 0 = \frac{-B_1}{R_{opt}^2} + C_1 \tag{3.175}$$

$$R_{opt}^2 = \frac{B_1}{C_1} = r_b^2 - X_{opt}^2\frac{\alpha_0}{|\alpha|^2}\frac{r_e(2r_b + r_e)}{a} \tag{3.176}$$

$$F_{min} = A_1 + 2C_1 R_{opt} = a\frac{r_b + R_{opt}}{r_e} + \frac{\alpha_0}{|\alpha|^2} \tag{3.177}$$

The factor a can be simplified in terms of a simple symmetrical function of f_e and f_b:

$$a = \left(1 - \frac{|\alpha|^2}{\alpha_0} + w^2 C_{Te}^2 r_e^2\right) \frac{\alpha_0}{|\alpha|^2} \tag{3.178}$$

$$= \left[1 + \frac{f^2}{f_b^2} - \alpha_0 + \left(1 + \frac{f^2}{f_b^2}\right) \frac{f^2}{f_e^2}\right] \frac{1}{\alpha_0} \tag{3.179}$$

$$= \left[\left(1 + \frac{f^2}{f_b^2}\right)\left(1 + \frac{f^2}{f_b^2}\right) - \alpha_0\right] \frac{1}{\alpha_0} \tag{3.180}$$

Special case: When C_{Te} and X_{opt} are zero and factor a can be expressed as follows:

$$a = \left(1 + \frac{f^2}{f_b^2} - \alpha_0\right) \frac{1}{\alpha_0} \tag{3.181}$$

$$R_{\mathrm{opt}}^2 = \frac{B_1}{C_1} = r_b^2 + \frac{1 + f^2/f_b^2}{1 + f^2/f_b^2 - \alpha_0} \frac{r_e(2r_b + r_e)}{a} \tag{3.182}$$

$$F_{\min} = A_1 + 2C_1 R_{\mathrm{opt}} = a \frac{r_b + R_{\mathrm{opt}}}{r_e} + \frac{\alpha_0}{|\alpha|^2} \tag{3.183}$$

$$= \left(1 + \frac{f^2}{f_b^2} - \alpha_0\right) \frac{r_b + R_{\mathrm{opt}}}{\alpha_0 r_e} + \left(1 + \frac{f^2}{f_b^2}\right) \frac{1}{\alpha_0} \tag{3.184}$$

$$Z_{\mathrm{opt}} = R_{\mathrm{opt}} + j X_{\mathrm{opt}} \tag{3.185}$$

$$= r_b^2 + \frac{1 + f^2/f_b^2}{1 + f^2/f_b^2 - \alpha_0} \frac{r_e(2r_b + r_e)}{a} + j \frac{\alpha_0}{|\alpha|^2} \frac{w C_{Te} r_e}{a} \tag{3.186}$$

$$Y_{\mathrm{opt}} = \frac{1}{Z_{\mathrm{opt}}} \tag{3.187}$$

Noise Correlation Matrix   The T-equivalent configuration of the common-emitter transistor can be expressed in terms of a two-port admittance matrix. To apply the noise correlation matrix approach, we transform the above noise model to an equivalent one consisting of two noise sources, a voltage source and a current source proceeding a noiseless version of the bipolar circuit.

The transformed noise model takes the form shown in Figure 3.73 below. Since the system is linear, the two noise sources can be expressed in terms of three original noise sources by a linear transformation:

$$[Y]_{\mathrm{tr}} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \tag{3.188}$$

$$= \begin{bmatrix} [(1 - \alpha)g_e + jwC_e + Y_c] & -Y_c \\ \alpha g_e - Y_c & Y_c \end{bmatrix} \tag{3.189}$$

The matrices are defined, respectively, for the intrinsic device as N and for the transformed noise circuit as C, where
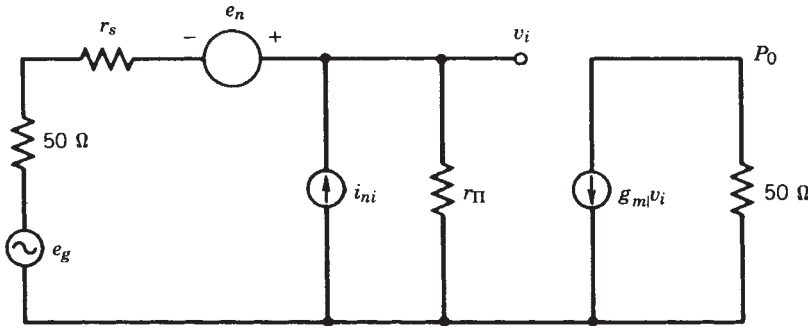
FIGURE 3.73 Low-frequency noise equivalent circuit of bipolar transistor.

$$[N]_{\text{intrinsic}} = \frac{1}{4KT\Delta f}\begin{bmatrix} \overline{e_e e_e^*} & \overline{e_e i_{cp}^*} \\ \overline{i_{cp} e_e^*} & \overline{i_{cp} i_{cp}^*} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{2g_e} & 0 \\ 0 & \dfrac{g_e(\alpha_0 - |\alpha|^2)}{2} \end{bmatrix} \tag{3.190}$$

$$[C]_{\text{transformd}} = \frac{1}{4KT\Delta f}\begin{bmatrix} \overline{e_n e_n^*} & \overline{e_n i_n^*} \\ \overline{i_n e_n^*} & \overline{i_n i_n^*} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \tag{3.191}$$

The noise correlation matrix C can be obtained in terms of N by a straightforward application of the steps outlined as

$$C = AZTN(AZT)^{\oplus} + ARA^{\oplus} \tag{3.192}$$

The sign $\oplus$ denotes the Hermitian conjugate. The matrix Z is just the inverse of the admittance matrix Y for the intrinsic portion of the model and T is a transformation matrix which converts noise sources e_e and i_{cp} to shunt current sources, respectively, across the base–emitter and collector–emitter ports of the transistor:

$$T = \begin{bmatrix} -(1-\alpha)g_e & 1 \\ -\alpha g_e & -1 \end{bmatrix} \tag{3.193}$$

$$A = \begin{bmatrix} 1 & \dfrac{Z_{11} + r_b}{Z_{21}} \\ 0 & -\dfrac{1}{Z_{11}} \end{bmatrix} \tag{3.194}$$

$$R = \frac{1}{4KT\Delta f}\begin{bmatrix} \overline{e_b e_b^*} & 0 \\ 0 & 0 \end{bmatrix} = \begin{bmatrix} r_b & 0 \\ 0 & 0 \end{bmatrix} \tag{3.195}$$

Here Y_c is added as a fictitious admittance across the α-current generator to overcome the singularity of the actual Z matrix. However, in the final evaluation of C, Y_c is set equal to zero. The matrix A is a circuit transformation matrix whereas matrix R is a noise correlation matrix representing the thermal noise of the extrinsic base resistance:

$$C = \begin{bmatrix} C_{uu\bullet} & C_{ui\bullet} \\ C_{u\bullet i} & C_{ii\bullet} \end{bmatrix} = \begin{bmatrix} R_n & \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}}^\bullet \\ \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}} & R_n |Y_{\text{opt}}|^2 \end{bmatrix} \quad (3.196)$$

$$R_n = \frac{C_{uu\bullet}}{2kT} \quad (3.197)$$

$$Y_{\text{opt}} = \sqrt{\frac{C_{ii\bullet}}{C_{uu\bullet}} - \left[\text{Im} \left(\frac{C_{ui\bullet}}{C_{uu\bullet}} \right) \right]^2} + j\text{Im} \left(\frac{C_{ui\bullet}}{C_{uu\bullet}} \right) \quad (3.198)$$

The noise correlation matrix C contains all necessary information about the four extrinsic noise parameters $F_{\min}$, $R_{g_{\text{opt}}}$, and $X_{g_{\text{opt}}}$, and R_n of the bipolar. The expressions for $F_{\min}$, $R_{g_{\text{opt}}}$, and $X_{g_{\text{opt}}}$ are derived above and R_n is expressed as

$$\begin{aligned} R_n &= \frac{C_{uu\bullet}}{2kT} \\ &= r_b \left(\frac{1 + (f/f_b)^2}{\alpha_0^2} - \frac{1}{\beta_0} \right) + \frac{r_e}{2} \left(\frac{1 + (f/f_b)^2}{\alpha_0^2} + (g_e r_b)^2 \right. \\ &\quad \left. \times \left\{ 1 - \alpha_0 + \left(\frac{f}{f_b} \right)^2 + \left(\frac{f}{f_e} \right)^2 + \left[\frac{1}{\beta_0} - \left(\frac{f}{f_b} \right) \left(\frac{f}{f_e} \right) \right]^2 \right\} \right) \end{aligned} \quad (3.199)$$

Low-Frequency Noise in Transistor   The mechanisms causing low-frequency $1/f$ noise have been summarized by vander Ziel in a recent review [3.45]. An equivalent circuit for analyzing low-frequency noise in the bipolar transistor is shown in Figure 3.73, where two noise sources are present in the input. The dominant source of flicker noise is the current generator. This is due primarily to minority-carrier recombination in the emitter region [3.46]. The voltage noise source due to the thermal noise of the resistance is usually a much lower contribution, so the noise power referred to the input is [3.47]

$$\begin{aligned} P_{ni} &= \frac{e_t^2}{200} + \frac{e_n^2}{200} + \frac{i_{ni}^2}{200}(r_s + 50)^2 + 2Ce_n i_{ni}(r_s + 50) \\ &\simeq \frac{i_{ni}^2}{200}(r_s + 50)^2 = \frac{P_0}{G} \end{aligned} \quad (3.200)$$

where e_t = thermal noise voltage of r_s, assume zero, = $4kTr_s \Delta f$
$\quad\quad e_n$ = equivalent input noise voltage, assume zero (determine by letting $r_s = 0$)
$\quad\quad C$ = correlation factor, assume zero
$\quad\quad P_0$ = noise output power to 50-Ω load
$\quad\quad G$ = low-frequency gain

Since the noise is essentially current noise, the data are usually plotted in dBA/$\sqrt{\text{Hz}}$, as given in Figure 3.74. For this measurement, a typical value of r_s is 1 kΩ.

It should be remembered that the finite base resistance, r_b', will allow a certain amount of the base current flicker noise, $i_b r_{bb}'$, to appear in the equivalent voltage source, e_n. Because the thermal noise due to r_{bb}' tends to dominate this flicker noise component, the e_n flicker noise corner frequency is well below that of the base current
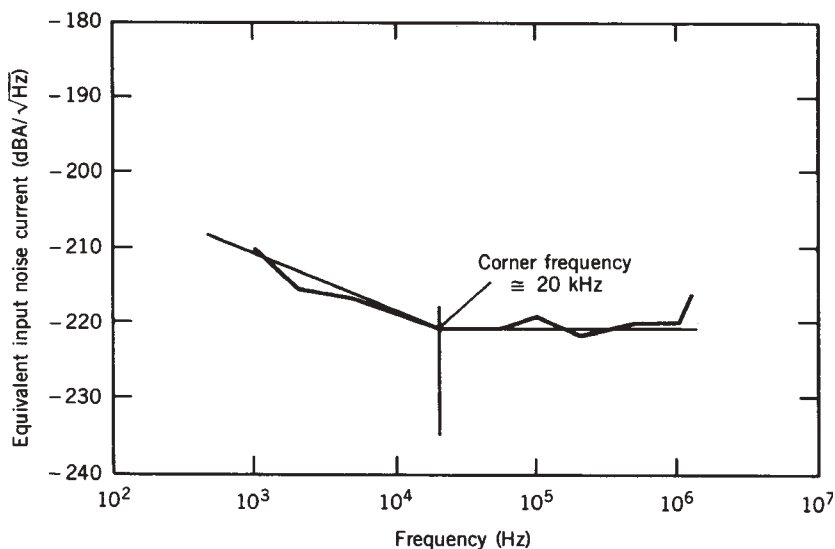
FIGURE 3.74   Equivalent input noise current versus frequency for AT-22000 silicon bipolar transistor bias at $V_{CB} = 10$ V, $I_E = 10$ mA. (From Ref. 3.48.)

flicker noise. As the source impedance presented to the base approaches zero, the e_n noise source will begin to dominate i_{ni}.

A major advantage of silicon bipolar transistors is the low corner frequency for flicker noise. The data reported in Figure 3.74 for the Agilent/Avantek AT-22000 at a bias of $V_{CB} = 10$ V, $I_E = 10$ mA gives a corner frequency of about 20 kHz at room temperature. Values below 100 kHz are typical of silicon bipolar transistors [3.45].

3.4   HETEROJUNCTION BIPOLAR TRANSISTOR

Because of the superior material properties of compounds of groups III to V such as GaAs, a bipolar transistor using this material has been a goal since 1957 [3.49]. The use of the heterojunction emitter–base has made the HBT a reality. Three primary advantages result from this structure (Fig. 3.75) [3.50]:

1. The forward-bias emitter injection efficiency is very high since the wider bandgap AlGaAs emitter injects electrons into the GaAs base at a lower energy level but the holes are prevented from flowing into the emitter by an energy barrier.
2. The base can be doped heavily to reduce the base resistance.
3. Implant damage can be used to reduce the parasitic collector–base capacitance.

Other advantages for this bipolar transistor are high output current per device unit width or periphery, high current gain, and potentially low $1/f$ noise. Since the entire emitter area cross section can carry current because of the lower base resistance, the power-handling capability of this structure will be very high. Output power of greater
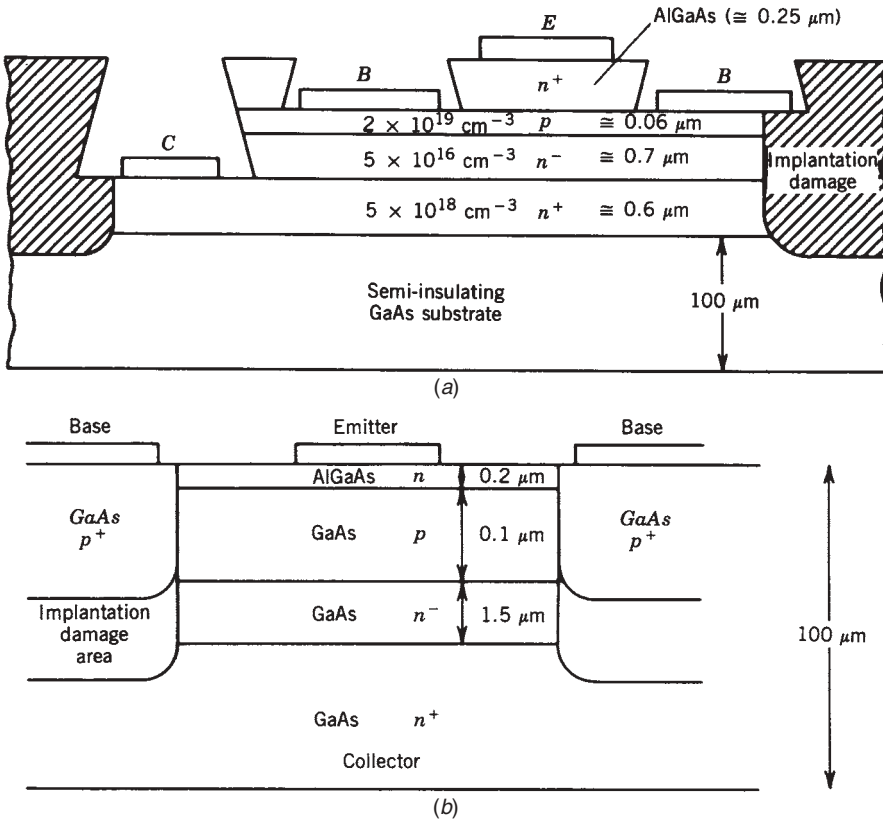
FIGURE 3.75 (*a*) Heterojunction bipolar transistor structure (HBT), single-chip structure. (*b*) HBT structure for GaAs monolithic circuits. (From Ref. 3.50 © IEEE 1987.)

than 4.0 W/mm at 10 GHz has already been reported [3.51]. Although these transistors were not yet available commercially, excellent results have been reported [3.51]:

$$f_t = 75 \text{ GHz} \qquad f_{\max} = 175 \text{ GHz} \qquad g_m/Z = 7 \text{ S/mm}$$

$$P/Z = \begin{cases} 4.0 \text{ W/mm} & \text{at 10 GHz} \\ 1.5 \text{ W/mm} & \text{at 36 GHz} \end{cases}$$

The high output power is a particularly useful feature of this transistor. If the maximum junction temperature can be made high, the realization of a high-power GaAs bipolar transistor may occur.

Another important feature of this transistor is the low $1/f$ noise, since the surface states of GaAs no longer contribute significant noise to the emitter current. A corner frequency below 1 MHz has been found for the HBT [3.52], which is becoming comparable to silicon bipolar transistors. This effect could be very significant for oscillator applications.

The small-signal equivalent circuit of a 1987 HBT from Texas Instruments is given in Figure 3.76 and Table 3.18 for the *npn* transistor reported by Bayraktaroglu et al. [3.53–3.55]. This is a millimeter-wave transistor with an emitter periphery of
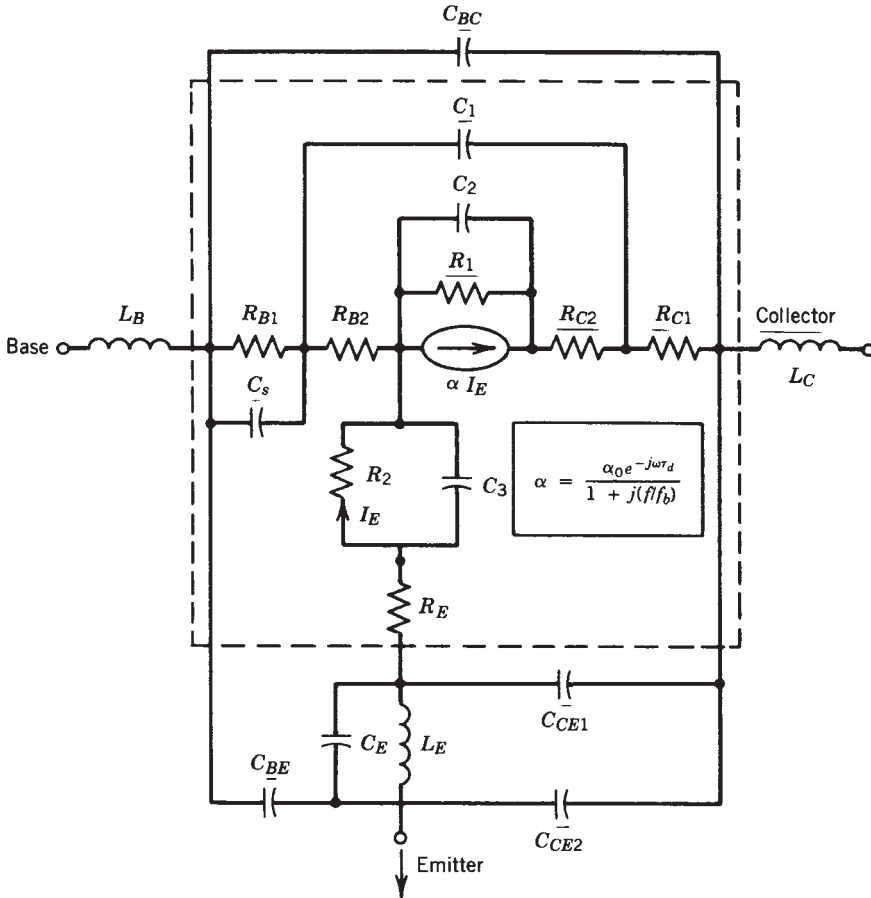
FIGURE 3.76   Model of HBT to 26.5 GHz. (From Ref. 3.50 © IEEE 1988.)

60 μm and an emitter pitch of 4 μm. There are two emitter fingers each of length 15 μm. The total perimeter was calculated by including all of the emitter periphery, both sides. By a different method which includes only the length of the emitter metal, one obtains 30 μm, a factor of 2 lower. This second method is the one to be used. The normal bias condition for this model is $V_{CE} = 4$ V, $I_C = 20$ mA.

The S parameters of this model are compared to the measured data in Figure 3.77 up to 26.5 GHz. As low-noise oscillators, these transistors have given the results summarized in Table 3.18.

A more modern treatment of HBTs is given by Liu [3.56] and [3.59] in Figure 3.78.

TABLE 3.17   HBT Oscillator Results

| f (GHz)	P_0 (dBm)	$\mathcal{L}(f)$ (dBc/Hz)	Reference
4	10	−73 at 1 kHz	Agarwal [3.57] (Rockwell)
15.6	6.5	−60 at 10 kHz	Lesage et al. [3.58] (NEC)
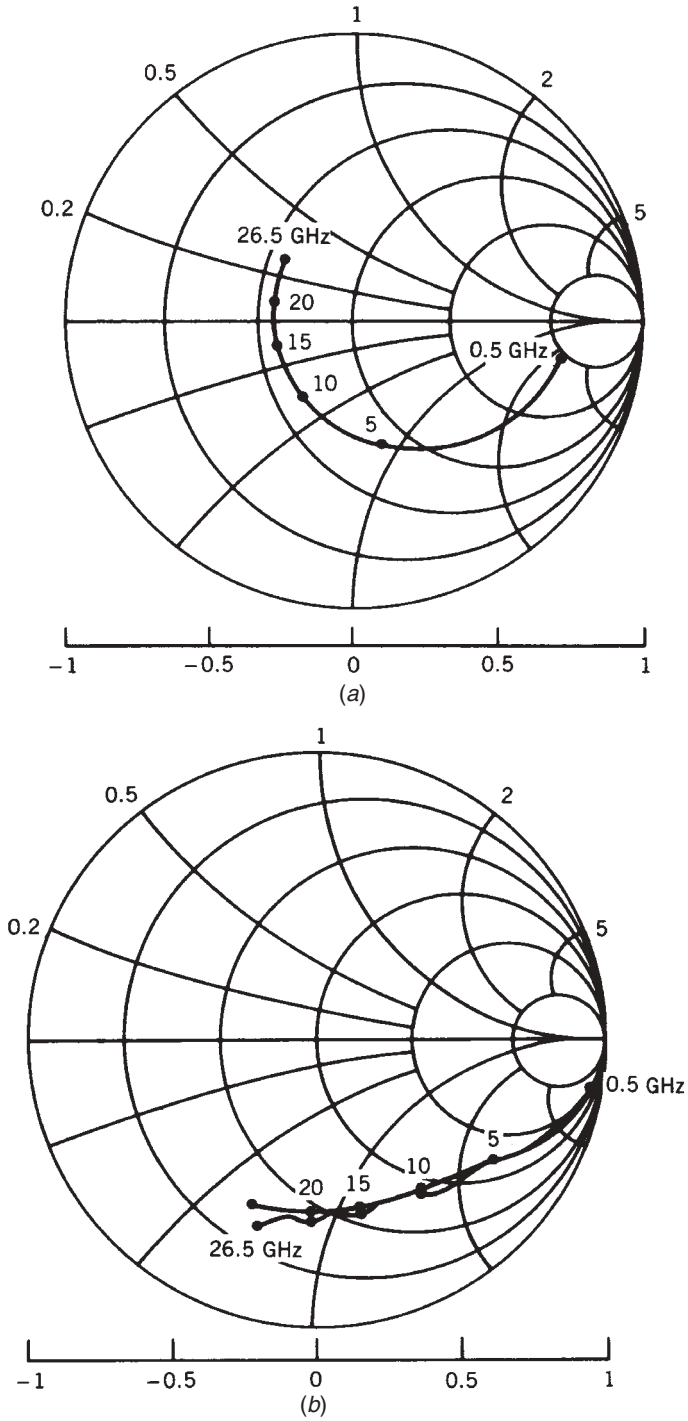
FIGURE 3.77   (*a*) S_{11} of HBT and model to 26.5 GHz. (From Ref 3.51.) (*b*) S_{22} of HBT and model to 26.5 GHz. (From Ref 3.51.)
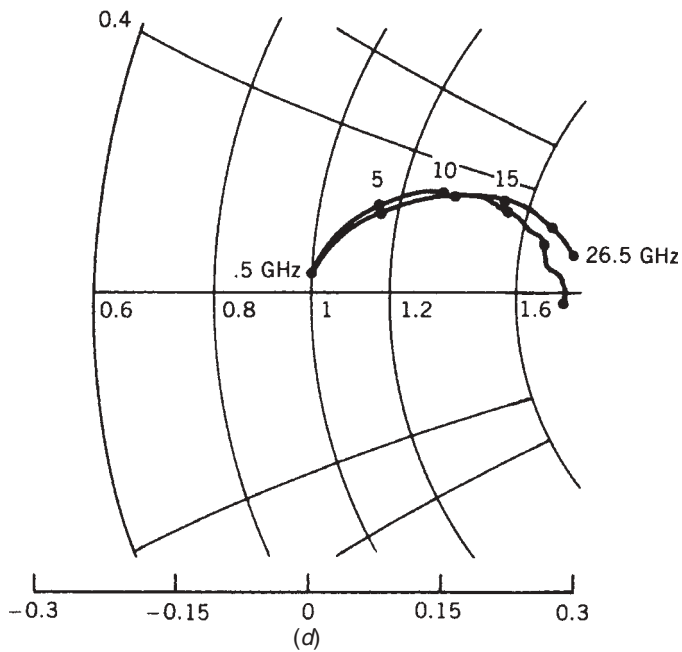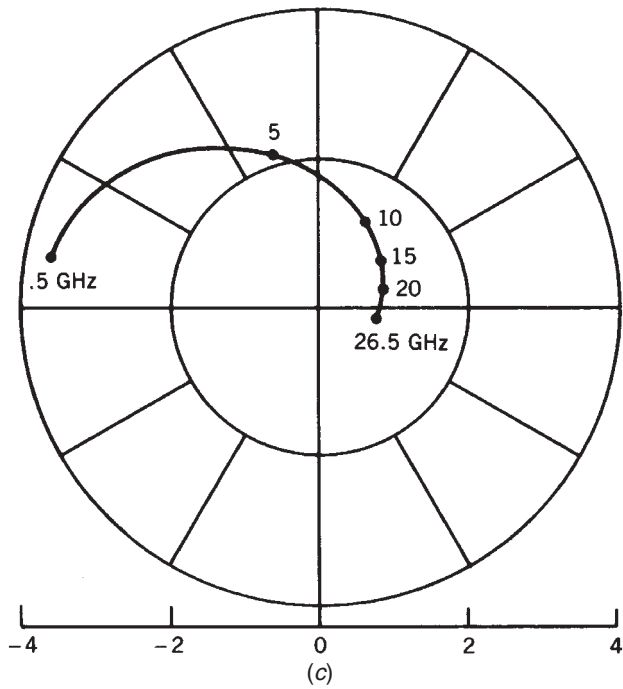
FIGURE 3.77 (*c*) S_{21} of HBT and model to 26.5 GHz. (From Ref 3.51.) (*d*) S_{12} of HBT and model to 26.5 GHz. (From Ref 3.51.) (*continued*)

TABLE 3.18   Parameter Values for 60-μm Emitter Periphery *npn* and *pnp* HBTs

Parameter	*npn*	*pnp*	Parameter	*npn*	*pnp*
f_t	22 GHz	19 GHz	C_s	1.34 pF	0
f_{max}	40 GHz	25 GHz	R_{C1}	1 Ω	7.4 Ω
α_0	0.93	0.96	R_{C2}	4 Ω	3.3 Ω
τ	2 ps	4 ps	R_E	8.5 Ω	7.0 Ω
f_b	65 GHz	35 GHz	C_{BC}	0.012 pF	0.012 pF
C_1	0.06 pF	0.04 pF	C_{BE}	0.022 pF	0.022 pF
C_2	0.01 pF	0.1 pF	C_{CE1}	0.012 pF	0.012 pF
C_3	0.4 pF	0.3 pF	C_{CE2}	0.06 pF	0.08 pF
R_1	1.0×10^6	1.0×10^6	C_E	0.022 pF	0.03 pF
R_2	10 Ω	6.8 Ω	L_B	0.165 nH	0.26 nH
R_{B1}	17 Ω	3.0 Ω	L_E	0.032 nH	0.09 nH
R_{B2}	27.5 Ω	4.4 Ω	L_C	0.06 nH	0.134 nH
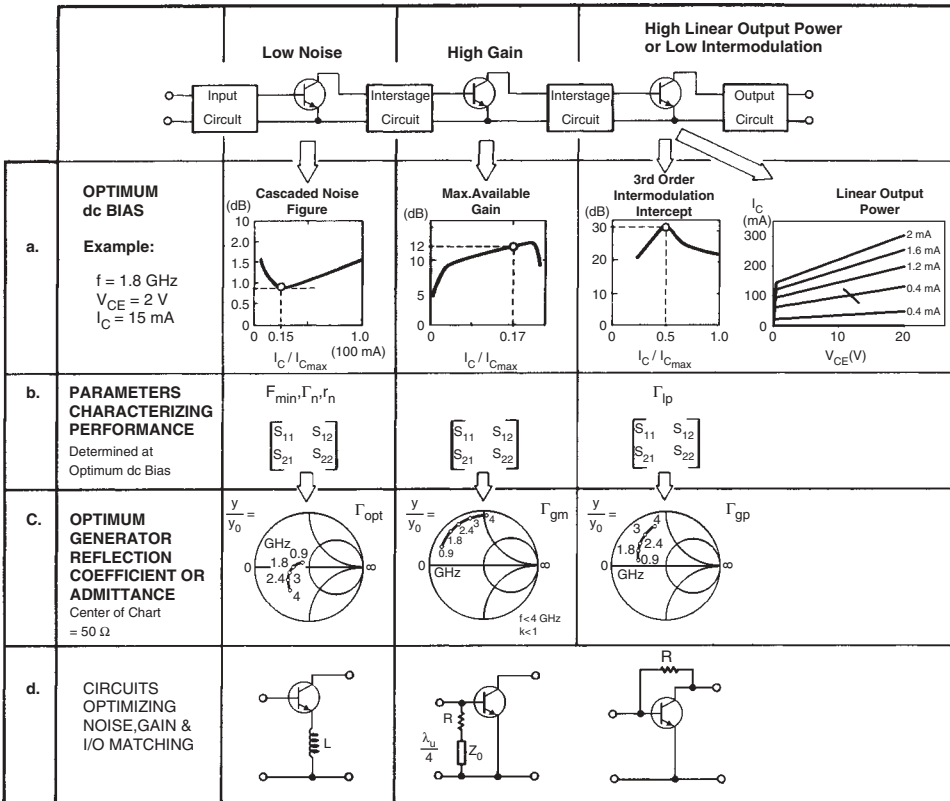
FIGURE 3.78   Key parameters in applying a BJT in low-noise front-end, high-gain and linear power stages. (*a*) BJT characteristics that lead to optimum dc bias for low-noise front end. (*b*) Parameters characterizing device performance. (*c*) Γ_{opt} for first stage and S_{11} and S_{22} for output stage as simulated by CAD software. The example is based on the Siemens BJTs BFP420 (low-noise stage), BFP450 (high-gain stage), and BFG235 (output stage). (*d*) Circuits to optimize stage noise, gain and input/output matching. (Presentation based on Figure 14 in Ref. 3.59.)

3.5   MICROWAVE FET

For microwave application, the major FET types are now Si MOSFETs and GaAs MESFETs followed by PHEMTs and MHEMTs. The MOSFETs are used specifically in RF integrated circuits (RFICs) and will be introduced next.

3.5.1   MOSFETs

There are several members of the FET family that can be used to high frequencies. The junction FET, which has been used for many years, is limited to about 500 MHz for reasonable performance, for the most 1 GHz. A more detailed discussion of its capabilities can be found. However, coming from the bipolar process, CMOS transistors have become a strong competitor to gallium arsenide in the RFIC world. Figure 3.79 shows examples of a modern BiCMOS process.

The MOS transistors are typically used only in integrated circuits (ICs), but not as discrete devices. To build circuits with them, one typically needs a manual for the IC process. For the large-signal simulation as well as dc simulation, there are several models available:

> Level 1   Schichman–Hodges model
> Level 2   Geometry-based model
> Level 3   Semiempirical model

In addition to this, the Bipolar/FET simulation Version 3 (BSIM3V3) model is a much more complex model which is used for much more detailed analysis.

For microwave and RF application, a variety of other models, which are more or less complex, have been developed. It appears that the most attractive model is the one called EKV. The abbreviation EKV comes from the authors Enz, Krummenacher, and Vittoz. The model extractors for this are Aurora, IC-CAP (Agilent program for parameter Extraction) and A vertical Gate Structure for MOS transistor (VTMOS).

However, the RFIC design is a task which goes beyond the scope of this book and the references at the end of the chapter will give good insight [3.60].

CMOS transistors with 0.35-μm technology are used in many applications and even 0.12-μm devices are now available. Operating frequencies up to 2.5 GHz have been
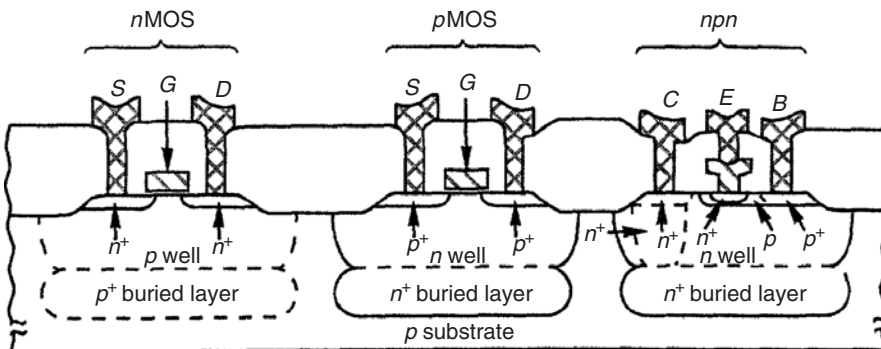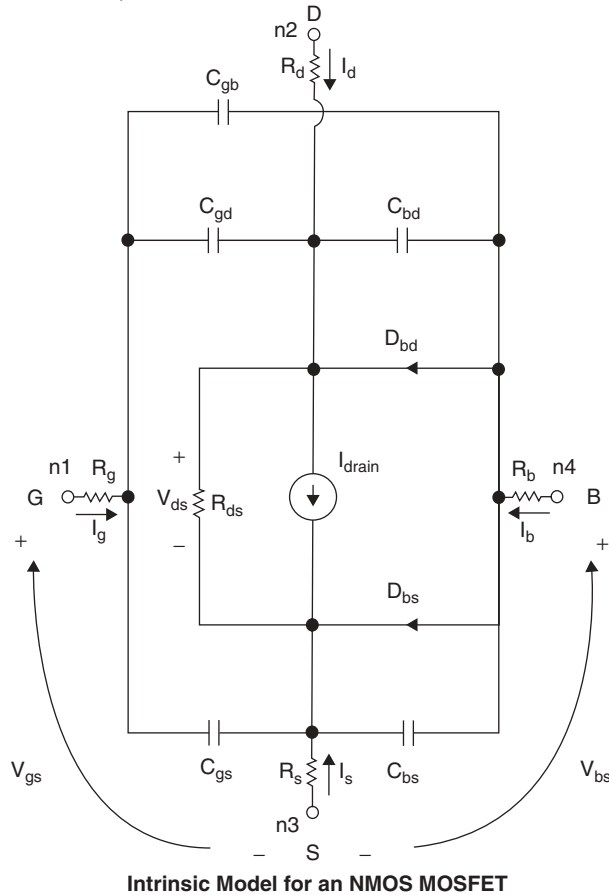

FIGURE 3.79   Example of modern BiCMOS process.

The following models are supported:
- Level 1 - Schichman-Hodges model
- Level 2 - Geometry-based model
- Level 3 - Semi-empirical model

Intrinsic Model for an NMOS MOSFET

FIGURE 3.80 FET–MOSFET model. An n-channel MOSFET model is shown. For P-channel MOSFET, all voltages and currents are reversed.

shown. The general circuit design rules, however, are the same as for GaAs FETs; one needs to know the measured S parameters or the SPICE parameters. Besides the RFIC MOS and DMOS transistors, the LDMOS transistors (discussed in Chapter 9) have become very popular for power application. The following discussion shows the large-signal MOSFET model, which are popular models as shown in Figure 3.80. At the moment we are concentrating on the level 3 model, which can be used for microwave applications. For more critical applications, the BSIM model has been developed. The model levels 1 and 2 are more frequently used for switching applications rather than linear or slightly nonlinear applications.

For example, the following describes a cascode low-noise amplifier in CMOS technology. The transistor is described in level 3 nonlinear parameters:

$$\text{Level} = 3 \qquad l = 0.3 \ \mu\text{m} \qquad w = 500 \ \mu\text{m} \qquad r_{ds} = 10{,}000$$

$$\text{is} = 6.53 \times 10^{-16} \qquad c_{gs0} = 0.2 \text{ pF} \qquad c_{gd0} = 0.02$$

$$\phi = 0.58 \qquad \gamma = 0.21 \qquad t_{ox} = 4 \times 10^{-8} \qquad n_{sub} = 10^{15} \qquad x_{qc} = 0.51$$

Figure 3.81 is a schematic for the amplifier arranged in an RFIC and entered into a harmonic balance simulator.

In analyzing this amplifier from 3 to 5 GHz, we obtain a gain of 8 dB, a noise figure of about 1 dB, input match of -10 dB, and an output match of -34 dB for S_{21}, S_{11}, and S_{22} (Fig. 3.82). The inductor in the source compensates for the Miller effect detuning. Therefore, the noise figure and minimum noise figure are quite close together. The circuit simulator is capable of predicting the exact noise figure based on a complex noise model similar to the one we will develop for the GaAsFET. This is an example for MOSFET application. Design rules on how to construct amplifiers like this will follow in Chapter 8.

The BSIM model is much more challenging because the parameter extraction effort for so many parameters is a huge task. It is difficult to judge if the parameters are incorrect or the model itself is incorrect if the measured results do not agree with the result of the modeling.

Figures 3.83 and 3.84, from an Infineon presentation, show two exciting examples of what can be done with 0.13-μm technology, and they speak for themselves. Figure 3.85 shows the U-channel MOSFET intrinsic model.

3.5.2   Gallium Arsenide MESFETs

Introduction   The GaAs MESFET is more commonly used in microwave IC designs because of higher gain, higher output power, and a lower noise figure in amplifiers. The higher gain is due to higher mobility of electrons (compared to silicon). The
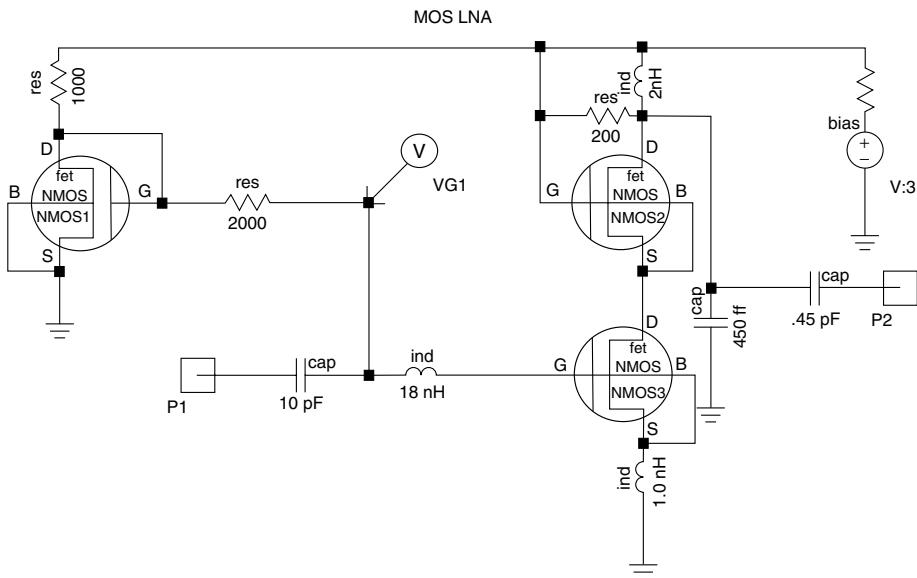

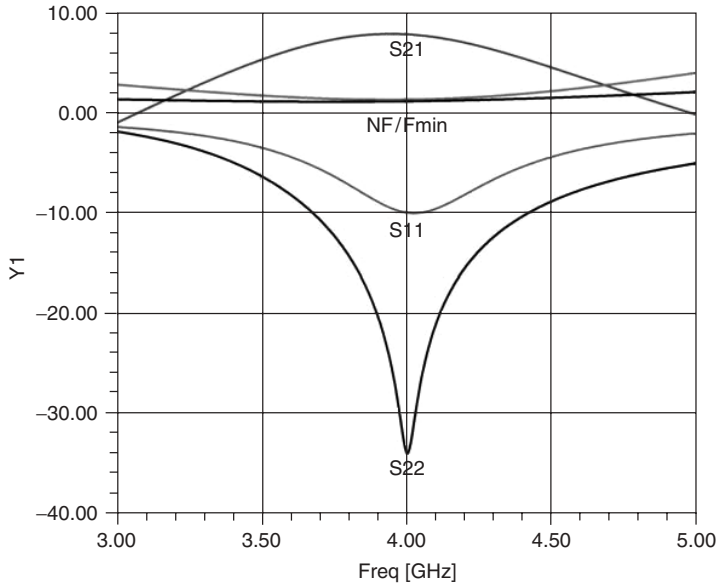**FIGURE 3.81**   Cascode low-noise amplifier in CMOS technology.
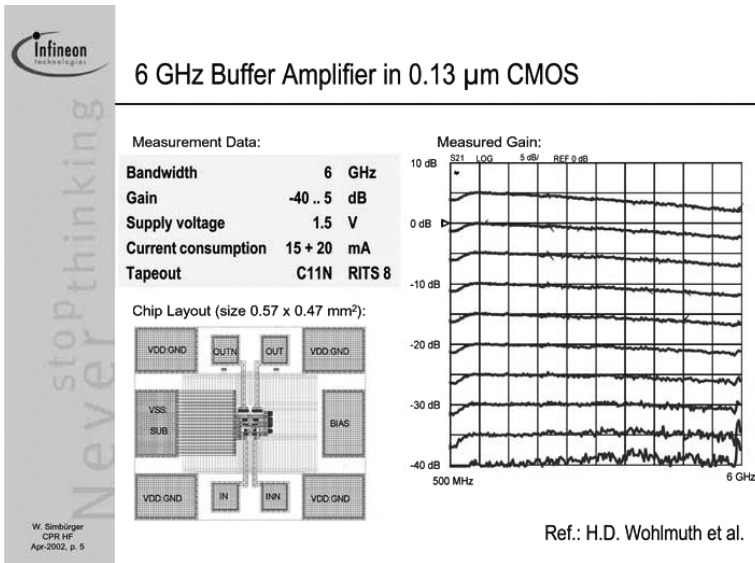
FIGURE 3.82 Design result.

FIGURE 3.83 A 6-GHz buffer amplifier in 0.13-μm CMOS.

improvement in output power is due to the higher electric field and higher saturated drift velocity of the electrons [Eqs. (3.93)]. The lower noise figure is partially due to the higher mobility of the electron carriers. Moreover, fewer noise sources are present in the FET (no shot noise) as compared to the bipolar transistor. A disadvantage of the GaAs MESFET is the higher $1/f$ flicker noise compared to silicon bipolar transistors.
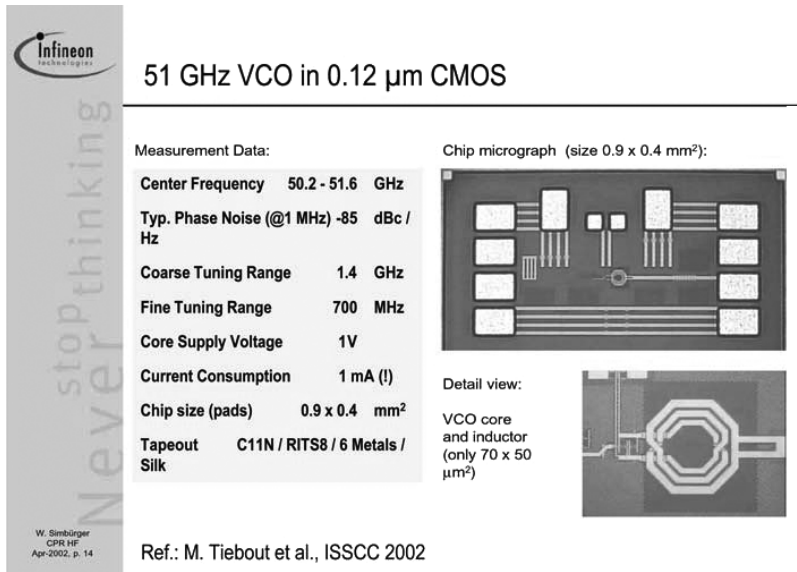
FIGURE 3.84   A 51-GHz VCO in 0.13-μm CMOS.

Before considering the large-signal behavior of MESFETs, a small-signal property of these and other FETs is the unusual discovery of real (Y_{12}), which shows a negative resistance as opposed to the positive resistance of bipolar transistors [3.61]. No one has explained the origin of this negative resistance, but it undoubtedly plays a significant role in feedback amplifiers (see Chapter 8). Including this effect in small-signal models has virtually no effect so far. The S_{12} is so small that an accurate model of this parameter seems to be unnecessary. A domain capacitance has been proposed to account for this effect [3.62], but excluding this additional feedback capacitance seems to have minor effects. One of the major challenges of MESFET/PHEMT modeling is to account for this unusual effect in Y_{12}/S_{12}.

Large-Signal Behavior of GaAs MESFETs   The mathematics for the large-signal behavior of the GaAs FET is basically quite similar to that for the junction field-effect transistor (JFET); however, the computation of JFET channel current, diode currents, and capacitance is much simpler than necessary for the GaAs FET. Temperature effects are embedded in all the equations for all the transistors mentioned so far. In our opinion, the modified Materka model used by Ansoft and many others is the most complete one; however, the following models are supported by most CAD tools:

- Angelov (Chalmers) [3.63–3.65]
- Curtice-Ettenberg cubic [3.66]
- Curtice Quadratic [3.67]
- IAF (Berroth) [3.68–3.70]
- ITT PFET and TFET [3.71]
- Modified Materka–Kacprzak [3.72]
- Raytheon (Statz) [3.72]

Intrinsic Model for an NMOS MOSFET
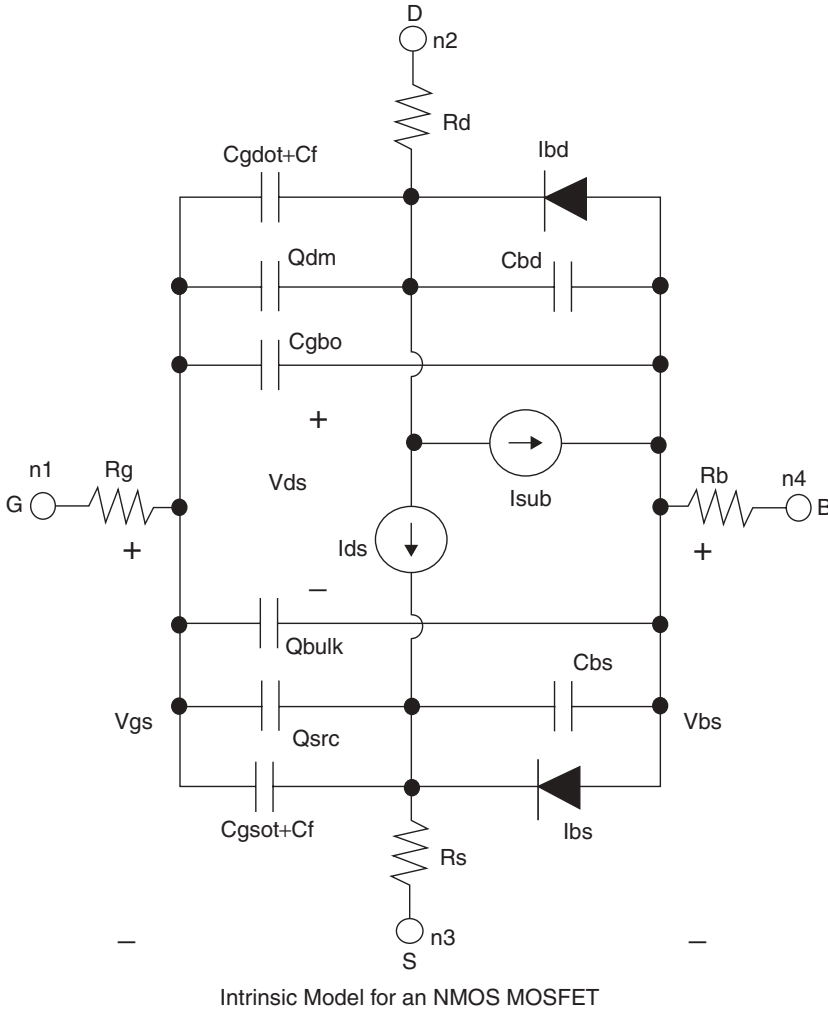
FIGURE 3.85 FET–BSIM3V3 MOSFET model. An *n*-channel MOSFET model is shown. For *P*-channel MOSFET, all voltages and currents are reversed.

- Physics-based MESFET [3.73–3.76]
- TriQuint (TOM1, TOM2, and TOM3) [3.77–3.80]
- With some restrictions, metal–insulator–semiconductor FETs (MISFETs), modulation-doped FETs (MODFETs), and high-electron-mobility transistors (HEMTs)

The main advantages of GaAs FET technology derive from the fact that it uses a metal–semiconductor junction with a barrier voltage of 0.8 V, its input capacitance is typically less than 0.2 pF, and the reverse feedback capacitance is less than 0.02 pF, or roughly 10% of the input capacitance. As a result of this, f_{max} is approximately five times higher than f_T. Table 3.19 shows a comparison of silicon BJT and GaAsFET

TABLE 3.19 Comparison of Si BJT, SiGe HBT, and GaAs FET Technologies

Parameter	Si Bipolar	SiGe HBT	GaAs MESFET
f_T	25 GHz	300 GHz	22 GHz
f_{max}	40 GHz	350 GHz	110 GHz
Features	Low cost, low $1/f$ noise ($5 \text{ kHz} = 1/F_C$)	Low $1/f$ noise, very low distortion	Highest flexibility, lowest NF_0, well established

technologies. While f_{max} for the bipolar transistor is

$$f_{max} \cong \sqrt{\frac{f_t}{8\pi r'_{bb}C_C}} \tag{3.201}$$

the f_{max} determination for the GaAs FET is given by

$$f_{max} = \frac{f_T}{2}\sqrt{\frac{R_0}{R_i + R_s + R_g}} \tag{3.202}$$

As a sample calculation,

$$f_{max}\frac{21.9 \text{ GHz}}{2}\sqrt{\frac{450}{1 + 1.5 + 2}} = 110 \text{ GHz} \tag{3.203}$$

The three major drawbacks of the GaAs MESFET are as follows:

1. Much higher flicker corner frequency (somewhere between 10 and 100 MHz, perhaps lower in special cases), probably due to a lack of a surface passivation. It should be noted that Gunn diodes also made from GaAs have very low $1/f$ flicker corner frequencies because these devices perform below the surface (estimated as low as 100 Hz).
2. Much higher output conductance. This tends to load down any circuit connected to the drain. On the other hand, since the transconductance is quite high for even low currents, these devices have very high gains at low frequencies, which can make them quite unstable. In the saturated mode it is not uncommon to find a drain–source resistance of 100 to 500 Ω, while BJTs and JFETs offer values of several kilohms and higher.
3. Because of the very high flicker corner frequency (from 10 to 100 MHz), MES-FETs are really not useful for low-noise mixers and oscillators, and unless there are no devices available in the frequency range above 30 GHz, they should be avoided for these applications.

As to the MESFET's construction and dc properties, Figure 3.86 shows a MESFET's cross section and dc $I-V$ characteristics.

It was outlined in the beginning of the chapter that, while the GaAsFET is a close relative to the JFET and MOSFET, its actual behavior was found to be best described
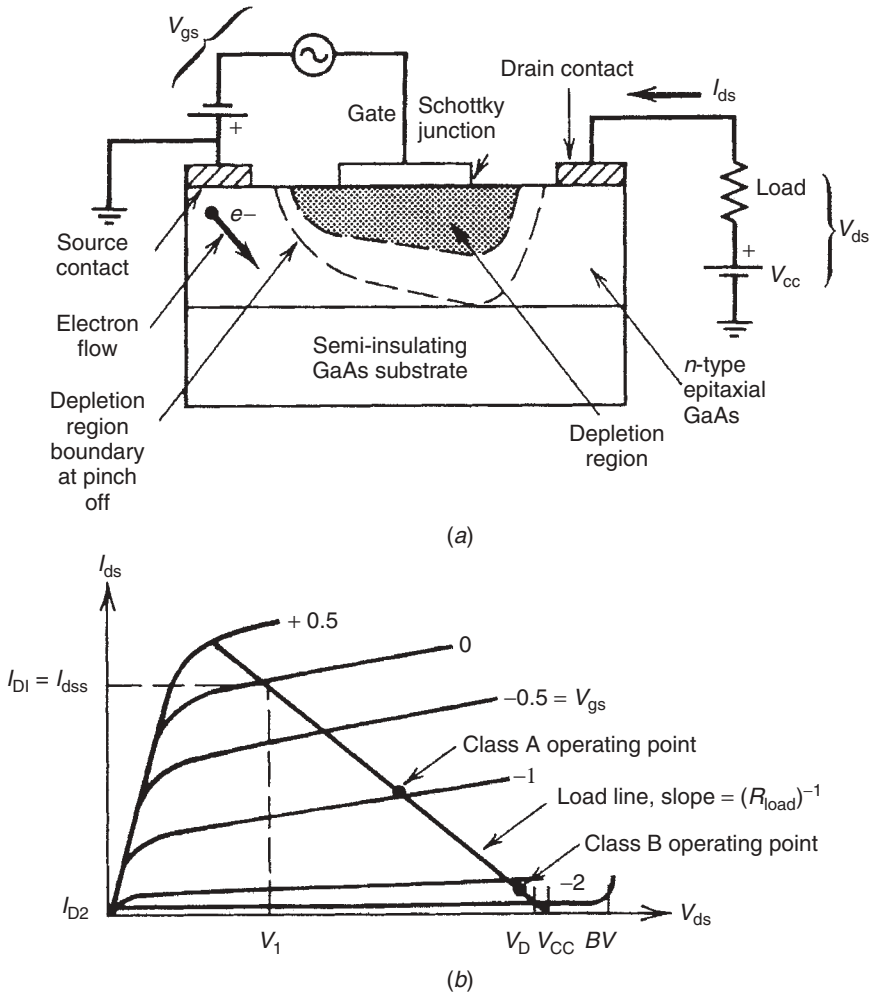
FIGURE 3.86   (*a*) Cross section and bias circuit. (*b*) A dc $I-V$ curve, including ac load line, for MESFET.

by a set of analytic equations. The first such model was the one by Curtice in the form of quadratic and cubic models, but it does not have enough correct derivatives to give enough insight into such subteties as third- and higher order intermodulation distortion and accurate harmonic generation. Other researchers have addressed various areas, but we still find that the Materka model has the best success in nonlinear applications. The large-signal topology for all FETs consists of an intrinsic model with some extrinsic parameters, further complicated by the package, as shown by Figures 3.87 and 3.88. Table 3.20 lists their keywords. The actual intrinsic model and its parameter definition depend on the particular model, and since designs using GaAs-FET will always be done using CAD tools, we will not go into any detail of the equations but will list them. They are not dissimilar from the JFET and MOSFET equations.
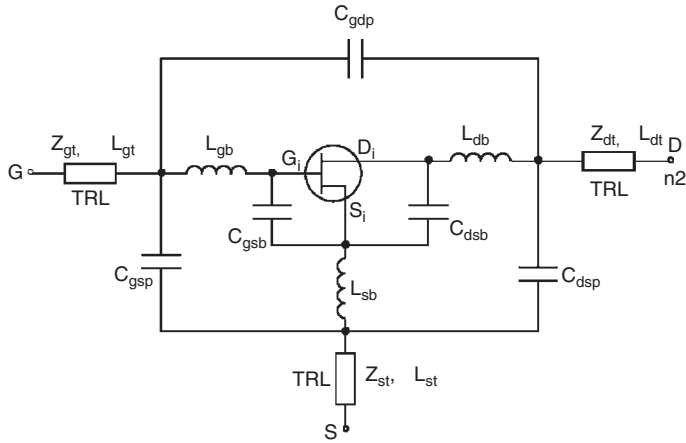
FIGURE 3.87   MESFET extrinsic model.
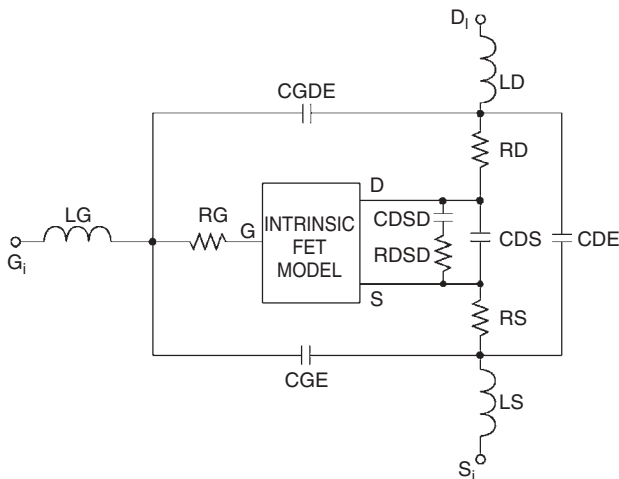
FIGURE 3.88   MESFET package model.

Modified Materka–Kacprzak SP Check Model   Figure 3.89 shows the intrinsic model of the Materka FET. Table 3.21 lists its keywords:

Large-Signal Equations

Device equations

$$V_{gsi} = \text{intrinsic gate–source voltage}$$

$$V_{dsi} = \text{intrinsic drain–source voltage}$$

$$V1 = \text{voltage across } C_{GS} \text{ and } R_i$$

$$V_{gdi} = \text{intrinsic gate–drain voltage}$$

TABLE 3.20   MESFET Nonlinear Model: *Extrinsic Keywords*

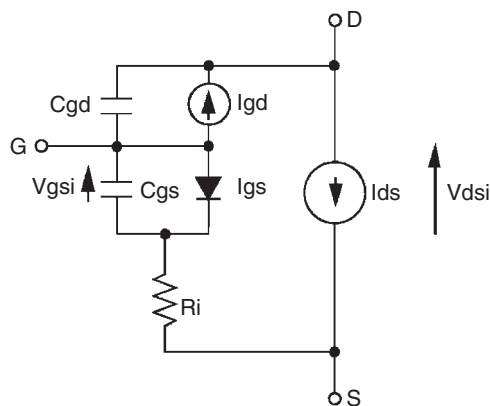| Keyword	Description	Unit	Default
RG	Gate bulk and ohmic resistance	Ω	0.0
RD	Drain bulk and ohmic resistance	Ω	0.0
RS	Source bulk and ohmic resistance	Ω	0.0
LG	Gate lead inductance (metallization)	H	0.0
LD	Drain lead inductance (metallization)	H	0.0
LS	Source lead inductance (via)	H	0.0
CDS	Drain–source capacitance	F	0.0
CDSD	Low-frequency trapping capacitor	F	0.0
RDSD	Channel trapping resistance	Ω	∞
CGE	Gate–source electrode capacitance	F	0.0
CDE	Drain–source electrode capacitance	F	0.0
CGDE	Gate–drain electrode capacitance	F	0.0
LGB	Gate wirebond inductance	H	0.0
LDB	Drain wirebond inductance	H	0.0
LSB	Source wirebond inductance	H	0.0
CGSB	Gate bondpad to source capacitance	F	0.0
CDSB	Drain bondpad to source capacitance	F	0.0
CGSP	Gate-to-source package capacitance	F	0.0
CDSP	Drain-to-source package capacitance	F	0.0
CGDP	Gate-to-drain package capacitance	F	0.0
ZGT	Gate transmission line impedance	Ω	50
ZDT	Drain transmission line impedance	Ω	50
ZST	Source transmission line impedance	Ω	50
LGT	Gate transmission line length for $\varepsilon_r = 1$	m	0.0
LDT	Drain transmission line length for $\varepsilon_r = 1$	m	0.0
LST	Source transmission line length for $\varepsilon_r = 1$	m	0.0

FIGURE 3.89   Intrinsic model of modified Materka–Kacprzak MESFET.

TABLE 3.21 Parameters for Materka Model

Keyword	Description	Unit	Default
	Area, Noise and Name		
AREA	Area multiplier	—	1.0
KFN	Flicker noise coefficient (Materka model only)	—	0
AF	Flicker noise exponent	—	1.0
FCP	Flicker noise frequency shape factor	—	1.0
	Channel Current Model		
IDSS	Drain saturation current for $V_{GS} = 0$	A	0.1
VP0	Pinchoff voltage for $V_{DS} = 0$	V	−2.0
GAMA	Voltage slope parameter of pinchoff voltage	V^{-1}	0.0
E	Constant part of power law parameter	—	2.0
KE	Dependence of power law on V_{GS}	V^{-1}	0.0
SL	Slope of the $V_{GS} = 0$ drain characteristic in the linear region	A/V	0.15
KG	Drain dependence on V_{GS} in the linear region	V^{-1}	0.0
SS	Slope of the drain characteristic in the saturated region	A/V	0.0
T	Channel transit time delay	s	0.0
IG0	Diode saturation current	A	0
AFAG	Slope factor of forward diode current	V^{-1}	38.696
IB0	Breakdown saturation current	A	0
AFAB	Slope factor of breakdown current	V^{-1}	0
VBC	Breakdown voltage	V	∞
GMAX	Breakdown conductance	A/V	0
K1D	Fitting parameter	V^{-1}	0
K2D	Fitting parameter	V	0
K3D	Fitting parameter	V^2	0
R10	Intrinsic channel resistance for $V_{GS} = 0$	Ω	0.0
KR	Slope factor of intrinsic channel resistance	V^{-1}	0.0
	Materka Capacitance Model		
C10	Gate–source Schottky barrier capacitance for $V_{GS} = 0$	F	0.0
K1	Slope parameter of gate–source capacitance	V^{-1}	1.25
MGS	Gate–source grading coefficient	—	0.5
C1S	Constant parasitic component of gate–source capacitance	F	0.0
CF0	Gate–drain feedback capacitance for $V_{GD} = 0$	F	0.0
KF	Slope parameter of gate–drain feedback capacitance	V^{-1}	1.25
MGD	Gate–drain grading coefficient	—	0.5
FCC	Forward-bias depletion capacitance coefficient	—	0.8

Note: The flicker noise parameter of the Materka model is KFN so as not to conflict with the KF parameter in the capacitance model.

$$VT = k \, TJ/q \text{ (thermal voltage)}$$

$$k = \text{Boltzmann's constant}$$

$$q = \text{electron charge}$$

$$TJ = \text{analysis temperature (K)}$$

Channel current

$$I_{ds} = \text{IDSS}\left(1 + \text{SS}\frac{V_{dsi}}{\text{IDSS}}\right)\left(1 - \frac{V_{gsi}(t - \text{T})}{\text{VP0} + \text{GAMA } V_{dsi}}\right)^{(\text{E}+\text{KE } V_{gsi}(t-\text{T}))}$$
$$\times \tanh\left(\frac{\text{SL } V_{dsi}}{\text{IDSS}[1 - \text{KG } V_{gsi}(t - \text{T})]}\right) \tag{3.204}$$

Diode

$$I_{gd} = I_{gdc} - \begin{cases} \text{IB0 } \exp[-\text{AFAB}(V_{gdi} + \text{VBC})] \\ \dfrac{\text{GMAX}}{4}\{\tanh[\text{K1D}(V_{gsi} - \text{K2D})] - 1\} \\ \quad \times [V_{gdi} + VBC - \sqrt{(V_{gdi} + \text{VBC})^2 + \text{K3D}}] \end{cases} \tag{3.205}$$

where
$$I_{gdc} = \text{IG0}[\exp(\text{AFAG } V_{gdi}] - 1) \tag{3.206}$$

Channel resistance

$$R_i = \begin{cases} \text{R10}(1 - \text{KR } V_{gsi}) & \text{KR } V_{gsi} < 1.0 \\ 0 & \text{KR } V_{gsi} \geq 1.0 \end{cases} \tag{3.207}$$

Capacitance model

$$C_{gs} = \text{CGS0}\frac{F_1 F_2}{\sqrt{1 - V_{\text{new}}/\text{VBI}}} + \text{CGD0 } F3 \tag{3.208}$$

$$C_{gd} = \text{CGS0}\frac{F_1 F_3}{\sqrt{1 - \dfrac{V_{new}}{\text{VBI}}}} + \text{CGD0 } F2 \tag{3.209}$$

where
$$F_1 = \frac{1}{2}\left(1 + \frac{V_{\text{eff}} - \text{VT}}{\sqrt{(V_{\text{eff}} - \text{VT})^2 + \delta^2}}\right) \tag{3.210}$$

$$F_2 = \frac{1}{2}\left(1 + \frac{V_{gsi} - V_{gdi}}{\sqrt{(V_{gsi} - V_{gdi})^2 + (1/\text{ALFA})^2}}\right) \tag{3.211}$$

$$F_3 = \frac{1}{2}\left(1 - \frac{V_{gsi} - V_{gdi}}{\sqrt{(V_{gsi} - V_{gdi})^2 + (1/\text{ALFA})^2}}\right) \tag{3.212}$$

$$V_{\text{new}} = \begin{cases} A_1 & A_1 < V_{\text{max}} \\ V_{\text{max}} & A_1 \geq V_{\text{max}} \end{cases} \tag{3.213}$$

$$A_1 = \frac{1}{2}\left(V_{\text{eff}} + \text{VT} + \sqrt{(V_{\text{eff}} - \text{VT})^2 + \delta^2}\right) \tag{3.214}$$

$$V_{\text{eff}} = \frac{1}{2} \left(V_{gsi} + V_{gdi} + \sqrt{(V_{gsi} - V_{gdi})^2 + (1/\text{ALFA})^2} \right) \qquad (3.215)$$

$$\text{VT} = \text{VP0} + \text{GAMA } V_{dsi} \qquad (3.216)$$

$$\delta = 0.2 \qquad (3.217)$$

Some of the modifications to the Materka model have been done by CAD companies under various Department of Defense contracts.

The most relevant equation is really the channel current. Its derivatives are largely responsible for the accuracy of the intermodulation distortion (which favors the Angelov model), power-added efficiency, and, of course, its dc $I-V$ curves.

Besides having measured S parameters, it is useful to generate a linear equivalent circuit from them in order to extend the frequency range for the device. Modern CAD tools have a linear equivalent circuit similar to what we used in the bipolar transistor case. Figure 3.90 shows such an equivalent circuit with the parameters entered to match the measured data.

The curves in Figure 3.91 show very good agreement between measured and modeled data based upon the equivalent circuit above for a Texas Instrument model TI 335-µm FET. The curves show S_{11}, S_{12}, S_{21}, and S_{22} over a frequency range up to 18 GHz.

It should be noticed that the same curves will be generated if the S parameters are being generated from the large-signal model of the FET. The test circuit for this is given in Figure 3.92.

Enhancement/Depletion FETs To make the designer's life more difficult, it turns out that there are two types of GaAsFETs:

1. *Depletion FETs (DFETs)* Most similar to the JFET; here V_G must be negative to control the device. They are the most commonly produced and are the FET type most referred to in this book. On the one hand:

- They require a negative gate voltage with respect to the source.
- Self-bias allows operation from a single supply voltage.

On the other hand:

- For low-voltage operation, a negative voltage generator may be required.
- Supply voltage must be doubled to accommodate full-swing operation.

2. *Enhancement FETs (EFETs)* Most similar to the MOSFET; here V_G must be positive to bring life to the device. Practically speaking, EFETs are used mostly in integrated circuits; they are typically not available in discrete, packaged form. On the one hand:

- They need only positive supply for biasing.
- They provide higher g_m/mA (for the same device width)—5.1 mS versus 3.9 mS at 8 mA.
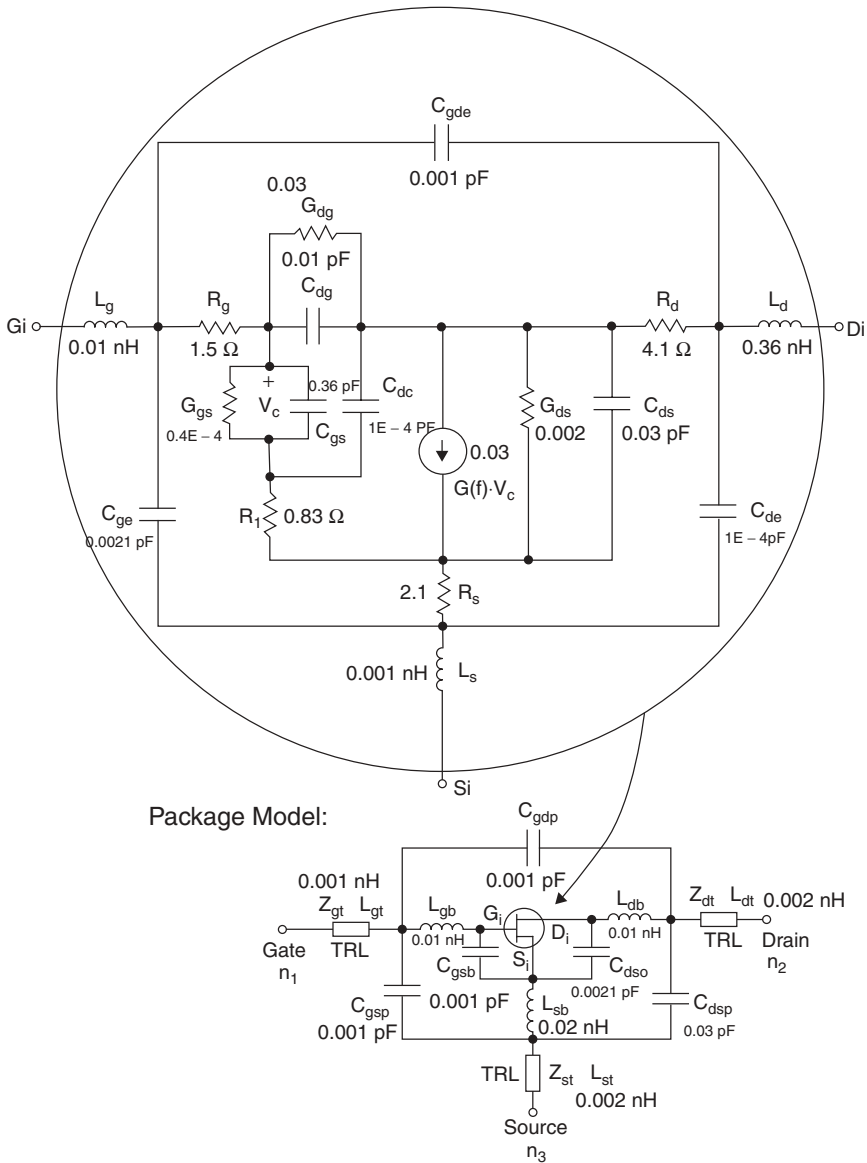
FIGURE 3.90 Texas Instruments 335-μm MESFET model.

- They are good for low-power LNAs, giving slightly better NF that DFETs, a NF of better than 1 dB at 1 GHz, and $I_{dd} < 10$ mA.

On the other hand:

- They have a very limited gate bias range (V_{GS} between 0.15 and 0.7 V).
- The gate conduction degrades NF and input impedance.
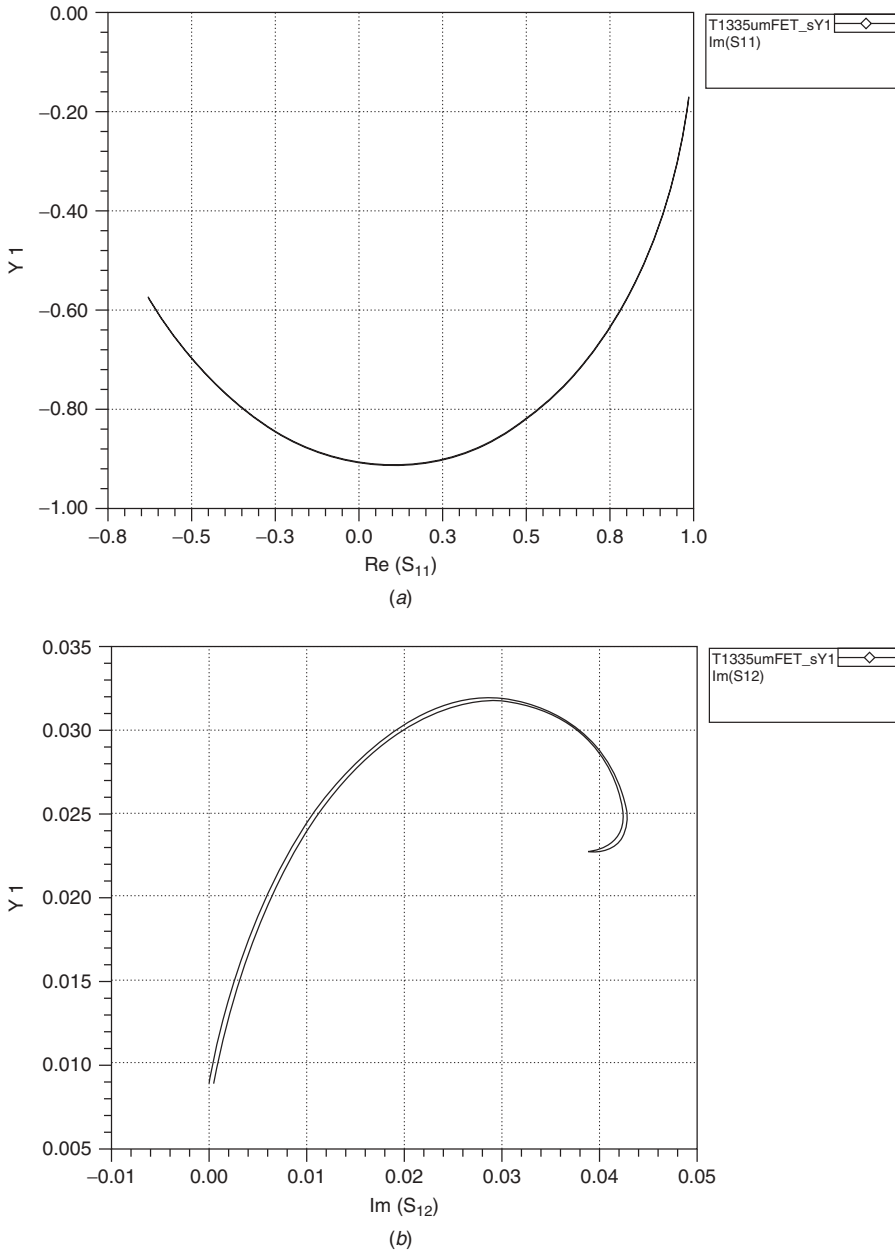
FIGURE 3.91   Plot of (*a*) S_{11}, (*b*) S_{12}, (*c*) S_{21}, and (*d*) S_{22} for a Texas Instruments 335-μm FET.

- The gate capacitance is higher than that of DFETs.
- The linearity is not as good as that of DFETs, although this may be changing.

With today's technologies, all GaAs devices are *n*-channel; we have not seen any *p*-channels yet. More information about biasing will be given in the next chapter.

(c)

(d)
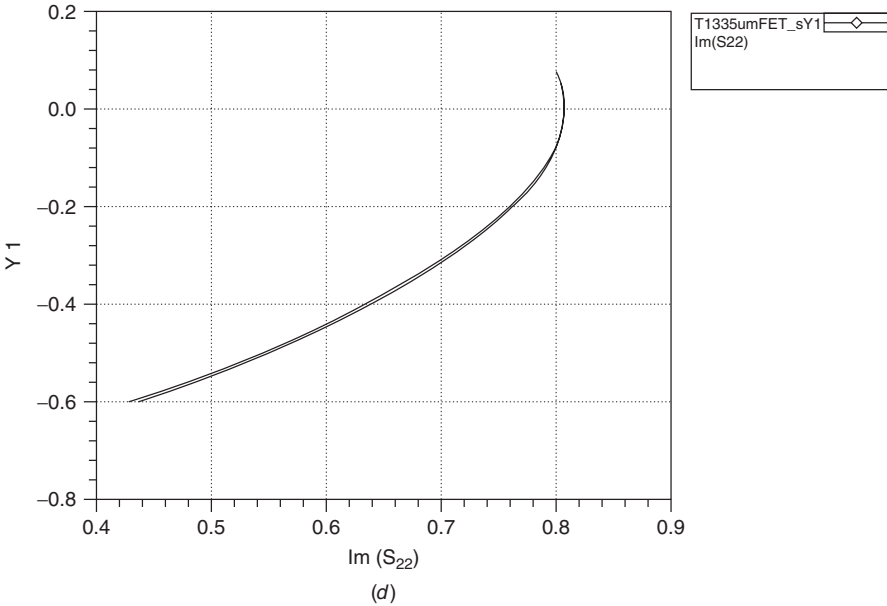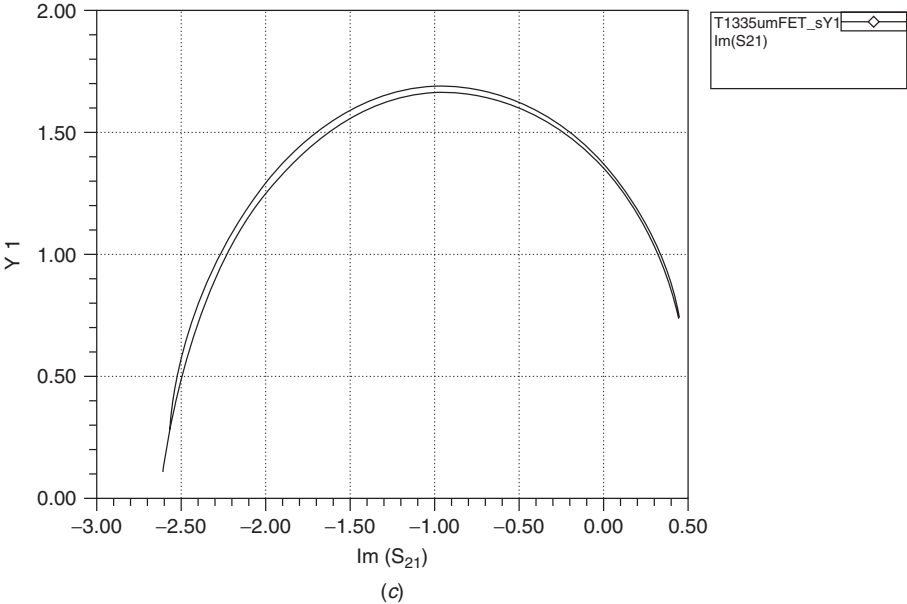
FIGURE 3.91 (*continued*)

Figure 3.93 is a lumped-element, two-part equivalent circuit of a MESFET showing the location of lumped-element components.

Small-Signal GaAs MESFET Model Figure 3.94 shows the applicable linear equivalent circuit for a MESFET and Table 3.22 lists its keywords. As with the MOS transistors, there is a GaAs dual-gate MOSFET available that is mostly used in special

S–Parameter Generation (TI335μm_FET)
(VDS = 2V, V_{gs} = 1.5V, ID = 20mA)
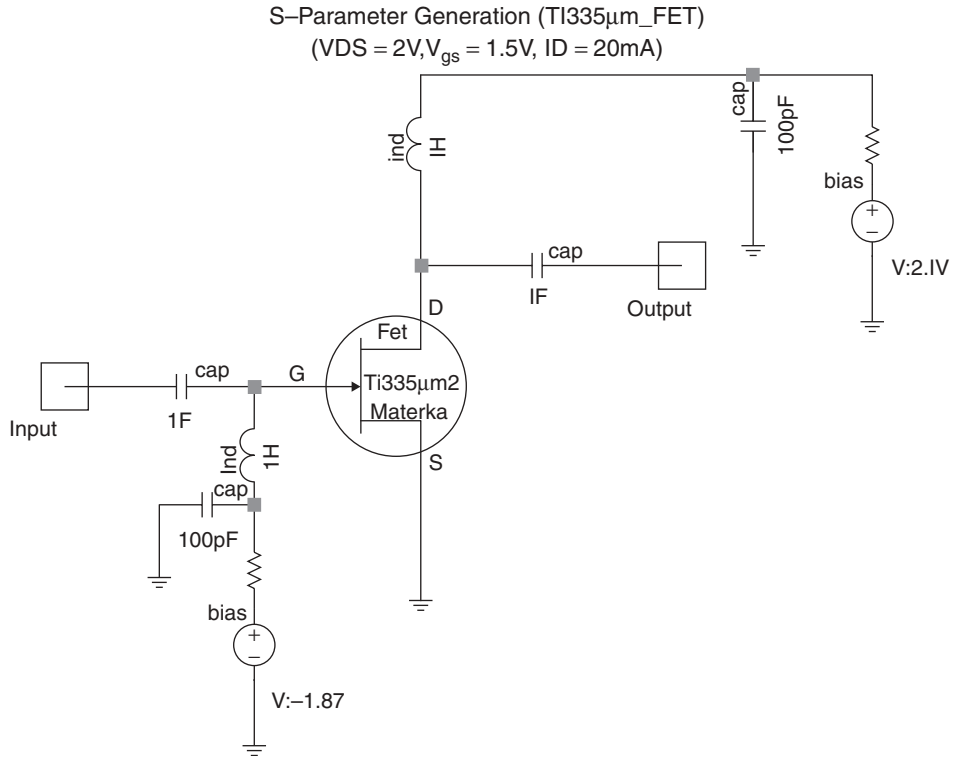
FIGURE 3.92 Texas Instruments 335-μm simulation schematic.
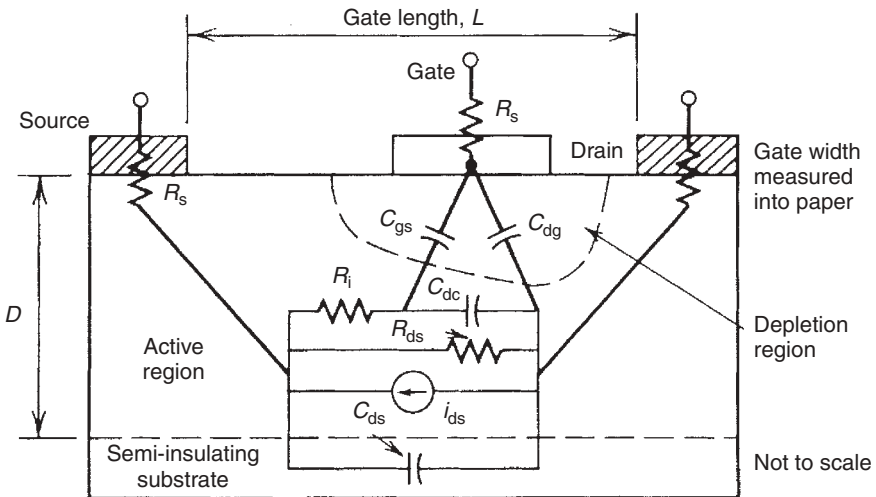
FIGURE 3.93 Location of lumped-element components for MESFET.
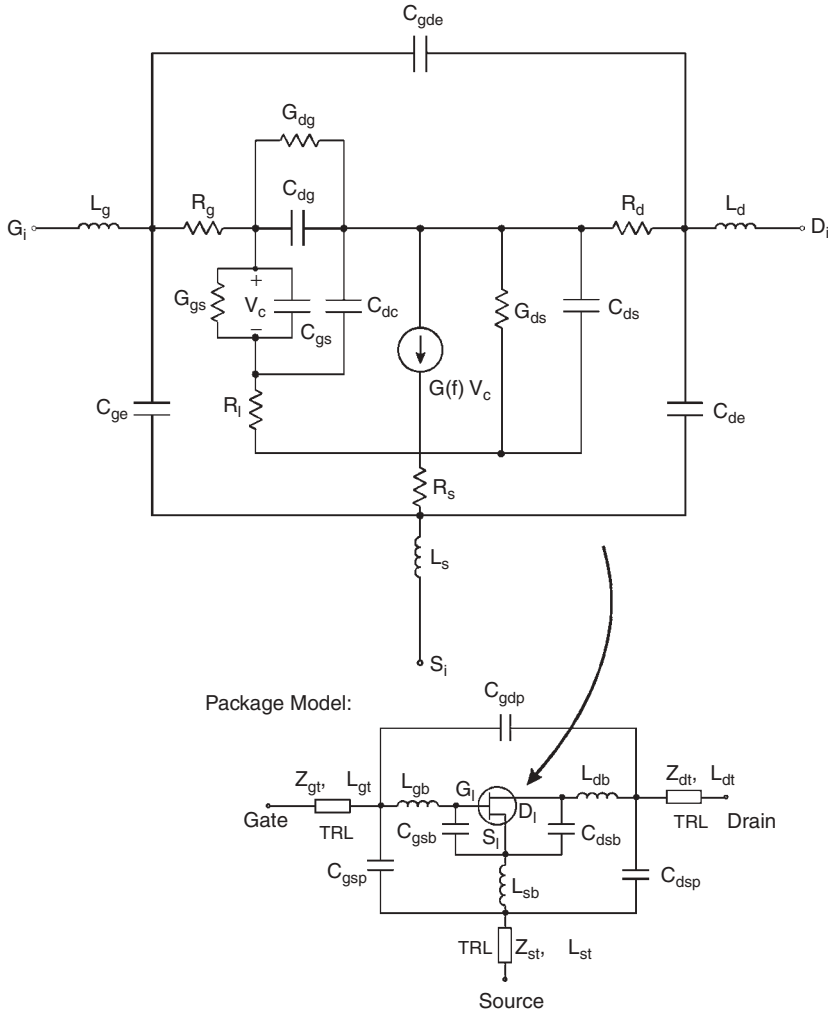
FIGURE 3.94   Small-signal model of MESFET.

circuits, such as preamplifiers and mixers, whose IF has to be significantly higher than the flicker corner frequency, for example, higher than 20 MHz.

The cross section of the GaAs MESFET is shown in Figure 3.95. The name MESFET has been adopted because of the similarity to MOSFET. In Figures 3.95 and later in Figure 3.98, the electrons are drawn to the drain by a V_{DS} supply that accelerates the carriers to the maximum drift velocity, $v_s = 2 \times 10^7$ cm/s. The reverse bias of the Schottky barrier gate allows the width of the channel to be modulated at a microwave frequency. Thus, the majority-carrier electrons are modulated by the input signal voltage applied across the input capacitance. Several interesting contrasts between the FET and the bipolar transistor are summarized in Table 3.23.

The frequency limitation of the FET is due to the gate length, which should be as short as possible. The frequency limits can be derived from the simplified hybrid-Π model in Figure 3.96.

TABLE 3.22 MESFET Nonlinear Parameters

Keyword	Description	Unit	Default
G	Transconductance at dc, G_o^a	Ω^{-1}	—
CGS	Gate–source capacitance	F	—
F	3-dB Rolloff frequency	Hz	∞
T	Time delay	s	0.0
TDS	Drain–source time delay	s	0.0
GGS	Gate–source conductance	Ω^{-1}	0.0
CDG	Drain–gate capacitance	F	0.0
CDC	Dipole layer capacitance	F	0.0
CDS	Drain–source capacitance	F	0.0
GDS	Drain–source conductance	Ω^{-1}	0.0
RI	Channel resistance	Ω	0.0
RG	Gate resistance	Ω	0.0
RD	Drain resistance	Ω	0.0
RS	Source resistance	Ω	0.0
CGE	External gate capacitance	F	0.0
CDE	External drain capacitance	F	0.0
LG	Gate lead inductance	H	0.0
LD	Drain lead inductance	H	0.0
LS	Source lead inductance	H	0.0
CGDE	External gate–drain capacitance	F	0.0
GDG	Gate–drain conductance	Ω^{-1}	0.0
TJ	Chip temperature	K	298
	Package Parasitics		
LGB	Gate wirebond inductance	H	0.0
LDB	Drain wirebond inductance	H	0.0
LSB	Source wirebond inductance	H	0.0
CGSB	Gate bondpad-to-source capacitance	F	0.0
CDSB	Drain bondpad-to-source capacitance	F	0.0
CGSP	Gate-to-source package capacitance	F	0.0
CDSP	Drain-to-source package capacitance	F	0.0
CGDP	Gate-to-drain package capacitance	F	0.0
ZGT	Gate transmission line impedance	Ω	50
ZDT	Drain transmission line impedance	Ω	50
ZST	Source transmission line impedance	Ω	50
LGT	Gate transmission line length for $\varepsilon_r = 1$	m	0.0
LDT	Drain transmission line length for $\varepsilon_r = 1$	m	0.0
LST	Source transmission line length for $\varepsilon_r = 1$	m	0.0
FC	Corner frequency of flicker $(1/f)$ noise[b]	Hz	10 MHz
FCP	Shape factor of the $1/f$ noise response		1.0
Label	User-defined term that refers to temperature coefficient		

[a] The transconductance of this model may be approximately described by

$$g_m = G \frac{e^{-j\omega T}}{1 + jf/F_b}$$

where $\omega = 2\pi f$, f = frequency and F is 3-dB rolloff frequency.
[b] The flicker noise frequency dependence is given by $1/(f/F_c)^{\text{FCP}}$.
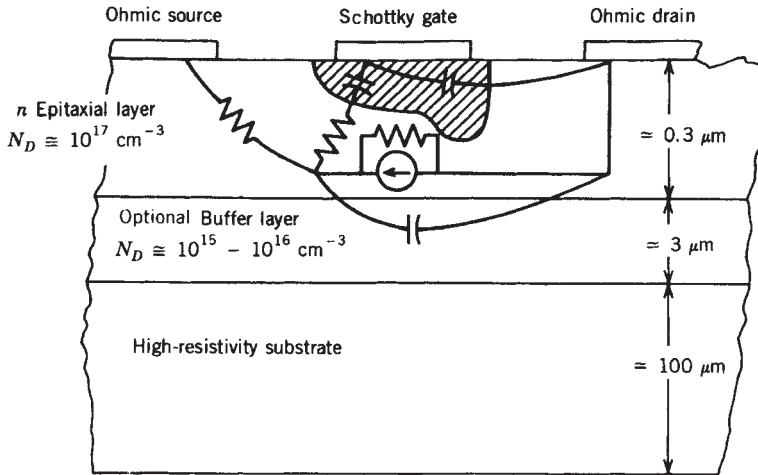
FIGURE 3.95   GaAs MESFET cross section.

TABLE 3.23   Characteristics of Bipolar Transistor MESFET

Property	Common-Emitter Bipolar	Common-Source MESFET
Geometry	Vertical	Horizontal
Modulation	Base current	Gate voltage
Control signal	Current	Voltage
Frequency limitation	Base length	Gate length
Low-frequency transconductance	High	Low

For the simplified model, the short-circuit current gain is

$$h_{21} = \frac{I_{\text{out}}}{I_{\text{in}}} = \frac{g_{m0}v_c}{I_{\text{in}}} \tag{3.218}$$

$$I_{\text{in}} = \frac{V_{\text{in}}}{R_c + 1/j\omega C_{gs}} \tag{3.219}$$

At low frequencies,

$$I_{\text{in}} \simeq V_{\text{in}}\,j\omega C_{gs} \simeq v_c\,j\omega C_{gs} \tag{3.220}$$

$$h_{21} \simeq \frac{g_{m0}}{j\omega C_{gs}} \tag{3.221}$$

$$|h_{21}| = \frac{f_t}{f} = \frac{g_{m0}}{2\pi C_{gs}}\frac{1}{f} \tag{3.222}$$

Thus the frequency where the short-circuit current gain becomes unity is

$$f_t = \frac{g_{m0}}{2\pi C_{gs}} \tag{3.223}$$
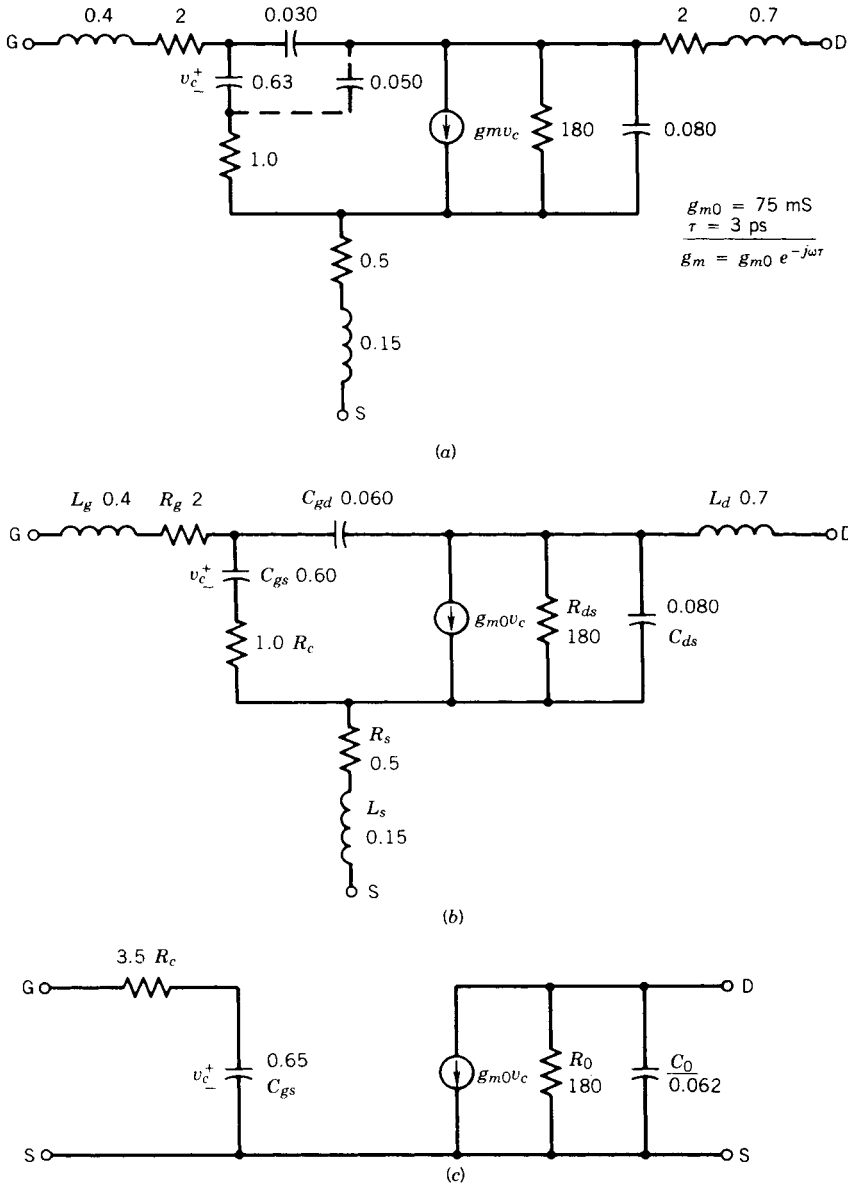
FIGURE 3.96 GaAs MESFET small-signal model (AT-8251): (*a*) complete model; (*b*) simple model; (*c*) simplified model, $V_{DS} = 5$ V, $Z = 500$ μm; $I_{DS} = 50$ mA, $L_G = 0.3$ μm.

which is an important figure of merit for the GaAs MESFET. The unilateral gain of the FET may be simply calculated from the y parameters in Figure 3.96:

$$y_{11} = \frac{1}{R_c + 1/j\omega C_{gs}} \tag{3.224}$$

$$y_{21} = g_{m0} \tag{3.225}$$

$$y_{22} = 1/R_0 + j\omega C_0 \qquad (3.226)$$

$$y_{12} = 0 \qquad (3.227)$$

$$U = \frac{|y_{21}|^2}{4 \, \text{Re}(y_{11}) \, \text{Re}(y_{22})} \qquad (3.228)$$

$$U = \frac{1}{4} \frac{1}{f^2} \left(\frac{g_{m0}}{2\pi C_{gs}} \right)^2 \frac{R_0}{R_c}$$

$$= (f_{\max}/f)^2 \qquad (3.229)$$

Thus $f_{\max}$ is given by

$$f_{\max} = \frac{f_t}{2} \sqrt{\frac{R_0}{R_c}} \qquad (3.230)$$

A high-gain FET requires a high f_t, a high output resistance, a low input resistance, and minimum parasitic elements. Under normal bias conditions the device is biased for maximum drift velocity of the electron carriers (about 3 kV/cm), so we have

$$f_t = \frac{g_{m0}}{2\pi C_{gs}} = \frac{1}{2\pi \tau} = \frac{v_s}{2\pi L_g} \qquad (3.231)$$

This equation shows the importance of short gate length L_g. Another interesting figure of merit for the FET is the g_{m0} per unit gate periphery (Z), given by

$$C_{gs} = \frac{\varepsilon A}{d} = \varepsilon \frac{L_g Z}{d} \qquad (3.232)$$

$$g_{m0} = \frac{v_s C_{gs}}{L_g} = \frac{v_s \varepsilon Z}{d} \qquad (3.233)$$

$$\frac{g_{m0}}{Z} = \frac{v_s \varepsilon}{d} \qquad (3.234)$$

For a typical ($Z = 500\text{-}\mu\text{m}$ gate) FET, this parameter is

$$\frac{g_{m0}}{Z} \simeq \frac{2 \times 10^7 \text{ cm/s} \ 10^{-12}\text{F/cm}}{0.13 \ \mu\text{m}}$$

$$= 150 \ \mu\text{S}/\mu\text{m} = 150 \text{ mS/mm}$$

$$g_{m0} \simeq 150 \times 0.50 = 75 \text{ mS}$$

which is in good agreement with measurements. Scaling the device larger in Z increases the transconductance, but the f_t and gain remain constant with scaling if parasitics are negligible. The g_{m0} is about a factor of 6 higher than a silicon MOSFET [3.2, 3.4] with an oxide thickness of 650 Å.

The velocity saturating effect of the GaAs MESFET has several interesting consequences. Referring to Figure 3.97, we see that the channel can be considered to be two regions: a low-field region with a constant number of carriers and a high-field region
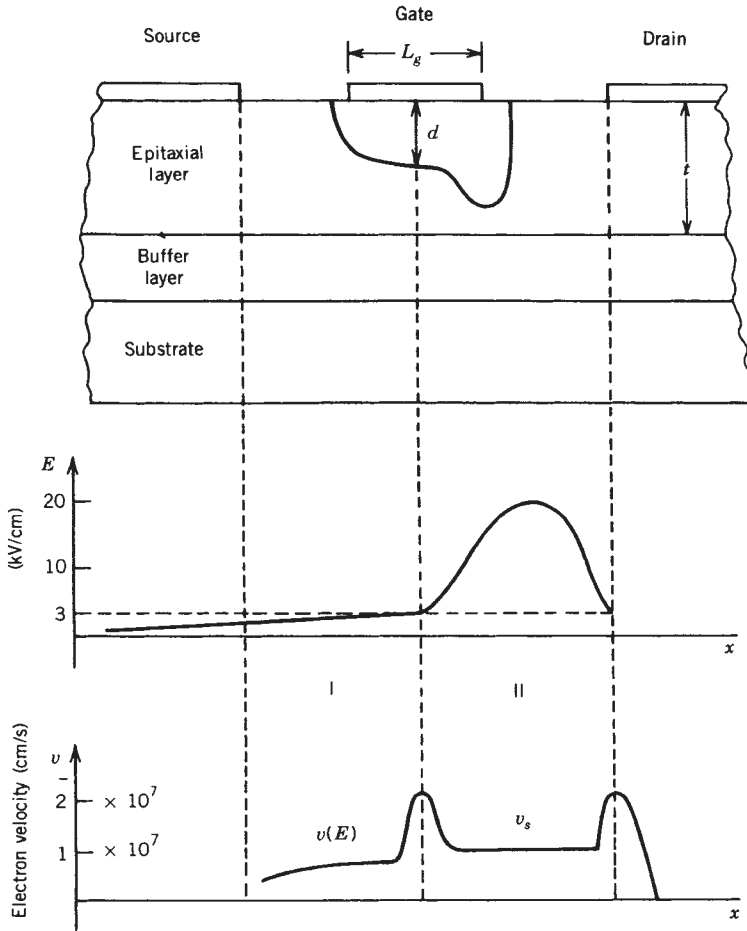
FIGURE 3.97   GaAs MESFET at high electric field. (From Ref. 3.59 © IEEE 1976.)

with a "constant" velocity, which is discussed later. Since the current continuity is required,

$$I_{DS}/A = qn(x)v(x) \tag{3.235}$$

where

$$n(x)_{\max} = N_D \qquad v(x)_{\max} = v_{\text{sat}} = v_s$$

the number of carriers must increase above N_D in region II. This causes an electron accumulation at the drain edge of the channel followed by an electron depletion. In effect, a charge dipole occurs at the drain edge of the channel, which is a very small capacitive effect in the model ($\simeq 0.05$ pF in Fig. 3.96).

In GaAs, the electron carriers will slow down at an electric field greater than 3 kV/cm. The electrons move from a high-mobility state to a low-mobility state in about 1 ps, and thus the velocity of the carriers reaches a peak and slows down in the
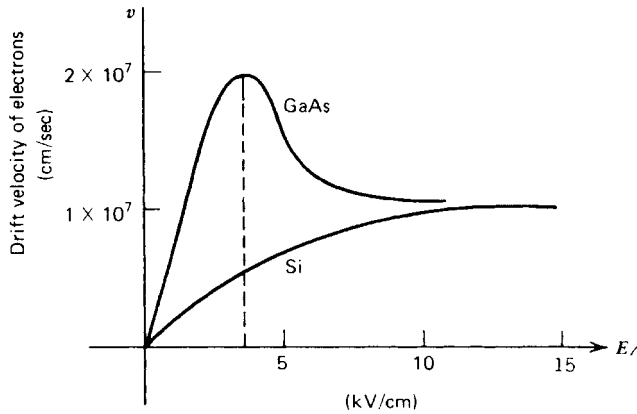
FIGURE 3.98   Equilibrium electron drift velocity versus electric field.

middle of the channel. The velocity versus electric field of GaAs and silicon is shown in Figure 3.98. The change in velocity of the carriers in GaAs is the cause of the Gunn effect in Gunn diodes or TEOs (transfer electron oscillators).

In short-channel devices (less than 3 μm), a nonequilibrium velocity field characteristic must be considered. When the electrons enter the high-field region, they are accelerated to a higher velocity. This effect can cause peak velocities of about 4×10^7 cm/s, which relax to 1×10^7 cm/s after traveling about 0.5 μm. The overshoot in velocity reduces the transit time and shifts the dipole charge to the right of the channel.

An estimate of the drain current I_{DSS} can be made using (3.235). For a small-signal GaAs MESFET with

$$N_D \simeq 2 \times 10^{17} \text{ cm}^{-3}$$

$$v_{\text{sat}} = 2 \times 10^7 \text{ cm/s}$$

$$A = Z(t - d) = Z(0.03)(10^{-4}) \text{ cm}^2$$

$$\frac{I_{DSS}}{A} = qN_D v_{\text{sat}} = 1.6 \times 10^{-19} \times 2 \times 10^{17} \times 2 \times 10^7 = 6.4 \times 10^5 \text{A/cm}^2$$

$$\frac{I_{DSS}}{Z} = (0.3)(6.4) \text{ A/cm} \simeq 200 \text{ mA/mm}$$

which is in good agreement with measurements.

The high-frequency gain of the GaAs MESFET is maximized by achieving the minimum gate length without introducing excessive device parasitics. Computer studies have shown that the R_G series gate resistance increases and R_0 decreases as the gate length is shortened. The practical limit is $L_g/t > 1$, which implies a thin channel and therefore higher channel doping. As a result of breakdown considerations, the maximum channel doping is 4×10^{17} cm^{-3}, and about 2×10^{17} cm^{-3} in practical devices. Thus modern 0.3-μm gate GaAs MESFETs are probably within a factor of 3 of the highest f_{max} that can be achieved from the present device structure.

Evaluating $f_{\max}$ for the device shown in Figure 3.96 gives

$$f_t = \frac{0.075}{2\pi(0.60)} = 20 \text{ GHz}$$

$$f_{\max} = \frac{20}{2}\sqrt{\frac{180}{3.5}} = 72 \text{ GHz}$$

These frequencies are typical of modern 0.3-μm GaAs MESFETS.

The small-signal models of several GaAs MESFET chips are given in Table 3.24. The perimeter of the transistor will determine the output power capability and the maximum frequency of broadband gain. The low-frequency (LF) broadband gain is given by

$$S_{21}(\text{LF}) = -2g_m Z_0 \tag{3.236}$$

which indicates that high gain requires a large gate perimeter for a large transconductance. The smaller perimeter devices provide more gain at higher frequency because the gate fingers are shorter (less phase shift) and the input capacitance C_{gs} is smaller.

The selection of a low-noise transistor is also based on the transistor perimeter. Above 12 GHz, a gate perimeter less than 250 μm is needed for a minimum noise figure [3.81] and high gain. At 4 GHz, a 500-μm perimeter is recommended and at 2 GHz a 750-μm perimeter would usually give best noise figure and gain performance.

The dual-gate GaAs MESFET is simply two adjacent gates with a cascade connection normally used [common source (CS) followed by common gate (CG)]. The cross section in Figure 3.99 is typical of the dual-gate transistor. The second gate can be used for automatic gain control (AGC) by varying the dc voltage at gate 2. As an amplifier, the dual-gate FET has higher gain with gate 2 RF grounded.

The dual-gate FET is also called a cascode [3.82] from the vacuum-tube prototype. From investigation of two device pairs with nine possibilities, the CS (cathode) CG (grid) combination was found to have the lowest noise figure and was given the name cascode, which has continued to be used for the bipolar common-emitter and common-base pair, the FET common-source and common-gate pair, and the dual-gate GaAs MESFET, where the second gate is assumed to be at RF ground in the cascode connection. Since this device is simple to dc bias and has a low noise figure with

TABLE 3.24   GaAs MESFET Chip Models from Avantek

Name and Bins	L_g (nH)	L_d (nH)	L_s (nH)	R_c (Ω)	R_g (Ω)	R_s (Ω)	R_{ds} (Ω)	C_{gs} (pF)	C_{gd} (pF)	C_{ds} (pF)	g_{m0} (mS)	Z (μm)
AT-10600, $Z = 250$ μm												
3 V, 10 mA	0.6	0.7	0.15	2	5	5	275	0.16	0.03	0.06	27	250
5 V, 30 mA	0.6	0.7	0.15	2	5	5	275	0.26	0.015	0.06	42	250
AT-8251, $Z = 500$ μm												
3 V, 20 mA	0.4	0.7	0.15	2	2.5	1	150	0.36	0.07	0.16	48	500
5 V, 50 mA	0.4	0.7	0.15	1	2	0.5	180	0.60	0.06	0.08	75	500
AT-8111, $Z = 750$ μm												
3 V, 20 mA	0.4	0.5	0.15	1.5	1.5	1	180	0.70	0.10	0.14	68	750
5 V, 80 mA	0.4	0.5	0.15	1	1	0.5	180	1.2	0.08	0.15	115	750
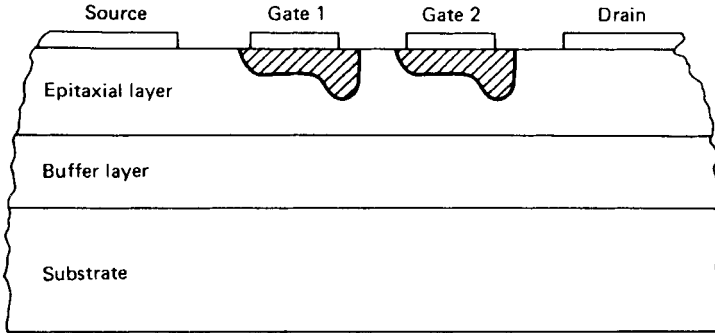
FIGURE 3.99   Dual-gate GaAs MESFET cross section.

high gain, it continues to be useful for many amplifier applications. In addition, the dual-gate FET can be used for mixers, multipliers, AGC amplifiers, and oscillators.

The dual-gate FET has an S_{11} similar to the common-source FET, an S_{22} similar to the common-gate FET, a very low S_{12} which is given by

$$S_{12} = \frac{(S_{12})_1 (S_{12})_2}{1 - (S_{22})_1 (S_{11})_2} \simeq 0 \tag{3.237}$$

and a high S_{21} given approximately by

$$S_{21} = \frac{(S_{21})_1 (S_{21})_2}{1 - (S_{22})_1 (S_{11})_2} \tag{3.238}$$

The effective transductance is given by

$$g_m = y_{21} = \frac{-(y_{21})_1 (y_{21})_2}{(y_{22})_1 + (y_{11})_2} \simeq g_{m1} \tag{3.239}$$

In dual-gate amplifier or oscillator applications, the two-port S parameters can be used in the same manner as the single-gate GaAs FET; usually, the second gate is at RF ground for this two-port measurement.

Low-Frequency Noise   For the FET, the low-frequency equivalent circuit is given in Figure 3.100. The noise is caused by traps in the gate-channel depletion layer [3.83], traps in the substrate, and possibly surface states created by the passivation [3.84]. Much higher $1/f$ noise occurs in MOSFETs because of the traps in the oxide [3.85]. The noise power referred to the input becomes

$$P_{ni} \simeq e_n^2 / 200 = P_0 / G \qquad (r_s = 0) \tag{3.240}$$

Since the noise is voltage noise, the data are usually plotted in dBV/$\sqrt{\text{Hz}}$ (Figure 3.101).

Both sets of data have been plotted as noise power in Figure 3.102 to demonstrate the superior, much lower, corner frequency for the silicon bipolar transistor. These data are representative of microwave transistor noise at low frequencies but are very
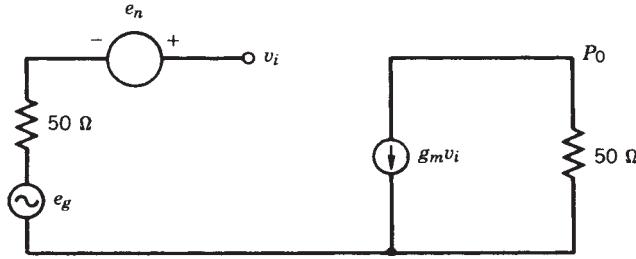
FIGURE 3.100   Low-frequency noise equivalent circuit of FET.
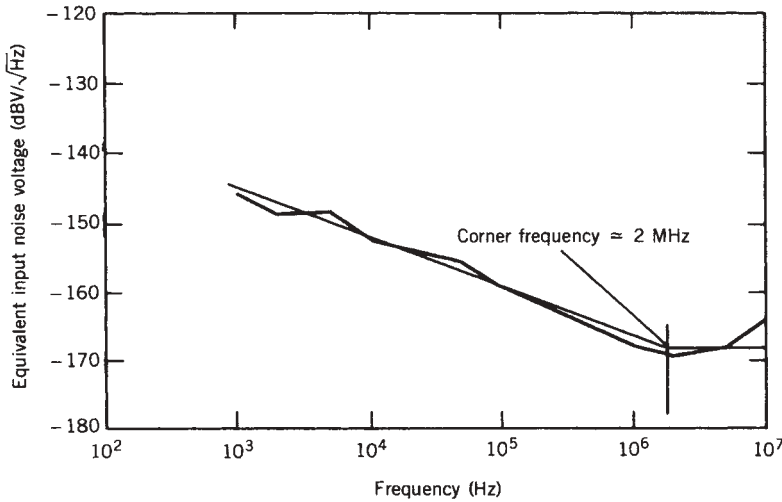
FIGURE 3.101   Equivalent input noise voltage versus frequency for AT-10600 GaAs MESFET at $V_{DS} = 3$ V, $I_D = 40$ mA [3.48].

dependent on the process for making the transistors. As improvements are found, the corner frequencies should continue to decrease.

Note that straight-line approximations of device low-frequency noise are rarely accurate. Since most of the observed noise is due to discrete traps (which have a noise spectrum like a first-order low-pass filter), the device noise spectrum varies about the $1/f$ line. As MESFETs are cooled, the discrete trap frequencies are more apparent.

Finally, to summarize the noise performance of GaAs MESFETs and silicon bipolar transistors, the minimum noise figure of these transistors has been plotted in Figure 3.103 for room temperature. The GaAs MESFETs will dominate the microwave region, but silicon bipolars will continue to find applications, especially for low-noise oscillators.

3.5.3   HEMT

By using heterojunction semiconductor material, AlGaAs interfacing with GaAs, a new field-effect microwave semiconductor device can be manufactured with superior microwave performance. This device is the MODFET, which is also called a HEMT,
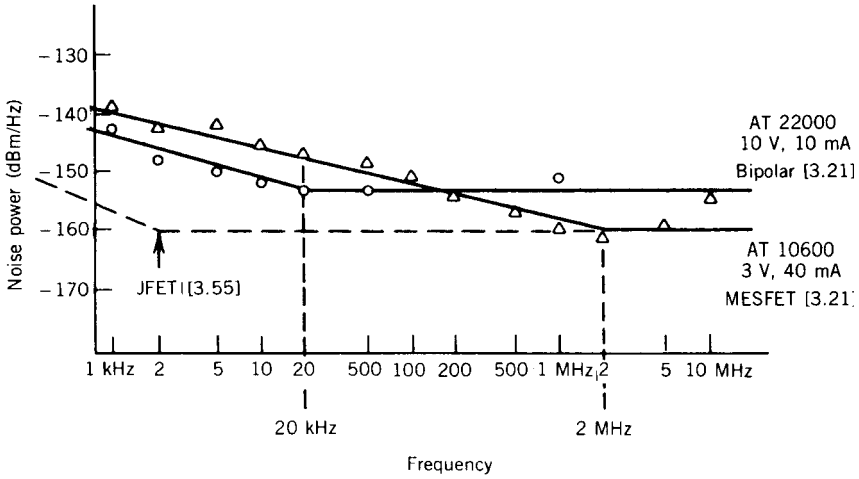
FIGURE 3.102   The $1/f$ noise for microwave transistors [3.48].
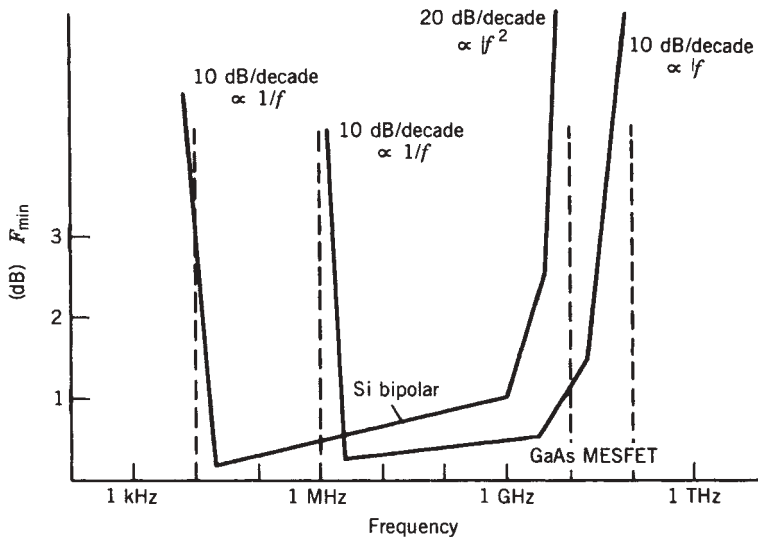
FIGURE 3.103   The F_{min} versus frequency for low-noise silicon bipolar transistor and low-noise GaAs FET.

a SDHT (selectively doped heterostructure transistor), or a TEGFET (two-dimensional electron gas FET); the cross section of this transistor is given in Figure 3.104 [3.86].

The basic properties of the heterojunction can be understood from the difference in energy gap between the two materials, which causes band bending, resulting in an electron gas with high electron mobility in the undoped GaAs provided by the donors in the AlGaAs. The band bending results in a quantum well where a large population of electrons forms a two-dimensional gas which can easily be modulated by the gate voltage. This is analogous to an n-channel MOSFET, where the number of conduction
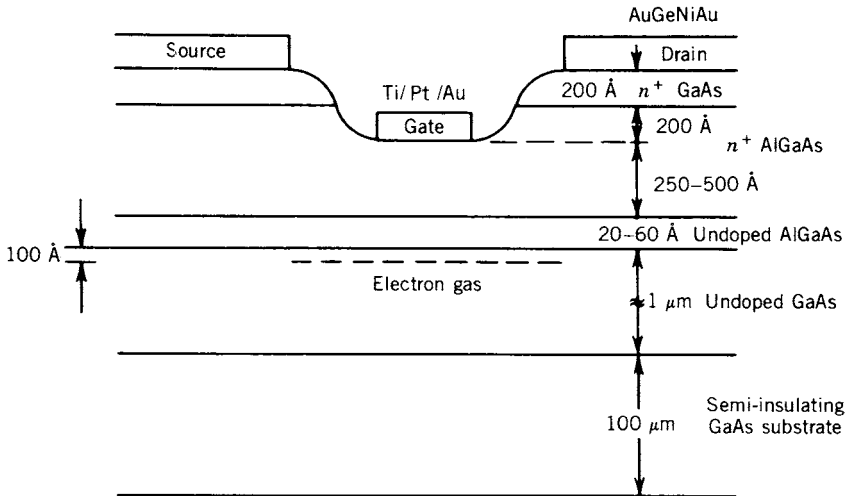
FIGURE 3.104 HEMT structure.

electrons in the channel is controlled by the gate voltage. Since the band bending forces the electrons to be resident in the undoped GaAs layer, the electrons exhibit a very high mobility and high v_s even at room temperature, which accounts for the superior microwave performance.

The structure of the MODFET can be explained by treating the region beneath the gate metal and the GaAs buffer layer (Fig. 3.104). If the width of the n^+ AlGaAs donor layer is very thin ($\sim$250 Å), the depletion layer below the Schottky gate metal will extend into the undoped GaAs electron gas and interrupt the electron gas; this gives an enhancement-mode FET, since no channel flows if $V_{GS} = 0$ (a positive V_{GS} is needed). If the n^+ AlGaAs donor layer is thicker ($\sim$500 Å), the depletion region only reaches the undoped AlGaAs layer, which is also depleted; this gives a depletion-mode FET. The voltage V_{GS} will modulate the population of electrons in the quantum well and therefore the I_{DS} of the FET. Since the electrons travel in an undoped GaAs region with few ionized donors, the mobility and v_s are larger for this structure compared to a normal GaAs FET with $N_D \simeq 10^{17}$ cm^{-3}.

The output power of this structure is limited by the sheet carrier concentration of about 10^{12} electrons/cm^2, which limits the maximum output current. A technique for raising the sheet concentration is the use of multiple heterojunctions to form series superlattice structures. As an example, a four-layer MODFET gave about three times the output power of the comparable single-layer MODFET at 10 GHz [3.87].

Table 3.25 shows the optimum operation points of bipolar and MESFETs for low noise, high gain class B operation Figure 3.105 shows the PC characteristics of bipolar Transistors and FETS.

3.5.4 Foundry Services

In Chapter 2 we gave an overview of the passive components found in planar circuits, specifically, used on GaAs or other substrate material. In this chapter we have dealt with active three-terminal devices, both bipolar and field-effect transistors.

TABLE 3.25   Transistor Bias Points

Application	Si Bipolar (AT-41400)	GaAs MESFET($I_{DSS} = 100$ mA) (AT-8251)
Low noise	$V_{CE} = 8$ V, $I_{CE} = 10$ mA	$V_{DS} = 3$ V, $I_{DS} = 20$ mA
High gain	$V_{CE} = 8$ V, $I_{CE} = 50$ mA	$V_{DS} = 3$–5 V, $I_{DS} = 100$ mA
High output power and low distortion	$V_{CE} = 8$ V, $I_{CE} = 25$ mA	$V_{DS} = 5$–7 V, $I_{DS} = 50$ mA
Class B	$V_{CE} = 10$ V, $I_{CE} = 0$ (with $P_{in} = 0$)	$V_{DS} = 8$ V, $I_{DS} = 0$ (with $P_{in} = 0$)
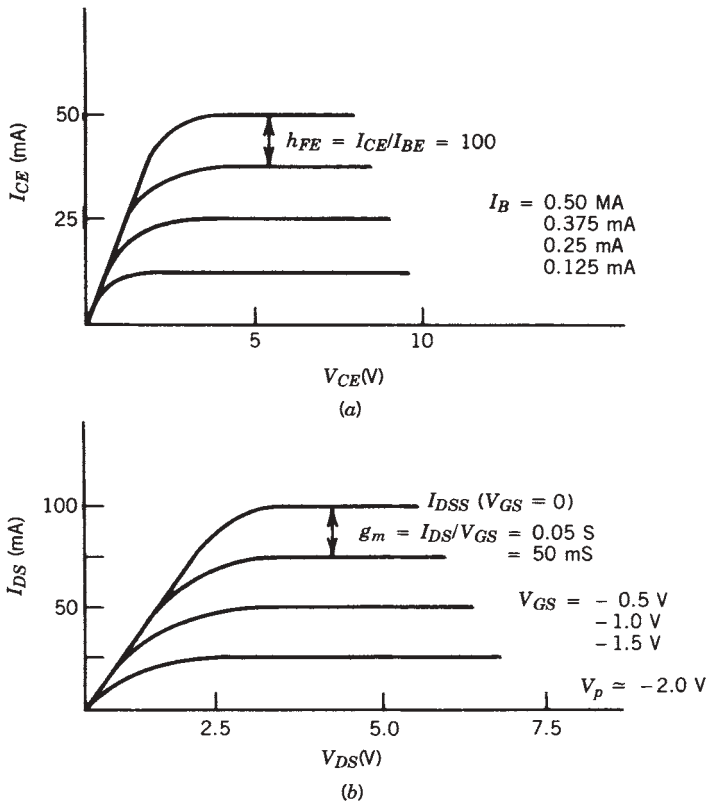
FIGURE 3.105 The dc characteristics of (*a*) a silicon bipolar transistor (AT-41400) and (*b*) GaAs MESFET (AT-8251).

In designing a microwave circuit, which will be built on a material such as GaAs, one needs to go to a GaAs alternative silicon or silicon germanium foundry. The foundries seem to be very secretive about their information, and the first experience with a foundry is a shock because one needs to sign a nondisclosure agreement and pay up to $5000 to obtain a foundry manual. These foundry manuals are somewhat unique to each foundry and vary. The foundry supplies information about passive and active structures as well as interconnect information. The following is an example of

a foundry manual which was put together from information from various foundries. It does not apply to a particular foundry but is generic in its contents. In the area of passive components, typically a variety of inductor cells are recommended: the same applies to spiral inductors/rectangular inductors and interconnect components such as bends, tees, crosses, and other components as outlined in Chapter 2 and further described in Chapter 13.

Example: Foundry Design Manual

1.0 Technology Overview
    1.1 Typical Applications
    1.2 Components
        1.2.1 Transistors
        1.2.2 Diodes
        1.2.3 Resistors
        1.2.4 MIM capacitors
        1.2.5 Inductors and other metal structures
    1.3 Interconnects
    1.4 Substrate Vias
    1.5 Chip and Reticle Dimensions
        1.5.1 Chip thickness
        1.5.2 Chip size and orientation
        1.5.3 Reticle size
    1.6 Process Control Monitor Size and Placement
2.0 Design Layout Rules
    2.1 Process Flow and Mask Level Description
        2.1.1 Step 1: Defining active areas
        2.1.2 Step 2: Active device contacts
        2.1.3 Step 3: Metal 0 interconnect
        2.1.4 Step 4: MIM capacitor
        2.1.5 Step 5: First-layer interlayer dielectric
        2.1.6 Step 6: Metal 1 interconnect
        2.1.7 Step 7: Metal 2 interconnect
    2.2 Layout Definitions
        2.2.1 Intrusion: inclusion; extension; exclusion
        2.2.2 Closed structures
        2.2.3 Layer-to-layer contacts
        2.2.4 Labeling
    2.3 Circuit Element Layout Rules
        2.3.1 Heterojunction bipolar transistors
        2.3.2 Bias heterojunction bipolar transistor
        2.3.3 Gate contacts
        2.3.4 Single-Gate MESFETs
        2.3.5 Double-Gate MESFETs
        2.3.6 Single-Gate MESFETs with merged drain and/or source
        2.3.7 Overlap Schottky diodes
        2.3.8 Implanted resistors
        2.3.9 NiCr thin-film resistors
        2.3.10 Spiral inductors

Example for the Use of the Foundry   The examples in Figures 3.106 and 3.107 are simple cases for foundry use and have been done with the TriQuint Foundry service. Figure 3.106 shows the layout of a simple LO medium-power amplifier. The input is
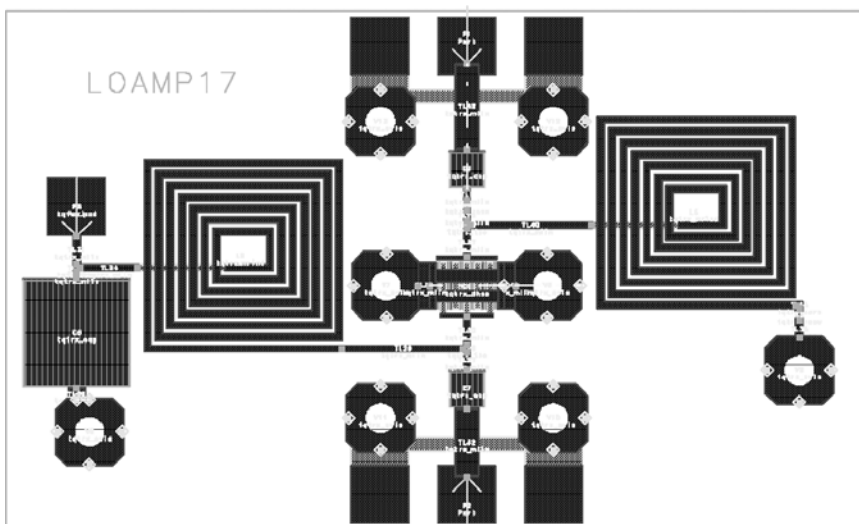
FIGURE 3.106   Layout of Star Mixer with four FETs switching to ground. The left lower corner contains the local oscillator (LO) amplifier. The RF input occurs in the middle of the transformer on the left, and because of a very low IF frequency, a huge transformer, as shown on the right, is needed. It may be a better decision to use an external transformer, but this was an experiment, again built around the TriQuint Foundry, to evaluate the mixer performance.
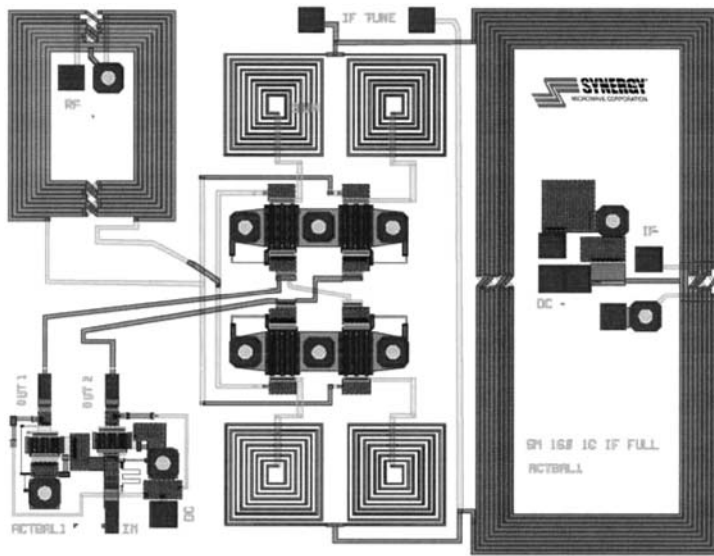
FIGURE 3.107   MMIC for star mixer using TriQuint foundry.

50 Ω; the output will drive the double-balanced mixer. The input of the amplifier is on the top. The center pad is the RF input, and the pads left and right are at ground. The signal travels via a capacitor to the gate, which is grounded via a rectangular inductor and a small resistor. On the drain side, we have a similar inductor as an RF choke. The output is grounded via a larger capacitor. The drain voltage is applied to the square pad. The output from the drain is also available via a capacitor and a similar output terminal with two grounds. It is noteworthy to look at the sizes. The inductors determine most of the space followed by one large capacitor and the transistor. Since the cost is determined by the surface area, higher frequencies would mean lower cost.

As outlined above, there are much more complex foundry models and interconnects available. Some of them were described in Chapter 2, and the following chapters will show their application.

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PROBLEMS

3.1 Using a bipolar low-frequency hybrid-Π model, show that the 50-Ω gain is

$$S_{21}(\text{LF}) = \frac{-2\, Z_0 g_m r_\pi}{r_b + r_\pi + Z_0}$$
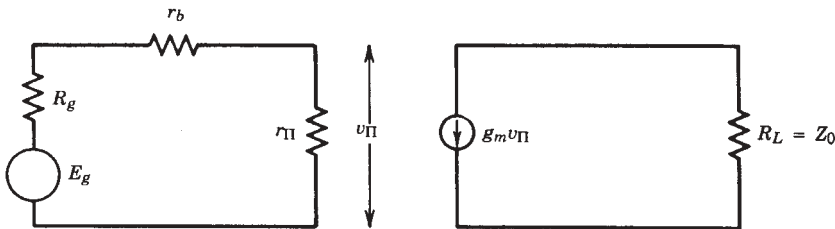
Estimate this gain for the AT-41400 model in decibels.

3.2 From a low-frequency model of the GaAs FET, show that the 50-Ω gain is

$$S_{21}(LF) = -2g_m Z_0$$
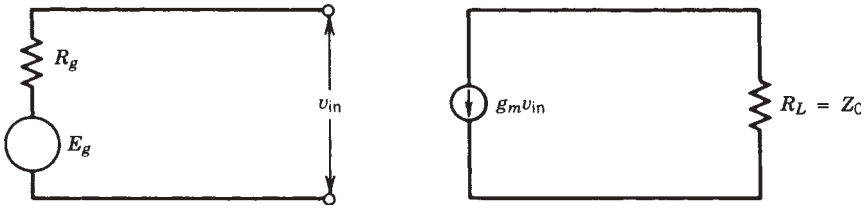
(*Note:* For an open-circuit line, $|v_{\text{in}}| = 2|E_g|$.) Estimate this gain for the transistors given in Table 3.15 at the high gain bias in decibels.

3.3 Derive the S parameters of the following FET model (omiting L_g, L_s, L_d) for $\tau_d = 0$ at $f = 4$ GHz:
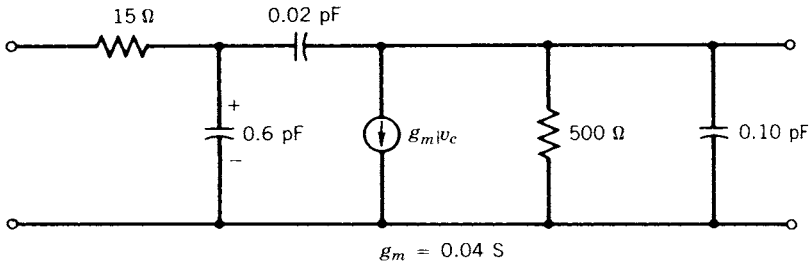
CHAPTER 4

TWO-PORT NETWORKS

4.1 INTRODUCTION

This chapter describes some of the tools needed for RF/microwave design, including two-port parameters, the three-port parameters, the four-port parameters required for differential two-port S parameters, the noise parameters, the power gains for a two-port, and the properties of twisted-wire pairs for circuit design. The dc biasing of amplifiers or oscillators is described at the beginning of Chapter 8. *Small signal* implies the ac signals are much smaller than the dc bias parameters, so linear two-port parameters such as S parameters may be used for the design. *Linear* implies that if the input power doubles, the output power doubles, that is, the gain is constant with input power level. Eventually a nonlinear analysis is needed to evaluate the large-signal performance of the circuit, which must saturate at some output power level. The temperature effects of the small-signal design must also be evaluated in the linear and nonlinear modes.

The basic small-signal two-port design of amplifiers and oscillators is shown in Figure 4.1 [4.1], which will be explained in detail further in this chapter. Basically, the amplifier is simultaneously matched at both ports if this is possible, that is if $k > 1$, the stability factor. If $k < 1$, where k will be defined in Eq. (4.7), an amplifier design is still possible, but the location of Γ_G and Γ_L must be located in the stable regions, as determined by stability circles [4.1]. In other words, the input and output ports may be mismatched, but the gain is still very good. The oscillator uses the same transistors mounted in a configuration where $k < 1$. Then the circuit is resonated at one port (M_3) and matched for oscillation at the other port (M_4). Further details will follow.

4.2 TWO-PORT PARAMETERS

A two-port network may be characterized by several equivalent parameter sets given in Table 4.1. A particular set may be more useful, depending on the interconnections of the two-ports. For example, if the two-ports are cascaded as a chain, the *ABCD* matrix is the simplest representation of the total circuit. Designers frequently use *ABCD* parameters for passive networks and *S* parameters for active components. The *Z* parameters are used when two-ports are put in series, for example, common-lead inductance of a transistor. The *Y* parameters are used when two-ports are put in parallel, for example, a parallel capacitance from base to collector. The hybrid, or *H*, parameters (named hybrid since the units of each parameter are different) are used for transistors since h_{21} is a good representation of the current gain of a BJT, $\alpha = 0.99$ for a typical microwave common-base (CB) transistor, and $\beta = 100$ for a typical microwave common-emitter transistor. The frequency where $|h_{21}| = 1$ for the common emitter (CE) or common source (CS) transistor is the ft of the transistor, an important figure-of-merit. The data sheets usually give the CE or CS *S* parameters versus bias and frequency from a calibrated network analyzer, since this configuration gives the highest gain and best stability. A plot of CE current gain versus frequency is given in Figure 4.2 for a typical common-emitter BJT; similar plots are possible for FETs.

An example of the application of *ABCD* parameters to passive networks is the design of resistive tee attenuators, as shown in Figure 4.3. The *ABCD* matrix for this circuit
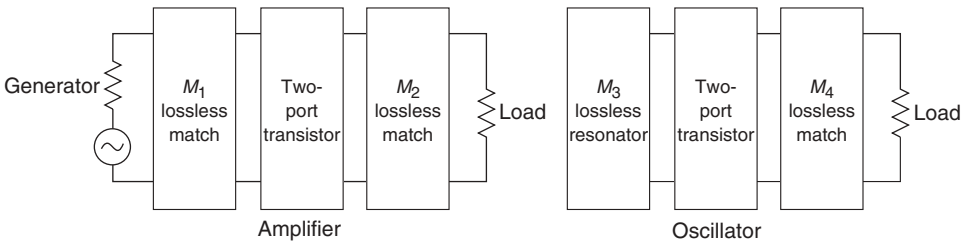
FIGURE 4.1   Amplifier and oscillator diagrams.
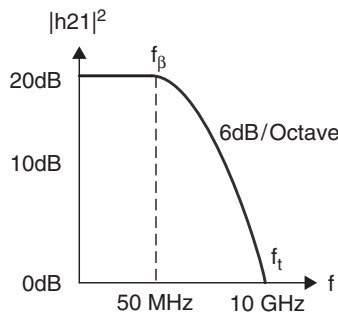
FIGURE 4.2 $|h_{21}|$ versus f for CE BJT versus frequency.

TABLE 4.1 Two-Port Parameters: $Z_0 = 1$ with $\Delta^K = K_{11}K_{22} - K_{12}K_{21}$

	S	z	y	h	A
S	$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}\begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$	$S_{11} = \dfrac{(z_{11}-1)(z_{22}+1)-z_{12}z_{21}}{(z_{11}+1)(z_{22}+1)-z_{12}z_{21}}$ $S_{12} = \dfrac{2z_{12}}{(z_{11}+1)(z_{22}+1)-z_{12}z_{21}}$ $S_{21} = \dfrac{2z_{21}}{(z_{11}+1)(z_{22}+1)-z_{12}z_{21}}$ $S_{22} = \dfrac{(z_{11}+1)(z_{22}-1)-z_{12}z_{21}}{(z_{11}+1)(z_{22}+1)-z_{12}z_{21}}$	$S_{11} = \dfrac{(1-y_{11})(1+y_{22})+y_{12}y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$ $S_{12} = \dfrac{-2y_{12}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$ $S_{21} = \dfrac{-2y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$ $S_{22} = \dfrac{(1+y_{11})(1-y_{22})-y_{12}y_{21}}{(1+y_{11})(1+y_{22})-y_{12}y_{21}}$	$S_{11} = \dfrac{(h_{11}-1)(h_{22}+1)-h_{12}h_{21}}{(h_{11}+1)(h_{22}+1)-h_{12}h_{21}}$ $S_{12} = \dfrac{2h_{12}}{(h_{11}+1)(h_{22}+1)-h_{12}h_{21}}$ $S_{21} = \dfrac{-2h_{21}}{(h_{11}+1)(h_{22}+1)-h_{12}h_{21}}$ $S_{22} = \dfrac{(1+h_{11})(1-h_{22})+h_{12}h_{21}}{(h_{11}+1)(h_{22}+1)-h_{12}h_{21}}$	$\dfrac{A+B-C-D}{A+B+C+D} \quad \dfrac{2(AD-BC)}{A+B+C+D}$ $\dfrac{2}{A+B+C+D} \quad \dfrac{-A+B-C+D}{A+B+C+D}$
Z	$z_{11} = \dfrac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$ $z_{12} = \dfrac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$ $z_{21} = \dfrac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$ $z_{22} = \dfrac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}\begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$	$\dfrac{y_{22}}{\Delta^y} \quad \dfrac{-y_{12}}{\Delta^y}$ $\dfrac{-y_{21}}{\Delta^y} \quad \dfrac{y_{11}}{\Delta^y}$	$\dfrac{\Delta^h}{h_{22}} \quad \dfrac{h_{12}}{h_{22}}$ $\dfrac{-h_{12}}{h_{22}} \quad \dfrac{1}{h_{22}}$	$\dfrac{A}{C} \quad \dfrac{\Delta^A}{C}$ $\dfrac{1}{C} \quad \dfrac{D}{C}$
Y	$y_{11} = \dfrac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$ $y_{12} = \dfrac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$ $y_{21} = \dfrac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$ $y_{22} = \dfrac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\dfrac{z_{22}}{\Delta^z} \quad \dfrac{-z_{12}}{\Delta^z}$ $\dfrac{-z_{11}}{\Delta^z} \quad \dfrac{z_{11}}{\Delta^z}$	$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$	$\dfrac{1}{h_{11}} \quad \dfrac{-h_{12}}{h_{11}}$ $\dfrac{h_{21}}{h_{11}} \quad \dfrac{\Delta^h}{h_{11}}$	$\dfrac{D}{B} \quad \dfrac{-\Delta^A}{B}$ $\dfrac{-1}{B} \quad \dfrac{A}{B}$

$$h_{11} = \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}$$

$$h_{12} = \frac{2S_{12}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}$$

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}$$

$$h_{22} = \frac{(1-S_{22})(1-S_{11}) - S_{12}S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}$$

$$A = \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{2S_{21}}$$

$$B = \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{2S_{21}}$$

$$C = \frac{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}{2S_{21}}$$

$$D = \frac{(1-S_{11})(1+S_{12}) + S_{12}S_{21}}{2S_{21}}$$

$$\frac{\Delta^z}{z_{22}} \qquad \frac{z_{12}}{z_{22}}$$

$$\frac{-z_{11}}{z_{22}} \qquad \frac{1}{z_{22}}$$

$$\frac{z_{11}}{z_{21}} \qquad \frac{\Delta^z}{z_{21}}$$

$$\frac{1}{z_{21}} \qquad \frac{z_{22}}{z_{21}}$$

$$\frac{1}{y_{11}} \qquad \frac{-y_{12}}{y_{11}}$$

$$\frac{y_{21}}{y_{11}} \qquad \frac{\Delta^y}{y_{11}}$$

$$\frac{-y_{22}}{y_{21}} \qquad \frac{-1}{y_{21}}$$

$$\frac{-\Delta^y}{y_{21}} \qquad \frac{-y_{11}}{y_{21}}$$

$$H \qquad \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$$\frac{-\Delta^h}{h_{21}} \qquad \frac{-h_{11}}{h_{21}}$$

$$\frac{-h_{22}}{h_{21}} \qquad \frac{-1}{h_{21}}$$

$$\frac{B}{D} \qquad \frac{\Delta^A}{D}$$

$$\frac{-1}{D} \qquad \frac{C}{D}$$

$$A \qquad \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

195
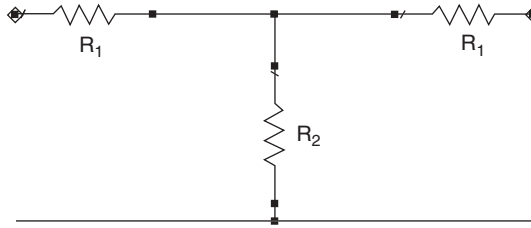
FIGURE 4.3   Resistive tee attenuator.

is given by [4.2] Figure 4.3:

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & \dfrac{R_1}{Z_0} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \dfrac{Z_0}{R_2} & 1 \end{bmatrix} \begin{bmatrix} 1 & \dfrac{R_1}{Z_0} \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 + \dfrac{R_1}{R_2} & 2\dfrac{R_1}{Z_0} + \dfrac{R_1{}^2}{R_2 Z_0} \\ \dfrac{Z_0}{R_2} & 1 + \dfrac{R_1}{R_2} \end{bmatrix}
\tag{4.1}
$$

In order for $S_{11} = 0$, $A + B/Z_0 = C/Y_0 + D$, so

$$
\frac{R_2}{Z_0} = \frac{1 - (R_1/Z_0)^2}{2\dfrac{R_1}{Z_0}}
\tag{4.2}
$$

The attenuation is simply given by (see Table 4.2)

$$
L_T = 10 \log |C + D|^2 \qquad \text{(dB)}
\tag{4.3}
$$

which reduces to

$$
L_T = 20 \log \left(\frac{1 + R_1/Z_0}{1 - R_1/Z_0} \right)
\tag{4.4}
$$

Defining a voltage loss ratio $V_R = \text{antilog}(L_T/20) = 10^{L_T/20}$, we restate the above equation as

$$
\frac{R_1}{Z_0} = \frac{V_R - 1}{V_R + 1}
\tag{4.5}
$$

This is the final result, and typical values which follow from this analysis are summarized in Table 4.2 for some useful attenuators.

TABLE 4.2   Normalized Resistors for Tee Attenuator

L_T (dB)	V_R	R_1/Z_0	R_2/Z_0
0	1	0	∞
3	1.41	0.17	2.86
6	2	0.33	1.33
10	3.16	0.52	0.70
20	10	0.82	0.20

Returning to active two-ports, the block diagram of two-port oscillators and amplifiers was given in Figure 4.1. Both circuits deliver power to the 50-Ω load. The transistor must be dc biased at the recommended operating point where the *S* parameters are known. When the stability factor k is greater than unity, the ports may be simultaneously matched to the 50-Ω generator and load for the maximum available gain G_{ma} [4.1]:

$$G_{ma} = \left| \frac{S_{21}}{S_{12}} \right| [k - (k^2 - 1)^{1/2}] \tag{4.6}$$

$$k = \frac{1 + |D|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \tag{4.7}$$

$$D = S_{11}S_{22} - S_{21}S_{12} \tag{4.8}$$

A necessary and sufficient condition for unconditional stability is $k < 1$ and $|D| > 1$, where the second condition is almost always satisfied, so it is usually assumed to be true. If k is less than unity, amplifier design is still possible, but the generator and load impedances seen by the active transistor must be in the stable regions [4.1]. The gain is approximately the maximum stable gain

$$G_{ms} = \left| \frac{S_{21}}{S_{12}} \right| \tag{4.9}$$

The maximum stable gain is defined as the gain you would obtain if you add resistors to the network to make $k = 1$ and then simultaneously match both ports. In practice, it is not necessary to add resistance to the network since this will lower the gain. The G_{ms} is simply a goal that is possible to achieve when $k < 1$.

If the amplifier is a LNA, the input matching circuit is designed to provide Γ_{on}; for a high-power amplifier (HPA), the output circuit is designed to provide Γ_{op}. The designs of these two types of amplifiers are duals of each other, as will be discussed later.

4.3 *S* PARAMETERS

While passive circuits are usually described by the *ABCD* matrices, the active transistors are usually described by the two-port or three-port *S* parameters, which are defined by

$$b_1 = S_{11}a_1 + S_{12}a_2 \qquad b_2 = S_{21}a_1 + S_{22}a_2 \tag{4.10}$$

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 + S_{13}a_3 \\ b_2 &= S_{21}a_1 + S_{22}a_2 + S_{23}a_3 \\ b_3 &= S_{31}a_1 + S_{32}a_2 + S_{33}a_3 \end{aligned} \tag{4.11}$$

as a function of bias, frequency, and temperature. The waves a_1, b_1, ... are defined such that

$$|a_1|^2 = P_{\text{inc1}} \tag{4.12}$$

$$|b_1|^2 = P_{\text{ref1}} \tag{4.13}$$

where P_{inc1} is the incident power at port 1 and P_{ref1} is the reflected power at port 1, so

$$a_1 = \frac{V_{inc1}}{\sqrt{Z_0}} \qquad (W^{1/2}) \tag{4.14}$$

$$b_1 = \frac{V_{ref1}}{\sqrt{Z_0}} \qquad (W^{1/2}) \tag{4.15}$$

These waves a_1 and b_1 are root-mean-square (rms) voltages normalized by $\sqrt{Z_0}$. The parameters S_{11} and S_{22} are the reflection coefficients with the opposite port terminated in Z_0 (usually 50 Ω). The parameters S_{21} and S_{12} are the forward and reverse 50-Ω transducer gains, which will be discussed further below. Notice the voltages are rms values, whereas most transmission line books have them as peak voltages.

4.4   *S* PARAMETERS FROM SPICE ANALYSIS

Using any SPICE (Semiconductor Processing with IC Emphasis) program (e.g., PSPICE), it is a simple task to generate the *S* parameters of an active transistor using the diagram in Figure 4.4 [4.3]. Using two 1-V generators, S_{21} is simply V_2 and S_{11} is simply V_{10}. The analysis is the following:

$$2V_g - V_1 = Z_{01}I_1 \tag{4.16}$$

$$V_{10} = V_1 - V_g \tag{4.17}$$

$$V_2 = -Z_{02}I_2 \tag{4.18}$$

$$a_1 = \frac{V_1 + Z_{01}I_1}{2Z_{01}^{1/2}} = \frac{V_g}{Z_{01}^{1/2}} \tag{4.19}$$

$$b_1 = \frac{V_1 - Z_{01}I_1}{2Z_{01}^{1/2}} = \frac{V_{10}}{Z_{01}^{1/2}} \tag{4.20}$$

$$b_2 = \frac{V_2 - Z_{02}I_2}{2Z_{02}^{1/2}} \tag{4.21}$$
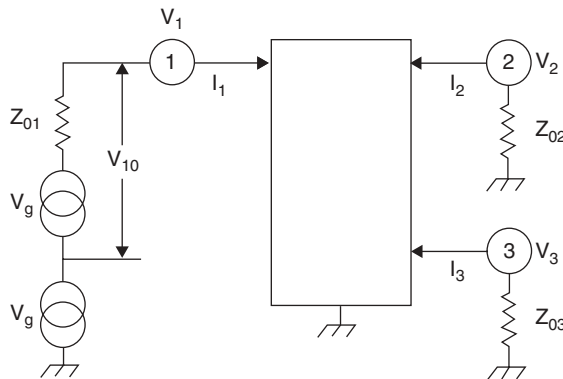
FIGURE 4.4   *S* parameters from SPICE analysis.

$$S_{11} = \frac{b_1}{a_1} = \frac{V_{10}}{V_g} \tag{4.22}$$

$$S_{21} = \frac{b_2}{a_1} = \frac{V_2}{V_g(Z_{01}/Z_{02})^{1/2}} \tag{4.23}$$

This analysis may be extended to any number of ports, where, for example,

$$S_{31} = \frac{V_3}{V_g(Z_{01}/Z_{03})^{1/2}} \tag{4.24}$$

Since many design problems may be solved using a SPICE engine, it is very useful to check the S parameters as soon as possible using this simple derivation in order to verify the validity of the nonlinear device model used by SPICE.

4.5 STABILITY

The stability of an active two-port may be viewed from at least three points of view:

1. In the Γ_L plane, what values of Γ_L give $|S'_{11}| > 1$?
2. In the S'_{11} plane, where does $|\Gamma_L| = 1$ plot?
3. If both ports are simultaneously matched so $S'_{11} = \Gamma_G^*$ and $S'_{22} = \Gamma_L^*$, the resistive portion of the terminations are positive.

This concept is often plotted in the Γ_G and Γ_L planes of the transistor, with stability circles marking the boundary $k = 1$. A stability factor [Eq. (4.7)] of $k < 1$ may be either an amplifier or an oscillator, which have different requirements. For an oscillator, the dc power is converted to RF power at the load; there is no RF generator. The RF power is started as random noise, which quickly builds up in a resonator circuit to the final steady-state output power. The resonator may be placed at either port; the load is always at the opposite port. The load circuit is designed (after the input is resonated) to satisfy either

$$\Gamma_L S'_{22} = 1 \tag{4.25}$$

or

$$\Gamma_G S'_{11} = 1 \tag{4.26}$$

which are equivalent requirements. If either equation above is satisfied, the other one is automatically satisfied [4.1]. In other words, if oscillation occurs at the input, it also occurs at the output. An oscillator is a one-port, where the port is terminated by a 50-Ω load.

For amplifier design, when high gain is required where $k < 1$, we often refer to G_{ms} as the desired gain. This is the gain you would achieve if the two-port is resistively loaded to give $k = 1$ and the two-port is simultaneously matched with lossless matching networks. This is only a concept, and it is not necessarily the method used to design the amplifier, since a gain greater than G_{ms} may be obtained. Notice all passive networks

indep (L_StabCircle1) (0.000 to 51.000)

indep (S_StabCircle1) (0.000 to 51.000)
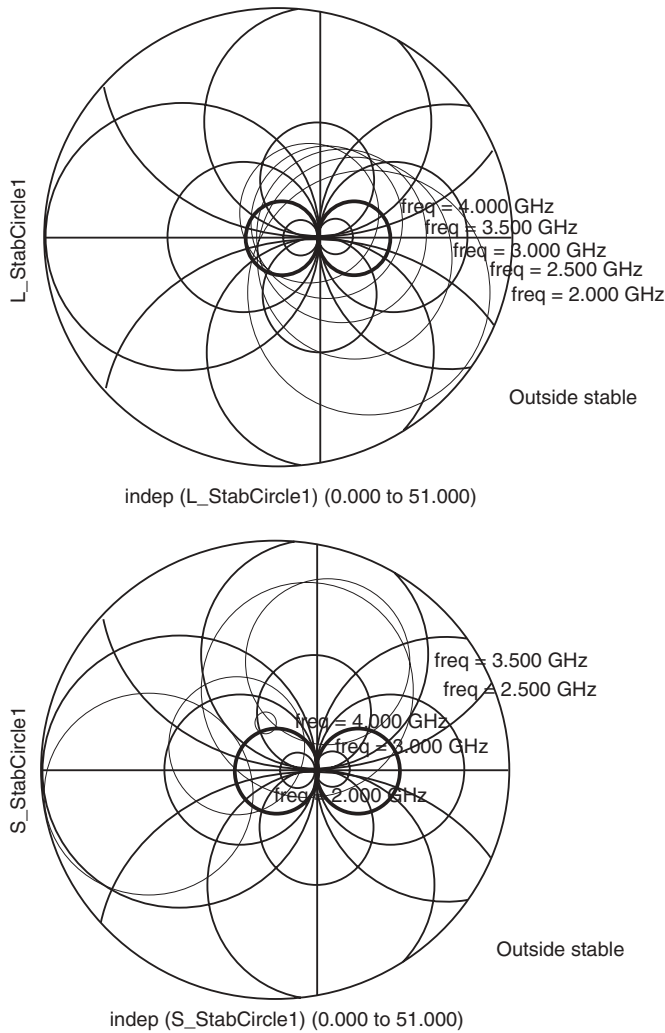
FIGURE 4.5   Stability circles at 2 to 4 GHz for Agilent ATF34143 PHEMT.

(with $R = 0$) have $k = 1$; negative resistors have $k < 1$, which is sometimes used to model oscillators.

Smith charts (which will be discussed in Chapter 5 and simply represent all impedances with positive and negative R) are used for describing the locations of stable and unstable terminations. An example for an 800-μm Agilent PHEMT is given in Figure 4.5 for the suggested bias point of $V_{ds} = 4$ V and $I_{ds} = 60$ mA over the frequency range 2 to 4 GHz. Both depletion- and enhancement-mode PHEMTs are available from Agilent (see Table 4.3). At low frequencies, k will usually be less than unity, so we must design the amplifier for stability at all frequencies:

1. Below the band
2. In the band
3. Above the band

TABLE 4.3   Agilent PHEMTs

Part No.	Type	Size (μm)	Suggested Bias	Application
ATF-541M4	Enhancement	800	3 V, 60 mA	Low noise
ATF-551M4	Enhancement	400	2.7 V, 10 mA	Low noise
ATF-34143	Enhancement	800	4 V, 60 mA	IP3, low noise
			4 V, 20 mA	
ATF-35143	Enhancement	400	4 V, 30 mA	IP3, low noise
			4 V, 10 mA	
ATF-36163	Depletion	200	2 V, 15 mA	Low noise

Short-circuited stubs may help satisfy this requirement at low frequencies where stability is usually more difficult, in addition to contributing to the matching circuit and the dc bias circuit.

Using the ATF34143 800-μm enhancement-mode PHEMT, a 3-GHz lumped-element amplifier designed for about $G_{ms} = 18.1$ dB is given in Figure 4.6. The elements were tuned for $S_{21} = 18.2$ dB and S_{11} and S_{22} low, about 0.5 or less. Then the terminations Γ_G and Γ_L were checked against the stability circles given in Figure 4.5, which is shown in Figure 4.7 to be in the stable region for Γ_L but in the unstable region for Γ_G, using Table 4.4. As the gain is increased even further, the S_{11} and
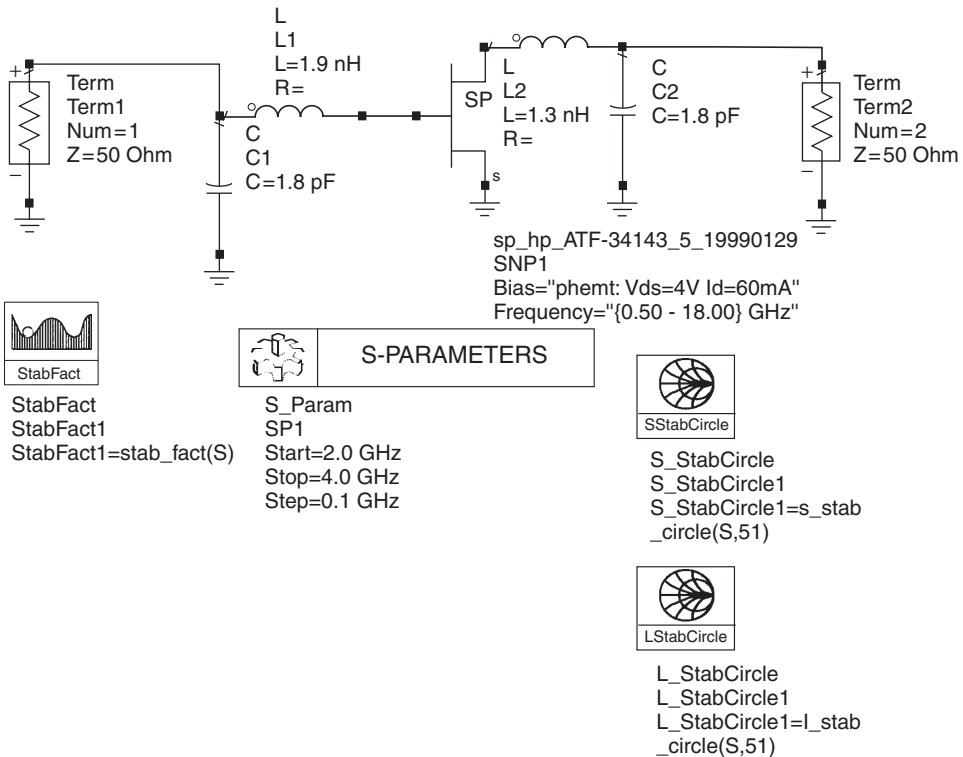
(a)

FIGURE 4.6   A 3-GHz amplifier using ATF34143 PHEMT.

m1
freq=3.000 GHz
dB(S(2,1))=18.221

m2
freq = 3.000 GHz
nF (2) = 0.573

(b)
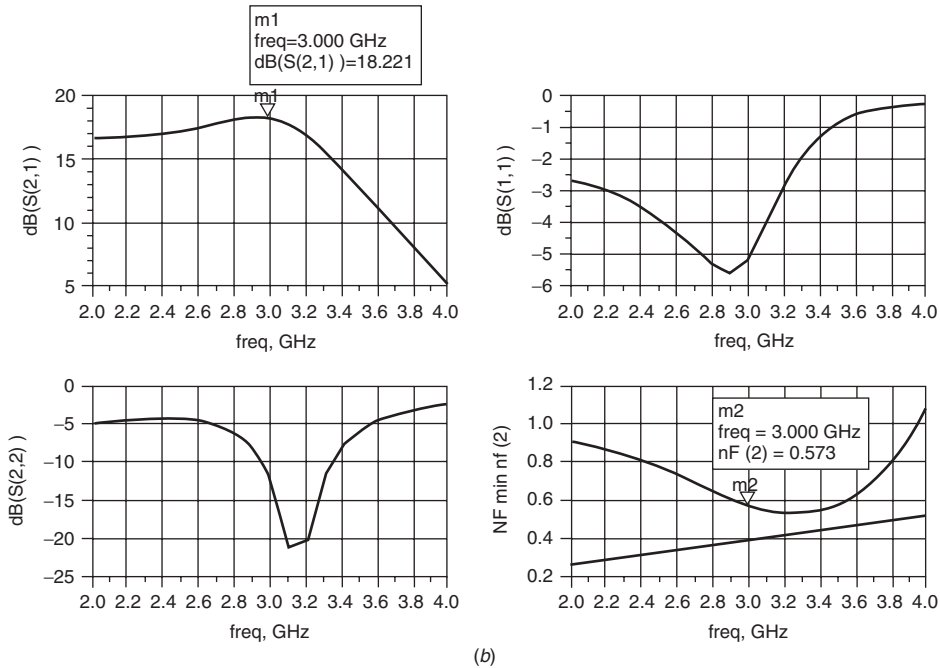
FIGURE 4.6   (*continued*)

TABLE 4.4   *S* **Parameters for ATF34143 PHEMT at 4 V, 60 mA**

$S_{11} = 0.67 < -168$	$k = 0.746$
$S_{12} = 0.083 < 15$	
$S_{21} = 5.345 < 60$	
$S_{22} = 0.19 < -171$	

S_{22} parameters of the matching circuits will come closer to the unstable region and eventually become unstable; thus $G_{ms} = 18.1$ dB or slightly less is a reasonable choice for gain when $k < 1$. A similar design using 400-µm enhancement-mode PHEMTs is also given in Chapter 8.

4.6   POWER GAINS, VOLTAGE GAIN, AND CURRENT GAIN

4.6.1   Power Gain

There are nine (or more) definitions of power gain tabulated in Table 4.5. The smallest gain is simply the 50-Ω transducer gain $|S_{21}|^2$, where no matching circuits are used. The highest gain is Mason's unilateral power gain [4.4, 4.5], where the *S*-parameter matrix has been reduced to three zeros and $U < \theta_u$:

$$S_u = \begin{bmatrix} 0 & 0 \\ U^{1/2} \underline{/\theta_u} & 0 \end{bmatrix} \tag{4.27}$$

(a)

(b)
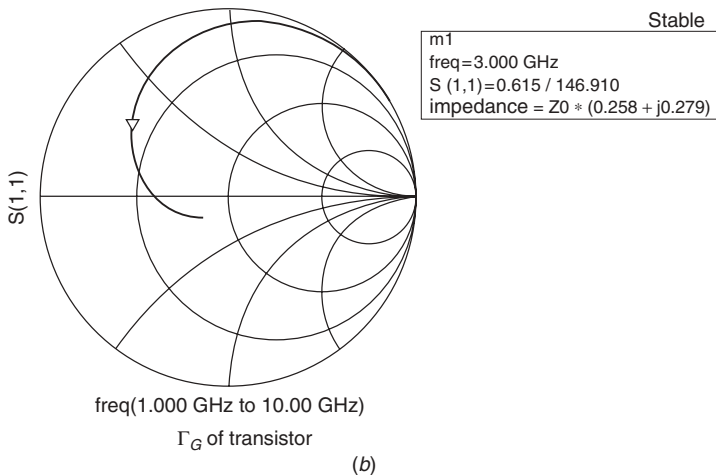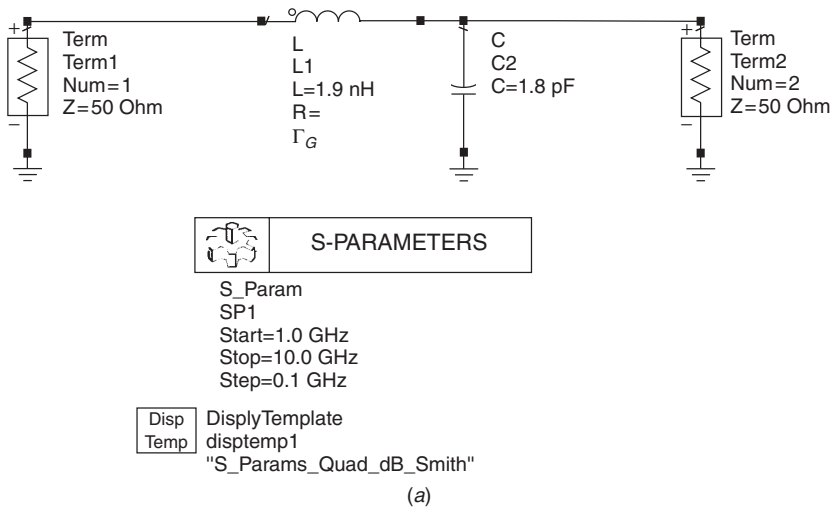
FIGURE 4.7   Stability check for 3-GHz amplifier.

by lossless feedback and matching. It is of interest to note that the unilateral gain is invariant to common lead, that is, $U_{CE} = U_{CB} = U_{CC}$. In practice, we rarely design for unilateral gain, since it is a narrow band (about 10% 3-dB gain bandwidth) and very sensitive to the accuracy of the S parameters, especially S_{12}, which is very small; even more important, the overall stability of a unilateral amplifier is difficult to achieve at all frequencies. The frequency where $|U| = 1$ is the f_{max} of the transistor, another useful figure of merit for the transistor. We rarely build amplifiers with this much gain; it is only a useful concept often quoted by the device manufacturer. A more complete discussion of unilateral gain and other types of lossless feedback amplifiers is found in Chapter 8. High-gain amplifiers (with $k > 1$) will have an S parameter set of

$$S_{ma} = \begin{bmatrix} 0 & (G_{mar})\underline{/\theta_2} \\ (G_{ma})^{1/2}\underline{/\theta_1} & 0 \end{bmatrix} \qquad (4.28)$$

Term	L	C	Term
Term1	L1	C1	Term2
Num=1	L=1.3 nH	C=1.8 pF	Num=2
Z=50 Ohm	R=		Z=50 Ohm
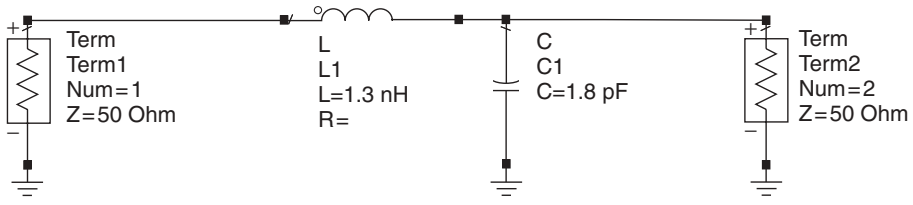
S-PARAMETERS

S_Param
SP1
Start=1.0 GHz
Stop=10.0 GHz
Step=0.1 GHz

Disp
Temp

DisplyTemplate
disptemp1
"S_Params_Quad_dB_Smith"

(*c*)
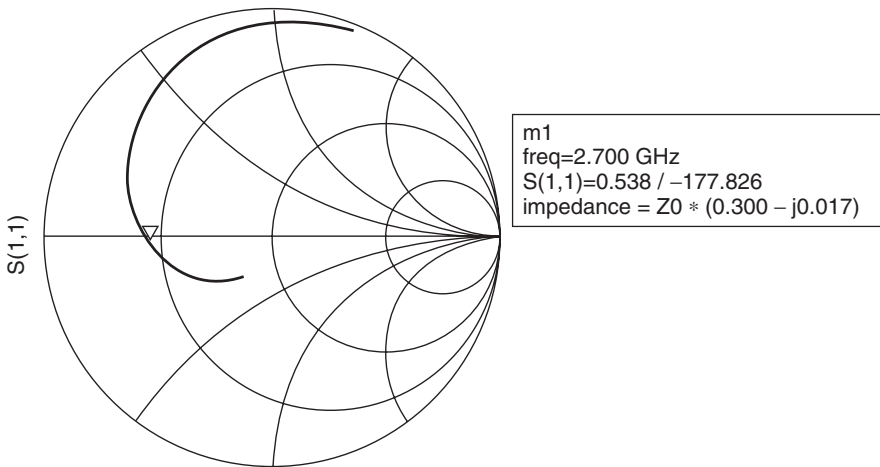
m1
freq=2.700 GHz
S(1,1)=0.538 / −177.826
impedance = Z0 ∗ (0.300 − j0.017)

S(1,1)

freq(1.000GHz to 10.00GHz)
Gamma_L vs Frequency

(*d*)

FIGURE 4.7   (*continued*)

where

$$G_{mar} = \left| \frac{S_{12}}{S_{21}} \right| [k - (k^2 - 1)^{1/2}] \tag{4.29}$$

If $k < 1$ the zeros for S_{11} and S_{22} are not possible but the coefficients may be small.

Since Eqs (4.27) and (4.28) contain phase angles, it is of interest to calculate these angles, which is a straightforward application of *S*-parameter analysis [4.6]. This analysis is based upon problem 1.17 of Ref. 4.1, which is repeated here. If two two-ports S_m

TABLE 4.5   Nine Power Gains

Transducer power gain in 50-Ω system	$G_T = \|S_{21}\|^2$
Transducer power gain for arbitrary Γ_G and Γ_L	$G_T = \dfrac{(1 - \|\Gamma_G\|^2)\|S_{21}\|^2(1 - \|\Gamma_L\|^2)}{\|(1 - S_{11}\Gamma_G)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_G\Gamma_L\|^2}$
Unilateral transducer power gain	$G_{TU} = \dfrac{\|S_{21}\|^2(1 - \|\Gamma_G\|^2)(1 - \|\Gamma_L\|^2)}{\|1 - S_{11}\Gamma_G\|^2\|1 - S_{22}\Gamma_L\|^2}$
Power gain with input conjugate matched	$G = \dfrac{\|S_{21}\|^2(1 - \|\Gamma_L\|^2)}{\|1 - S_{22}\Gamma_L\|^2(1 - \|S_{11}\|^2)} = \dfrac{\|S_{21}\|^2}{1 - \|S_{11}\|^2}$ (for $\Gamma_L = 0$)
Available power gain with output conjugate matched	$G_A = \dfrac{\|S_{21}\|^2(1 - \|\Gamma_G\|^2)}{\|1 - S_{11}\Gamma_G\|^2(1 - \|S_{22}\|^2)} = \dfrac{\|S_{21}\|^2}{1 - \|S_{22}\|^2}$ (for $\Gamma_G = 0$)
Maximum available power gain	$G_{ma} = \left\|\dfrac{S_{21}}{S_{12}}\right\| (k - \sqrt{k^2 - 1})$
Maximum unilateral transducer power gain	$G_{TU\,\max} = \dfrac{\|S_{21}\|^2}{(1 - \|S_{11}\|^2)(1 - \|S_{22}\|^2)}$
Maximum stable power gain	$G_{ms} = \dfrac{\|S_{21}\|}{\|S_{12}\|}$
Unilateral power gain	$U = \dfrac{1/2\|S_{21}/S_{12} - 1\|^2}{k\|S_{21}/S_{12}\| - \mathrm{Re}(S_{21}/S_{12})}$

FIGURE 4.8   Cascaded two-ports.

and S_n are cascaded, the resulting two-port has the following S parameters (Fig. 4.8):

$$S_{11} = S_{m11} + \frac{Sm_{12}S_{m21}S_{n11}}{1 - S_{m22}S_{n11}} \tag{4.30}$$

$$S_{12} = \frac{S_{n12}S_{m12}}{1 - S_{m22}S_{n11}} \tag{4.31}$$

$$S_{21} = \frac{S_{m21}S_{n21}}{1 - S_{m22}S_{n1}1} \tag{4.32}$$

$$S_{22} = \frac{S_{n22} + S_{n12}S_{n21}S_{m22}}{1 - S_{m22}S_{n11}} \tag{4.33}$$

Since the G_{ma} amplifier is the cascade of three two-ports, applying the above formulas gives the result

$$S_{21} = \frac{S_{g21}S_{m21}S_{n21}}{(1 - S_{g22}S_{m11})(1 - S_{m22}S_{n11}) - S_{g22}S_{m21}S_{m12}S_{n11})} = \frac{S_{g21}S_{m21}S_{n21}}{D} \tag{4.34}$$

$$S_{12} = \frac{S_{g12}S_{m12}S_{n12}}{D} \tag{4.35}$$

$$S_{11} = S_{22} = 0 \tag{4.36}$$

This result gives both the magnitude and phase of the gain (G_{ma}); the phase will depend upon the particular matching structure used, since they are not unique. Notice the equation for S_{21}, (4.34), bears a startling resemblance to the transducer gain equation, which follows below.

For the case of unilateral gain, we may use a variable coupler and line stretcher to make the reverse gain zero, as proposed by Lange [4.7]. The circuit diagram is given in Figure 4.9, where we have a unilateralizing variable coupler, a line stretcher, and the G_{ma} amplifier. For S_{12} to cancel, a portion of the input signal at port 2 is coupled by the amount S_{12} to the input port; the line stretcher varies the phase such that the coupled S_{12} is 180° out of phase with the S_{12} from the transistor amplifier. The analysis is more complicated since the directional coupler is a four-port, but using the techniques already presented, the result is [4.6]

$$S_{21} = -\sqrt{U} \qquad \text{if } \varphi + \theta_1 = 0° \tag{4.37}$$

where φ is the phase shift of the line stretcher and θ_1 is the phase shift of the S_{21} of the transistor:

$$S_{12} = 0 \tag{4.38}$$

if $\varphi + \theta_2 = 0°$ and $c = \sqrt{G_{mar}}$, where θ_2 is the phase shift of the S_{12} of the transistor and c is the coupling coefficient of the directional coupler.

This result also includes both the magnitude and phase for the gain, and it has been verified on both Ansoft's Serenade and Agilent's ADS, a nonlinear simulator. Applying these concepts to transistor S-parameter data [4.6], one finds the phase angle of U tends to be 180°, the same value of CS or CE transistors at low frequencies.

The most general amplifier is described by the transducer gain,

$$G_T = \frac{P_L}{P_A} \tag{4.39}$$
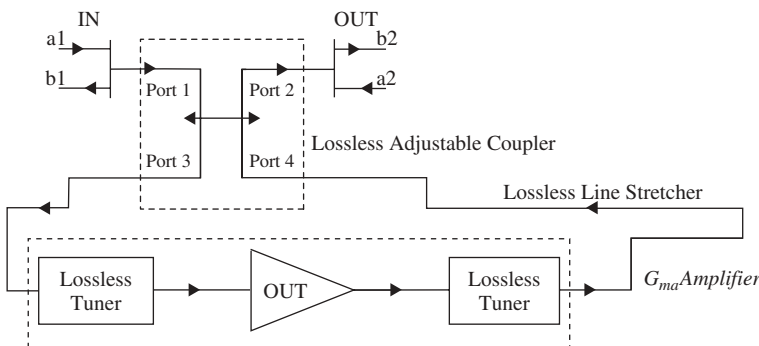
FIGURE 4.9 Lange measurement setup for unilateral amplifier [4.7].

which is a function of all four S parameters, Γ_G, and Γ_L. A useful approximation is G_{TU}, which assumes $S_{12} = 0$; this leads to $G_{TU,\max}$, an expression that indicates which port needs to be matched first for highest gain:

$$G_{TU,\max} = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} \tag{4.40}$$

A LNA will always be a stable design (in the band) when the input is mismatched for noise and the output is conjugately matched for gain, leading to the available power gain.

$$G_T = G_A = \frac{|S_{21}|^2(1 - |\Gamma_G|^2)}{|1 - S_{11}\Gamma_G|^2(1 - |S_{22}'|^2)} \tag{4.41}$$

The dual is the HPA, leading to "power gain":

$$G_T = G = \frac{|S_{21}|^2(1 - |\Gamma_L|^2)}{|1 - S_{22}\Gamma_L|^2(1 - |S_{11}'|^2)} \tag{4.42}$$

Figure 4.10 illustrates the frequency dependence of power gains for a typical transistor. Power gains are normally (from low to high)

$$|S_{21}|^2 < G_T < G_A \qquad \text{or} \qquad G < G_{ma} \text{ or } G_{ms} < U$$

4.6.2 Voltage Gain and Current Gain

The voltage gain of a two-port can be given by the S parameters as

$$A_v = \frac{V_2}{V_1} = \frac{a_2 + b_2}{a_1 + b_1} = \frac{a_2/a_1 + b_2/a_1}{1 + b_1/a_1} = \frac{b_2/a_1(a_2/b_2 + 1)}{1 + S_{11}'} \tag{4.43}$$
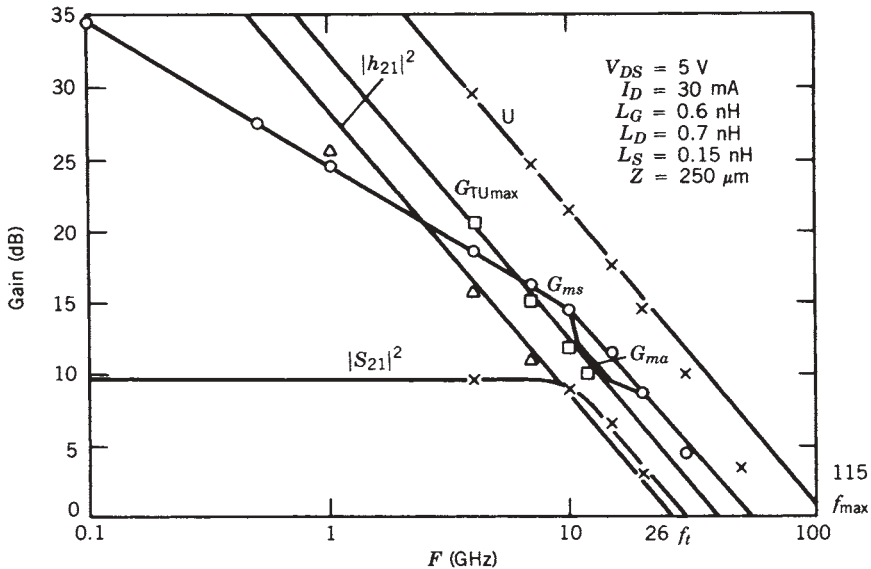
FIGURE 4.10   Power gains versus f.

Since

$$\frac{b_2}{a_1} = \frac{S_{21}}{1 - S_{22}\Gamma_L} \tag{4.44}$$

and

$$\Gamma_L = \frac{a_2}{b_2} \tag{4.45}$$

we find

$$A_v = \frac{S_{21}(1 + \Gamma_L)}{(1 - S_{22}\Gamma_L)(1 + S'_{11})} \tag{4.46}$$

Notice A_v and S_{21} are similar but S_{21} is only defined for a 50-Ω load termination, but A_v is completely general for any generator and load terminations.

4.6.3 Current Gain

In a similar way, we may define current gain as

$$\begin{aligned} A_i = \frac{I_2}{I_1} &= \frac{a_2 - b_2}{a_1 - b_1} \\ &= \frac{a_2/a_1 - b_2/a_1}{1 - b_1/a_1} \\ &= \frac{b_2/a_1(a_2/b_2 - 1)}{1 - S'_{11}} \\ &= \frac{S_{21}(\Gamma_L - 1)}{(1 - S_{22}\Gamma_L)(1 - S'_{11})} \end{aligned} \tag{4.47}$$

Since we often think of current gain in terms of h_{21}, it will be useful to derive both A_v and A_i in terms of h parameters. Setting up the equations gives

$$v_1 = h_{11}i_1 + h_{12}v_2 \tag{4.48}$$

$$i_2 = h_{21}i_1 + h_{22}v_2 \tag{4.49}$$

$$v_1 = v_1 \tag{4.50}$$

$$v_2 = -Z_0 i_2 \tag{4.51}$$

Thus, we obtain

$$i_2 = h_{21}i_1 - h_{22}Z_0 i_2 \tag{4.52}$$

$$A_i = \frac{i_2}{i_1} = \frac{h_{21}}{1 + h_{22}Z_0} \tag{4.53}$$

which is a result that is more intuitively understandable. In a similar way, we obtain the voltage gain from h parameters as follows:

$$v_2 = -Z_0 i_2 = -Z_0 h_{21} i_1 - Z_0 h_{22} v_2$$

$$v_2(1 + Z_0 h_{22}) = -Z_0 h_{21} i_1$$

$$i_1 = \frac{v_1 - h_{12} v_2}{h_{11}}$$

$$v_2(1 + Z_0 h_{22}) = -Z_0 h_{21} \left(\frac{v_1}{h_{11}} - \frac{h_{12} v_2}{h_{11}} \right)$$

$$v_2 \left(1 + Z_0 h_{22} - \frac{Z_0 h_{21} h_{12}}{h_{11}} \right) = -\frac{Z_0 h_{21} v_1}{h_{11}} \tag{4.54}$$

$$A_v = \frac{v_2}{v_1} = \frac{-Z_0 h_{21}/h_{11}}{1 + Z_0 h_{22} - Z_0 h_{21} h_{12}/h_{11}}$$

$$= \frac{-Z_0 h_{21}}{h_{11} + Z_0 h_{11} h_{22} - Z_0 h_{21} h_{12}}$$

$$= -\frac{Z_0 h_{21}}{h_{11} + Z_0 D_n} \tag{4.55}$$

where D_n is defined by

$$D_n = h_{11} h_{22} - h_{21} h_{12} \tag{4.56}$$

Finally we obtain the power gain from A_v and A_i as follows:

$$P = \frac{P_L}{P_{in}} = \frac{\text{Re}(-v_2 i_2^*)}{\text{Re}(v_1 i_1^*)} = -A_v A_i^*$$

$$= -\frac{S_{21}(1 + \Gamma_L) S_{21}^* (\Gamma_L^* - 1)}{(1 - S_{22}\Gamma_L)(1 + S_{11}')(1 - S_{22}^*\Gamma_L^*)(1 - S_{11}'^*)}$$

$$= \frac{|S_{21}|^2 (1 - |\Gamma_L|^2)}{(|1 - S_{22}\Gamma_L|^2)(1 - |S_{11}'|^2)} \tag{4.57}$$

which is the same result given in the table for power gains (Table 4.1). It will be helpful to think in terms of voltage gain, current gain, and power gains when designing active circuits.

Using similar algebra as above, we can easily show that

$$G_m = \frac{i_2}{v_1} = \frac{y_{21}}{1 + Z_L y_{22}} = \frac{-S_{21}}{1 + S_{11}} \tag{4.57a}$$

is the transconductance gain of the transistor and

$$Z_m = \frac{v_2}{i_1} = \frac{Z_{21}}{1 + Z_{22} Y_L} = \frac{S_{21}}{1 - S_{11}} \tag{4.57b}$$

is the transimpedance gain of the transistor Ref. [4.7a].

4.7 THREE-PORTS

A three-terminal transistor may be considered a three-port where

$$b_1 = S_{11}a_1 + S_{12}a_2 + S_{13}a_3$$
$$b_2 = S_{21}a_1 + S_{22}a_2 + S_{23}a_3 \qquad (4.58)$$
$$b_3 = S_{31}a_1 + S_{32}a_2 + S_{33}a_3$$

These nine S parameters are not independent. The sum of the rows and columns are unity due to power considerations [4.8].

Similarly, for three-port Y parameters,

$$i_1 = y_{11}v_1 + y_{12}v_2 + y_{13}v_3$$
$$i_2 = y_{21}v_1 + y_{22}v_2 + y_{23}v_3 \qquad (4.59)$$
$$i_3 = y_{31}v_1 + y_{32}v_2 + y_{33}v_3$$

where the sum of every row and column is zero from Kirchhoff's laws [4.8]. The network must have no internal shunt elements to ground for this condition to be satisfied.

The proof of this simple and important result can be seen from Figure 4.11, which is a three-port with a reference ground labeled r. To prove that the sum of any column equals zero, apply Kirchhoff's current law at the reference node r. Then

$$I_1 + I_2 + I_3 = 0 \qquad (4.60)$$

Letting $V_2 = V_3 = 0$ gives $I_1 = y_{11}V_1$, $I_2 = y_{21}V_1$, $I_3 = y_{13}V_1$, so substituting in Eq (4.59) completes the proof. To prove that the sum of any row equals zero, let all three signal voltages be equal to V_0. Since all three terminal voltages are at the same voltage relative to node r, there can be no current. Therefore,

$$I_1 = y_{11}V_1 + y_{12}V_2 + y_{13}V_3 = 0 = (y_{11} + y_{12} + y_{13})V_0 \qquad (4.61)$$

Since V_0 is not zero, this completes the proof.
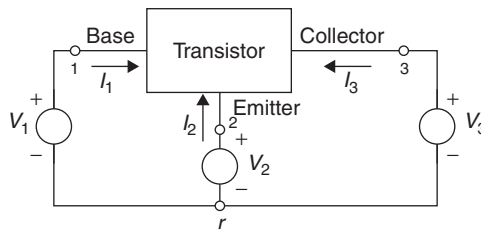
FIGURE 4.11   Transistor with external reference node r [4.8].
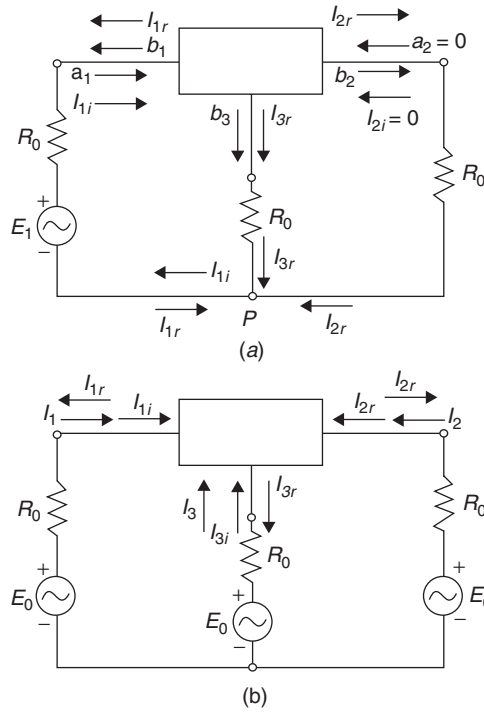
FIGURE 4.12   Circuits used to establish properties of indefinite scattering matrix [4.8].

A similar proof for S parameters follows from Figure 4.12, where the reference node (ground) is P. Applying Kirchhoff's current law to P gives

$$I_{1i} = I_{1r} + I_{2r} + I_{3r} \tag{4.62}$$

Since $b_1 = S_{11}a_1$, $b_2 = S_{21}a_1$, and $b_3 = S_{31}a_1$, adding these three terms leads to

$$S_{11} + S_{21} + S_{31} = \frac{I_{1r} + I_{2r} + I_{3r}}{I_{1i}} = 1 \tag{4.63}$$

which completes the proof for the columns.

In Figure 4.12b, all generators are set to E_0, which gives all currents I_1, I_2, I_3 equal to zero. Thus $I_{1i} = I_{1r}$, $I_{2i} = I_{2r}$, $I_{3i} = I_{3r}$. Also, $I_{1i} = I_{2i} = I_{3i}$ because the generators are identical. Substituting into Eq (4.58) gives

$$S_{11} + S_{12} + S_{13} = 1 \tag{4.64}$$

where we have used $I_{1i} = I_{1r}$, which completes the proof for rows.

Notice the two-port and three-port S parameters of a transistor may be confused since they are different measurements but nevertheless are labeled the same. For example, the two-port S_{21} is measured with the emitter at ground, but the three-port S_{21} is measured with the emitter connected to a 50-Ω resistor. The two-port and three-port Y parameters are the same measurement and thus the same parameters. Since k is
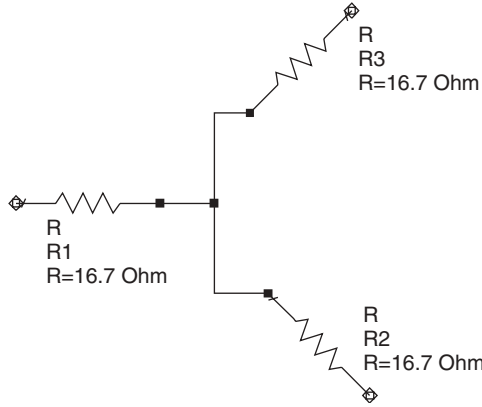
FIGURE 4.13   Three-port power divider.

defined for a two-port, there are three stability factors: k_{CE}, k_{CB}, and k_{CC}, which are independent parameters of the transistor. Usually the CE or CS configuration yields the highest value of k and therefore the best stability [4.1, pp. 177, 191].

A three-port power divider which helps to clarify these concepts is a matched two-way power divider as shown in Figure 4.13 with 6 dB loss. The S matrix is

$$S_{16.7} = 0.5 \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} \tag{4.65}$$

If the resistors are changed to 50 Ω, the S matrix is

$$S_{50} = 0.33 \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \tag{4.66}$$

For all three-ports, the rows and columns always add up to unity for S parameters and zero for Y parameters. This is not true for two-ports, four-ports, and so on. There are three ports which violate this general rule, for example, a Wilkinson power divider which has an internal resistor between two internal nodes; also imagine adding another resistor to ground at the y junction of the 16.7-Ω network above. However, for simple networks, the rule holds.

The three-port matrices are useful for converting CE to CB and CC configurations. This is most easily done using the three-port Y parameters, since the three-port and two-port Y parameters are measured to be the same. If we arbitrarily label the emitter port 1, the collector port 2, and the emitter port 3, we may easily show the common-emitter Y parameters of the two-port are

$$Y_{CE} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \tag{4.67}$$

the common-base Y parameters are

$$Y_{CB} = \begin{bmatrix} y_{33} & y_{32} \\ y_{23} & y_{22} \end{bmatrix} \tag{4.68}$$

and the common-collector Y parameters are

$$Y_{CC} = \begin{bmatrix} y_{11} & y_{13} \\ y_{31} & y_{33} \end{bmatrix} \tag{4.69}$$

So if you begin with CE two-port S parameters from the data sheet, convert this to two-port Y parameters, find the three-port Y parameters, then use the appropriate Y parameters to obtain the CB or CC two-port Y parameters, and finally convert the Y parameters to S parameters.

4.8 DERIVATION OF TRANSDUCER POWER GAIN

All of the nine power gains in Table 4.5 were derived in Ref 4.1, but it is instructive to derive the transducer power gain in detail, since this is usually the gain of interest in system design.

Referring to Figure 4.14, when a generator or source of power is connected to a two-port, the generator emits a wave b_G if a nonreflecting load is connected ($\Gamma_1 = 0$). In the general case where the load is not matched, use Figure 4.14 to compute the sum of the reflected waves coming to the generator:

$$\begin{aligned} b_1 &= b_G \Gamma_1 [1 + \Gamma_1 \Gamma_G + (\Gamma_{1G})^2 + \cdots] \\ &= \frac{b_G \Gamma_1}{1 - \Gamma_1 \Gamma_G} \end{aligned} \tag{4.70}$$
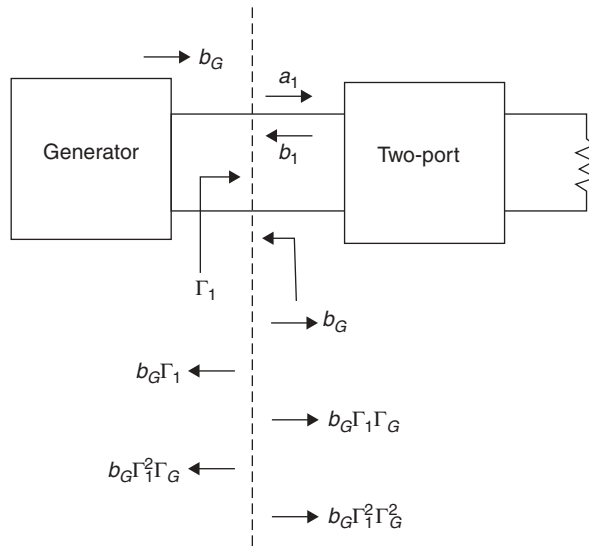
FIGURE 4.14   Generator representation.

Since $\Gamma_1 = b_1/a_1$,

$$b_1 = \frac{b_G b_1}{a_1 - \Gamma_G b_1} \tag{4.71}$$

$$a_1 = b_G + b_1 \Gamma_G \tag{4.72}$$

which seems to be intuitively obvious. Another representation for a_1 is

$$a_1 = b_G + \Gamma_1 \Gamma_G a_1 \tag{4.73}$$

$$a_1 = \frac{b_G}{1 - \Gamma_1 \Gamma_G} \tag{4.74}$$

The net power delivered to a load from a generator is

$$P_L = |a_1|^2 - |b_1|^2 = |a_1|^2 (1 - |\Gamma_L|^2) \tag{4.75}$$

which may be changed to the power delivered by port 2 of the active transistor to the load:

$$P_L = |b_2|^2 \, (1 - |\Gamma_L|^2) \tag{4.76}$$

The available power from a generator is obtained by connecting a conjugate load to give

$$P_A = \frac{|b_G|^2}{1 - |\Gamma_G|^2} \tag{4.77}$$

We are now ready to derive the transducer power gain in terms of the S parameters:

$$G_T = \frac{P_L}{P_A} = \frac{|b_2|^2}{|b_G|^2 [(1 - |\Gamma_L|^2)(1 - |\Gamma_G|^2]} \tag{4.78}$$

Using the above results and the basic definitions of S parameters, we can show

$$\frac{b_2}{a_1} = \frac{S_{21}}{1 - S_{22}\Gamma_L} \tag{4.79}$$

$$\frac{a_1}{b_G} = \frac{1}{1 - \Gamma_1 \Gamma_G} \tag{4.80}$$

$$G_T = \frac{1 - |\Gamma_L|^2 |S_{21}|^2 (1 - |\Gamma_G|^2}{|1 - S_{22}\Gamma_L|^2 |1 - \Gamma_1 \Gamma_G|^2} \tag{4.81}$$

where

$$\Gamma_1 = S_{11}' = S_{11} + \frac{S_{12} S_{21} \Gamma_L}{1 - S_{22}\Gamma_L} \tag{4.82}$$

The unilateral transducer power gain is the same result as G_T with $S_{12} = 0$. The maximum unilateral transducer power gain is found by setting $\Gamma_L = S_{22}^*$ and $\Gamma_G = S_{11}^*$ to give

$$G_{TU,\text{max}} = \frac{|S_{21}|^2}{(1 - |S_{22}|^2)(1 - |S_{11}|^2)} \tag{4.83}$$

which gives a clear understanding of the effect of matching each individual port. For example, if $|S_{11}| > |S_{22}|$, matching the input port will produce more gain than matching the output port, but of course both ports should be matched.

4.9 DIFFERENTIAL *S* PARAMETERS

A differential (or balanced) port is one that typically consists of two electrodes neither of which is explicitly tied to ground. Balanced devices are becoming increasingly common in modern wireless and other devices. The reasons for this trend are manyfold but include better noise immunity, more efficient use of power (i.e., longer battery life), lower cost (e.g., no mixer baluns), higher levels of integration, smaller size, and some fundamental harmonic rejection. Certain structures such as many mixers and analog-to-digital converters are naturally balanced, thus making circuit design somewhat simpler if all devices in the chain are balanced. To properly characterize these devices, a formalism for their behavior is required. Following the concepts for single-ended devices (i.e., where the port is defined by an active line and a ground), it is natural to try an analog of *S* parameters that bring out important behavioral characteristics of these balanced versions.

The concepts of differential and common-mode signals should be familiar from low frequency circuit analysis [4.9]. A purely differential signal applied to a port pair will have each port being driven with the same amplitude signal (relative to a virtual node) 180° out of phase with each other. A purely common-mode signal will have each port driven with the same amplitude and same phase. The expectation for an example device, a differential amplifier, is that a differential input would produce a larger differential output (with better noise immunity and very little common-mode output) and a common-mode input would produce little output. These concepts are illustrated in Figure 4.15; the two single-ended ports being driven as a pair are termed a *composite port*.

While standard four-port *S* parameters, discussed previously (see also Ref. 4.10), can be used to characterize the device (at least in the small-signal limit), they do
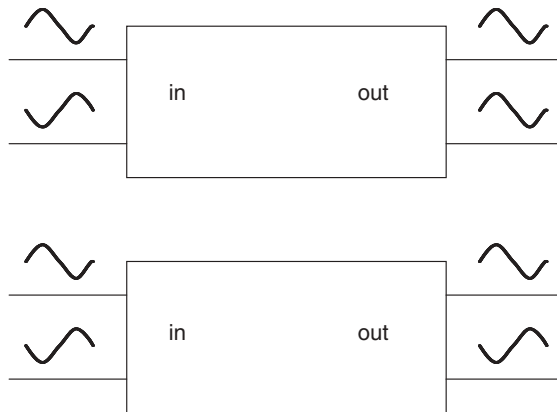
FIGURE 4.15 Concepts of differential and common-mode drive (and output) are illustrated for a pair of scenarios (common-mode input is also possible). Output can be thought of as a reflection or transmission.

not readily display the important circuit performance parameters like differential gain, common-mode gain, and differential-to-common-mode conversion. We would prefer a set of *mixed-mode S parameters* [4.11] defined in terms of signals applied to composite ports (pairs of single-ended ports driven as a pair).

Return to the wave variable definition of S parameters and define differential and common-mode input signals. As in ordinary differential amplifier analysis, any signal pair applied to a composite port can be decomposed (making linearity assumptions so superposition can be applied) into its differential and common mode portions (see Fig. 4.16): for signals A and B applied to the two ports, the differential portion is $\pm (A - B)/2$ and the common-mode portion is $(A + B)/2$.

Changing some constants to normalize power properly, the a and b wave variables can be defined as

$$a_{d1} = \frac{1}{\sqrt{2}}(a_1 - a_2) \qquad a_{c1} = \frac{1}{\sqrt{2}}(a_1 + a_2) \tag{4.84}$$

where the subscript $d1$ refers to the differential portion on composite port 1 and $c1$ refers to the common-mode portion on composite port 1. Similarly the input wave variables for the second composite port and the output wave variables for both composite ports can be defined.

With the wave variables defined (four input and four output for a device with two composite ports), it remains to define S parameters relating them. A natural definition is the following [4.12, 4.13]:

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \begin{bmatrix} S_{d1d1} & S_{d1d2} & S_{d1c1} & S_{d1c2} \\ S_{d2d1} & S_{d2d2} & S_{d2c1} & S_{d2c2} \\ S_{c1d1} & S_{c1d2} & S_{c1c1} & S_{c1c2} \\ S_{c2d1} & S_{c2d2} & S_{c2c1} & S_{c2c2} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} = \begin{bmatrix} S_{dd} & S_{dc} \\ S_{cd} & S_{cc} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} \tag{4.85}$$

where S_{d1d1} is defined as b_{d1}/a_{d1} when the other a_i are zero, and so on. *Note:* Some variations in the subscript notation of the S parameters are in use; the same symbols are generally used but they may be grouped differently.

The first portion of the equation can be interpreted just like four-port single-ended S parameters. The output wave b_i is a linear superposition of responses to four inputs. The last portion of the equation is simply a shorthand notation where each element (e.g., S_{dd}) represents a 2×2 matrix with a particular interpretation. The upper left quadrant (S_{dd} composed of S_{d1d1}, S_{d1d2}, ...) represents differential responses to differential inputs. These are usually the parameters of most interest in a balanced device. The

Differential part   *Common-mode part*
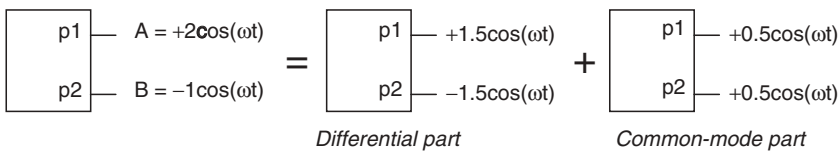
FIGURE 4.16   Any signal applied to a composite port (p_1 and p_2 driven as a pair) can be linearly broken into differential (related to the difference between the port nodes) and common-mode (related to the sum of the port nodes) portions. This is used to define the mixed-mode wave variables.

lower right quadrant (S_{cc}) is composed of common-mode responses to common-mode inputs. The other two quadrants represent *mode conversion* These are responses of a different form than was input (e.g., a common-mode output in response to a differential input). While sometimes desired (in certain transformers), these responses are often the result of nonidealities in the device.

Since the above equation looks like that of four-port single-ended *S* parameters and the input and output wave variables have already been expressed in terms of the single-ended *S* parameters, it is natural to assume there is a simple linear relationship between the mixed-mode *S* parameters and the single-ended *S* parameters. These relationships are easily derived:

$$
\begin{aligned}
S_{d1d1} &= \tfrac{1}{2}(S_{11} - S_{21} - S_{12} + S_{22}) & S_{c1c1} &= \tfrac{1}{2}(S_{11} + S_{21} + S_{12} + S_{22}) \\
S_{d1d2} &= \tfrac{1}{2}(S_{13} - S_{23} - S_{14} + S_{24}) & S_{c1c2} &= \tfrac{1}{2}(S_{13} + S_{23} + S_{14} + S_{24}) \\
S_{d2d1} &= \tfrac{1}{2}(S_{31} - S_{41} - S_{32} + S_{42}) & S_{c2c1} &= \tfrac{1}{2}(S_{31} + S_{41} + S_{32} + S_{42}) \\
S_{d2d2} &= \tfrac{1}{2}(S_{33} - S_{43} - S_{34} + S_{44}) & S_{c2c2} &= \tfrac{1}{2}(S_{33} + S_{43} + S_{34} + S_{44}) \\
S_{d1c1} &= \tfrac{1}{2}(S_{11} - S_{21} + S_{12} - S_{22}) & S_{c1d1} &= \tfrac{1}{2}(S_{11} + S_{21} - S_{12} - S_{22}) \\
S_{d1c2} &= \tfrac{1}{2}(S_{13} - S_{23} + S_{14} - S_{24}) & S_{c1d2} &= \tfrac{1}{2}(S_{13} + S_{23} - S_{14} - S_{24}) \\
S_{d2c1} &= \tfrac{1}{2}(S_{31} - S_{41} + S_{32} - S_{42}) & S_{c2d1} &= \tfrac{1}{2}(S_{31} + S_{41} - S_{32} - S_{42}) \\
S_{d2c2} &= \tfrac{1}{2}(S_{33} - S_{43} + S_{34} - S_{44}) & S_{c2d2} &= \tfrac{1}{2}(S_{33} + S_{43} - S_{34} - S_{44})
\end{aligned}
\tag{4.86}
$$

4.9.1 Measurements

Conceptually the simplest approach to measure a balanced device is to drive a composite port with a $180°$ hybrid or a splitter to generate the required differential and common-mode signals [4.13] The received signal could be sent through similar structures to convert them back to single ended for processing. In some cases this is done, but the switching may be complex and the bandwidth may be limited. Alternatively, simple single-ended *S* parameters may be measured and mathematically converted to the differential and common-mode parameters using Eq. (4.86).

While much simpler (and potentially of very large bandwidth), this latter approach has at least two limitations:

- Since the parameters are computed by subtraction, there is a potential loss of dynamic range at low levels when nearly equal numbers are subtracted to produce the small result. This issue is one of numerical sensitivity. *Example:* A nearly perfect device has low S_{c2d1}. The individual *S* parameters are on the order of 1 or 0.1 but the absolute difference ($\sim S_{c2d1}$) is about three to four orders of magnitude smaller. A very small error on S_{21} leads to a large change in S_{c2d1}.

- If the device is approaching nonlinearity, the principle of superposition used in the derivations comes into question. In a nonlinear device, the results of driving single-ended ports 1 and 2 separately cannot be simply added together to get the result if composite port 1 is driven by a differential or common-mode signal. Indeed, the device under test (DUT) may not even be in the correct operating state if not driven by the intended signal.
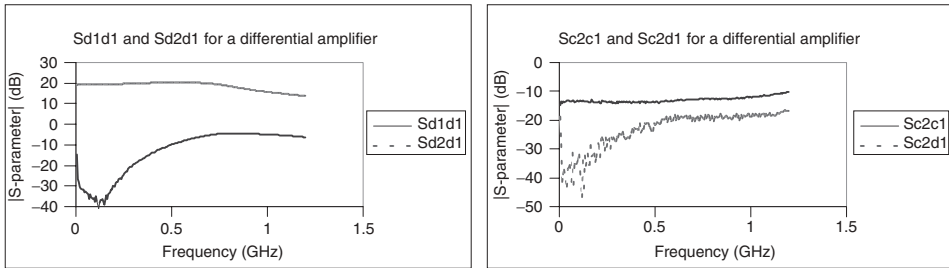
FIGURE 4.17   Four of the mixed-mode parameters for a balanced amplifier are shown. The differential gain (S_{d2d1}) is much higher than the common-mode gain (S_{c2c1}) and mode conversion (S_{c2d1}), as one might expect.

4.9.2 Example

To illustrate the concepts in this section, consider the measurement of a simple differential amplifier. It will be driven small-signal so the superposition of signals can be considered valid. The mixed-mode S parameters are calculated from the single-ended measurements and some of the results are plotted in Figure 4.17.

The differential gain (S_{d2d1}) and match (S_{didi}, $i = 1$, 2) are usually of the most interest to the circuit designer since the device will be used in a balanced system. The common-mode response and mode conversion are low (with respect to differential gain), as one would expect for a balanced device. The nonnegligible values of these latter two parameters are often due to asymmetries in the device or its test fixture.

4.10   TWISTED-WIRE PAIR LINES

Transmission line principles are applied to twisted-wire lines made of two wires. Reference 4.14 provides a practical design procedure in order to realize a desired characteristic impedance, including expressions developed to predict the effects of wire film insulation, pitch angle, and twisting. It provides practical graphs to determine the characteristic impedance if the dimensions and the dielectric constant are known. The characteristic impedance versus wire size (with and without insulation) is shown in Figure 4.18. The data can be used for the design of RF broadband transformers, signal combiners, and pulse transformers [4.15, 4.16].

In many other applications, twisted pairs are being used when the signal transmitted is a differential signal. One of the key problems in transmitting data or any kind of digital type of signal from one device to another is the electrical "noise," or radio-frequency interference (RFI), that penetrates the cable and gets mixed with the useful data or signal.

The first line of defense against RFI is to shield the cable with a conductive material that has been electrically grounded. However, even with the best shielding, cable length is quite limited. To overcome such limitations, equipment designers have turned to a technique of transmitting computer signal called the differential system.

With the differential system each signal is transmitted on two lines at the same time. On one, the signal is transmitted as a positive signal, on the other as a negative signal. At the receiving end of the cable the receiver device gets two signals. Both of
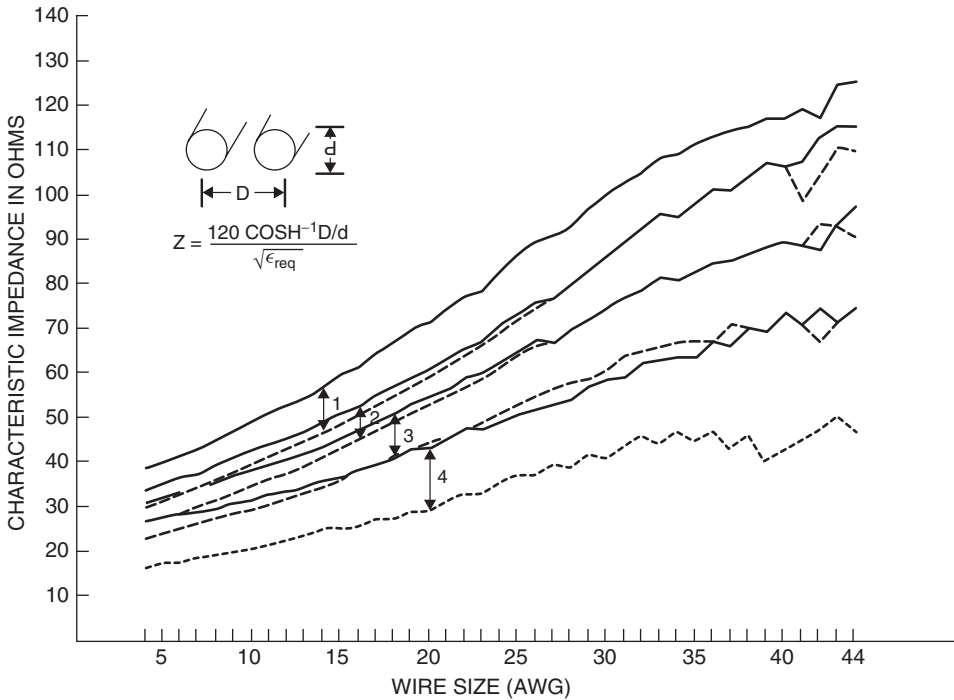
FIGURE 4.18 Characteristic impedance for bifilar magnet wire transmission line based on MIL-W-583 dimensions and with relative dielectric constant of 1. (From Ref. 4.14 © IEEE 1971.)

them, however, have been changed by the noise that penetrated the cable. The changes came in the form of unwanted voltage added to the wanted signal. At this point it is important to note that the unwanted voltage got added to both lines at the same time and by the same amount. The essence of the differential system is that the receiver is designed to take the difference between the two signals on the two lines. In doing that, the noise part of the signal, equal on both lines, gets eliminated, and what remains is clear signal.

As indicated above, the differential system works well if the noise added is equal on the two lines, that is, the positive and the negative. To ensure that the noise hits both of these lines identically, both of them need to occupy theoretically the same physical space. Practically, the closest we can get to this requirement is to have the two lines twisted together tightly. The tighter the twist of positive and negative lines, the cleaner the transmission and the longer the acceptable length of the cable.

Differential devices are devices that use the above-described differential system for transmitting data and control signals. The most common communications standards dealing with interconnecting differential type devices are RS-422, RS-449, RS-423, RS-530, V.35, X.21, SCSI, Token Ring, Ethernet, and so on.

By comparison, devices that do not use the differential system when transmitting data to another device are called single ended. Examples of single-ended communications standards are RS-232 Serial, CENTRONICS Parallel, and some SCSI. Another application for twisted pairs is the Firewire.

Firewire originally was developed by Apple Computer as a high-speed serial bus. While it was developed, many thought it was actually too fast, and some lower speed interconnect like USB would be cheaper to implement. Firewire languished. Suddenly, in 1995, a tiny connector showed up on the first DV camcorders shipped by Sony. DV was the killer application for Firewire. In late 1995, Firewire was accepted as a standard by the IEEE, henceforth called IEEE 1394.

The standard Firewire cable consists of six wires. Data are sent via two separately shielded twisted-pair transmission lines. The two twisted pairs are crossed in each cable assembly to create a transmit–receive connection. Two more wires carry power (8 to 40 V, 1.5 A maximum) to remote devices. Currently, these power lines are rarely used. The wires terminate in gameboy-style plugs.

Sony uses a four-conductor cable for the connection to the DV camcorders and DVCRs. They are like the above-mentioned setup but without the power wires. They terminate in smaller, four-prong connectors. To connect a Sony DV camcorder or DVCR with a standard IEE 1394 Firewire device or interface card, you need an adapter cable, four prongs on one side, six on the other. It simply connects the data lines while omitting the power connection.

According to the standard, the IEEE 1394 "wire" is good for 400 Megabits per second (Mbps) over 4.5 m. The standard cable uses 28 AWG (American Wire Gage) signal pairs with 40 twists/m. The power pair in the standard cable is 22 AWG.

Longer cable runs can be achieved by using thicker cable or by lowering the bit rate. DV users should keep in mind that the signaling rate of the Sony DV camcorders is only 100 Mbps. Can it use longer cables? The answer is yes. Although considerably out of the specification, several people have reported successful 100-Mbps transmissions over more than 20 m using standard cable. There are also reports of thicker cables being used to span lengths of 30 m or more at 100 Mbps.

The wiring used today by most of major telephone companies consists of four pairs of twisted wire in a plastic sheath. In the telephone industry it is called "four-pair." Technically it is category 3 UTP (unshielded twisted pair). It is a versatile wire in that it can handle four separate telephone lines or can be used for multiline PBX type sets.

Here's really good news for everyone who has Internet service at home, more than one home computer, one or more home telephone lines, and a fax machine and for anyone who expects to hook up any combination of these devices someday soon: The Federal Communications Commission (FCC) recently issued a new rule requiring that all telephone wiring installed inside homes and other buildings must meet new standards. The rule, which applies to new and retrofit telephone wire installations made after July 8, 2000, is aimed at assuring that all inside wiring can meet the demands of voice, video, and data transmissions now and for the foreseeable future.

Advanced telephone cables consisting of four twisted pairs of copper wire offer faster, higher quality transmission of data, voice, and fax signals. This so-called category-type wiring is now required inside homes and other buildings under a new FCC rule.

Category-type telephone cable consists of four twisted pairs of insulated copper wire and offers service benefits over old-style telephone cable, typically made up of two untwisted pairs, designed for analog voice service. The additional pairs of wires in category-type cable make it easier to hook up multiple phone lines and network home computers, and the precise twisting of the wires speeds communication while reducing static, signal degradation, and cross-talk between separate lines bundled together.

4.11 LOW-NOISE AND HIGH-POWER AMPLIFIER DESIGN

The block diagrams for LNAs and HPAs are given in Figure 4.19, where the design requires Γ_{on} or Γ_{op} of the transistor. A transistor has four noise parameters and four power parameters:

$$F = F_{\min} + \frac{R_n}{G_g|Y_g - Y_{on}|^2} \tag{4.87}$$

$$G_{LS} = G_{\max} - \frac{R_p}{G_L|Y_L - Y_{op}|^2} \tag{4.88}$$

where the four noise parameters are $F_{\min}$, G_{on}, B_{on}, and R_n and the four power parameters are $G_{\max}$, G_{op}, B_{op}, and R_p. Equation (4.88) is clearly an approximation, since the power contours for constant power in the Γ_L plane are usually elliptical, and the expression for gain is not valid at high power levels. Another form for the noise equation is

$$F = F_{\min} + \frac{4 \; R_n/Z_0|\Gamma_G - \Gamma_{0n}|^2}{G_g/Y_0 \; (1 - |\Gamma_G|^2)|1 + |\Gamma_{0n}|^2} \tag{4.89}$$

For LNAs you design for $F_{\min}$ by correctly matching the input for Γ_{0n} and conjugately matching the output for highest gain. We may ignore k since a low-noise design must be stable at the design frequency. The details of matching are covered in Chapter 5.

The design of HPAs is the dual. You design for $G_{\max}$ by matching the output for $\Gamma_L = \Gamma_{0p}$ and conjugately matching the input for highest gain. Again, we may ignore k since a high-power design is probably stable. Notice it is incorrect to design the output for a low value of S_{22}, a common error, unless you use lossless feedback, which is covered in Chapter 8. The conditions of stability are probably not correct since the small-signal S parameters are no longer applicable for the power amplifier in the high-power mode; hence we need a nonlinear analysis to investigate stability, a subject covered later in this book.

For low-noise designs, it is possible to introduce lossless feedback in the form of an inductor in the emitter (source) to bring Γ_{0n} closer to $S_{11}^{'*}$ [4.17]. In a similar fashion, introducing a capacitor in the emitter (source) will produce negative resistance at the base (gate) in order to design an oscillator. The same tricks apply to high-power amplifier designs, which will be discussed later.
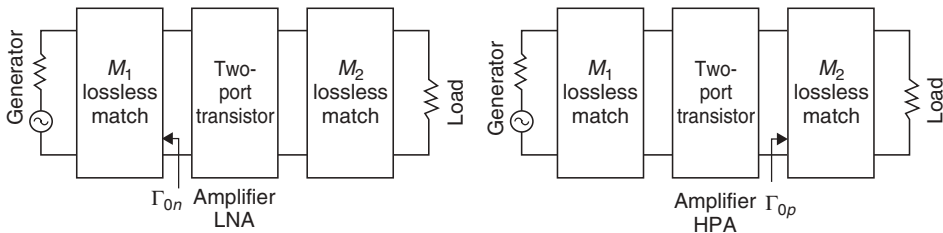
FIGURE 4.19   LNAs and HPAs.

The noise measure is defined as

$$M = \frac{F - 1}{1 - 1/G_A} \tag{4.90}$$

This allows us to calculate the total minimum noise figure of a cascaded amplifier using an infinite chain of identical devices from

$$F_{(tot)\,min} - 1 = \frac{F_{min} - 1}{1 - 1/G_A} = M_{min} \tag{4.91}$$

where the Friis equation for a cascaded amplifier calculates the total noise figure from

$$F_{tot} = F_1 + \frac{(F_2 - 1)}{G_{1A}} + \frac{F_3 - 1}{G_{A1}G_{A2}} + \cdots \tag{4.92}$$

We may also express noise figure in terms of equivalent noise temperature:

$$F = 1 + \frac{T_e}{T_0} \tag{4.93}$$

Another parameter is the invariant Lange parameter N [4.18] given by

$$N = R_{0n}G_n = G_{0n}R_n \tag{4.94}$$

which is invariant to lossless transformations (as is F_{min}). Some other useful noise limitations are given by the inequality [4.19, 4.20]

$$1 \le \frac{4\,NT_0}{T_{min}} < 2 \tag{4.95}$$

where the first inequality is fundamental [4.19] and occurs for i and u fully correlated and the second inequality comes from the model [4.20] and occurs for i and u uncorrelated. This inequality is important to verify because it may show the noise data is nonphysical or subject to measurement errors. The equation may be verified from the noise data provided on the data sheet by the manufacturer. The noise figure of a two-port is often represented by Figure 4.20, where u is the noise voltage referred
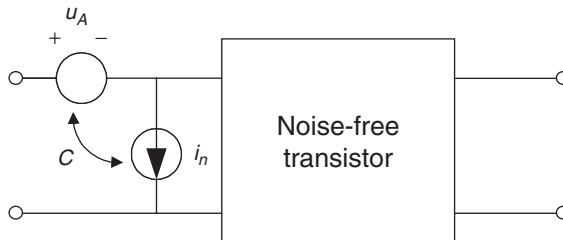
FIGURE 4.20 Noise sources for a noise-free transistor.
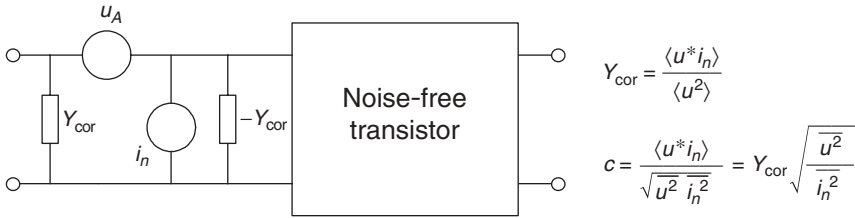
FIGURE 4.21   Redrawn noise sources using Y_{cor}.

to the input and i_n is the noise current referred to the input. The current generator is divided into a uncorrelated and correlated component by

$$i = i_n - Y_c u \qquad Y_c = \frac{\langle i u^* \rangle}{\langle u^2 \rangle} \tag{4.96}$$

so Figure 4.20 can be redrawn as Figure 4.21, where

$$Y_c = G_c + B_c \tag{4.97}$$

We can also state

$$Y_{0n} = G_{0n} + j B_{0n} = \left(\frac{G_n}{R_n} + G_c^2 \right)^{1/2} - j B_c \tag{4.98}$$

$$\langle i_n^2 \rangle = 4 k T_0 G_n \ \Delta f \qquad (\text{A}^2) \tag{4.99}$$

$$\langle u^2 \rangle = 4 k T_0 R_n \ \Delta f \qquad (\text{V}^2) \tag{4.100}$$

$$F = F_{\min} + \frac{R_n}{G_g |Y_g - Y_{0n}|^2} \tag{4.101}$$

$$N = G_{0n} R_n \tag{4.102}$$

where N is invariant to lossless networks, which means the imaginary part B_{0n} is not important. By definition of T_e,

$$F = 1 + \frac{T_e}{T_0} \tag{4.103}$$

We want to prove Eq. (4.95). From above eqns,

$$1 + \frac{T_{\min}}{T_0} = 1 + 2 R_n (G_c + G_{0n})$$

$$\frac{T_{\min}}{T_0} = 2 R_n (G_c + G_{0n}) = 2 R_n G_c + 2N \tag{4.104}$$

There are two cases to consider. The first is i and u are fully correlated, $i_n = 0$, and therefore $G_n = 0$ and $N = G_{0n} R_n$. From (4.87) $G_{0n} = G_c$, so $N = R_n G_{0n} = R_n G_c$.

From (4.93)

$$\frac{T_{\min}}{T_0} = 4N \tag{4.105}$$

$$\frac{4NT_0}{T_{\min}} = 1 \tag{4.106}$$

which is the left-hand equality. The second case is for i and u uncorrelated. Then $i_n \neq 0$, $G_c = 0$, $G_n \neq 0$. From (4.98) $G_{0n} = (G_n/R_n)^{1/2}$; from (4.104)

$$\frac{T_{\min}}{T_0} = 2N \qquad \frac{4NT_0}{T_{\min}} = 2 \tag{4.107}$$

From (4.106) and (4.107) we have $1 \leq 4NT_0/T_{\min} < 2$, which completes the proof. From the noise data provided for the transistor, one should verify this expression is satisfied; otherwise something is wrong with the data.

4.12   LOW-NOISE AMPLIFIER DESIGN EXAMPLES

The first low-noise design example is a three-stage 10-GHz monolithic microwave integrated circuit (MMIC) produced at Texas Instruments (TI) under the MMIC program [4.21]. This circuit uses a 335-µm by 0.5-µm gate MESFET, all stages biased at the same low-noise dc biasing point, $V_{ds} = 3$ V, $I_{ds} = 15$ mA. The I_{dss} is 90 mA, a typical value for this size transistor. The low-noise bias point is about $0.15I_{dss}$, or 14 mA, so the bias point has been set for low noise. The use of inductive feedback brings the noise match to the same point as the gain match [4.17], that is, we can make $S_{11} = 0$ for the LNA.

The nonlinear model for the MESFETs is given in Table 4.6, where the modified Materka model is used; this model was developed by Raytheon and Compact Software during the MMIC program. This amplifier has been designed for both lumped and distributed elements ($Z_0 = 83$ Ω) for demonstration purposes. It was only built as the TI EG8021 in distributed form. The transmission line elements use a line width of

TABLE 4.6   Modified Materka Nonlinear Model for 335-µm MESFET: Hewlett-Packard/Agilent ADS Format

IDSS	0.103	Cgs	0.467×10^{-12}
Vt0	-2.9	Gdcap	3
Beta2	-0.09	Cgd	0.0147×10^{-12}
Ee	1.41	Rd	4.45
Ke	-0.125	Rg	2.15
Kg	-0.268	Rs	1.5×10^{-9}
Si	0.158	Ls	0.012×10^{-9}
Ss	-0.002	Cds	0.07×10^{-12}
Tau	3.3×10^{-12}	Vbr	14
Gscap	3		

1.0 mil on 6-mil-thick GaAs, which is a characteristic impedance of 83 Ω. The 50-ΩS parameters of interest are

$$S = \begin{bmatrix} 0.87\underline{/-108} & 0.075\underline{/29°} \\ 2.08\underline{/93°} & 0.82\underline{/-35°} \end{bmatrix}$$

$$Z_{in} = 5 - j36 \quad \Omega \qquad Z_{out} = 50 - j250 \ \Omega$$

The input C_{gs} is about 0.4 pF or $-j35$ Ω. We cancel about half of this with a source inductance of 0.3 nH, $j\omega L_{s1} = j20$ Ω. The second stage uses about 0.15 nH in the source to keep the gain higher. The input design is illustrated in Figure 4.22 on a
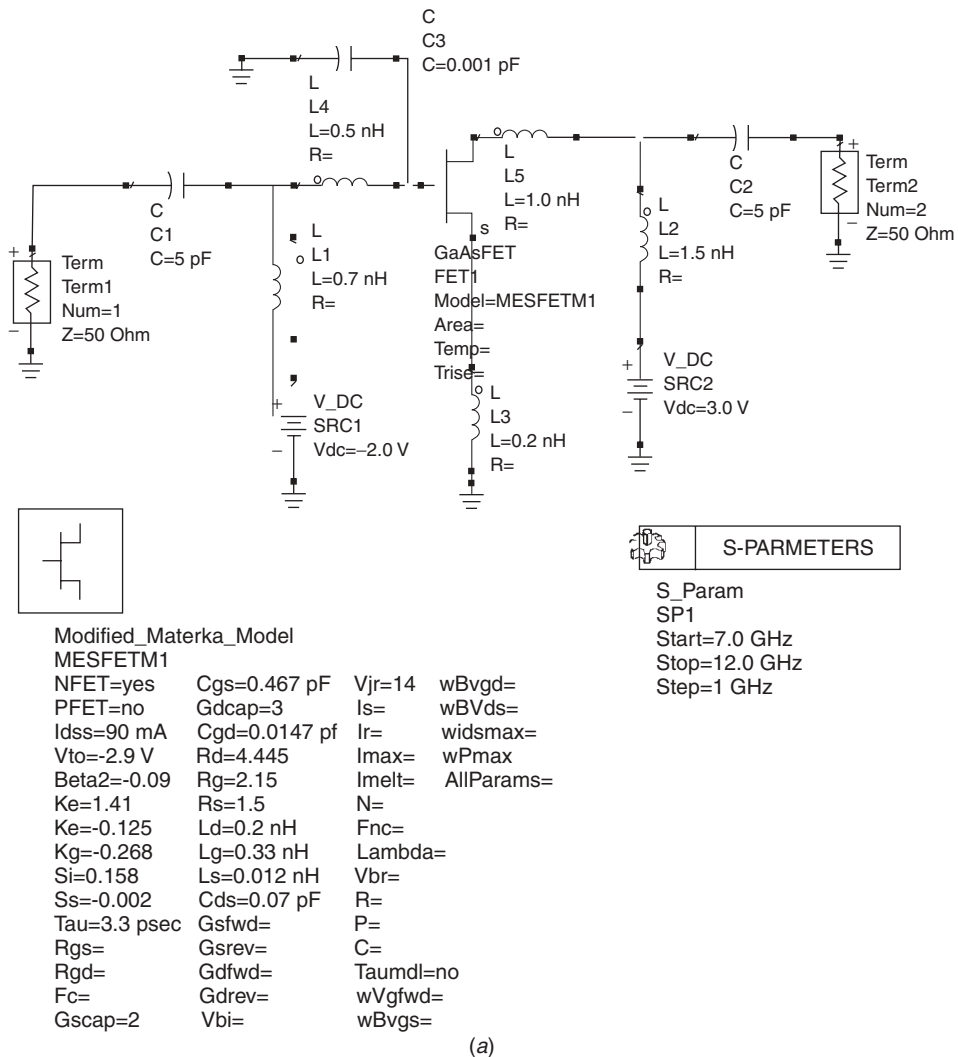
FIGURE 4.22   Input noise design for EG8021: (*a*) one-stage noise design.

m5
freq = 4.000 GHz
nf(2) = 3.032

m1
freq=4.000 GHz
dB(S (2,1))=9.224

m3
freq=4.000 GHz
S(1,1)=0.428 / 50.299
impedance = Z0 ∗ (1.283 + j1.036)

m2
freq=4.000 GHz
S(2,2)=0.064 / −90.964
impedance = Z0 ∗ (0.990 − j0.128)

m1
freq=4.000 GHz
Sopt=0.098 / −7.903
impedance = Z0 ∗ (1.215 − j0.033)
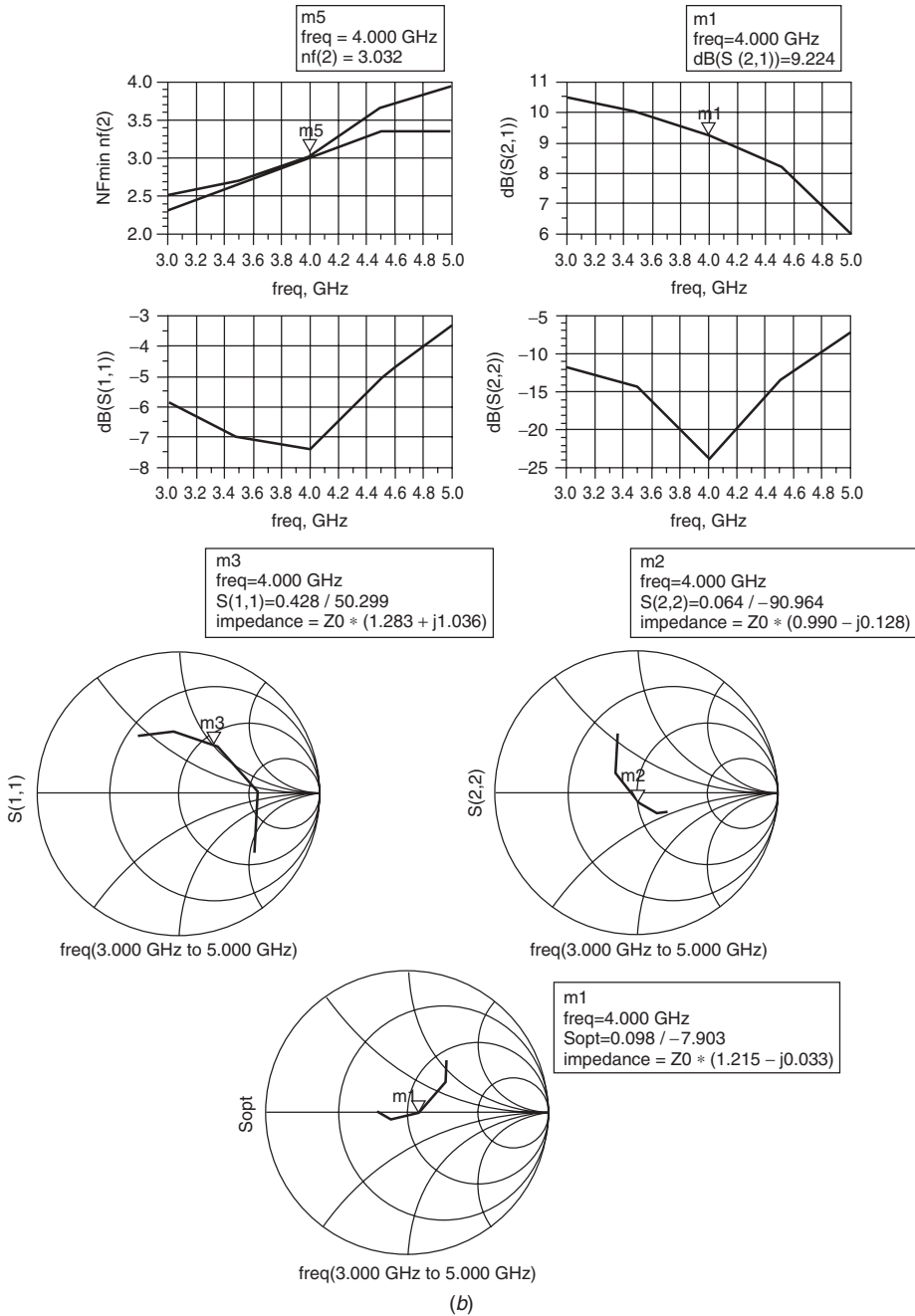
FIGURE 4.22 (*b*) performance of one-stage design. (*continued*)

Smith chart normalized to $Z_0 = 83 \ \Omega$. We first find point A, which is $Z_{in}/83$, and then match to the 50-Ω generator impedance, where $50/83 = 0.6$. We use a two-element match which is always labeled alphabetically for illustrative purposes. The Smith chart matching is explained in Chapter 5.

The pertinent calculations for matching S_{11} are

$$\frac{Z_{\text{in}}}{83} = \frac{5 - j36}{83} = 0.0602 - j0.434$$

$$S_{11}(83) = 0.90 < -133 \quad \text{(point A)}$$

$$2\beta l_1 = 12 \quad \text{Equivalent } L = 0.22(83)/6.28 \ 10 = 0.29 \text{ nH}$$

$$Y_{\text{in}} = 1 + j3.0$$

$$Y_{\text{stub}} = -j3.0$$

$$2\beta l_2 = 37 \quad \text{Equivalent shunt } L = 1/[3.6 \ (1/83)]6.28 \ 10 = 0.367 \text{ nH}$$

The source inductance was ignored in this calculation, since the values are optimized by the computer for the final design. The lumped element and distributed three-stage designs are given in Figures 4.23 and 4.24. To understand the distributed design, calculate the guide wavelength as follows:

$$\lambda_g = \frac{c}{f \ (k')^{1/2}} = \frac{30}{10 \times 2.54 \ (7.4)^{1/2}} = 0.434 \text{ in.} \qquad \frac{\lambda_g}{8} = 54 \text{ mils}$$

which is equivalent to an inductor of

$$L = \frac{83}{2\pi \ 10} = \frac{8.3}{6.28} = 1.3 \text{ nH}$$

If the first stage alone is optimized with distributed elements, the gain is 9.9 dB and the noise figure is 2.26 dB. For the full three-stage distributed amplifier, the gain was 27 dB and the noise figure was 2.9 dB. The lumped-element designs gave about 0.5 dB more gain with essentially the same noise figure.

The calculated performance of these amplifiers is given in Figures 4.25 and 4.26 using either Serenade (or Design Suite) or ADS. Normally the lumped-element design will give better performance, that is, higher gain and more bandwidth.

A second design example of a single-stage Si BJT LNA without the use of feedback will illustrate the more conventional approach to the design of LNAs. Consider a 4-GHz LNA with an AT41400 Agilent Si BJT for minimum noise figure. The parameters of interest are [4.1]

$$V_{CE} = 8\text{V} \qquad I_C = 10 \text{ mA} \qquad F_{\text{min}} = 3.0 \text{ dB} \qquad \Gamma_{0n} = 0.72 \underline{/-156} \qquad R_n = 16 \ \Omega$$

$$S = \begin{bmatrix} 0.61\underline{/152} & 0.099\underline{/79} \\ 1.89\underline{/55} & 0.47\underline{/-30} \end{bmatrix}$$

or using the ADS *S*-parameter library, which is more recent,

$$V_{CE} = 8\text{V} \quad I_C = 10 \text{ mA} \quad F_{\text{min}} = 3.0 \text{ dB} \quad \Gamma_{0n} = 0.52\underline{/-153} \quad R_n = 9.0 \ \Omega$$

and the same *S* parameters. It usually turns out that the $|\Gamma_{0n}|$ is less than $|S_{11}|$ and the angle is about the conjugate of S_{11}. This is a good check on your data. For this example we often use ADS and the noise parameters in the ADS *S*-parameter library.
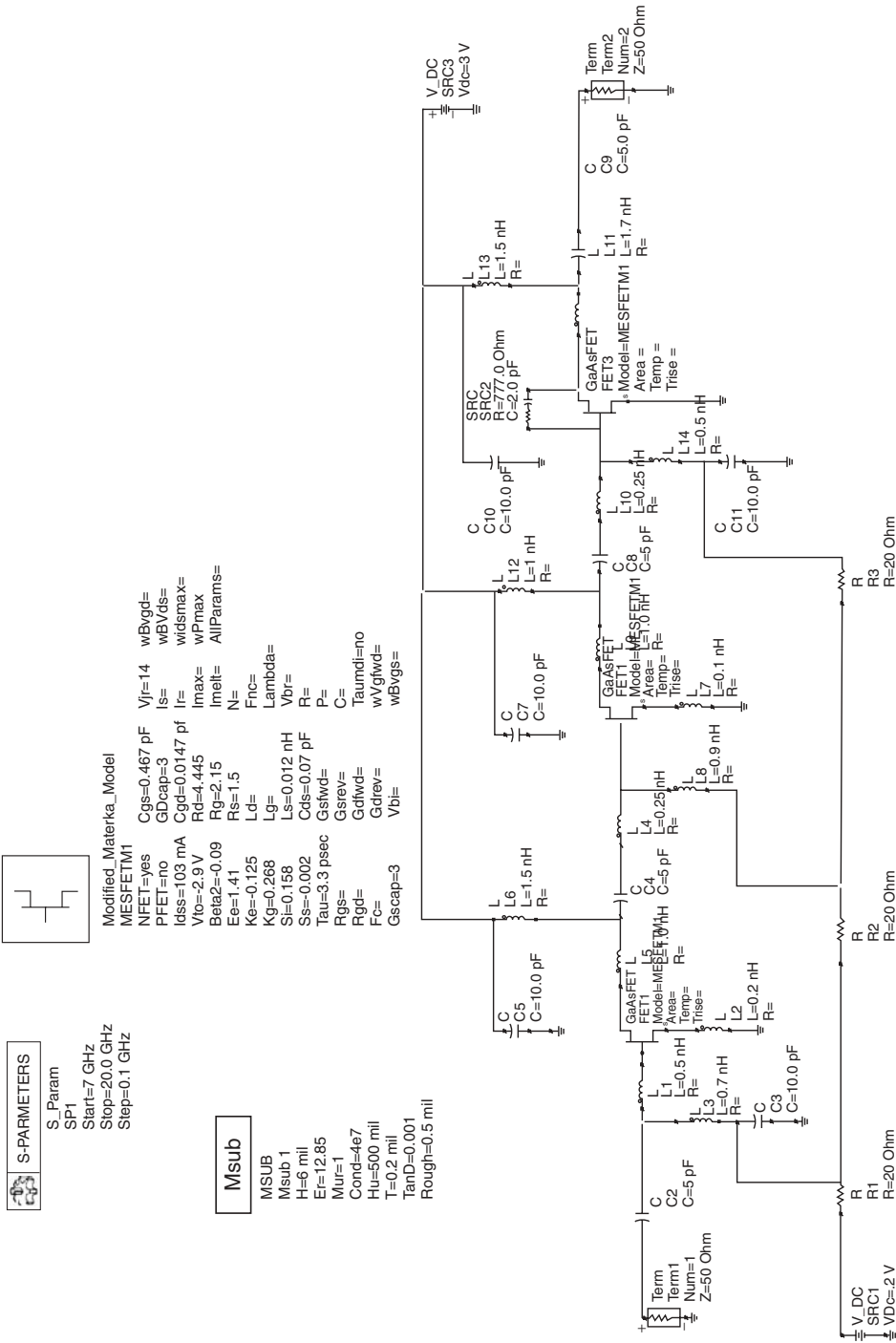
FIGURE 4.23 Three-stage lumped design.
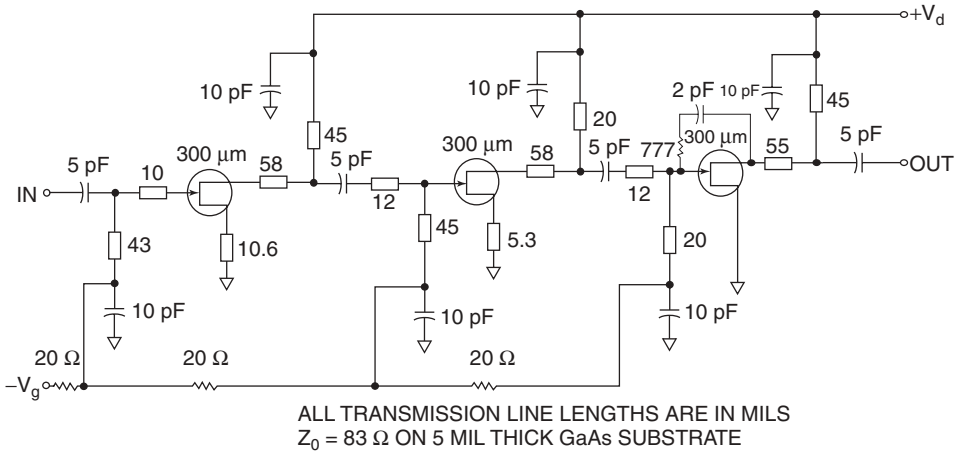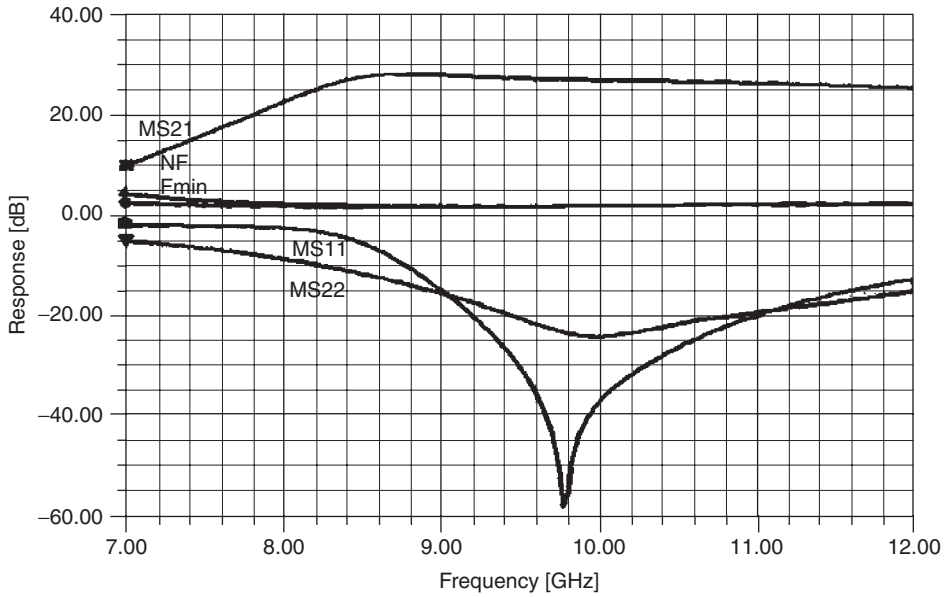
FIGURE 4.24   Three-stage distributed design using linear CAD approach.

Design M_1 by matching Γ_{0n}^* to 50 Ω. This technique presents Γ_{0n} looking at the base toward the generator. Using lumped elements, the design is given in Figure 4.27, where the output M_2 matches S_{22}' to the 50-Ω load, where

$$S_{22}' = S_{22} + \frac{S_{12}S_{21}\Gamma_{0n}}{1 - S_{11}\Gamma_{0n}} = 0.64 < -30$$

which always has a magnitude larger than $|S_{22}|$.
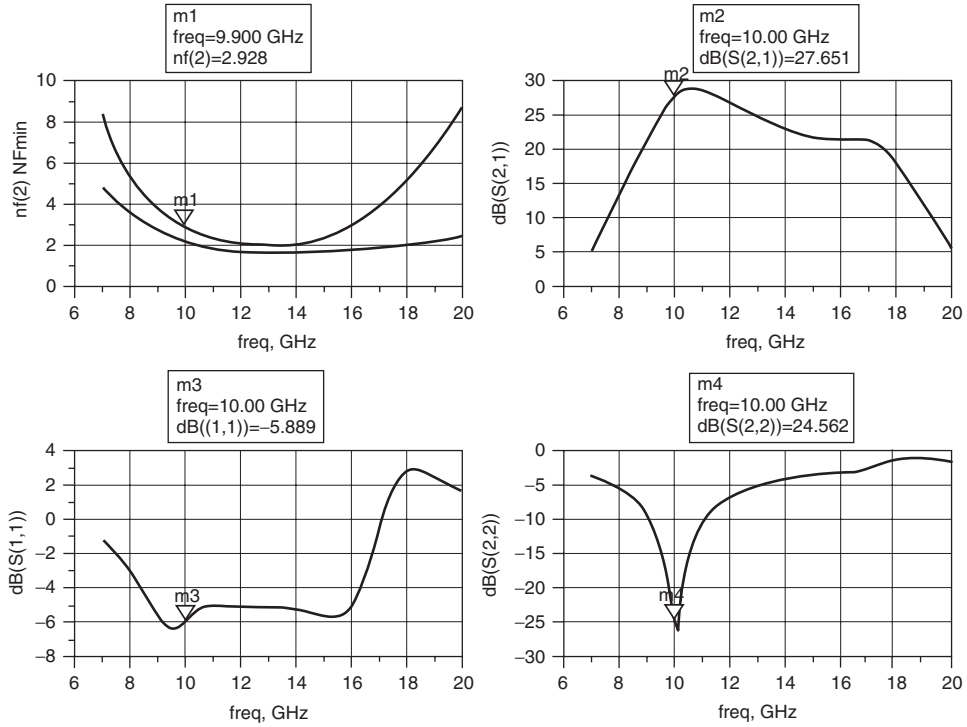
FIGURE 4.25   ADS-simulated performance of three-stage lumped design.
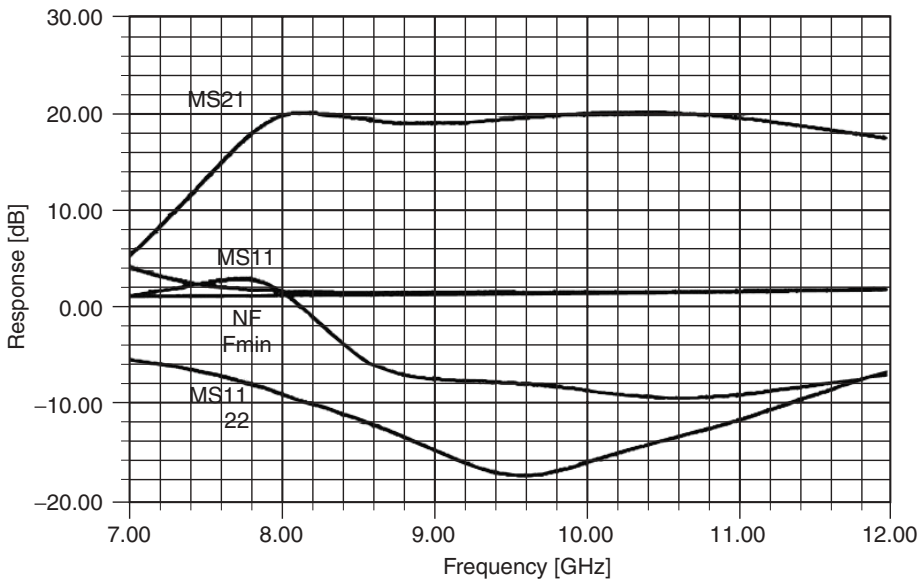
FIGURE 4.26   Prediction of the three-stage distributed design using nonlinear parameters (Materka model) for the FET. The prediction agrees with the actual measurements. In particular, gain and noise agree extremely well.
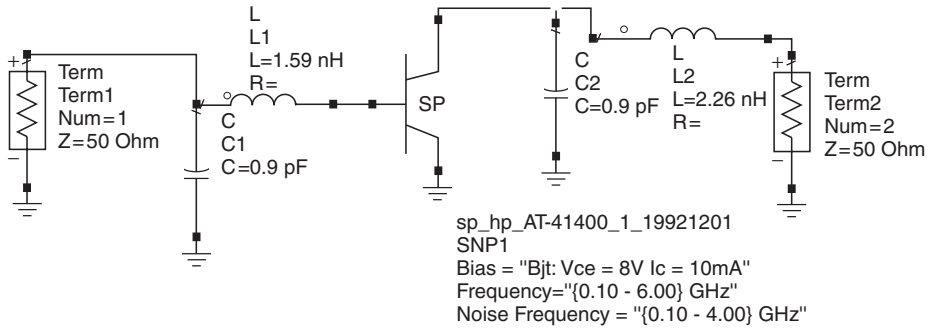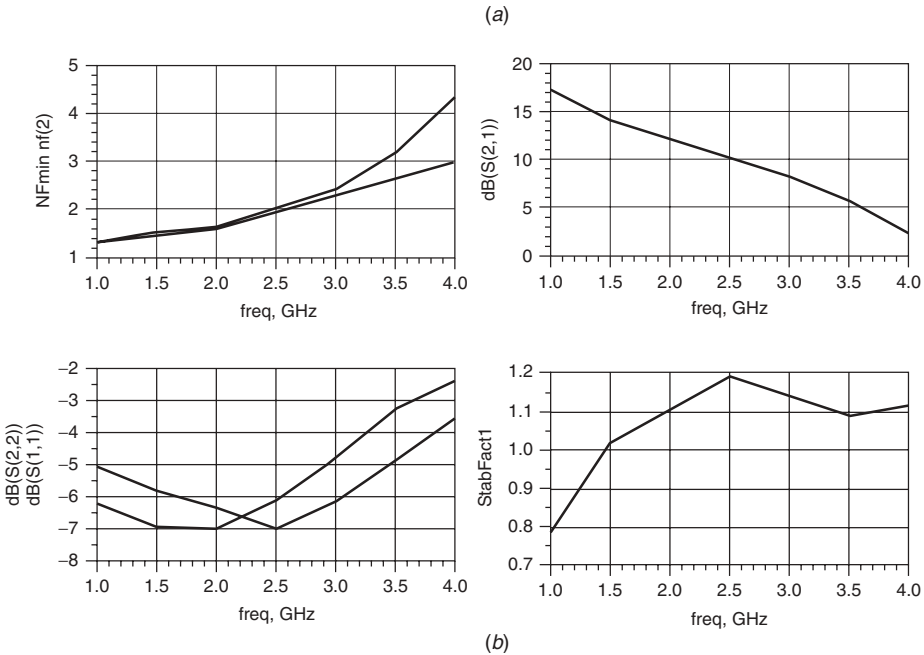
FIGURE 4.27 BJT LNA at 4 GHz: (*a*) schematic; (*b*) performance.

This amplifier has a noise figure of 3.0 dB and a gain of

$$G_T = G_A = \frac{|S_{21}|^2(1 - |\Gamma_{0n}|^2)}{|1 - S_{11}\Gamma_{0n}|^2(1 - |S'_{22}|^2)} = 3.06 = 9.9 \text{ dB}$$

where $|S_{22}| = 0$ but $|S_{11}| = 0.42 > 0$. The problem is that $|S_{11}| > 0$ may be solved by adding feedback or going to a balanced amplifier, as discussed in Chapter 8. Sometimes

there is a trade-off between F and $|S_{11}|$, which is an excellent problem for the computer, especially if there is a significant bandwidth.

Since the stability factor for this example is 1.12, it is also possible to design this amplifier for G_{ma}, which is

$$G_{ma} = \frac{|S_{21}|}{S_{12}|}(k - \sqrt{k^2 - 1}) = 11.8 = 10.7 \text{ dB}$$

In this case, Γ_G is given by [4.1]

$$\Gamma_G = \Gamma_{Gm} = \left(\frac{C_1^*}{|C_1|}\right)\left(\frac{B_1}{2|C_1|} - \sqrt{\frac{B_1^2}{|2C_1|^2 - 1}}\right) \tag{4.108}$$

$$B_1 = 1 - |S_{22}|^2 + |S_{11}|^2 - |D|^2 \tag{4.109}$$

$$C_1 = S_{11} - DS_{22}^* \tag{4.110}$$

which gives $B_1 = 1.14$ and $C_1 = 0.561\underline{/154°}$. Therefore, $\Gamma_{Gm} = 0.84\underline{/-154°}$, which is about S_{11}^*. The magnitude of Γ_{Gm} is always greater than $|S_{11}|$ for physical transistors. I offer no proof of this observation, except it has always been true for more than 40 years of my calculations. A similar set of equations holds for Γ_{Lm} [4.1]. To calculate the noise figure, we need to find Y_G and Y_{0n}, which involves the Smith chart, giving

$$Y_{0n} = Y_0(0.09 - j0.21)$$

$$Y_G = Y_0(0.09 - j0.23)$$

and therefore $F = 2.00142 = 3.01$ dB. This demonstrates that this transistor has ideal properties for low noise and high gain at 4 GHz.

It should be noted that the design of HPAs is the dual of the above designs, where the designer needs to know Γ_{0p} for the output design and then match the input for a conjugate match, If Γ_{0p} is unknown, it can be estimated from the curve tracer response and the dc bias point by drawing the expected load line over the expected dynamic range. For example, if a high-power design is needed from the AT-414 BJT biased at $V_{CE} = 8.0$ V and $I_C = 30$ mA, the change in V_{CE} is about $8 - 1 = 7$ V, the change in I_C is about 30 mA, so the desired load at the collector–emitter port is $7/.03 = 233$ Ω, which requires a matching circuit to convert the 50-Ω load to 233 Ω. There are many solutions to this problem, as shown in Chapter 5. The expected power at P_1dBc is $(7 \times 0.03)/2 = 105$ mW. A nonlinear analysis is needed for the final design of the high-power amplifier.

In this chapter we have given the basic two-port parameters in several equivalent forms, the voltage gain, the current gain, and the power gains. We have illustrated the design of several amplifiers, including enhancement-mode PHEMTs at 3 GHz, a three-stage TI MMIC amplifier at 10 GHz, and a silicon BJT amplifier for low noise and high gain at 4 GHz. All of these design examples use ideal lumped elements. In the next chapter we discover the methods for doing the impedance matching.

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PROBLEMS

4.1 Derive the S parameters of the following FET model (omiting L_g, L_s, L_d) for $\tau_d = 0$ at $f = 4$ GHz.

$g_m = 0.04$ S
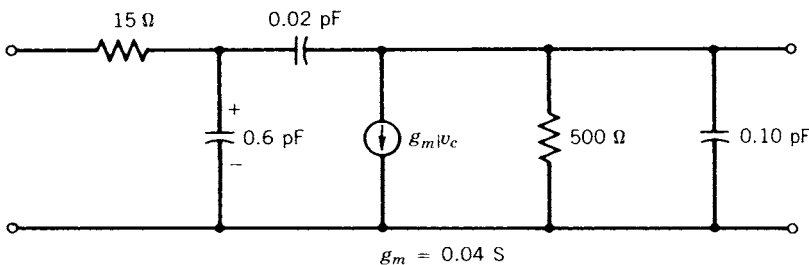
4.2 Given the S parameters of an AT-41400 chip at a bias of $V_{CE} = 8$ V, $I_c = 25$ mA, and $f = 4.0$ GHz;

$$S = \begin{bmatrix} 0.60 \; \underline{/149°} & 0.108 \; \underline{/83°} \\ 2.06 \; \underline{/57°} & 0.42 \; \underline{/-28°} \end{bmatrix}$$

(a) Design the RF schematic of a high-gain amplifier. What is the transducer gain, G_T? Use distributed elements.

(b) Design the dc bias circuit using only resistors; repeat using a *pnp* transistor for active bias. Assume two power supplies with $V_1 = +5$ V and $V_2 = -5$ V.

(c) Draw the complete RF and dc schematic for both of the dc circuits above.

4.3 Consider a frequency-variable tee attenuator over 6 to 12 GHz. Make an attenuator which has 6 dB loss at 6 GHz and 0 dB loss at 12 GHz.

4.4 Given the three-port Y parameters of a transistor, where 1 is the base, 2 is the collector, and 3 is the emitter, find the CE, CB, and CC y parameters:

$$Y = \begin{bmatrix} 0.4 \; \underline{/90°} & 0.1 \; \underline{/45°} & 0.4760 \; \underline{/-81°} \\ 2 \; \underline{/45°} & 0.5 \; \underline{/-45°} & 2.0614 \; \underline{/-149°} \\ 2.30 \; \underline{/-128°} & 0.511 \; \underline{/146°} & 2.3185 \; \underline{/65°} \end{bmatrix}$$

Notice the summation of all rows and columns are zero.

4.5 Given the CE S parameters of a transistor, find the CB and CC S parameters:

$$S = \begin{bmatrix} 0.5 \; \underline{/-60°} & 0.1 \; \underline{/45°} \\ 2.0 \; \underline{/45°} & 0.4 \; \underline{/-30°} \end{bmatrix}$$

Find the three-port S-parameters, where 1 is the base, 2 is the collector, and 3 is the emitter.

4.6 Given Eqs. (4.73) and (4.74) in the text, derive the relations for S_{d1d1} and S_{d2c1} in terms of the single-ended S parameters.

4.7 Consider the measurement of a balanced amplifier-driven small signal. Some of the single-ended S parameters were $S_{31} = 5.0 \underline{/0}$, $S_{41} = 5.0 \underline{/180}$, $S_{32} = 5.0 \underline{/179}$, $S_{42} = 5.0 \underline{/0}$ (magnitudes are linear, angles are in degrees).

(a) Calculate $|S_{d2d1}|$ and $|S_{c2d1}|$ in decibels.

(b) Typical measurement uncertainties on a transmission parameter at a few gigahertz might be .05 dB and 0.5°. Assuming only S_{41} has uncertainties applied to it (the others are considered perfect), what are the possible range of values of $|S_{c2d1}|$ (in decibels)?

(c) Which aspect of the measurement, magnitude or phase, would warrant extra care assuming the above uncertainties represent a measurement made with average skill in both respects?

4.8   Consider the BJT LNA given in Figure 4.27. Calculate the A_v, A_i, G_m, and Z_m for the transistor. Note:

$$G_m = y_{21} + y_{22}A_v \qquad Z_m = z_{21} + z_{22}A_i$$

4.9   **(a)** Using an ATF-13135 GaAs FET at $V_{GS} = -1.5$ V, $V_{DS} = 3$ V, and $I_{DS} = 20$ mA, design a two-stage low-noise amplifier at 12 GHz using distributed elements. What is the transducer gain and noise figure of this amplifier?

   (b) With a power supply of -12 V, design a dc bias circuit.

   (c) Give the complete RF and dc schematic diagram.

   (d) Explain what you need to do to convert this design to a high-gain amplifier (do not redesign it); what is the new gain and the new noise figure?

$$S = \begin{bmatrix} 0.61 \;\underline{/37°} & 0.144 \;\underline{/-89°} \\ 2.34 \;\underline{/-84°} & 0.15 \;\underline{/46°} \end{bmatrix}$$

$$F_{\min} = 1.2 \text{ dB} \qquad \Gamma_{0n} = 0.47 \;\underline{/-65°} \qquad R_n = 40 \;\Omega$$

4.10   Using the NEC-67383, design a single-stage LNA for 2.4 GHz using the following topology:
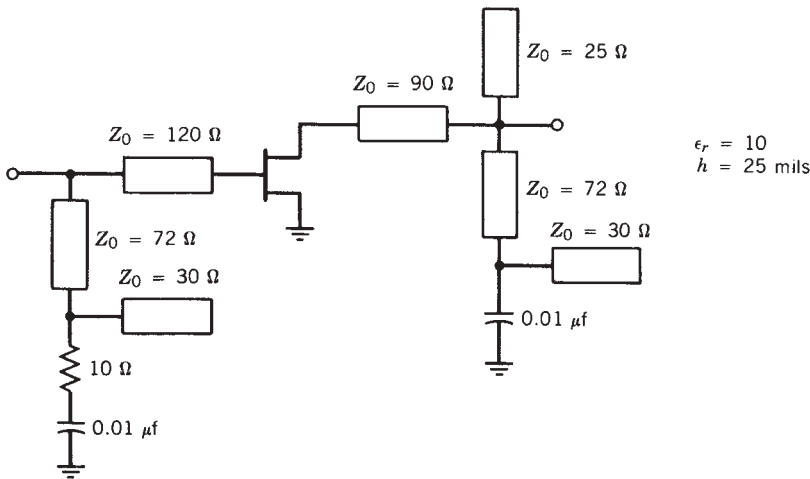
S parameters ($V_{DS} = 3$ V, $I_D 10$ mA):

Frequency (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
2.0	0.97	−46	3.30	136	0.020	70	0.63	−33
2.4	0.96	−53	3.30	132	0.029	64	0.62	−38
3.0	0.93	−60	3.0	118	0.045	50	0.62	−48
4.0	0.88	−79	2.64	107	0.06	35	0.61	−58

Noise parameters ($V_{DS} = 3$ V, $I_D = 10$ mA):

Frequency (GHz)	Γ_{0n}		R_n/Z_0	F_{min} (dB)
	Magnitude	Angle		
2.0	0.69	21	0.58	0.3
2.4	0.65	24	0.58	0.4
3.0	0.60	31	0.57	0.5
4.0	0.60	50	0.51	0.6

(a) Calculate the gain and noise figure of your design.

(b) Using a computer, calculate the gain and noise figure over the range 2 to 3 GHz. The goal is a noise figure of 0.8 dB maximum over the band.

4.11 Design an amplifier using the following data for the highest gain:

$$S = \begin{bmatrix} 0.65 \ \underline{/110°} & 0.10 \ \underline{/23°} \\ 1.96 \ \underline{/2°} & 0.36 \ \underline{/-93°} \end{bmatrix} \qquad \begin{array}{l} k = 1.149 \\ f = 4 \text{ GHz} \\ G_{ma} = 10.59 \text{ dB} \end{array}$$

$$\varepsilon_r = 2.56 = k \text{ (relative dielectric constant)}$$
$$h = 0.031 \text{ in.}$$
$$V_{CE} = 8 \text{ V}$$
$$I_c = 10 \text{ mA}$$
$$V_{CC} = +15 \text{ V (power supply)}$$

(a) Give the RF design using lossless microstrip lines.

(b) Give the dc design.

(c) Draw the complete RF and dc schematic.

(d) From the microstrip line design charts (Figs. 1.24 and 1.25), give the width and length of each matching element.

4.12 A feedback amplifier was designed with the following transistor at 8 GHz. Using a y-parameter analysis, find the transducer power gain $|S_{21}|^2$ of the amplifier in decibels. What is S_{11} and S_{22} of the amplifier?
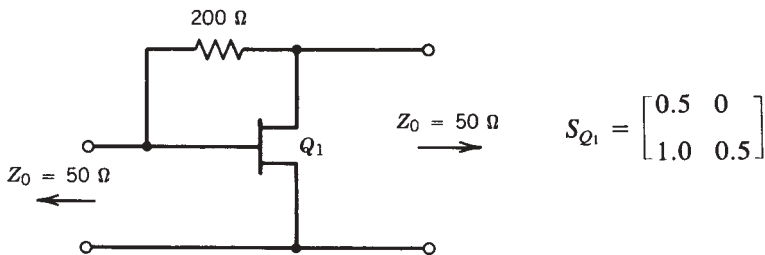
4.13 The S parameters of a GaAs MESFET are given below at $f = 8$ GHz. Find the stability factor k and G_{ma} and G_{ms} in decibels. Design an amplifier using distributed elements for $h = 25$ mils, $\varepsilon_r = 10$. Give the dimensions of each matching element (length and width). Include a method of dc biasing the transistor. What is the gain of the amplifier? Draw a complete RF and dc schematic of the amplifier for $V_{DD} = 15$ V.

$$S = \begin{bmatrix} 0.8 \ \underline{/180°} & 0.01 \ \underline{/0°} \\ 1 \ \underline{/90°} & 0.6 \ \underline{/-90°} \end{bmatrix}$$

$$V_{DS} = 5 \text{ V} \qquad V_{GS} = -1.5 \text{ V} \qquad I_{DS} = 0.03 \text{ A}$$

4.14 **(a)** Design a 4-GHz LNA (low-noise amplifier) using the following packaged FET and lossless microstrip lines. Give the complete RF and dc schematic. Give the width and length of each matching element.

$$S = \begin{bmatrix} 0.65 \ \underline{/-145°} & 0.125 \ \underline{/7°} \\ 3.34 \ \underline{/58°} & 0.37 \ \underline{/-84°} \end{bmatrix}$$

Power supply $= -12$ V

$$F_{\min} = 0.80 \text{ dB} \qquad V_{DS} = 3 \text{ V}$$

$$\Gamma_{0n} = 0.46 \ \underline{/143°} \qquad I_{DS} = 20 \text{ mA}$$

$$R_n = 12 \ \Omega \qquad V_{GS} = -1.0 \text{ V}$$

Assume that a low-noise design is stable.

$$\varepsilon_r = 2.56 = k \qquad h = 0.031 \text{ in.}$$

  (b) Redesign the input with lossless lumped elements.
  (c) What is the gain of this amplifier (transducer power gain) in decibels?

4.15 Design a two-stage low-noise amplifier using the following GaAs FET at $f = 8$ GHz using microstrip line matching elements:

$$S = \begin{bmatrix} 0.7 \ \underline{/-135°} & 0.01 \ \underline{/60°} \\ 1.4 \ \underline{/45°} & 0.6 \ \underline{/-90°} \end{bmatrix}$$

$$_F\min = 2 \text{ dB} \qquad V_{DS} = 4 \text{ V}$$
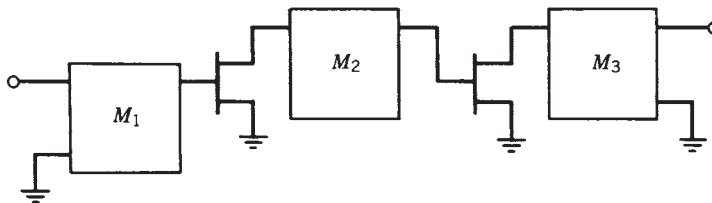
$$\Gamma_{0n} = 0.6 \underline{/135°} \qquad I_{DS} = 20 \text{ mA}$$

$$R_n = 25 \text{ Ω} \qquad V_{GS} = -1.5 \text{ V}$$

(a) Calculate k and G_{ma} or G_{ms} in decibels.
(b) Design M_1 for a low-noise figure.
(c) Design M_2 for a low-noise figure (assume that $S_{12} = 0$, if convenient).
(d) Design M_3 for gain (assume $S_{12} = 0$).
(e) Calculate the amplifier noise figure.
(f) Calculate the amplifier transducer gain.
(g) Design the bias circuit for $V_{DD} = 15$ V.
(h) Draw the complete amplifier schematic.

4.16 A two-stage low-noise amplifier is to be designed for the minimum possible noise figure. The noise parameters and S parameters are given below (at the low-noise bias point). Design M_1, M_2, and M_3 using transmission line matching circuits. Calculate the total amplifier noise figure and the total amplifier transducer power gain.
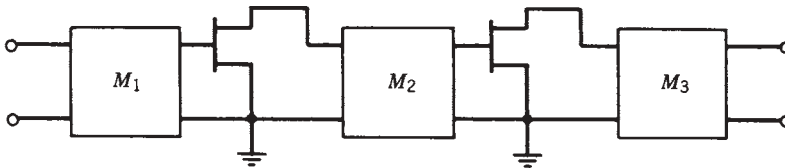
$$f = \text{GHz} \qquad Z_0 = 50 \text{ Ω}$$

Noise parameters:

$$F_{\min} = 3 \text{ dB}$$

$$R_n = 30 \text{ Ω}$$

$$\frac{Y_{0n}}{Y_0} = 0.23 - j0.55$$

$$S = \begin{bmatrix} 0.8 \underline{/-60°} & 0 \\ 1.414 \underline{/60°} & 0.9 \underline{/-50°} \end{bmatrix}$$

4.17 Using the AT-10600 FET at 3 V, 10 mA, with low-noise bias, design a four-stage distributed amplifier for 1 to 18 GHz.
(a) Use C_{ADDED} in the drain to equalize the phase velocities.
(b) Use L_1 in series with the drain to equalize the phase velocities.

$$G = 6 \pm 0.7 \text{ dB} \qquad |S_{11}| < 8 \text{ dB Return Loss}$$

$$\text{NF} < 8 \text{ dB} \qquad |S_{22}| < 8 \text{ dB Return Loss}$$

4.18 Using the AT-8251 GaAs MESFET at $V_{ds} = 5$ V, $I_d = 50$ mA, and $f = 4$ GHz, design a one-stage high-power amplifier for maximum dynamic range. Estimate the gain, the dynamic range, and the spurious-free dynamic range.

$$R_p = 15 \ \Omega \qquad R_n = 35 \ \Omega$$

$$G_{\max} = 12 \ \text{dB} \qquad F_{\min} = 1.0 \ \text{dB}$$

$$\Gamma_{0p} = 0.3 < 18 \qquad \Gamma_{0n} = 0.5 \ \underline{/60}$$

$$P_{1 \ \text{dBc}} = 21 \ \text{dBm}$$

4.19 Using the AT-8251 GaAs MESFET at $V_{ds} = 3$ V, $I_d = 20$ mA, and $f = 8$ GHz:
  (a) Design a one-stage low-noise amplifier with $\Gamma_{\text{out}} = 0$; give the gain and noise figure and Γ_{in}.
  (b) Design a one-stage low-noise amplifier with $\Gamma_{\text{in}} = 0$; give the gain and noise figure and Γ_{out}.
  (c) Repeat design with Γ_{out} and Γ_{in} both low; give the gain and noise figure.

CHAPTER 5

IMPEDANCE MATCHING

5.1 INTRODUCTION

This chapter describes more of the tools needed for RF/microwave design, including the impedance matching techniques using a Smith chart. The match is accomplished using lossless elements, either lumped or distributed. For a two-element match, we use an L network. Sometimes the match may be done with a single lumped or distributed element. Examples of these techniques will be illustrated in this chapter, including broadbanding techniques.

5.2 SMITH CHARTS AND MATCHING

The most important tool for the microwave designer is the Smith chart, or transmission line calculator, which was first presented in the United States by Philip Smith in 1939 [5.1, 5.2]. Prior to this date, the same chart was published in 1937 in Japan (in Japanese) by T. Mizuhashi [5.3], thus giving it the name Mizuhashi–Smith chart [5.4], usually shortened to Smith chart in most of the literature. This is a bilinear transformation between the infinite Z or Y plane to the finite reflection coefficient plane. The relevant equations are

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{5.1}$$

$$\frac{Z}{Z_0} = \frac{1 + \Gamma}{1 - \Gamma} \tag{5.2}$$

The Smith charts for $|\Gamma| = 1$ and $|\Gamma| = 3.16$ (or 10 dB) are given in Figure 5.1. The first is used for passive impedance matching, and the second (a compressed Smith chart) is useful for negative resistance (oscillators). The scale for $|\Gamma|$ is given at the bottom left side of the chart, where $0 < |\Gamma| < 1$.

Impedance matching uses lossless elements (lumped or distributed) to move any point in the $Z-Y$ plane to any other point, usually the center of the Smith chart,
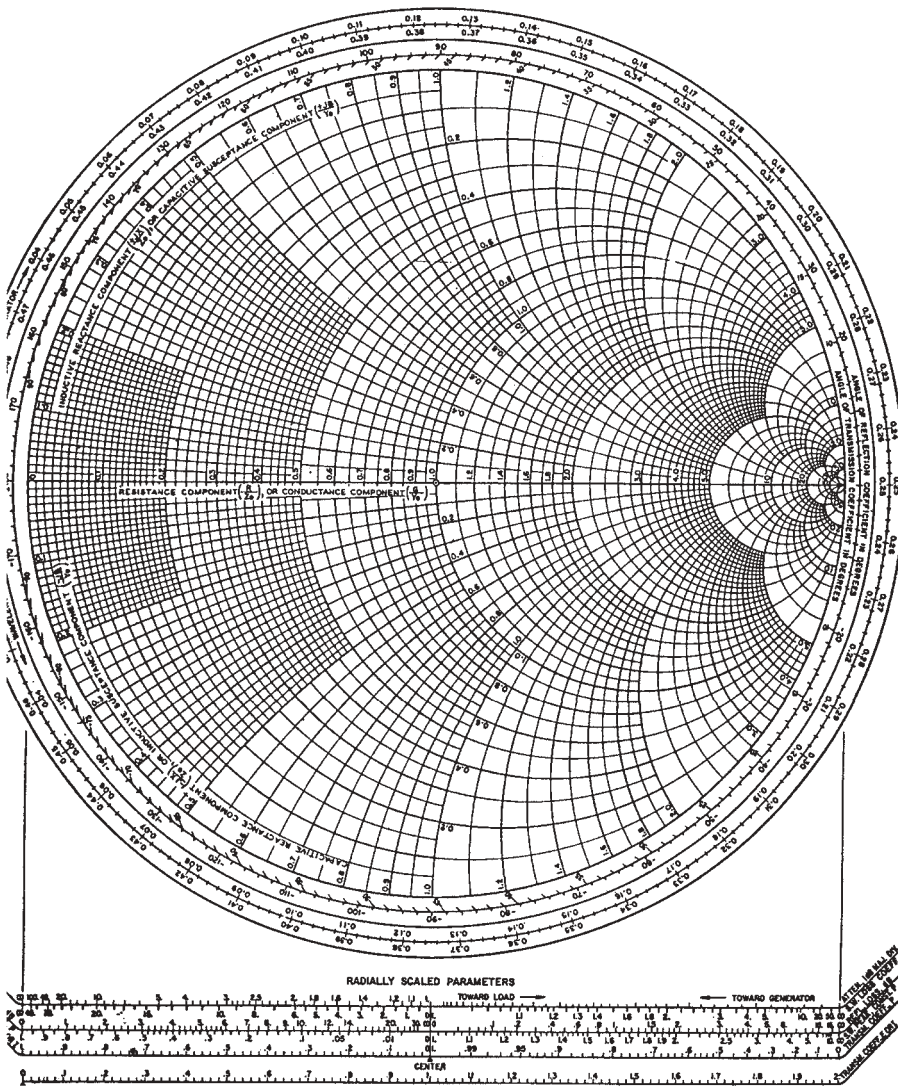
(a) $|\Gamma| = 1.0$

FIGURE 5.1   Smith charts. (a) $|\Gamma| = 1.0$.

(*b*) |Γ| = 3.16
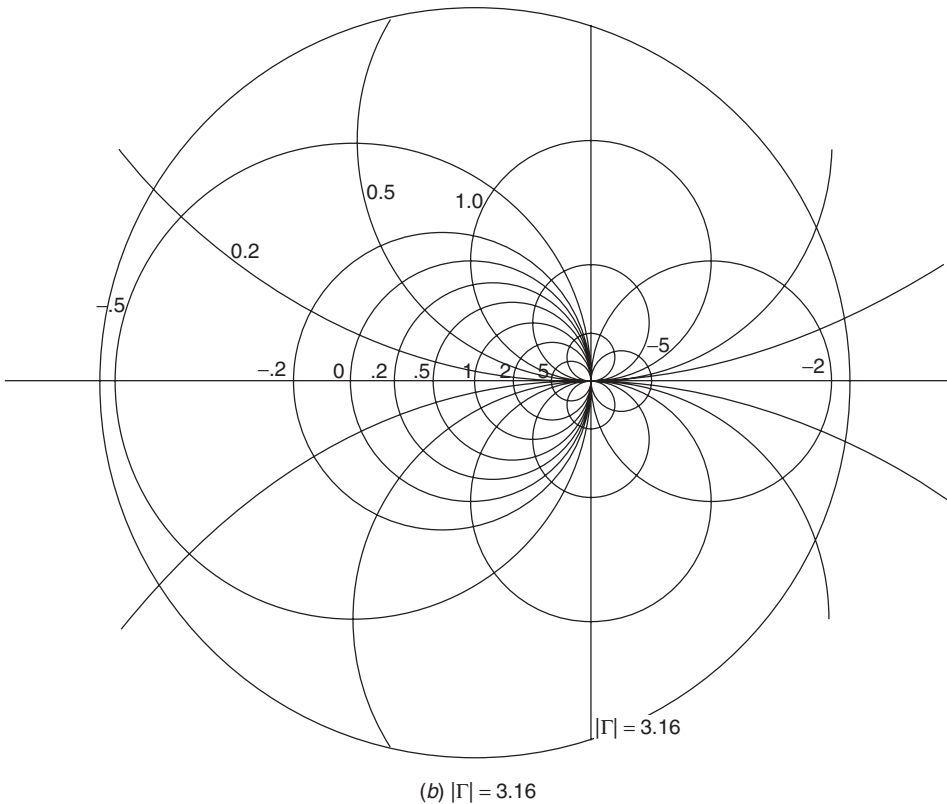
FIGURE 5.1   Smith charts. (*b*) |Γ| = 3.16. (*continued*)

where $\Gamma = 0$, with two or more elements. This will be illustrated by a simple example, which has many solutions using lumped elements, distributed transmission line elements (lossless), and a hybrid combination of both.

Consider the load marked by point A on the Smith chart as $Z/Z_0 = 0.15 + j0.60$ at a frequency of 4 GHz, where $Z_0 = 50 \ \Omega$ [5.5]. It is very helpful if you label your Smith chart solutions alphabetically; this is a roadmap of how the solution was obtained, and we urge you to adopt this practice. The four lumped-element solutions are given in Figure 5.2. Some distributed and hybrid solutions are given in Figure 5.3. This problem has 19 solutions, given in Table 5.1 (so far); in fact, there are probably an infinite number of two-element solutions if the characteristic impedance of the line is not restricted to 50 Ω. The best solution will depend upon bandwidth, dc biasing considerations, and realizability. Often the best solution is the one with the least movement on the Smith chart, since this usually results in the best performance over the frequency. A computer is needed for designs over a wide frequency range, where the initial design is first calculated at the center or high end of the band using the Smith chart.

There are many "tricks" to using the Smith chart efficiently for obtaining minimum-topology designs, wideband designs, low-Q designs, single-element designs, and so on. We usually look for narrow-band two-element designs which allow dc biasing and perhaps ensure low-frequency stability. For broadband high-power designs where the
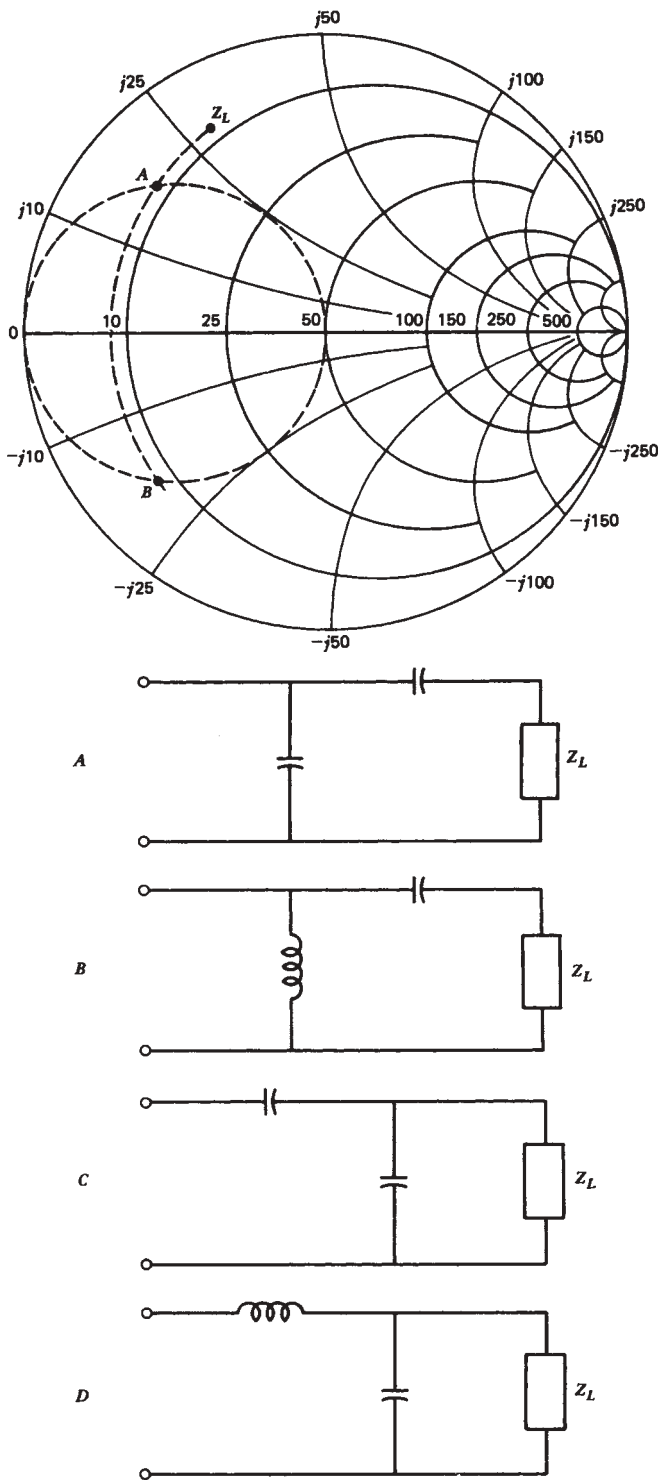
FIGURE 5.2 Lumped-element impedance match.
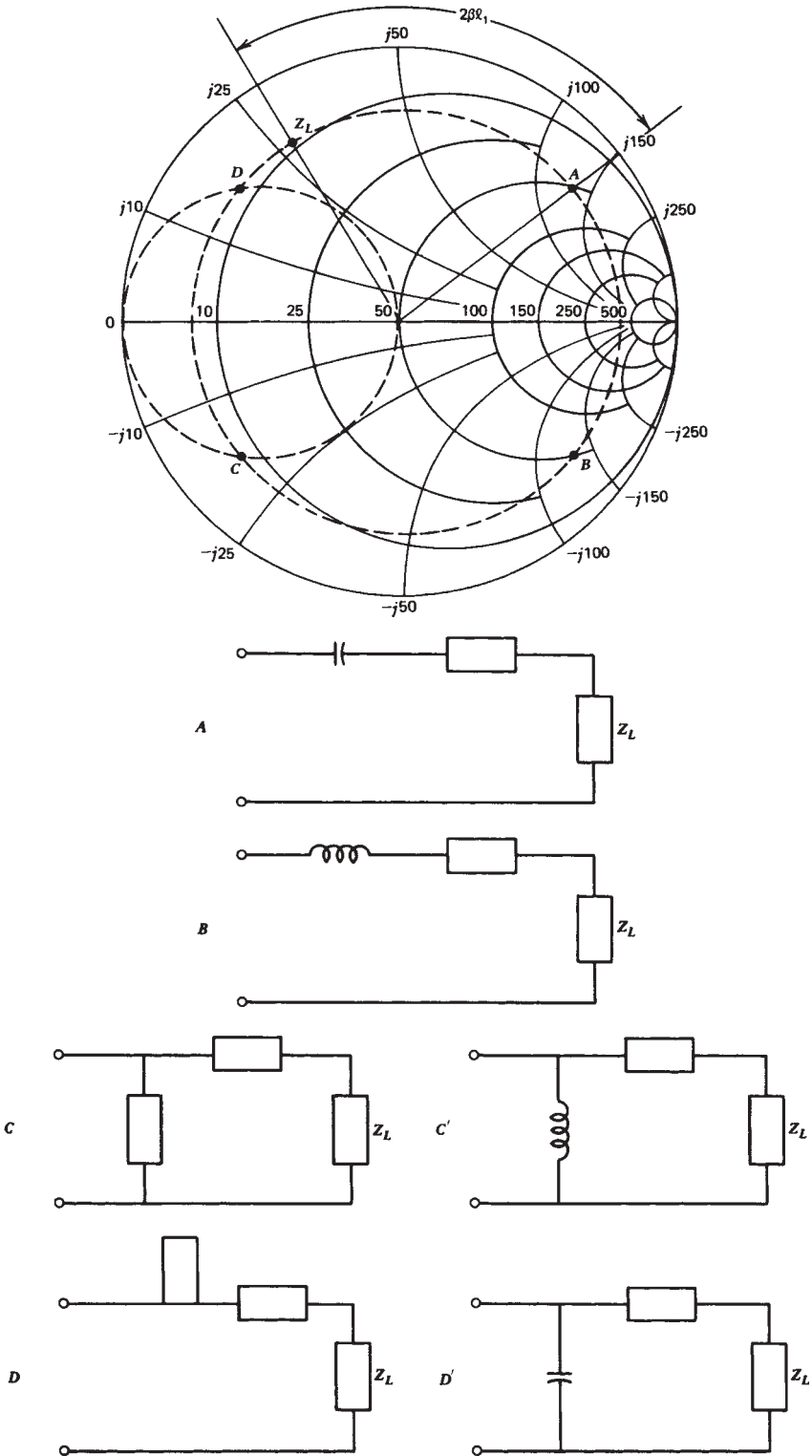
FIGURE 5.2 (*continued*)
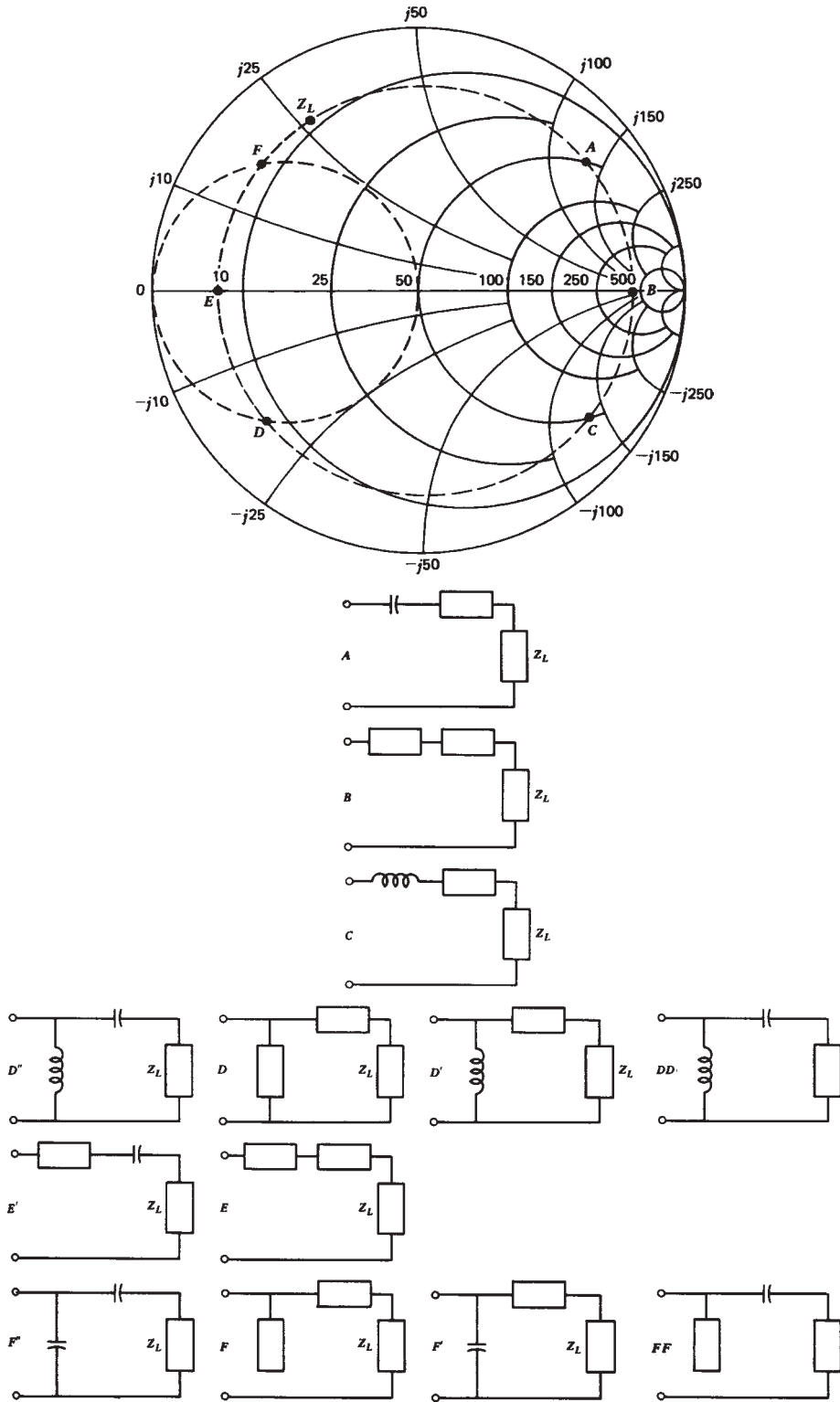
FIGURE 5.2   (*continued*)
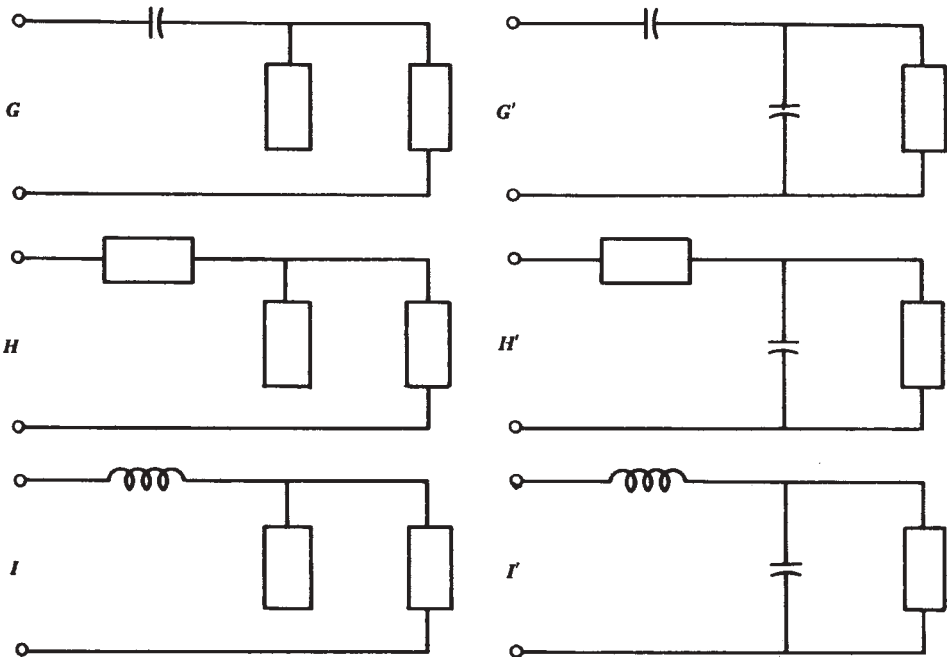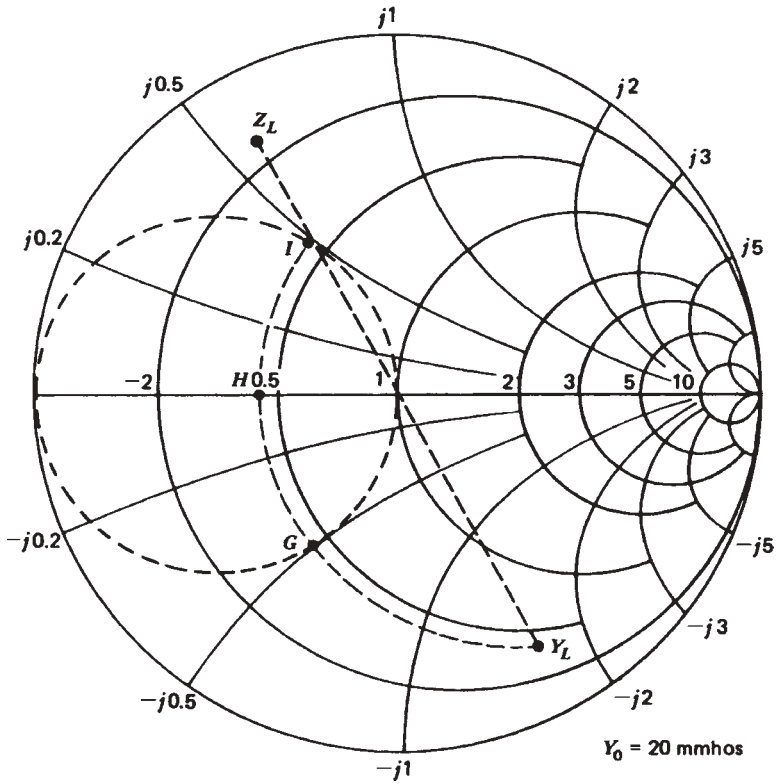
FIGURE 5.3 Distributed and hybrid impedance match.

TABLE 5.1   Solutions to Impedance Matching Example

Solution Number	Figure 5.3 Label	First Element	Second Element
1	A	$Z_0 = 50\ \Omega,\ l = 0.112\lambda$	$C = 0.295$ pF
2	B	$Z_0 = 50\ \Omega,\ l = 0.163\lambda$	$Z_0 = 154\ \Omega,\ l = 0.250\lambda$
3	C	$Z_0 = 50\ \Omega,\ l = 0.214\lambda$	$L = 5.28$ nH
4	D	$Z_0 = 50\ \Omega,\ l = 0.362\lambda$	$Z_0 = 50\ \Omega,\ l = 0.057\lambda$
5	D'	$Z_0 = 50\ \Omega,\ l = 0.362\lambda$	$L = 0.74$ nH
6	D''	$C = 0.84$ pF	$L = 0.78$ nH
7	D'''	$C = 0.84$ pF	$Z_0 = 60\ \Omega,\ l = 0.064\lambda$
8	E	$Z_0 = 50\ \Omega,\ l - 0.413\lambda$	$Z_0 = 16.6\ \Omega,\ l = 0.250\lambda$
9	E'	$C = 1.32$ pF	$Z_0 = 19.6\ \Omega,\ l = 0.250\lambda$
10	F	$Z_0 = 50\ \Omega,\ l = 0.464\lambda$	$Z_0 = 50\ \Omega,\ l = 0.192\lambda$
11	F'	$Z_0 = 50\ \Omega,\ l = 0.464\lambda$	$C = 2.1$ pF
12	F''	$C = 3.20$ pF	$C = 1.89$ pF
13	F'''	$C = 3.20$ pF	$Z_0 = 50\ \Omega,\ l = 0.186\lambda$
14	G	$Z_0 = 50\ \Omega,\ l = 0.132\lambda$	$C = 0.64$ pF
15	G'	$C = 0.86$ pF	$C = 0.64$ pF
16	H	$Z_0 = 50\ \Omega,\ l = 0.160\lambda$	$Z_0 = 81\ \Omega,\ l = 0.250\lambda$
17	H'	$C = 1.25$ pF	$Z_0 = 81\ \Omega,\ l = 0.250\lambda$
18	I	$Z_0 = 50\ \Omega,\ l = 0.178\lambda$	$L = 2.46$ nH
19	I'	$C = 1.64$ pF	$L = 2.46$ nH
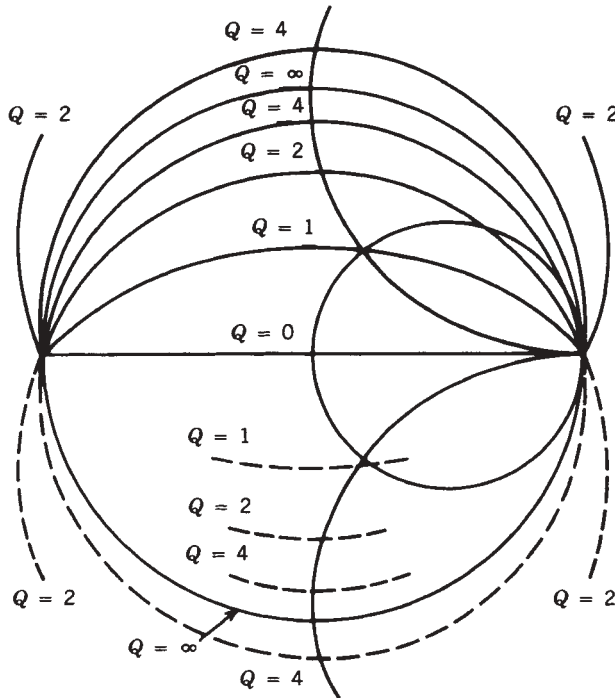
FIGURE 5.4   Smith chart Q plots.
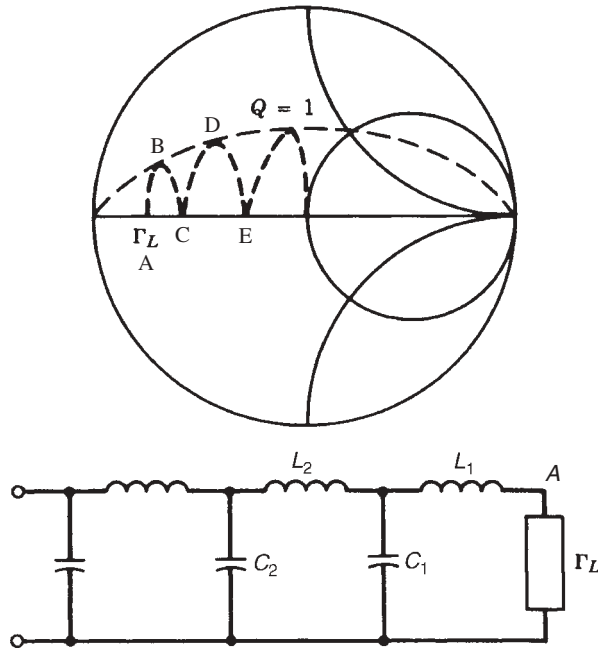
FIGURE 5.5   Low-impedance broadband match.

impedance to be matched is very low, we need to keep the Q low for best matching over a broad frequency range, where Q on the Smith chart is given in Figure 5.4. The matching for a broadband high-power design is given in Figure 5.5, where we have used six elements instead of two to keep the circuit Q low. Single-element matching is an extension of $\lambda/4$ matching, where this has been previously explained in Ref. 5.5 and later in this chapter.

5.3   IMPEDANCE MATCHING NETWORKS

The general design problem for amplifiers, oscillators, and mixers is to impedance match the device to the 50-Ω port impedance or to move any point on the Smith chart to any other point with:

1. Lossless lumped elements
2. Lossless transmission line components, including parallel open and shorted stubs, usually using microstripline
3. A hybrid design consisting of a combination of the first two categories

Some authors [e.g., 5.6–5.10] include series matching stubs in categories 2 and 3; in practice, this is impossible to build, so we recommend ignoring this form of impedance matching. If it cannot be realized physically, it is of no value to the design engineer.

Pozar points out in a private communication that series stubs can be realized in CPW, but no working circuits have appearel in the literature at the time of this writing.

5.4 SINGLE-ELEMENT MATCHING

Single-element matching is a special case of a quarter-wavelength matching circuit, where the load impedance has already been moved over a portion of the $\lambda/4$ matching line. An example of this is given in Figure 5.6 [5.11]. This type of single-element
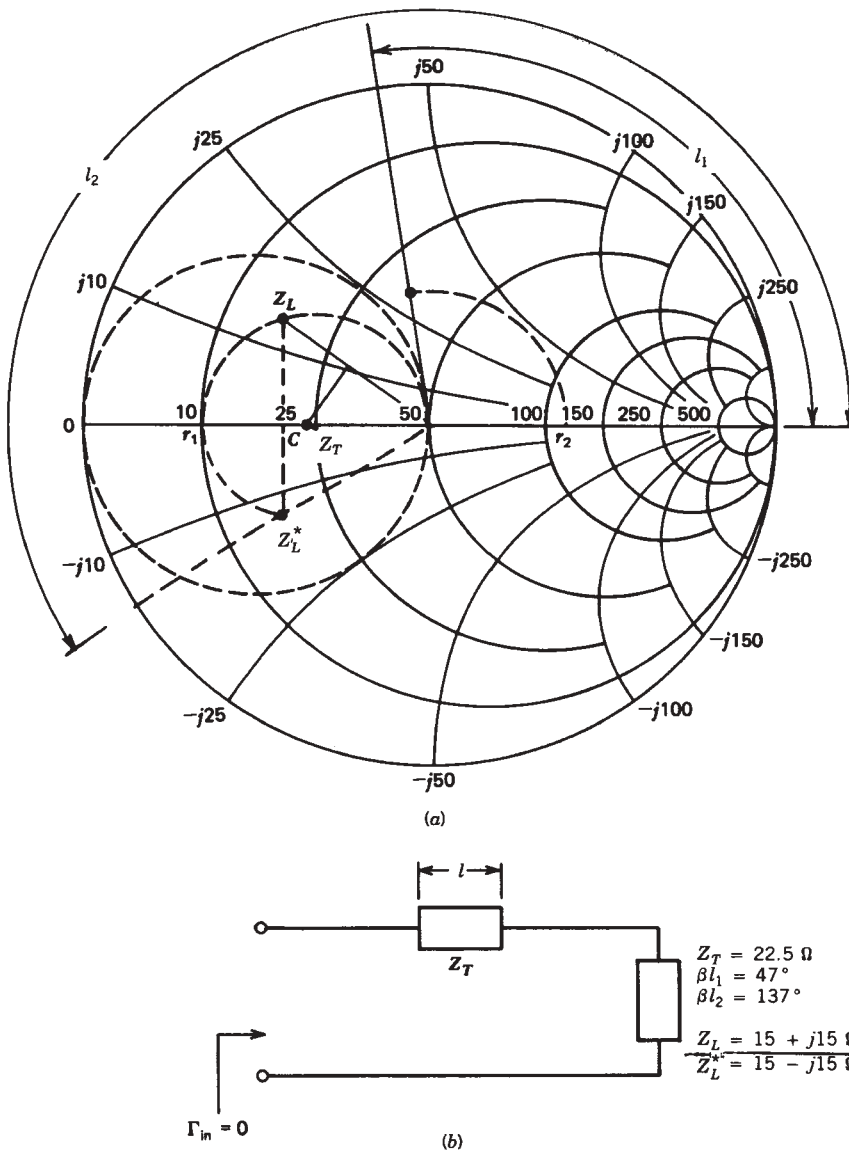
FIGURE 5.6   Single-element matching.

matching is only possible if the load falls within the $r = 1$ circle or the mirror image of that circle, which is always a useful graphical aid. The graphical solution proceeds as follows [5.11]:

1. Draw the line between Z_L and the center of the chart.
2. Draw the perpendicular bisector to locate C on the real axis.
3. Determine the characteristic impedance of the matching line from

$$\frac{Z_T}{Z_0} = (r_1)^{1/2}$$

4. Renormalize Z_L to Z_T.
5. Move toward the generator until the real axis is intersected at r_2.
6. Renormalize from Z_T to Z_0, which produces the center of the 50-Ω chart.

For this example the single-element matching section has $Z_T = 0.45$, $Z_0 = 22.5$ Ω, and $\beta l = 47°$; if Z_L is the conjugate, the length is $\beta l_2 = 137°$.

There are many designs which accomplish the Z_L match using the three techniques described above, where the design may begin in either the Z or Y plane. In Ref. 5.1 we show 17 solutions, which are repeated here in Table 5.1 along with 2 more solutions (DD and DD'); all of these solutions are valid, but some are more appropriate than others. Look for the minimum movement on the Smith chart which produces the widest bandwidth.

5.5   TWO-ELEMENT MATCHING

Consider the matching circuits to be L networks, either a series/shunt lossless network for Z_L inside the $1 + jx$ circle or a shunt/series lossless network for Z_L outside the $1 + jx$ circle. An analytic or graphical solution may be easily found for the match to the center of the Smith chart. The analytic approach for the series/shunt L network is [5.6]

$$Z_0 = jX + \frac{1}{jB + 1/R_L + jX_L} \tag{5.3}$$

which states that the impedance looking into the matching circuit followed by the load impedance must be equal to Z_0. Rearranging and separating into real and imaginary parts give two equations for the two unknowns X and B:

$$B(XR_L - X_L Z_0) = R_L - Z_0 \tag{5.4}$$

$$X(1 - BX_L) = BZ_0 R_L - X_L \tag{5.5}$$

Solving Eq. (5.4) for X and substituting into (5.5) radical gives a quadratic equation for B:

$$B = \frac{X_L \pm \sqrt{R_L/Z_0}\sqrt{R_L^2 + X_L^2 - Z_0 R_L}}{R_L^2 + X_L^2} \tag{5.6}$$

Note that since $R_L > Z_0$, the argument of the second square root is always positive. The series reactance is

$$X = \frac{1}{B} + \frac{X_L Z_0}{R_L} - \frac{Z_0}{BR_L} \tag{5.7}$$

There are two solutions for B and X, where the numbers may be positive (shunt C, series L) or negative (shunt L, series C).

In a similar way, consider the shunt/series L network, which implies $R_L < Z_0$. The admittance seen looking into the matching network followed by the load impedance must equal $1/Z_0$:

$$\frac{1}{Z_0} = jB + \frac{1}{R_L + j(X + X_L)} \tag{5.8}$$

Rearranging and separating into real and imaginary parts give two equations for the two unknowns X and B:

$$BZ_0(X + X_L) = Z_0 - R_L \tag{5.9}$$

$$X + X_L = BZ_0 R_L \tag{5.10}$$

Solving for X and B gives

$$X = \pm\sqrt{(R_L)\ (Z_0 - R_L)} - X_L \tag{5.11}$$

$$B = \pm\frac{\sqrt{(Z_0 - R_L)/R_L}}{Z_0} \tag{5.12}$$

Since $R_L < Z_0$, the arguments of the square roots are always positive.

Although both analytic and graphical techniques are available, the graphical approach seems to provide more insight into the bandwidth of the solution. This has already been demonstrated for the example of $Z_L/Z_0 = 0.15 + j0.6$; see Figures 5.2 to 5.3.

5.6 MATCHING NETWORKS USING LUMPED ELEMENTS

Up to frequencies of about 1 GHz, lumped elements are most often used. With modern microwave integrated circuit technology, lumped elements may be used even into the millimeter-wave region.

If the load impedance is inside the $1 + jx$ circle, you must start in the Y_L plane on the Smith chart. There are two values of B which move you to the mirror image of the $1 + jx$ circle (a very useful graphical aid). Next you move to the Z plane and add the appropriate value of X to find the center of the chart There are only two solutions for this problem.

If the load impedance is outside the $1 + jx$ circle, there are four solutions as shown in Figure 5.2.

Engineers often try to find an equivalence between lumped and distributed transmission line elements. This is not recommended, since they have different movement on the Smith chart. If you choose to ignore this warning, a rough equivalence between a series inductor and a series transmission line is

$$j\omega L = jZ_0 \tan(\beta l) \tag{5.13}$$

and a shunt capacitor is roughly equivalent to a shunt open-circuited transmission line by

$$j\omega C = jY_0 \tan(\beta l) \tag{5.14}$$

There is no equivalence for a series capacitor, but the case of a shunt inductor may also be approximated by Eq. (5.13).

5.7 MATCHING NETWORKS USING DISTRIBUTED ELEMENTS

For this case, you locate the load impedance on the Smith chart (point A) and draw the voltage standing-wave ratio (VSWR) circle of the constant-reflection coefficient. When you intersect the mirror image of the $1 + jx$ circle, you move to the Y plane and complete the match with either an open or shorted shunt stub. This was previously illustrated in Figure 5.3.

Before you attempt to draw the mask, you must consider junction effects where the microstrip line elements are joined, for example, a tee or cross junction. Generally, CAD is used to include these effects below 10 GHz, but as the frequency increases, a more accurate solution will include a 2-$\frac{1}{2}$ or 3D solution for the S parameters of the matching networks. This step is very time consuming and adds very little knowledge to understanding the circuit frequency response. Even a right-angle turn in the microstrip may introduce unwanted reactance effects which must be accounted for. The optimum miter is 0.7 instead of 0.5—the logical choice [5.12]. Think of the signal propagating along the center of the microstrip. If a 90° turn is made, the signal should continue down the center line as a first approximation. Since there is extra capacitance at the turn, we must compensate for this by reducing the capacitance or narrowing the metal at the turn or perhaps curving the turn, which produces a different discontinuity. The junction effects were previously discussed in Chapter 2. The computer will include these effects for you, but the engineer must understand why this extra cut for the miter or chamfer is made. The computer will even generate the final mask when the design is completed.

5.7.1 Twisted-Wire Pair Transformers

Twisted wires form a transmission line with many applications, including impedance matching and baluns. The frequency barely extends into the microwave range, currently with an upper limit of about 2 GHz. The literature has many excellent explanations which explain the impedance-transforming properties of these multiple-transmission-line circuits.

A classic reference on this topic is Ref. 5.13, which points out there are two basic analyses of this technique [5.14, 5.15], Guanella and Ruthroff. One employs the conventional transformer that transmits energy to the output by flux linkages; the other uses the transmission line transformer to transmit energy by a transverse transmission line mode. The first method will give very wide bandwidths; 2 kHz to 200 MHz is possible. The second method gives even wider bandwidths and greater efficiencies.

Ideal transmission line transformers (method 2) can be realized by two parallel lines, a twisted pair of lines, a coaxial cable, or a pair of wires on a ferrite core [5.16]. An analysis for a transmission line transformer which produces a 4:1 (or 1:4)
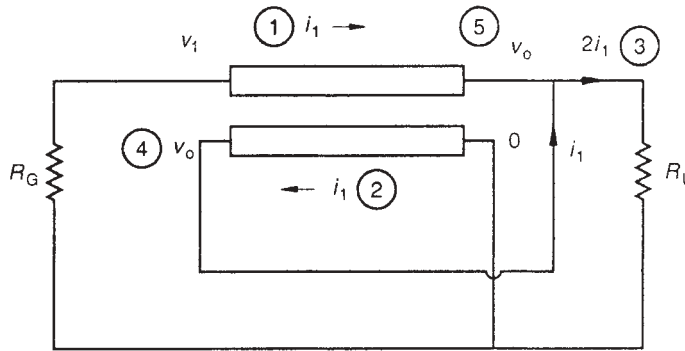
FIGURE 5.7   Analysis of the 4 : 1 transformer.
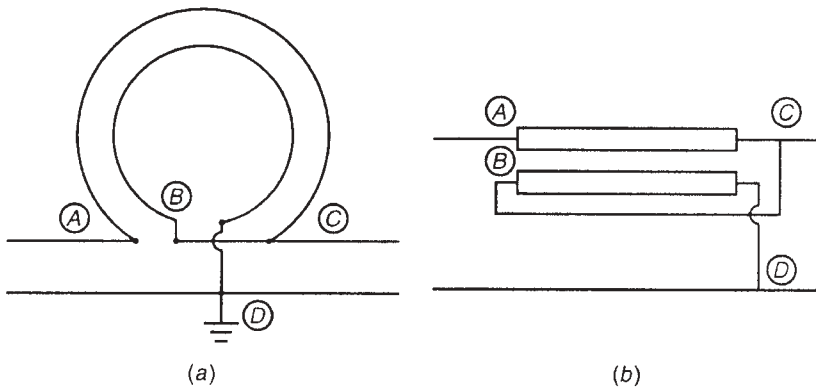
FIGURE 5.8   (*a*) Physical two-wire transmission line transformer and (*b*) equivalent formal representation.

impedance transformer is shown in Figure 5.7. The analysis is found in a later section of this chapter. Some physical realizations are shown in Figure 5.8. By increasing the number of transmission lines, the impedance ratio may be increased by n^2; thus three transmission lines may produce a 9 : 1 impedance transformation, four transmission lines may produce a 16 : 1 transformation, and so on.

5.7.2   Transmission Line Transformers

Transformers are very useful circuit elements because they can provide a discrete impedance transformation over a very wide bandwidth. The 4 : 1 transformer is the most common of all. Several forms are given in Figure 5.9 [5.16, 5.17].

An analysis of the currents and voltages in the 4 : 1 transformer explains how the impedance transformation occurs. Referring to Figure 5.7, assume a resistive load R_L is added to the circuit. If a current I is flowing through the load causing a voltage V across R_L, the same voltage will be impressed across the secondary of the transformer. Since the turns of the secondary and primary are identical, the voltage V will also be impressed across the primary. The voltage at the input of the transformer is the
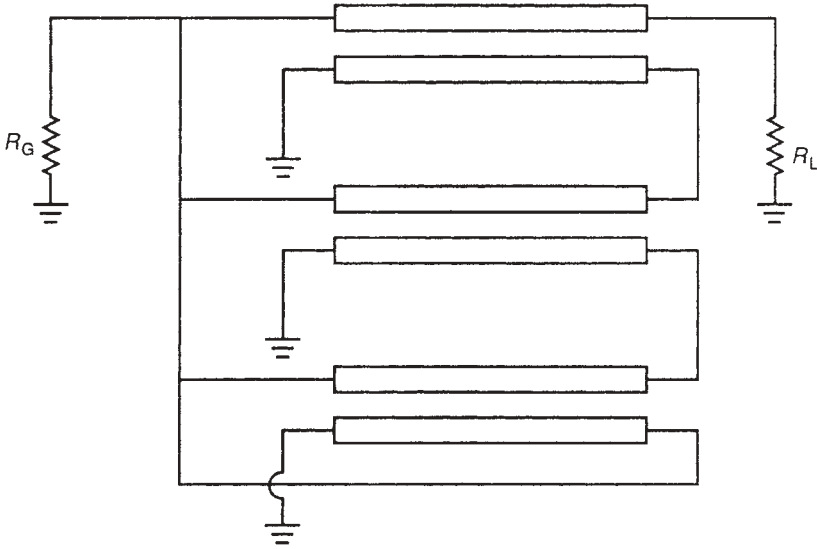
FIGURE 5.9   Configuration of 9:1 transformer.

sum of the voltage across the transformer primary and R_L, or 2 V. If a total current I is to flow through R_L, one-half must be provided from each transformer winding. Therefore, the input impedance will be 2 V divided by 1/2, or $4R_L$. Similar results are obtained from Figure 5.9, where a 9:1 impedance transformer is given.

The bandwidths of these types of transformers can be more than two decades if the transformer interconnects are short and the transmission line impedance is the geometric mean between the input and output:

$$Z_0 = \sqrt{R_{in} R_L} \tag{5.15}$$

Similar techniques may be used to design balun transformers to convert a balanced load to an unbalanced system. A good example of a 1:1 balun is shown in Figure 5.10, where a balanced 50-Ω load is transformed to an unbalanced 50-Ω load. Baluns are used extensively in balanced mixer circuits (see Chapter 11 for further details). Quarter-wave transmission lines also provide useful impedance transformers, as mentioned earlier in Section 5.4. A simple application of this concept to a push–pull amplifier is shown in Figure 5.11. If the input and output impedances of the amplifiers are 6.25 Ω, the total balanced impedance is 12.5 Ω; thus a quarter-wave 25-Ω transmission line will transform the low impedance of the power amplifier to 50 Ω. This simple concept is widely used to double the output power of the single-stage power amplifier, with many inherent advantages, including wider bandwidth (compared to paralleling the transistors), reduced even-order harmonics, better efficiency, and reduced common-lead inductance.

5.7.3 Tapered Transmission Lines

There are at least three types of tapered transmission line designs which produce a good broadband match. These are the simple triangular or linear taper, the exponential taper,

(a)

Dipole Antenna

Feed Line

(b)
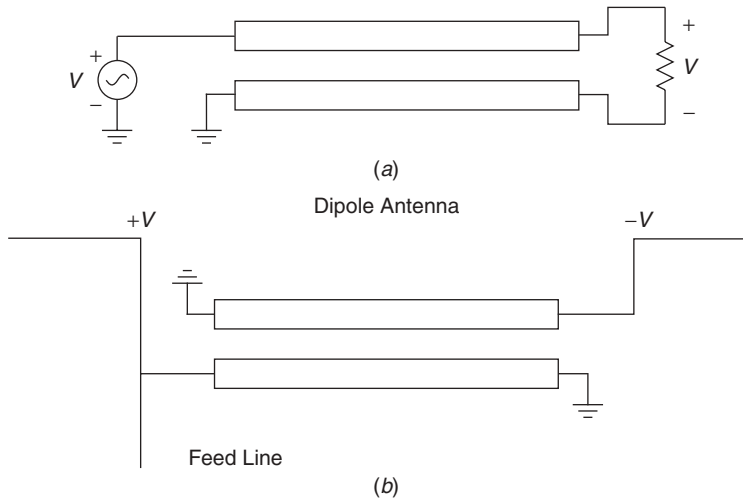
FIGURE 5.10   Simple balun transformer.
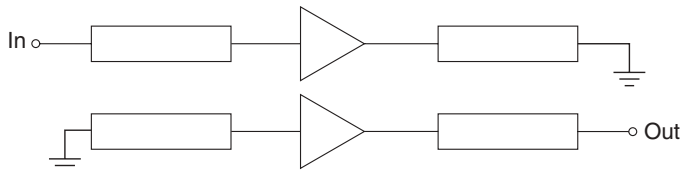
FIGURE 5.11   Push–pull amplifier using quarter-wave baluns.

and the Klopfenstein taper, which produce very similar results [5.6, 5.7]. In microstrip circuits, this type of matching is rarely used because it is very difficult to tune. The tuning needs to be done on the computer, but if the S parameters of the transistor are not accurate, this exercise may be unproductive.

In a broadband multisection quarter-wave matching circuit, there are n sections of line designed to keep the maximum reflection coefficient at some maximum value in the passband. The tapered transmission line is an approximation of this circuit, as shown in Figure 5.12. Other forms of tapered transmission line designs available on Serenade/Design Suite from Ansoft are as follows:

1. Linear taper with W as variable
2. Linear taper with Z_0 as variable
3. Exponential taper with W as variable
4. Exponential taper with Z_0 as variable

These four cases are compared in the example described in Figure 5.13, where the performance is very similar. The frequency response is high pass in this design. The length of the taper is crucial in these designs. As the length is increased, the frequency response goes lower (obviously). The nominal length for a 10-GHz design is about
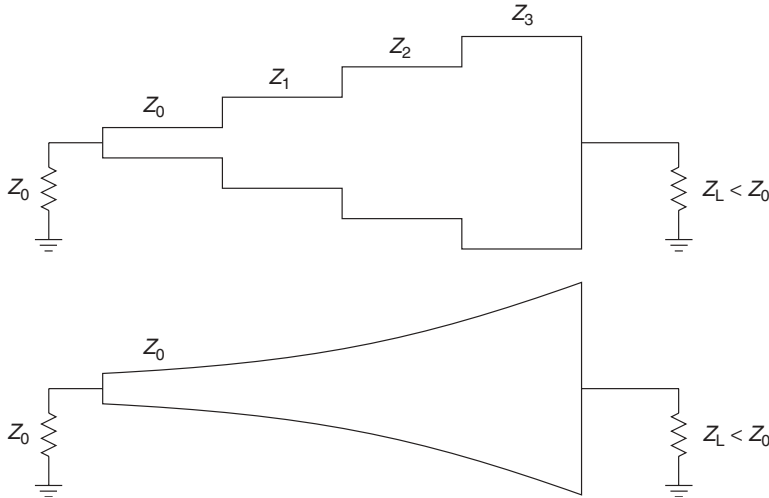
FIGURE 5.12 Comparison of multisection quarter-wave matching and tapered matching.

$\lambda/4 - \lambda/2$, which is calculated for a dielectric constant of 10 for a 50-Ω line as follows:

$$\frac{\lambda}{4} = \frac{7.5}{10\sqrt{6.7 \times 2.54}} = 0.114 \text{ in.}$$

where 6.7 is the effective dielectric constant for alumina ($\varepsilon_r = 10$) and a 50-Ω microstrip line. Therefore the calculations have been done for a taper of 200 mils in length, which seems to give the best performance.

5.8 BANDWIDTH CONSTRAINTS FOR MATCHING NETWORKS

When considering broadband matching, the engineer is faced with the trade-offs of a single-section quarter-wave transformer, which has a fractional bandwidth given by [5.6]

$$\frac{\Delta f}{f_0} = 2 - \frac{4}{\pi} \cos^{-1} \frac{\Gamma_m \times 2\sqrt{Z_0 Z_L}}{\sqrt{1 - \Gamma_m^2}|Z_L - Z_0|} \tag{5.16}$$

or a multisection quarter-wave transformer of either the maximally flat (binomial transformer) or the Chebyshev (equal-ripple) types, which have fractional bandwidths of [5.6]

$$\frac{\Delta f}{f_0} = 2 - \frac{4}{\pi} \cos^{-1} \left[1/2 \left(\frac{\Gamma_m}{|A|} \right)^{1/N} \right] \tag{5.17}$$

$$\frac{\Delta f}{f_0} = 2 - \frac{4\theta_m}{\pi} \tag{5.18}$$

or the three tapered designs discussed in the previous section of this chapter. A simple example will illustrate these concepts. Design a single-section quarter-wave

(*a*)

(*b*)
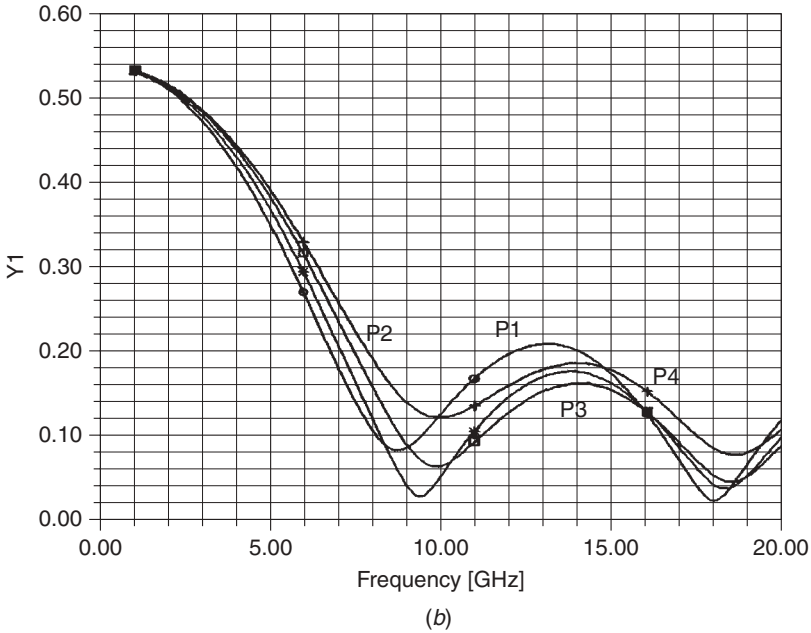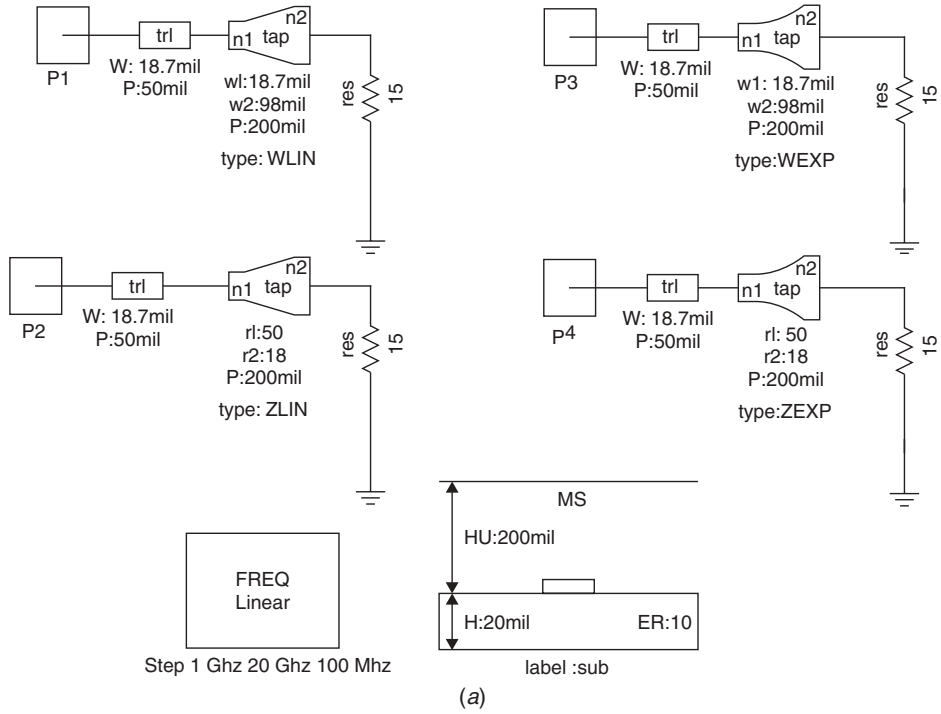
FIGURE 5.13 Four matching circuit responses for taper design example.

(c)
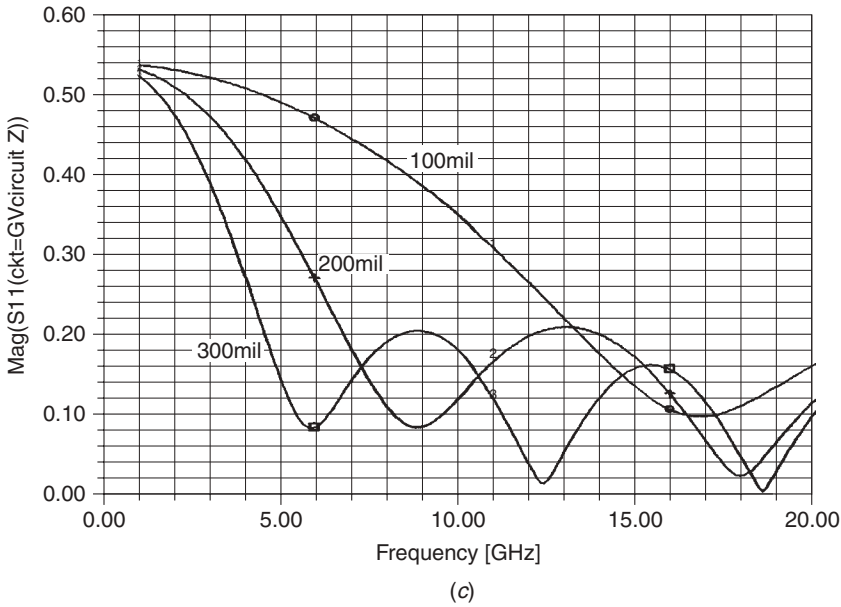
FIGURE 5.13 (*continued*)

transformer which matches a 15-Ω load to 50 Ω at 10 GHz. Find the fractional bandwidth where VSWR < 1.22, $Z_T = \sqrt{50 \times 15} = 27.4$ Ω. The maximum value of Γ is (VSWR $- 1$)/(VSWR $+ 1$) $= 0.10$. The fractional bandwidth is

$$\frac{\Delta f}{f_0} = 2 - \frac{4}{\pi} \arccos\left(\frac{0.10}{\sqrt{1 - 0.01}} \times 2 \times \frac{27.4}{|15 - 50|}\right) = 0.20$$

or a frequency range of 9 to 11 GHz. This circuit response is plotted in Figure 5.14. If we repeat the design with a three-section maximally flat or binomial transformer design, $A = \frac{1}{16} \ln(\frac{15}{50}) = -0.0752$, and the fractional bandwidth is:

$$\frac{\Delta f}{f_0} = 2 - \frac{4}{\pi} \arccos\left[0.5\left(\frac{0.10}{0.0752}\right)^{1/3}\right] = 0.74$$

or a frequency range of 6.3 to 13.7 GHz, which is also plotted in Figure 5.6. The required characteristic impedances are

$$\ln Z_1 = \ln 50 + 2^{-3} \ln \frac{15}{50} = 3.761 \quad Z_1 = 43 \ \Omega$$

$$\ln Z_2 = \ln 43 + 2^{-3} \times 3 \ln \frac{15}{50} = 3.308 \quad Z_2 = 27.3 \ \Omega$$

$$\ln Z_3 = \ln 27.3 + 2^{-3} \times 3 \ln \frac{15}{50} = 2.854 \quad Z_3 = 17.4 \ \Omega$$
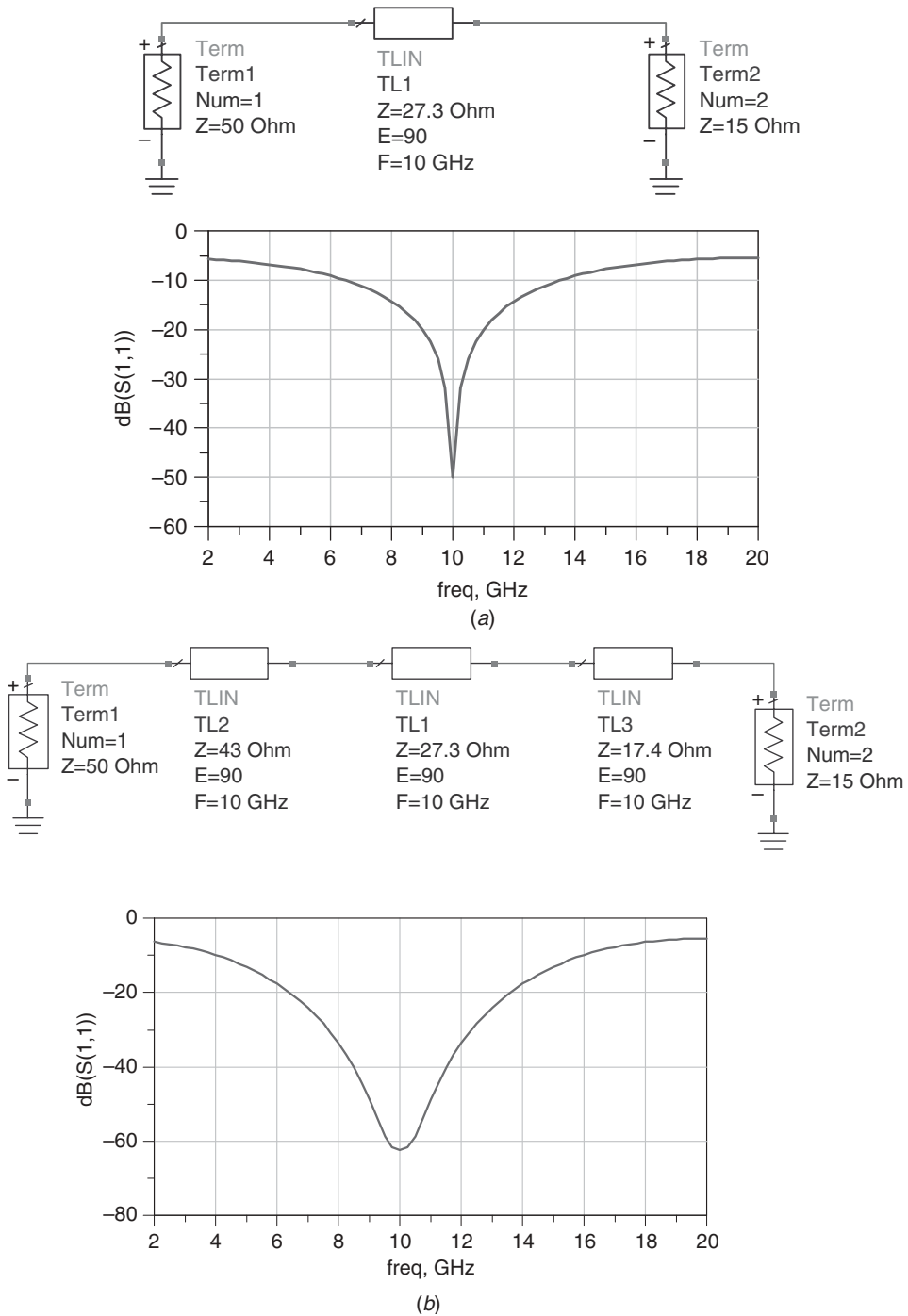
FIGURE 5.14 Multisection quarter-wave matching response for design example: (*a*) single
section; (*b*) maximally flat three-section design; (*c*) Chebyshev three-section design.

(c)
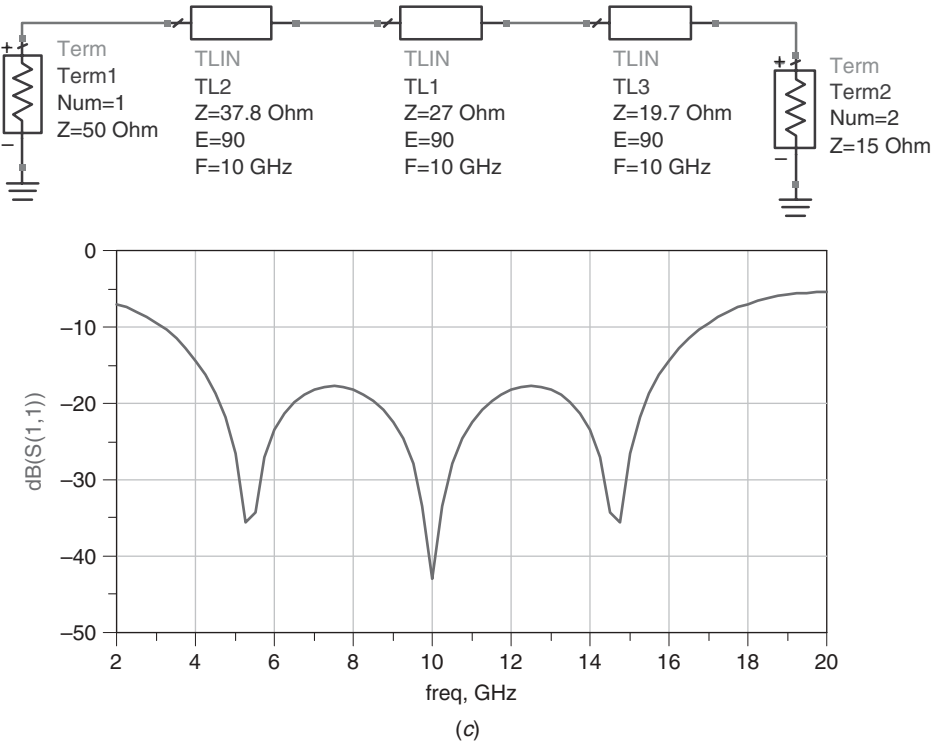
FIGURE 5.14 (*continued*)

TABLE 5.2 Load Q_1

Low-pass (LP) capacitor	ωRC
High-pass (HP) capacitor	$1/\omega RC$
LP inductor	$\omega L/R$
HP inductor	$R/\omega L$

For the three-section Chebyshev or equal-ripple case, using Table 5.2 of Ref. 5.6 by interpolation for $\Gamma_m = 0.10$ we find

$$\frac{Z_1}{Z_0} = 1.31 \qquad \frac{Z_2}{Z_0} = 1.80 \qquad \frac{Z_3}{Z_0} = 2.52$$

So the characteristic impedances are

$$Z_1 = 37.8 \ \Omega \qquad Z_2 = 27 \ \Omega \qquad Z_3 = 19.7 \ \Omega$$

very similar to the maximally flat design. A computer plot of each of these three cases illustrates the bandwidth variations (Fig. 5.14). The bandwidth for the single-section design is 0.20, for the three-section maximally flat design is 0.74, and for the three-section Chebyshev is 1.10 at the expense of the ripple of ±0.05 in the passband. A

comparison to the tapered design is given in Figure 5.14 using Serenade for the same design problem using a 20-mil alumina substrate. More bandwidth may be achieved from either the maximally flat or Chebyshev designs by using more sections and allowing more ripple. The tapered designs are high pass while the previous designs were bandpass. The best response for the tapered design was obtained for the linear tapers as opposed to the exponential cases. Some useful references in this area date back to 1938 [5.8, 5.9]. The limitation on broadband matching is given by the Bode–Fano limit:

$$|\Gamma_{\min}| = \exp\left(-\frac{\pi Q_2}{Q_1}\right) \tag{5.19}$$

where Q_1 is the load Q and Q_2 is the circuit Q. The load Q is given in Table 5.2 for the four possible cases. The circuit Q is

$$Q_2 = \frac{f_0}{\Delta f} = \frac{f_0}{\text{BW}} \tag{5.20}$$

The exact integrals are referred to as Fano's limit, and they can be found in Refs. 5.5 and 5.18.
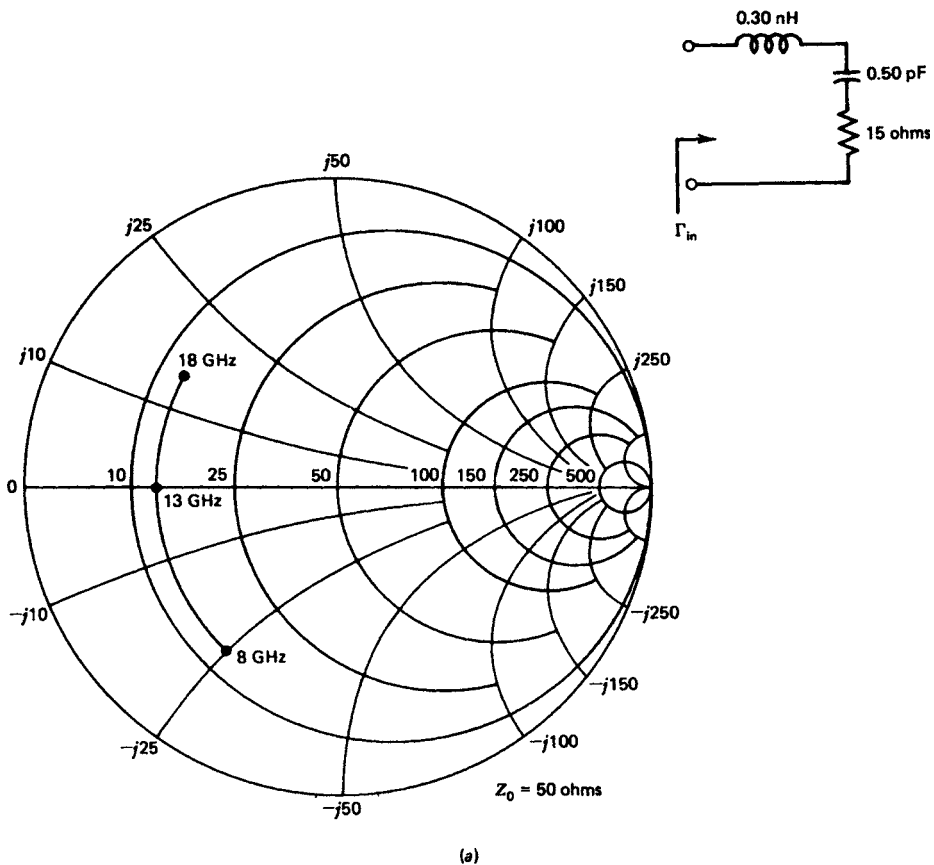
FIGURE 5.15 Broadband match to MESFET input.

(b)
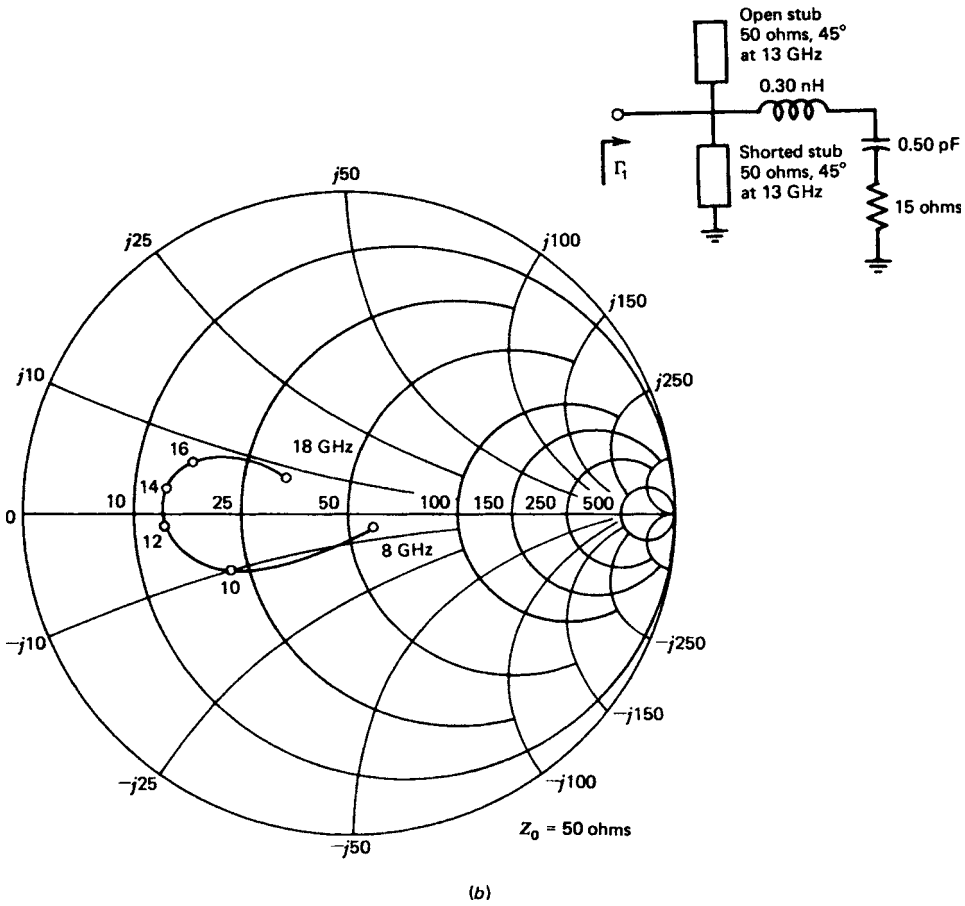
FIGURE 5.15 (*continued*)

Another broadband matching example is the 8 to 18-GHz match to a CS, GaAs MESFET, shown in Figure 5.15. The first element is the gate-bonding inductor of 0.3 nH, which series resonates the circuit. Next we add a λ/8 open stub to approximately match 18 GHz and a λ/8 shorted stub to approximately match 8 GHz. The final element is a λ/4 matching element for 13 GHz. Since there is a Cross parasitic in the design, this must be incorporated in the final circuit, which is optimized for best performance. The optimized design is given in Figure 5.16, including the microstrip cross. Further details of this design are found in Ref. 5.5.

Notice that for this design $|\Gamma_{\min}|$ is calculated as follows:

$$Q_1 = \frac{1}{\omega RC} = \frac{1}{2}\pi \times (13 \times 10^9)[(0.5 \times 10^{-12}) \times 15] = 1.63$$

$$Q_2 = \frac{13}{10} = 1.3$$

$$|\Gamma_{\min}| = \exp\left(-\frac{\pi \times 1.3}{1.63}\right) = 0.082$$

(c)

FIGURE 5.15   (*continued*)

(a)
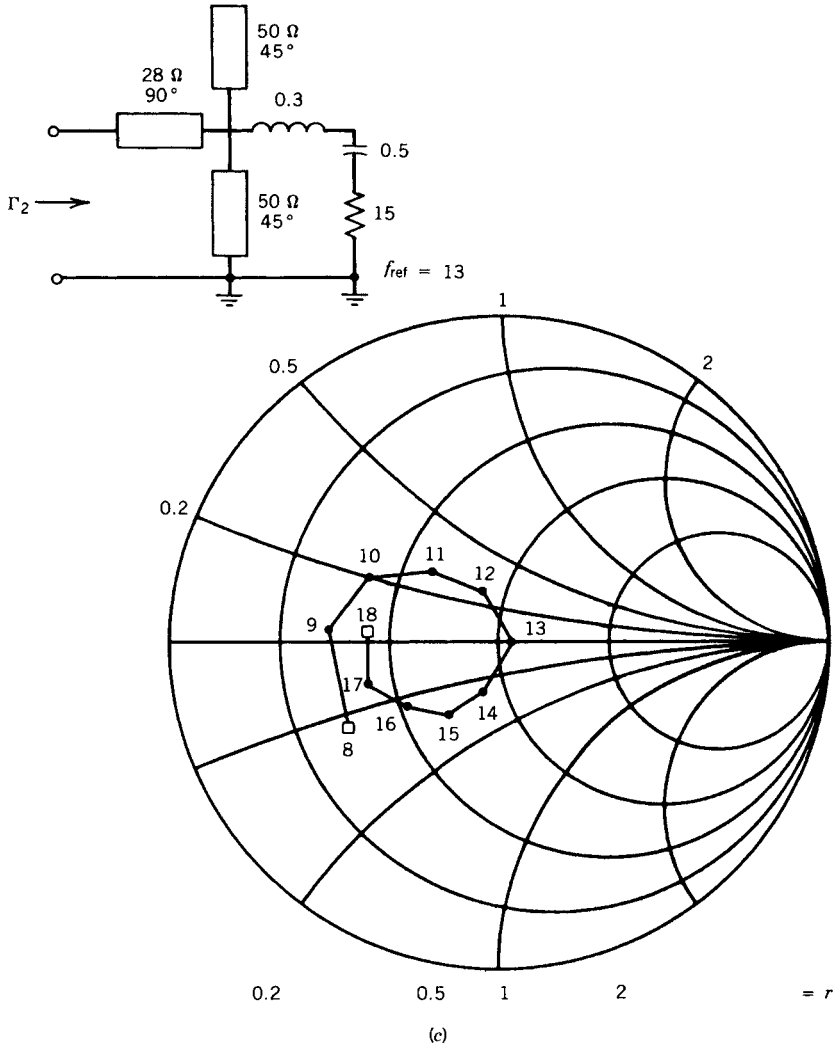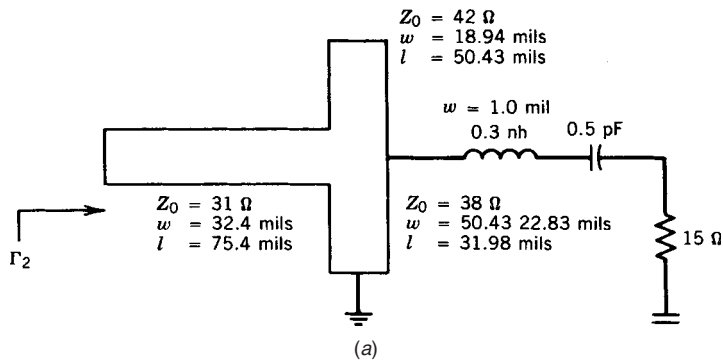
FIGURE 5.16   Broadband match to MESFET input with microstrip cross included.
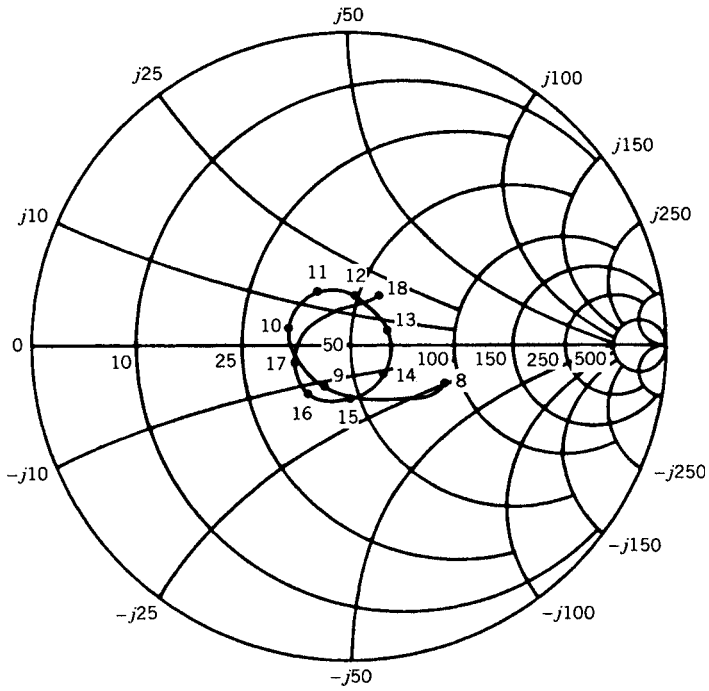
(b)
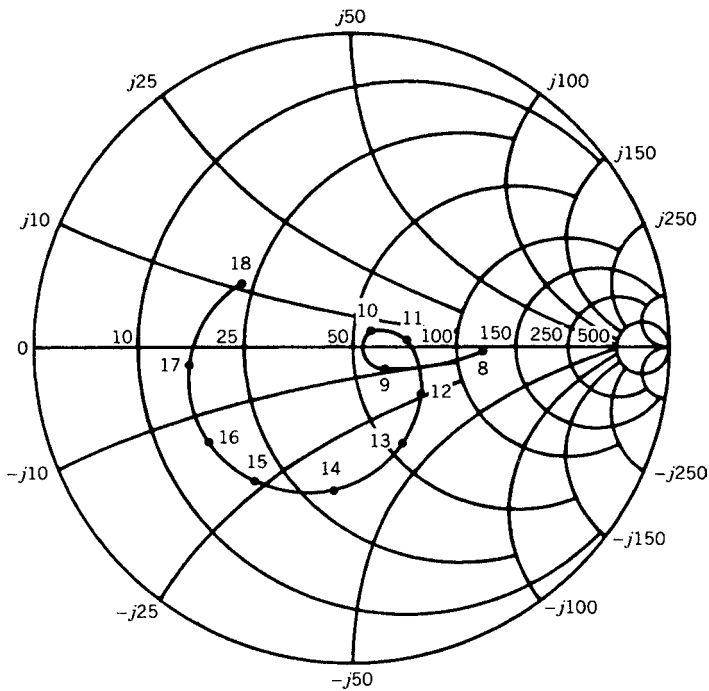
(c)

FIGURE 5.16   (*continued*)
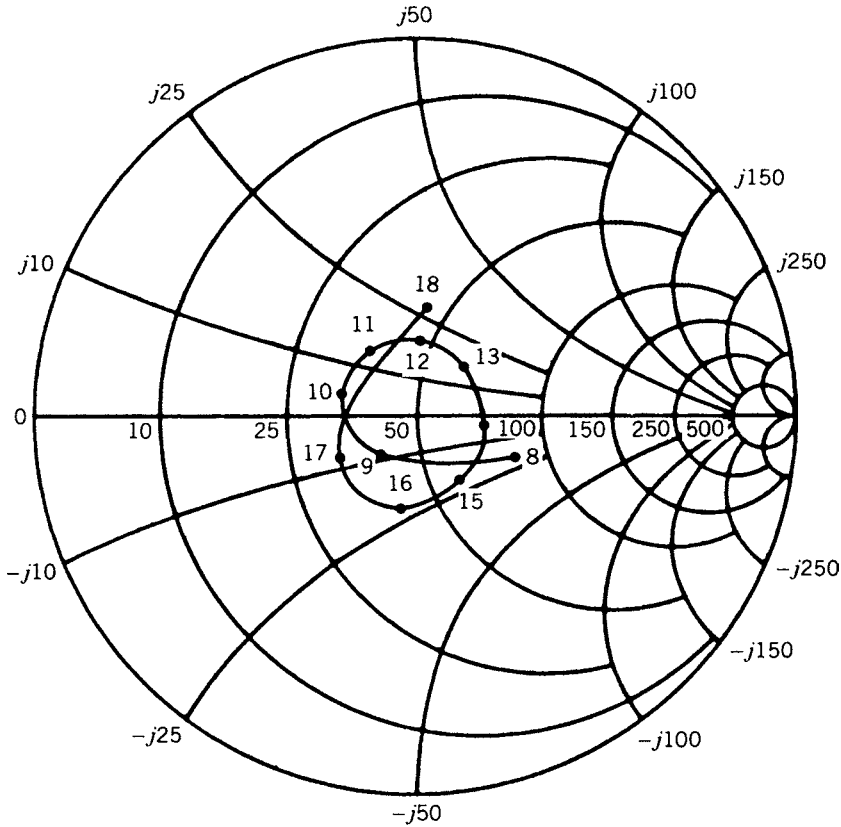
Element	Impedance, Z_0 (Ω)	Width (mils)	Length (mils)
Cascade line	29	32.6	66.7
Open stub	100	2.0	62.8
Shorted stub	100	2.0	18.5

(d)

FIGURE 5.16   (*continued*)

but the final performance gives a larger result of about 0.3. It becomes very difficult to approach Fano's limit.

From a practical point of view, a good choice for broadband matching is a low-pass/high-pass circuit, where there is at least one inductor to ground to ensure low-frequency stability. There is no theory here, just common sense. Any point on the Smith chart can be matched with two elements in either a low-pass structure or a high-pass structure. Combining both types of circuits will result in broader bandwidth results. Also, the minimum movement on the Smith chart will usually result in the best bandwidth.
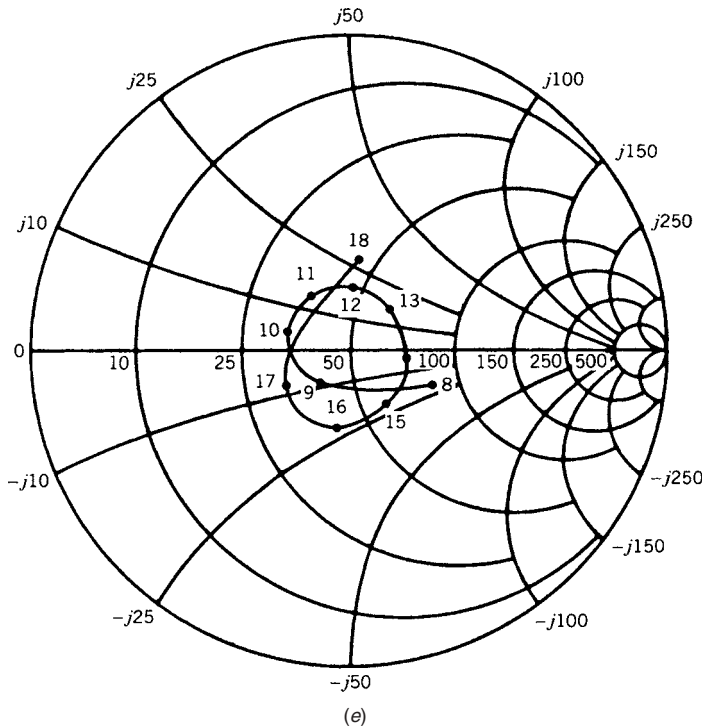
FIGURE 5.16   (*continued*)

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PROBLEMS

5.1   Using the concept of single-element matching, derive the three-element interstage-matching network shown.
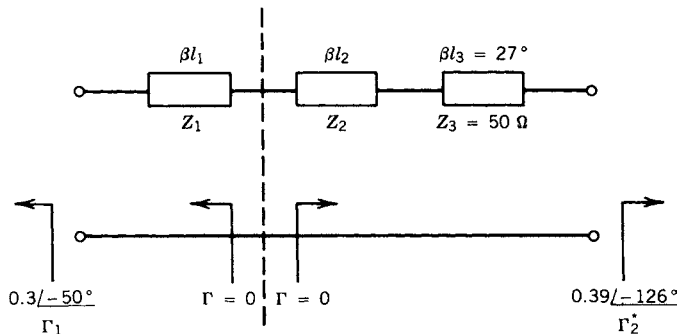
5.2 Find a single-element transmission line that performs the interstage match shown.

$Z_1 =$
$\beta l_1 =$
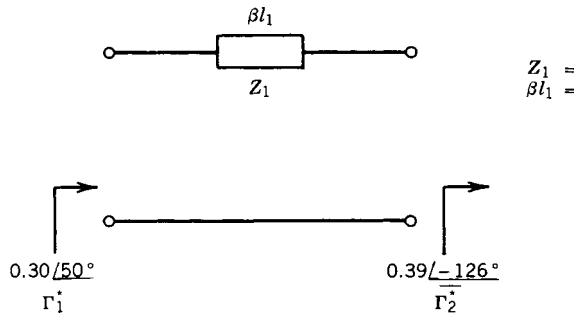
5.3 Complete or verify the following six interstage designs of $f = 4$ GHz. Show the six solutions on a Smith chart.

$S_{22}^* = 0.42\underline{/53°}$ $\qquad$ $S_{11} = 0.68\underline{/-120°}$
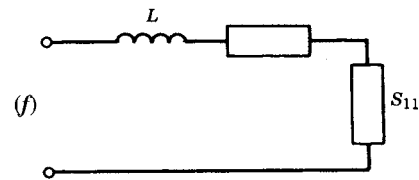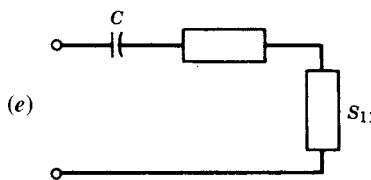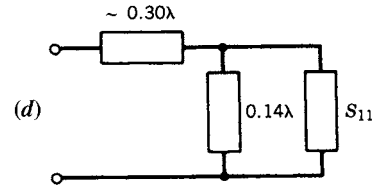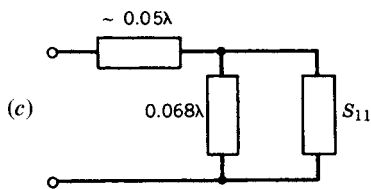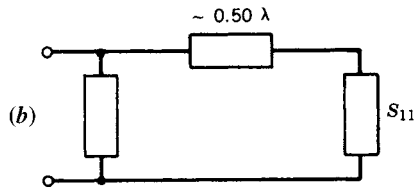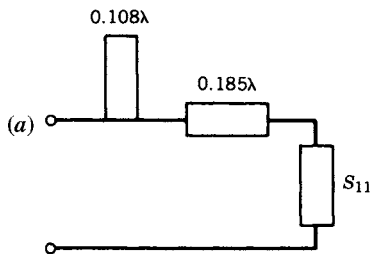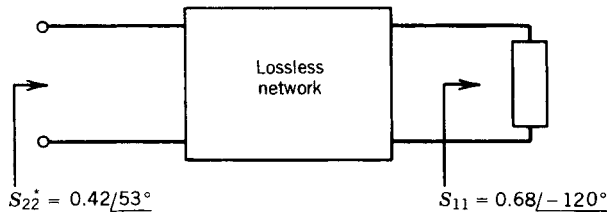
5.4 Design a three-element lossless lumped network M that matches the generator to the load at 10 GHz. What is the maximum VSWR for 20% bandwidth? Recommend modifications of M to increase bandwidth.
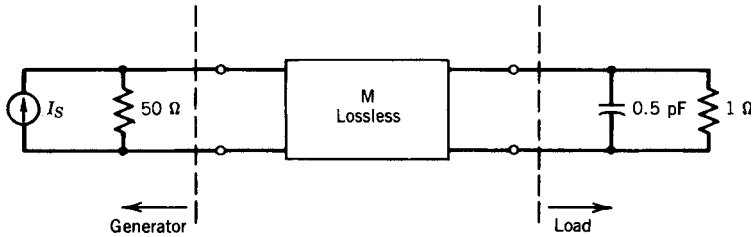
5.5 Repeat problem 3.8 with a single-element $\lambda/4$ line and two elements of $\lambda/4$ line (i.e., match 50 Ω to 7.07 Ω, then match 7.07 Ω to 1 Ω). Which circuit gives the widest bandwidth?

5.6 Given $Z_L/Z_0 = 1 - j1.2$ with $Z_0 = 50$ Ω:
  (a) Find Γ_L, Γ_L^*, $1/\Gamma_L$, and $1/\Gamma_L^*$.
  (b) Find Y_L/Y_0 and Y_L^*/Y_0.
  (c) Find the admittance of $1/\Gamma_L$ and the admittance of $1/\Gamma_L^*$.
  (d) Plot these eight points on a compressed Smith chart.

5.7 Match the following load to a 50-Ω generator using lumped elements.
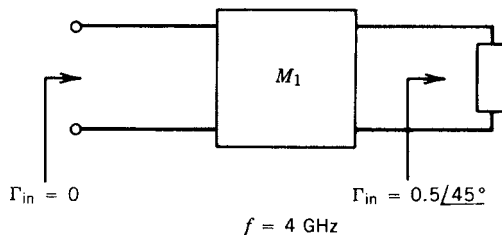
5.8 (a) Design four lossless matching networks using lumped elements.

  (b) Using only 50-Ω transmission lines (lossless), design two matching networks.

  (c) Using any lossless transmission line, design two matching networks.

  (d) Using lumped and transmission line elements, design four matching networks.
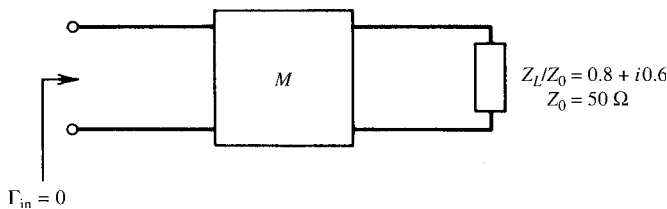
5.9   Find a single-section element that matches $Z_L/Z_0 = 1.4 - j0.6$ to a 50-Ω generator ($Z_0 = 50\ \Omega$).
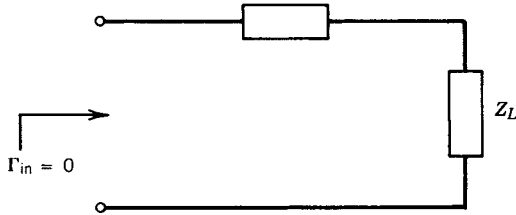
5.10   A low-noise amplifier is shown at $f = 8$ GHz for a 50-Ω generator and load. Find Γ_{on} for this transistor.
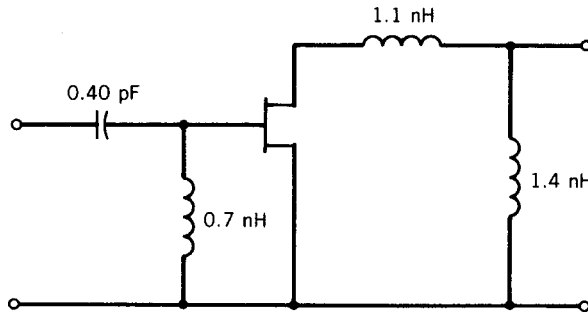
5.11   For the following distributed circuit, find the input impedance at $f = 2$ GHz and $f = 4$ GHz. Also calculate Γ_{in} at 2 and 4 GHz.
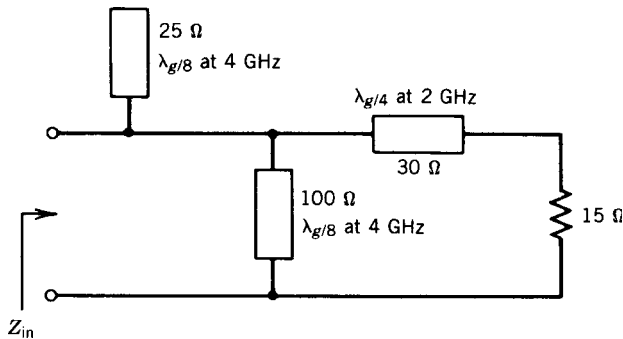
5.12   Calculate Z_{in} for the following two microstrip circuits. Assume $f = 10$ GHz, $\varepsilon_r = 10$, and $h = 25$ mils. Use Figures 1.24 and 1.25 to calculate Z_0 and k'.

(a)

Z_{in}

(b)

Z_{in}
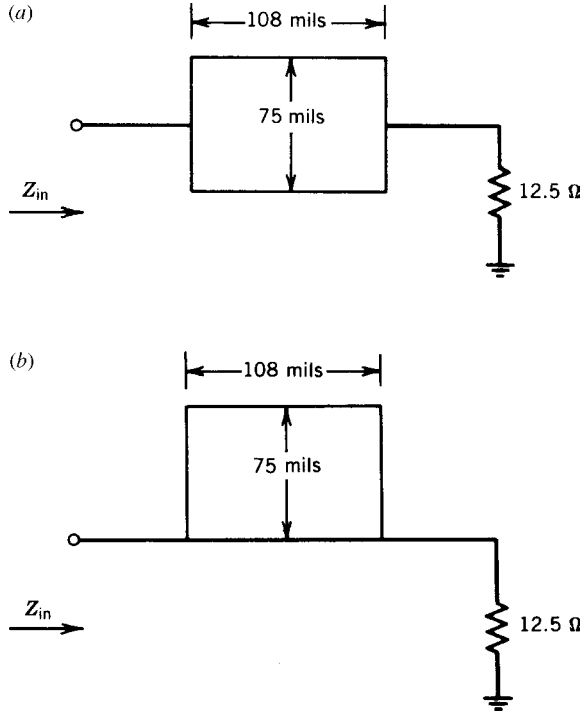
5.13   Given a LNA design, find Γ_{on} for $Z_0 = 50\ \Omega$. Assume $f = 6$ GHz.
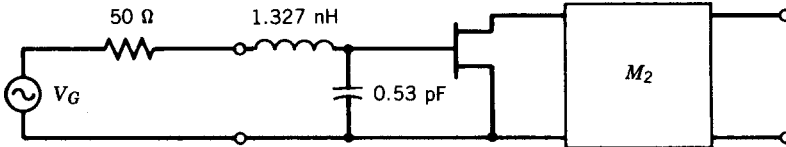
5.14   For the $4:1$ transformer shown in Figure 5.7, calculate the output power $P_o = 1/2\ |I_2|^2 R_L$, where the frequency dependence of the transmission lines is used. You will have three equations in the three unknowns I_1, I_2, and V_2. The final answer is

$$P_o = 1/2\ |I_2|^2 R_L = \frac{1/2\ (|V_g|^2(1 + \cos\theta)2R_L)}{[2R_G(1 + \cos\theta) + R_L\cos\theta]^2} + \left(R_G R_L + \frac{Z_0^2}{Z_0^2}\right)\sin^2\theta$$

CHAPTER 6

MICROWAVE FILTERS

6.1 INTRODUCTION

Filters are a crucial part of nearly every microwave system. The relatively high power of a cell phone transmitter must be kept out of the sensitive receiver, and this is done with a bandpass filter. The output of a microwave signal generator can include harmonics potentially confusing to the measurements being made: A low-pass or bandpass filter can clean this up. Transmitters of all kinds have stringent requirements on power outside of the licensed spectrum. Again, the solution is a high-quality bandpass filter.

The design of filters is a topic for which many books have been written. In this book, a number of simple practical design processes will be described which will solve most basic filter needs. For more complete catalogs of filter design, the reader is referred especially to a pair of books [6.1, 6.2] that are a good departure point for standard designs. In addition, several books on microwave circuit design also include material specifically on filters. Examples are books by Rizzi [6.3], Pozar [6.4], and Misra [6.5]. Later in the chapter, we will comment on complete synthesis techniques and software that can make more sophisticated filter needs practical. In fact, it is possible to do a lot of effective filter design using a basic spreadsheet program and the information collected here.

There are several divisions in the approach to filter design. A very intuitively satisfying method known as *image parameter design* (see Section 2.12 of Ref. 6.2) was the main approach for many years. In fact, it is still useful and is often included in filter surveys. However, the second division, the *insertion loss design* method, is simpler to learn and somewhat more flexible. We will explain that approach, realizing that there might be times when the other is still of use.

Design by insertion loss starts from a mathematical description of the overall desired response, usually $S_{21}(f)$ or some similar transfer property. From a prescribed response such as maximally flat (Butterworth), equal ripple (Chebyshev), and so on, a low-pass prototype is synthesized. Since this step of the process has been done many years ago, we will not concern ourselves with how the filter element values were obtained, just how to use them correctly. This is the subject of Section 6.2. Using frequency transformations of various kinds, high-pass, bandpass, and band-stop filters can be designed. That will be Sections 6.3 and 6.5. In microwave circuits, transmission lines often make the best filter elements, so we will include the Richards transformation in Section 6.4 to see how to design the most common microwave filters.

6.2 LOW-PASS PROTOTYPE FILTER DESIGN

A wide range of practical filters can be designed starting from normalized prototype designs. In this section, the characteristics of such prototypes are explored and the means of finding design values is described. A selection of tables of element values is included as a starting point for design.

The design procedures in this chapter are all based on low-pass prototypes such as are described below. In each of the designs, low pass, high pass, bandpass, or band-stop, the response will be based on some sort of frequency transformation of the low-pass response. To facilitate this, the low-pass responses will be given in a normalized frequency variable, x. For each filter, the appropriate transformation from x to the actual frequency being filtered will be given. Thus, we will start with the responses in this normalized variable.

6.2.1 Butterworth Response

As its name implies, a low-pass filter (LPF) favors low frequencies over high. More precisely, an ideal LPF would pass signals perfectly below some designated *cutoff frequency* and stop signals perfectly above cutoff. Basic signal analysis shows that the ideal is impossible, so we are left with the task of finding a *realizable* response. Without going into the details of realizability theory, there is a broad class of functions which meet this need. One of the simplest is the maximally flat, or Butterworth, response. To describe this response, let us define some terms. The radian cutoff frequency is $\omega_c = 2\pi f_c$. The normalized frequency variable will be $x = \omega/\omega_c$. Note that the cutoff in the normalized variable is $x_c = 1$. Then, for an n-element filter, the filter response will be

$$|S_{21}(x)|^2 = \frac{1}{1 + x^{2n}}$$

Figure 6.1 shows the maximally flat response in the passband for several values of n. Several general characteristics should be noted. First, the edge of the passband is always 3 dB down from the perfect response, which occurs only at dc. Second, more elements give a larger portion of the passband with low loss. Third, Figure 6.2 shows the stopband response, and more elements imply more selectivity (reduced signals in the stopband). In practice, the cutoff frequency can be adjusted from the 3-dB point to
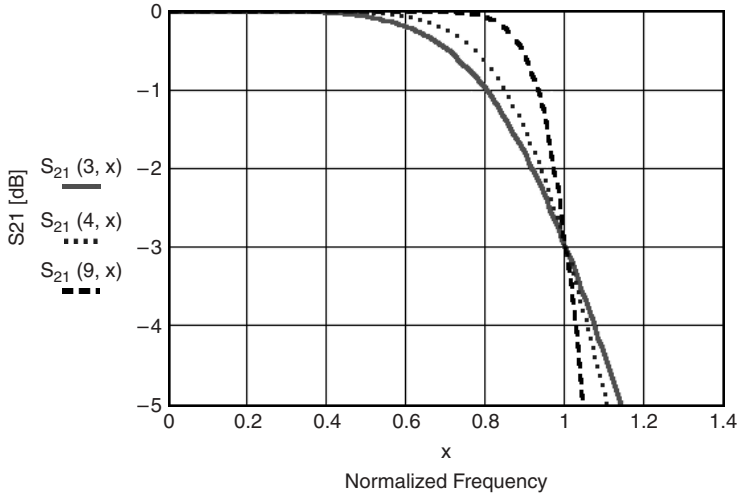
FIGURE 6.1 Butterworth passband response.
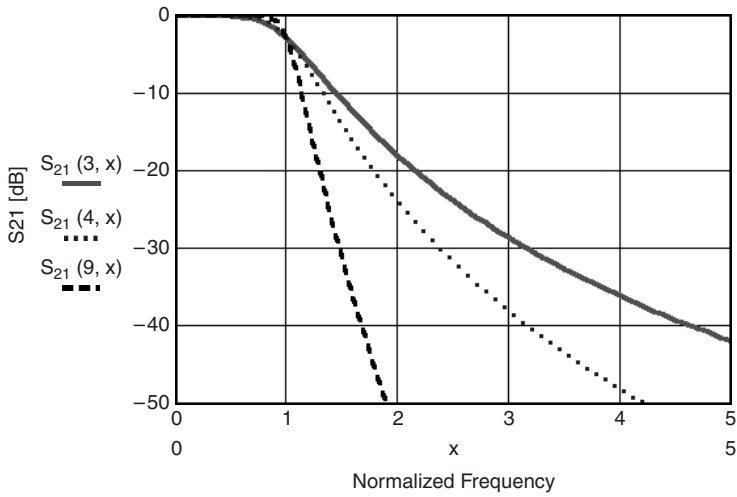
FIGURE 6.2 Butterworth stopband response.

some convenient value to improve passband performance, but this has a trade-off in stopband attenuation.

To be most useful, the prototype element values are usually designed for unity cutoff frequency and unity source and load impedance. Under that rule, the element values, known as *g values*, for maximally flat filters are

$$g_0 = 1$$

$$g_k = 2 \sin \left(\frac{(2^k - 1)\pi}{2n} \right)$$

$$g_{n+1} = 1$$
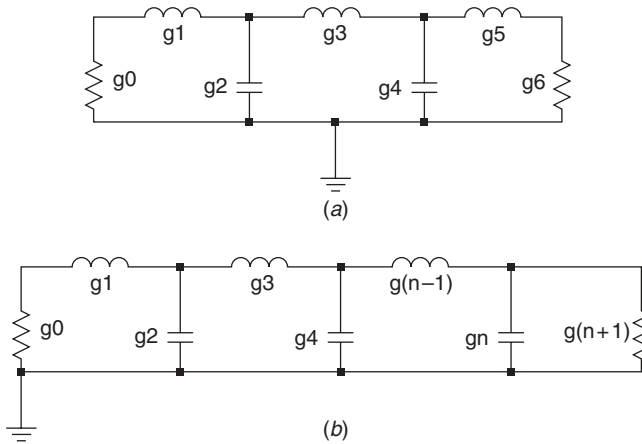
FIGURE 6.3 Low-pass filter: (*a*) prototype; (*b*) dual prototype.

where $k = 1, 2, \ldots, n$. The significance of the g values is as follows. Figure 6.3 shows the two possible prototype circuits based on this set of g values. In Figure 6.3a, g_0 has the units of ohms. (This distinction becomes important later when impedance scaling is to be applied.) The parallel capacitor immediately following has capacitance $C_1 = g_1$ farads. The next element is a series inductor, $L_2 = g_2$ henrys, and so on. The last element is the load resistor. Its value is 1, but the question of units depends on how many elements there are. The rule is that series (henrys or ohms) and parallel elements (farads or siemens) alternate. Thus, a filter ending with a parallel C will have a load resistance $R_{n+1} = g_{n+1}$ ohms. A filter ending with a series L will have a load conductance $G_{n+1} = g_{n+1}$ siemens. We will see later how to scale the elements for impedance and cutoff frequency so that reasonable element values can be obtained.

Figure 6.3b shows another possible circuit, one which is the dual of Figure 6.3a. Now, all of the parallel capacitors are replaced with series inductors and vice versa. The magnitude of the response of the two circuits is identical. One might be preferable because of specific element values or some other consideration, such as the need to reduce the number of inductors. Otherwise, they are equivalent.

Example 6.1 Butterworth Prototype Filter Even though the Butterworth prototype is a simple calculation, it is worthwhile to have an example. For $n = 5$,

$$g_0 = 1 = g_6 \qquad g_1 = 0.6180 = g_5 \qquad g_2 = 1.6180 = g_4 \qquad g_3 = 2.0000$$

For $n = 6$,

$$g_0 = 1 = \frac{1}{g_7} \qquad g_1 = 0.5176 = g_6 \qquad g_2 = 1.4142 = g_5 \qquad g_3 = 1.9319 = g_4$$

6.2.2 Chebyshev Response

The Butterworth response is a good starting point for learning to design prototype filters because it is simple and the student can concentrate on the basic operations.

However, the 3-dB cutoff or the need to readjust the passband to avoid that problem limit the flexibility of the maximally flat filter. (There are special cases in which the Butterworth response has advantages, but those are few and far between.) The *equal-ripple*, or *Chebyshev*, response is a much more flexible one at the expense of some complexity.

The basic Chebyshev response is based on the Chebyshev polynomial. The defining response comes in two related parts. Inside the passband, for $|x| < 1$,

$$C_n(x) = \cos[n \cos^{-1}(x)]$$

Outside the passband, for $|x| > 1$,

$$C_n(x) = \cosh[n \cosh^{-1}(x)]$$

Strictly speaking, this is the Chebyshev function of the first kind. By careful application of complex functions, one can easily see the linkage between these two formulations.

That these describe a polynomial is not obvious but can be seen from the following sequence. For $n = 0$, $C_0(x) = \cos(0) = 1$. Similarly, $C_1(x) = \cos[\cos^{-1}(x)] = x$. To go further, we can make use of the following recursion relationship:

$$C_{n+1}(x) = 2x C_n(x) - C_{n-1}(x)$$

Now, the functions for all of the higher orders can be constructed from the first two. By inspection, one can see that all higher functions will be polynomials in x. This has special significance in realizability theory and is somewhat simpler than using transcendental functions. For illustration, the next few functions are

$$C_2(x) = 2x^2 - 1$$
$$C_3(x) = 4x^3 - 3x$$
$$C_4(x) = 8x^4 - 8x^2 + 1$$
$$C_5(x) = 16x^5 - 20x^3 + 5x$$

Note that the polynomial definitions apply equally well in the passband or in the stopband. These functions have the property that $|C_n(x)|$ is bounded by 1 in the passband and grows without limit outside. To form a useful transfer function, one more parameter is needed. The extra control in design is the choice of the maximum loss in the passband, referred to as the *ripple*. This parameter is usually specified in decibels. The factor needed for the transfer response is usually labeled e. Its relationship to R, the ripple in decibels, is

$$\varepsilon = \sqrt{e^{R/10} - 1}$$

Then, the response is

$$|S_{21}(x)|^2 = \frac{1}{1 + \varepsilon^2 C_n^2(x)}$$
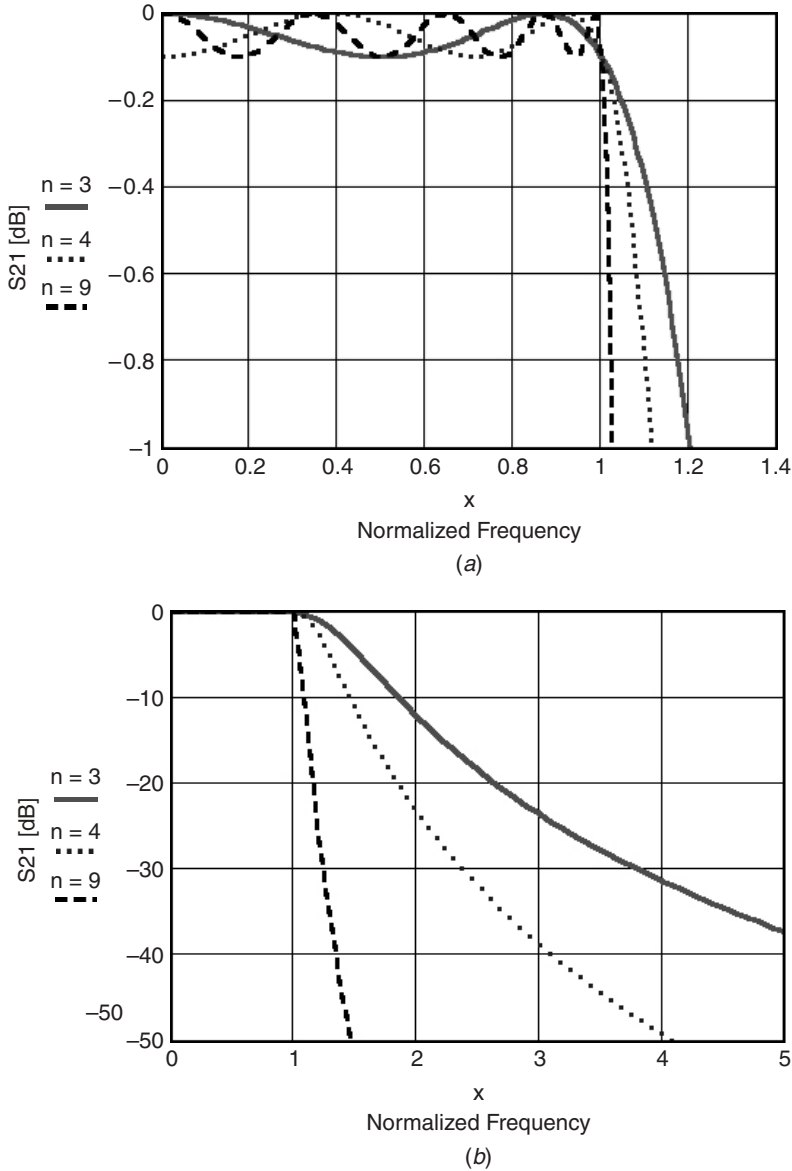
FIGURE 6.4   (*a*) Chebyshev passband response. (*b*) Chebyshev stopband response.

Figure 6.4 shows the response for several filters with varying orders for a ripple of 0.1 dB. Figure 6.4*a* shows the passband characteristics of three filters, $n = 3, 4, 9$. The higher order filter has more "ripples" in the passband, but it never exceeds the specified loss of 0.1 dB. Figure 6.4*b* shows the stopband response for the three filters. Some of the same trade-offs with Butterworth filters apply to Chebyshev designs. More sections mean more rejection. There is now the possibility of trading ripple (quality of passband response) for rejection (quality of stopband response). This makes a Chebyshev filter more flexible for design purposes.

Another trade-off is the complexity of calculating the prototype element values. The g values can be calculated as follows. Let R be the ripple in decibels. Define the following parameters:

$$\beta = \ln\left(\frac{1}{\tanh\left(R/40\log(e)\right)}\right) \qquad \gamma = \sinh\left(\frac{\beta}{2n}\right)$$

Then, for $k = 1, 2, \ldots, n$, calculate the following coefficients:

$$a_k = \sin\left[\frac{(2k-1)\pi}{2n}\right] \qquad b_k = \gamma^2 + \sin^2\left(\frac{k\pi}{n}\right)$$

Choose $g_0 = 1$. The first g value will be

$$g_1 = 2\frac{a_1}{\gamma}$$

Then, for $k = 2, 3, \ldots, n$,

$$g_k = \frac{4a_{k-1}a_k}{b_{k-1}g_{k-1}}$$

The final g value will depend upon whether n is even or odd. For n odd, $g_n + 1 = 1$. However, even-order circuits must have loss at dc equal to the ripple, so a small mismatch must be introduced. To do that,

$$g_{n+1} = \frac{1}{\tanh^2\left(\beta/4\right)}$$

Table 6.1 gives the Chebyshev g values for a few combinations of ripple and order. More complete tables can be found in Refs. 6.1 and 6.2. (When using Ref. 6.2, be certain to use the correct bandwidth. All of the tables there are given in terms of a 3-dB cutoff frequency. Figure 6.5 in Ref. 6.2 gives conversion values between the 3-dB and the ripple cutoff frequencies.)

6.3 TRANSFORMATIONS

6.3.1 Low-Pass Filters: Frequency and Impedance Scaling

The g values are clearly not practical for real-world circuits because they are intended for a theoretical 1-Ω source/load and 1 rad/s frequency. To make a practical low-pass filter, we need to include the actual desired cutoff and the load resistance. We will assume here that source and load are resistive and have the same impedance. The general rules are as follows:

1. Divide all element values by the radian cutoff frequency, $\omega_c = 2\pi f_c$. To find the frequency response, use the normalized frequency variable, $x = \omega/\omega_c$. This can also be done in the standard frequency variable, $x = f/f_c$.
2. Multiply all inductance values by the source/load impedance.
3. Divide all capacitance values by the source/load impedance.

TABLE 6.1   Chebyshev *g* Values

0.01 dB Ripple								
1	1	0.0960	1.0000					
2	1	0.4489	0.4078	1.1007				
3	1	0.6292	0.9703	0.6292	1.0000			
4	1	0.7129	1.2004	1.3213	0.6476	1.1007		
5	1	0.7563	1.3049	1.5773	1.3049	0.7563	1.0000	
6	1	0.7814	1.3600	1.6897	1.5350	1.4970	0.7098	1.1007
7	1	0.7969	1.3924	1.7481	1.6331	1.7481	1.3924	0.7969	1.0000
0.05 dB Ripple								
1	1	0.2152	1.0000					
2	1	0.6923	0.5585	1.2396				
3	1	0.8794	1.1132	0.8794	1.0000			
4	1	0.9588	1.2970	1.6078	0.7734	1.2396		
5	1	0.9984	1.3745	1.8283	1.3745	0.9984	1.0000	
6	1	1.0208	1.4141	1.9183	1.5475	1.7529	0.8235	1.2396
7	1	1.0346	1.4369	1.9637	1.6162	1.9637	1.4369	1.0346	1.0000
0.1 dB Ripple								
1	1	0.3052	1.0000					
2	1	0.8430	0.6220	1.3554				
3	1	1.0316	1.1474	1.0316	1.0000			
4	1	1.1088	1.3062	1.7704	0.8181	1.3554		
5	1	1.1468	1.3712	1.9750	1.3712	1.1468	1.0000	
6	1	1.1681	1.4040	2.0562	1.5171	1.9029	0.8618	1.3554
7	1	1.1812	1.4228	2.0967	1.5734	2.0967	1.4228	1.1812	1.0000
0.5 dB Ripple								
1	1	0.6986	1.0000					
2	1	1.4029	0.7071	1.9841				
3	1	1.5963	1.0967	1.5963	1.0000			
4	1	1.6703	1.1926	2.3661	0.8419	1.9841		
5	1	1.7058	1.2296	2.5408	1.2296	1.7058	1.0000	
6	1	1.7254	1.2479	2.6064	1.3137	2.4758	0.8696	1.9841
7	1	1.7373	1.2582	2.6383	1.3443	2.6383	1.2582	1.7373	1.0000

For example, let us choose a five-section Chebyshev filter with 0.1 dB ripple. For a source and load of 50 Ω and a cutoff frequency of 10 GHz, the actual L's and C's are

$$L_1 = L_5 = \frac{g_1 Z_0}{\omega_c} = 0.794 \text{ nH}$$

$$C_2 = C_4 = \frac{g_2}{Z_0 \omega_c} = 0.438 \text{ pF}$$

$$L_3 = \frac{g_3 Z_0}{\omega_0} = 1.455 \text{ nH}$$
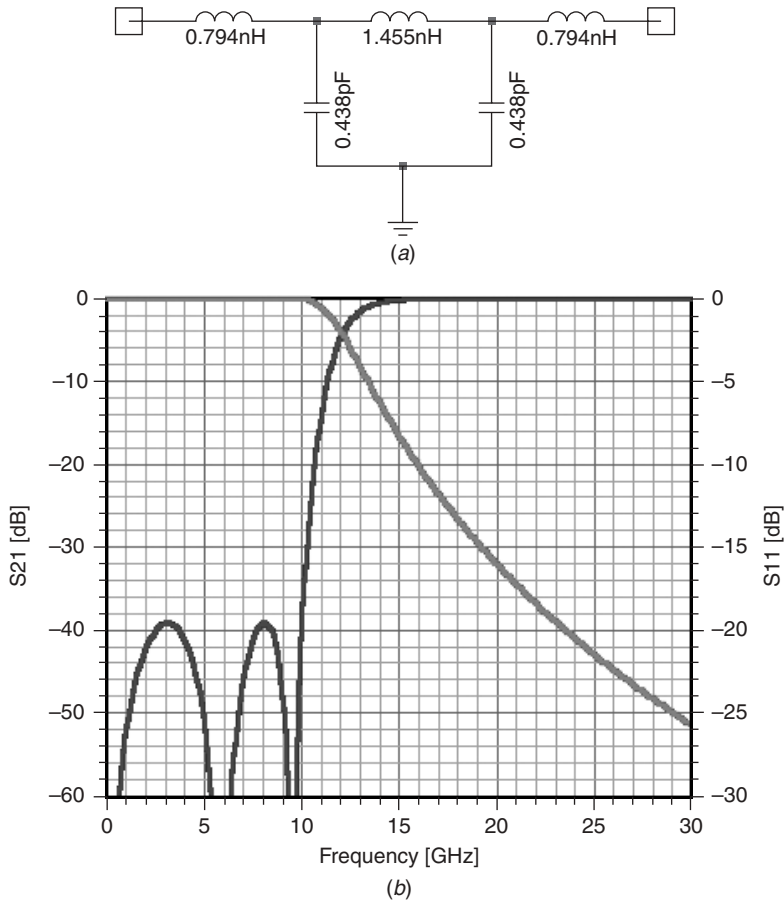
FIGURE 6.5 Lumped-element low-pass filter: (*a*) example circuit; (*b*) response.

The dual network has the following *L*'s and *C*'s:

$$C_1 = C_5 = 0.318 \text{ pF} \qquad L_2 = L_4 = 1.094 \text{ nH} \qquad C_3 = 0.582 \text{ pF}$$

Figure 6.5*a* shows the schematic of the first filter. Figure 6.5*b* shows the S_{11} and S_{21} response of both filters. Note that the amplitude response is identical for both dual networks.

6.3.2 High-Pass Filters

Low-pass filters are not the only types of filters that can be designed from the basic prototypes developed in Section 6.2. There is a considerable variety of filters that can be derived from the *g* values using frequency transformations. The simplest, of course, was the frequency-scaled low-pass filter discussed in the preceding section. In this section, we branch out to design a class of filters with a fundamentally different frequency response.

In the filter designs considered here, the normalized frequency variable will be the starting point. The first task is to identify the key parts of the response. Then, they can be modified using a mathematical transformation. Finally, the element values are derived based on the transformation.

The behavior of the low-pass filter can be summarized in outline:

1. Perfect transmission at dc
2. Perfect rejection at infinite frequency
3. Some appropriate low loss at cutoff, $x_{LP} = 1$

As a means of seeing the transition to high pass, consider an elementary low pass filter consisting of a single series inductance, L. The reactance, $X = \omega L$, easily meets criteria 1 and 2. The third requirement will be fulfilled by choosing the loss at cutoff such that $X = \omega_c L$. Now, consider the following frequency transformation:

$$x_{HP} = \frac{1}{x_{LP}} = \frac{\omega_c}{\omega} = \frac{f_c}{f}$$

Compare the behavior of this new circuit with the low-pass one:

1. At zero applied frequency, the transformed frequency becomes infinite. If the transformed filter is to be high pass, it needs to have high rejection. A series capacitance will do this.
2. At infinite frequency, the series C will pass signals perfectly.
3. The cutoff value will be the same in both cases, leading to the rule that

$$C_{HP} = \frac{1}{L_{LP}}$$

Note that, for the parallel elements in the low pass, the exchange is reversed:

$$L_{HP} = \frac{1}{C_{LP}}$$

Including the effects of impedance and frequency scaling, the design of a high-pass filter directly from the normalized g values is as follows:

$$L_j = \frac{Z_0}{\omega_c g_j} \qquad C_k = \frac{1}{g_k \omega_c Z_0}$$

As an example, choose $f_c = 2$ GHz and $n = 5$. In a 50-Ω system, the element values are

$$L_1 = L_5 = 3.985 \text{ nH} \qquad C_2 = C_4 = 1.158 \text{ pF} \qquad L_3 = 2.176 \text{ nH}$$

As with the low-pass case, there is a dual configuration. For the same design parameters,

$$C_1 = C_5 = 1.594 \text{ pF} \qquad L_2 = L_4 = 2.895 \text{ nH} \qquad C_3 = 0.871 \text{ pF}$$
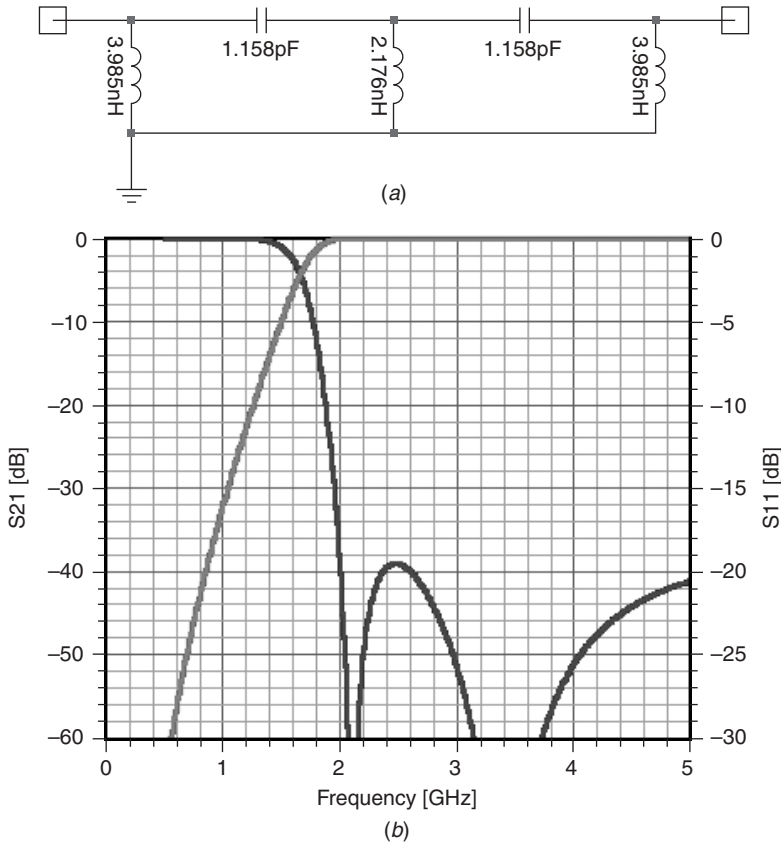
FIGURE 6.6 Lumped-element high-pass filter: (*a*) example circuit; (*b*) response.

Note that the range of the element values is roughly the same for a high-pass filter as for a low-pass circuit of the same cutoff and impedance level. As with the scaled low-pass design, the choice of which circuit to use can be made on criteria such as convenient element values or convenient topology. Figure 6.6*a* shows the schematic and Figure 6.6*b* the response of the scaled circuit.

6.3.3 Bandpass Filters

Many filtering applications require passing signals in a selected band. In basic terms, the passband will be from f_1 to f_2. For lumped-element filters, which we are considering here, the band center will be f_0, where

$$f_0 = \sqrt{f_1 f_2}$$

The bandwidth $\mathrm{BW} = f_2 - f_1$, with the usual order being $f_2 > f_1$. The fractional bandwidth is

$$w = \frac{\mathrm{BW}}{f_0} = \frac{f_2 - f_1}{f_0} = \frac{f_2 - f_1}{\sqrt{f_2 f_1}}$$

The normalized frequency must be calculated so that dc in the low-pass filter is at the band center and the cutoff is at both band edges. This will be true if the frequency transformation is

$$x_{\text{BP}} = \frac{1}{w}\left[\frac{f}{f_0} - \frac{f_0}{f}\right]$$

Substituting the definitions in terms of f_1 and f_2 will show the following:

1. When $f = f_1$, $x = -1$, which is still cutoff for the low-pass prototype.
2. When $f = f_2$, $x = +1$, also cutoff.
3. When $f = f_0$, $x = 0$, as desired.
4. When $f = 0$, x becomes infinite.
5. When f becomes infinite, x also goes to infinity.

The element values are a little more complicated for the bandpass filter. To summarize, the design procedure is as follows:

1. Design a low-pass filter with $f_{c,\text{LP}} = f_2 - f_1$. Impedance scaling can be performed at this step or done later.
2. For each element in the low-pass filter, resonate with the appropriate element at the center frequency, f_0. That is, for a series L, add a series C with

$$C = \frac{1}{\omega_0^2 L}$$

and for a shunt C, add a shunt L with

$$L = \frac{1}{\omega_0^2 C}$$

For example, let $n = 3$ with 0.01 dB ripple and a passband of

$$f_1 = 500 \text{ MHz} \qquad f_2 = 1000 \text{ MHz} \qquad \text{BW} = 500 \text{ MHz}$$

$$f_0 = 707.1 \text{ MHz} \qquad w = 70.7\%$$

First, the LPF design for cutoff $=$ BW,

$$L_1 = \frac{Z_0 g_1}{2\pi \text{ BW}} = 10.01 \text{ nH} = L_3 \qquad C_2 = \frac{g_2}{Z_0 2\pi \text{ BW}} = 6.178 \text{ pF}$$

Resonating each element at the center frequency,

$$C_1 = \frac{1}{\omega_0^2 L_1} = 5.059 \text{ pF} = C_3 \qquad L_2 = \frac{1}{\omega_0^2 C_2} = 8.2 \text{ nH}$$

Figure 6.7 shows the resulting schematic and response.
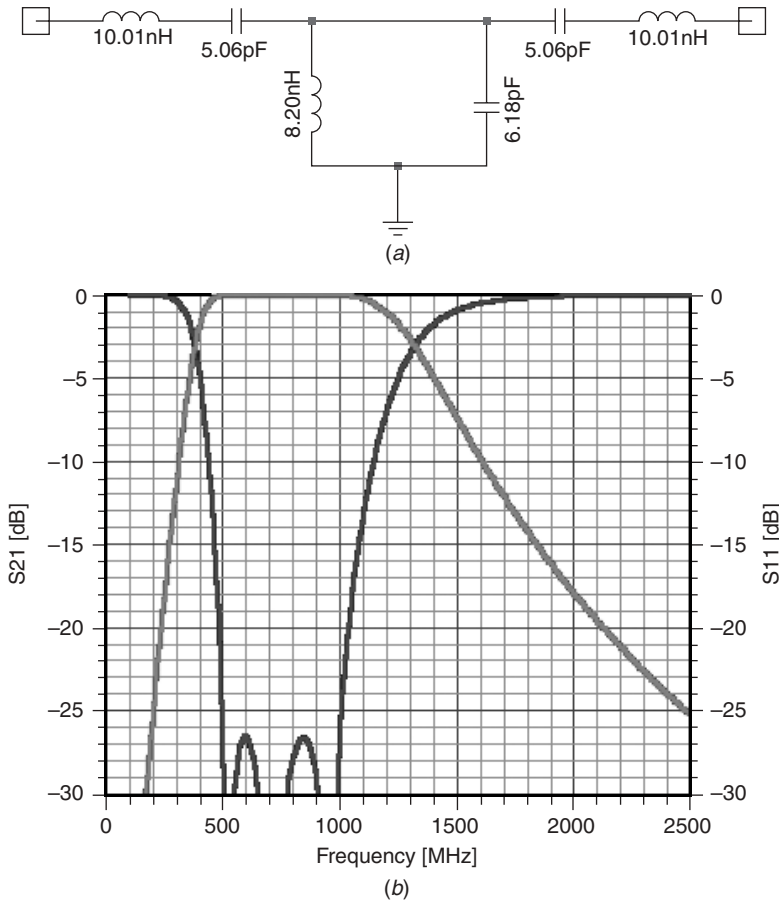
FIGURE 6.7 Lumped-element bandpass filter: (*a*) example circuit; (*b*) response.

For another example, an $n = 3$ filter has the following specifications:

$$f_1 = 824 \text{ MHz} \qquad f_2 = 849 \text{ MHz} \qquad f_0 = 836.4 \text{ MHz}$$

$$\text{BW} = 25 \text{ MHz} \qquad \text{Ripple} = 0.01 \text{ dB}$$

The Chebyshev g values are $g_1 = g_3 = 0.62918$ and $g_2 = 0.97028$. Then, the elements of the low-pass filter are

$$L_1 = L_3 = 200 \text{ nH} \qquad C_2 = 123 \text{ pF}$$

Resonating the L's with C's and the C with an L, we add

$$C_1 = C_3 = 0.1808 \text{ pF} \qquad L_2 = 0.2931 \text{ nH}$$

Note that the element values for this filter, which is pretty narrow in bandwidth, have a much larger range than previous filters. In fact, the large elements would likely have

resonances in the passband, while the small elements would be difficult to realize precisely. The design detailed above will work reasonably well for large-bandwidth filters. We will develop a design procedure for narrow-bandwidth filters which is much more practical by using coupled resonators.

6.3.4 Narrow-Band Bandpass Filters

To deal with narrow-band bandpass filters, it is useful to think of the filters in terms of coupled resonators of identical topology. For example, we will consider resonators consisting of a parallel *LC* topology. The resonators will be connected with coupling elements, which can be series or parallel, and *L* or *C*, as long as the coupling between resonators is small. We will stick to series *C* coupling in our example, but the coupling can be varied. Finally, to realize resonators of practical values, we will transform the impedance level of the filter using transformers or approximations to transformers.

One of the advantages of this approach is that there is flexibility in the types of elements used for resonators. The discussion here will be in terms of *LC* resonators, but quarter-wavelength or half-wavelength transmission lines would do as well. The common thread linking various types of resonators is the *reactance slope parameter* for series resonators and the *susceptance slope parameter* for parallel resonators. The general definition will serve to analyze specific resonator topologies. For series resonators, the reactance slope parameter is

$$\alpha = \frac{\omega_0}{2} \left. \frac{dX}{d\omega} \right|_{\omega=\omega_0}$$

where $\omega = 2\pi f$ is the radian frequency variable, ω_0 is the radian resonant frequency, and X is the reactance of the resonator. The dual case is that of the parallel resonator:

$$\beta = \frac{\omega}{2} \left. \frac{dB}{d\omega} \right|_{\omega=\omega_0}$$

For example and for later use, let us find the susceptance slope parameter of a parallel *LC* circuit. We start by finding the susceptance:

$$B = \omega C - \frac{1}{\omega L} = \omega C - \frac{\omega_0^2 C}{\omega}$$

$$\left. \frac{dB}{d\omega} \right|_{\omega=\omega_0} = C + C \left(\frac{\omega}{\omega_0} \right)^2 \Bigg|_{\omega=\omega_0} = 2C$$

$$\beta = \frac{\omega_0}{2} 2C = \omega_0 C = \frac{1}{\omega_0 L}$$

By a similar process it can be shown that, for a series resonator,

$$\alpha = \omega_0 L = \frac{1}{\omega_0 C}$$

The advantage of this approach is that any kind of resonator can be used as long as we can calculate the appropriate slope parameter.

Another change of outlook for narrow-bandwidth bandpass filters is the use of normalized k (coupling) and q (quality factor) values. For a full discussion of these parameters and an extensive set of tables, see Zverev [6.2]. For the purposes here, we will relate them to our standard g values. For an n-resonator filter, the normalized q values are $q_1 = g_1$ and $q_n = g_n$. Then, for $j = 1, \ldots, n - 1$, the normalized coupling values are

$$k_{j,j+1} = \frac{1}{\sqrt{g_j g_{j+1}}}$$

For example, if $n = 5$ and Ripple $= 0.1$ dB,

$$k_1 = g_1 = g_5 = k_5 = 1.146813$$

$$k_{12} = \frac{1}{\sqrt{g_1 g_2}} = 0.797446 = k_{45}$$

$$k_{23} = \frac{1}{\sqrt{g_2 g_3}} = 0.607664 = k_{34}$$

The narrow-band bandpass filter design method is as follows:

1. Choose the passband parameters f_1 and f_2, the order of response n, and the type of response (Chebyshev, Butterworth, etc.). From this, the center frequency $f_0 = \sqrt{f_1 f_2}$ and $\omega_0 = 2\pi f_0$ and the bandwidth BW $= f_2 - f_1$ are calculated.
2. Calculate the appropriate g values and, from them, the normalized k and q values.
3. Choose the desired node capacitances, CN_j. (They can be all the same or varied. The main criterion is practicality of the capacitance for the application. Note that the actual capacitor values will be adjusted slightly.)
4. From the node capacitances, calculate the resonator inductance values:

$$L_j = \frac{1}{\omega_0^2 CN_j}$$

Note that the inductance can be chosen and the node capacitances calculated if desired.
5. Calculate the capacitances coupling resonators: For $j = 1, 2, \ldots, n$

$$Cc_j = CN_j k_{j,j+1} \left(\frac{\text{BW}}{f_0}\right) \sqrt{CN_j CN_{j+1}}$$

6. Each resonator needs to resonate at the center frequency, ω_0. However, the adjacent circuit elements will affect this frequency somewhat. An approximate means of compensating for this is to consider the adjacent coupling capacitors to be shorted to ground, which is usually a good estimate. Then, the actual resonator capacitances will be

$$C_1 = CN_1 - Cc_{12}$$

$$C_n = CN_n - Cc_{n-1,n}$$

$$C_j = CN_j - Cc_{j-1,j} - Cc_{j,j+1} \qquad \text{for } j = 1, 2 \ldots, n$$

7. The impedance level of the filter has been arbitrarily set to ensure reasonable resonator element values. For narrow-bandwidth filters, this usually means a very high source and load resistance for good match. To adjust this to 50 Ω (or other useful resistance), we must insert a transformer at each end. Fortunately, a capacitive Π network can be used in place of an actual transformer. Finally, the Π network can be represented by only a single series capacitance. This is especially useful for narrow bandwidths. First, the resistance the filter naturally wants to see is found:

$$R_t = \omega_0 q_1 \left(\frac{f_0}{\text{BW}} \right) L_1$$

If the q values and the end-resonator values are not equal, a separate load will be needed for each end. Then, the transformer end-section capacitance will be

$$C_e = \frac{1}{\omega_0} \sqrt{\frac{1}{Z_0(R_t - Z_0)}}$$

8. As a last step, the end resonators must be adjusted slightly, since they will see a little capacitance through the end section. This equivalent capacitance is

$$C_t = \frac{1}{\omega_0^2 C_e Z_0^2 + 1/C_e}$$

Then, the end-resonator capacitances are adjusted:

$$C_1 = C_1 - C_t \qquad C_n = C_n - C_t$$

The following example will illustrate the calculations. The number of resonators is $n = 3$ with 0.01 dB ripple. The g values are

$$g_1 = g_3 = 1.03516 \qquad g_2 = 1.1474$$

From these, the k and q values are

$$q_1 = q_3 = 1.03516 \qquad k_{12} = k_{23} = 0.91757$$

The passband will be from 824 to 849 MHz, leading to $f_0 = 836.4$ MHz and BW $=$ 25 MHz. The node capacitances are chosen to be $CN_j = 2$ pF for $j = 1, 2, 3$. The resulting node inductances are 18.1 nH. The coupling capacitances are $C_{12} = C_{23} = 0.051$ pF. The end capacitance for the impedance transformation is $C_e = 0.588$ pF. After the final adjustments, the resonator capacitances will be

$$C_1 = C_3 = 1.222 \text{ pF} \qquad C_2 = 1.725 \text{ pF}$$

Figure 6.8 shows the schematic of the filter and the resulting frequency response.
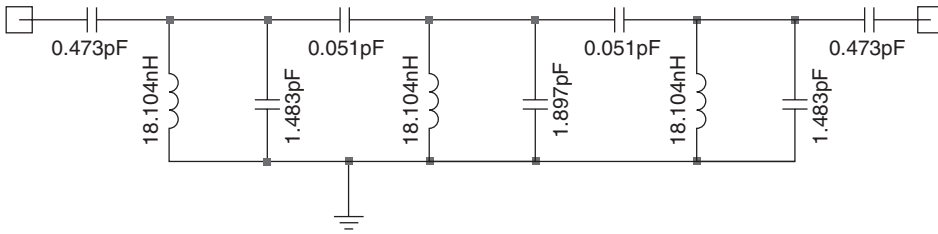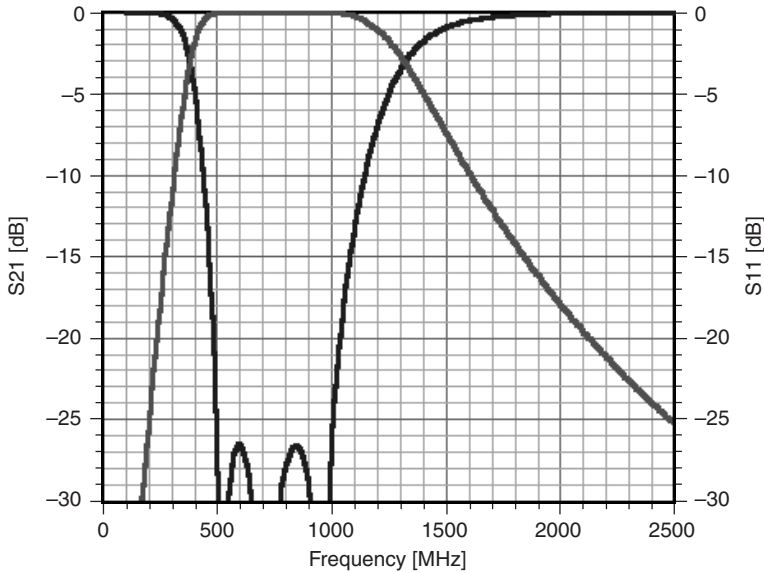
FIGURE 6.8   Lumped-element bandpass filter: (*a*) example circuit; (*b*) response.

6.3.5   Band-Stop Filters

In many applications it is desirable to filter out selected frequencies or bands of fre-
quencies. The passband now splits into two passbands, mirrored about the stopband.
The first passband looks very much like the traditional low-pass passband, going from
dc to the lower edge of the stopband, f_1. The stopband goes from f_1 to the upper
edge, f_2. The normalized transformed frequency is

$$x = \frac{w}{f/f_0 - f_0/f}$$

To calculate the element values, we again start with the prototype low-pass filter, the
g values. As with the bandpass filter, each element is resonated at f_0, which has
now become the middle of the stopband. The parallel elements consist of a series LC
resonator, while the series elements are a parallel LC resonator. Specifically, for the
parallel branch j,

$$L_j = \frac{Z_0}{wg_j\omega_0} \qquad C_j = \frac{wg_j}{\omega_0 Z_0}$$
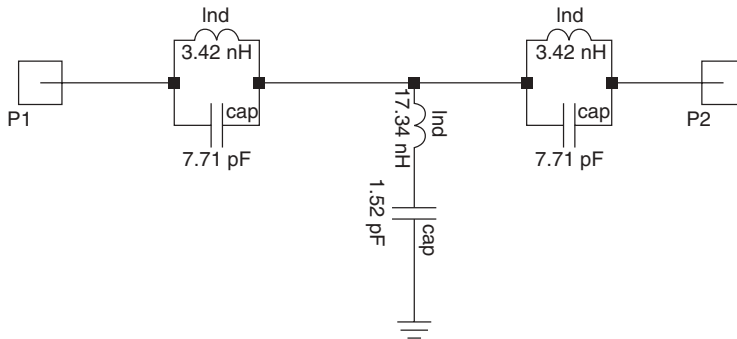
(a) Schematic
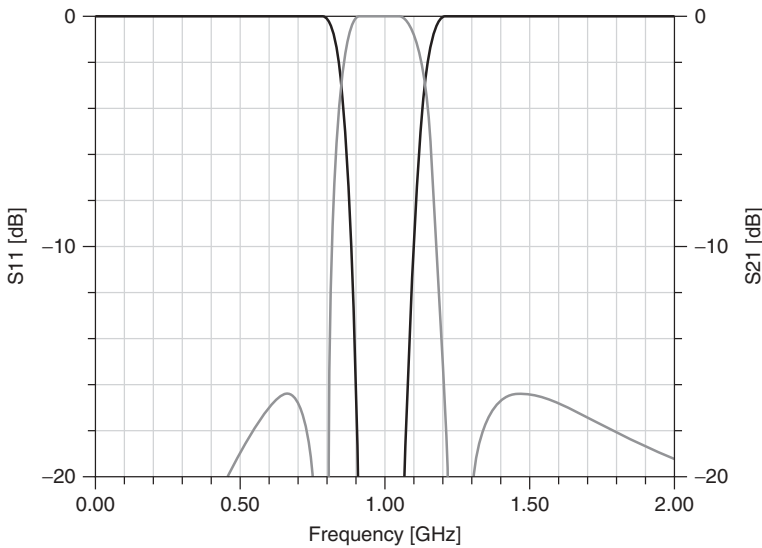
(b) Response

FIGURE 6.9 Band-stop filter: (a) Schematic. (b) Response.

where $\omega_0 = 2\pi f_0$ is the radian center frequency. Figure 6.9a shows the schematic for a three-section band-stop filter with the following specifications:

$$f_1 = 800 \text{ MHz} \qquad f_2 = 1200 \text{ MHz} \qquad f_0 = 979.8 \text{ MHz}$$

$$w = 40.8\% \qquad n = 3 \qquad \text{Ripple} = 0.1 \text{ dB}$$

The element values for a series–parallel–series filter are

$$L_1 = L_3 = \frac{wg_1 Z_0}{\omega_0} = 3.42 \text{ nH}$$

$$C_1 = C_3 = \frac{1}{w\omega_0 g_1 Z_0} = 7.71 \text{ pF}$$

$$L_2 = \frac{Z_0}{w g_2 \omega_0} = 17.34 \text{ nH}$$

$$C_2 = \frac{w g_2}{\omega_0 Z_0} = 1.52 \text{ pF}$$

Figure 6.9*b* shows the response of the filter. Note that the equal-ripple responses are from dc to f_1 and from f_2 to infinite frequency. The stopband has perfect attenuation at f_0 and moves monotonically down away from f_0. The attenuation at f_1 and f_2 is equal to the ripple, so the actual part of the band that does the filtering is between those two points.

Calculations for narrower stopbands show an increasing divergence in element values, eventually becoming impractical. For such cases, a series of resonators loosely coupled to the through path will serve.

6.4 TRANSMISSION LINE FILTERS

Lumped-element filters play a significant role in microwave filter applications, but the use of various kinds of transmission line filters is arguably of more utility. High-Q cavity and dielectric filters are useful for the most stringent filtering applications. Printed-circuit filters with relatively low Q are useful to be integrated into printed-circuit applications. Some of these filters can be designed from lumped circuits, and we will explore that area. However, there is a large class of unique filters based on transmission line properties.

Before proceeding, let us look at the properties of transmission lines. Their main feature is that they delay signals from one end of the line to the other. Consider a transmission line element shown in Figure 6.10 with impedance Z_c, phase length θ, and terminated at both ends in resistance Z_0. A wave entering port 1 will pass down the line and, in principle, be reflected at port 2 at the other end. The reflected wave will return to port 1, reflect again, and so on. Thus, the port voltages at each end will be sums of the individual wave voltages:

$$V_1 = V_1^+ + V_1^- \qquad V_2 = V_2^+ + V_2^-$$

At a point on the line, the wave current and wave voltage will be related by the line characteristic impedance. The sign of that relationship will depend on the direction of
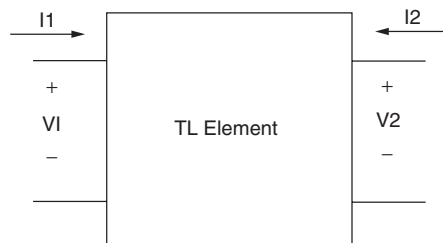
FIGURE 6.10   Transmission line element for *ABCD* parameter analysis.

travel along the line. Specifically, at the two ports

$$V_i^+ = Z_c I_i^+ \qquad V_i^- = -Z_c I_i^-$$

where $i = 1,2$ for this case. In the frequency domain, a wave launched into port 1 will be delayed by the phase shift θ before it reaches the other end. In detail,

$$V_2^- = V_1^+ e^{-j\theta} \qquad V_1^- = V_2^+ e^{-j\theta}$$

Finally, a wave leaving port 2 will be reflected back depending on the relationship between Z_c and Z_0:

$$V_2^+ = V_2^- \frac{Z_c - Z_0}{Z_c + Z_0} \qquad V_1^+ = V_1^- \frac{Z_c - Z_0}{Z_c + Z_0}$$

Now we can find the *ABCD* parameters of this element:

$$A = \left.\frac{v_1}{v_2}\right|_{i_2=0} = \left.\frac{v_1^+ + v_1^-}{v_2^+ + v_2^-}\right|_{i_2=0}$$

It will be convenient to express A in terms of one of the four variables. Since we can visualize this process as a wave entering port 1, we will choose v_1^+. The wave traveling to port 2 will be $v_2^- = v_1^+ e^{-j\theta}$. Since port 2 is open, the voltage will reflect back in phase, and $v_2^+ = v_2^- = v_1^+ e^{-j\theta}$. The newly reflected wave travels back to the input, leaving $v_1^- = v_2^+ e^{-j\theta} = v_1^+ e^{-2j\theta}$. Combining all of these parts,

$$A = \frac{v_1^+ + v_1^+ e^{-2j\theta}}{v_1^+ e^{-j\theta} + v_1^+ e^{-j\theta}} = \frac{e^{j\theta} + e^{-j\theta}}{2} = \cos(\theta)$$

It is practical to deal with the other case requiring an open circuit on port 2:

$$C = \left.\frac{i_1}{v_2}\right|_{I_2=0} = \frac{v_1^+/Z_c - v_1^-/Z_c}{v_2^+ + v_2^-} = \frac{v_1^+/Z_c - v_1^+ e^{-2j\theta}/Z_c}{v_1^+ e^{-j\theta} + v_1^+ e^{-j\theta}} = \frac{1}{Z_c} \frac{e^{j\theta} - e^{-j\theta}}{2}$$

$$= \frac{j\cos(\theta)}{Z_c}$$

Turning to B, the same wave process is in place, but port 2 now must be short circuited, causing a phase reversal in the reflected wave:

$$B = -\left.\frac{v_1}{i_2}\right|_{v_1=0} = -\frac{v_1^+ + v_1^-}{v_2^+/Z_c - v_2^-/Z_c} = -\frac{v_1^+ - v_1^+ e^{-2j\theta}}{v_1^+ e^{-j\theta}/Z_c + v_1^+ e^{-j\theta}/Z_c}$$

$$= -Z_c \frac{1 - e^{-2j\theta}}{2e^{-j\theta}} = j Z_c \sin(\theta)$$

Finally, D can be found by

$$D = -\left.\frac{I_1}{I_2}\right|_{V_2=0} = -\frac{v_1^+/Z_c - v_1^-/Z_c}{v_2^+/Z_c - v_2^-/Z_c} = -\frac{v_1^+ + v_1^+ e^{-2j\theta}}{v_1^+ e^{-j\theta} + v_1^+ e^{-j\theta}} = \frac{1 + e^{-2j\theta}}{2e^{-j\theta}}$$

$$= \cos(\theta)$$

Collecting the results,

$$\underline{A} = \begin{bmatrix} \cos(\theta) & jZ_c \sin(\theta) \\ j\dfrac{\sin(\theta)}{Z_c} & \cos(\theta) \end{bmatrix}$$

This matrix is a useful tool in analyzing various kinds of transmission line networks. It is also useful in revealing some important transmission line behavior. We will consider three: the shorted stub, the open stub, and the quarter-wavelength transformer section.

A short-circuited stub, or shorted stub, is terminated at one port in a short circuit. To find the impedance at the other port, we apply the *ABCD* matrix. In this case, let $v_2 = 0$. Using the $\underline{A}$ matrix, we can find the voltage and current at port 1 and, thus, the impedance:

$$v_1 = Av_2 - Bi_2 = -Bi_2$$

$$i_1 = Cv_2 - Di_2 = -Di_2$$

$$Z_{1\mathrm{SC}} = \frac{v_1}{i_1} = \frac{B}{D} = \frac{jZ_c \sin(\theta)}{\cos(\theta)} = jZ_c \tan(\theta)$$

An open-circuited stub, or open stub, is terminated at one port in an open circuit. Now, $i_2 = 0$:

$$v_1 = Av_2 - Bi_2 = Av_2$$

$$i_1 = Cv_2 - Di_2 = Cv_2$$

$$Z_{1\mathrm{OC}} = \frac{v_1}{i_1} = \frac{A}{C} = \frac{\cos(\theta)}{j[\sin(\theta)/Z_c]} = -j\frac{Z_c}{\tan(\theta)}$$

Finally, we load port 2 in a general impedance Z_L:

$$v_2 = -Z_L i_2$$

$$v_1 = Av_2 - Bi_2 = -AZ_L i_2 - Bi_2$$

$$i_1 = Cv_2 - Di_2 = -CZ_L i_2 - Di_2$$

$$Z_1 = \frac{v_1}{i_1} = \frac{AZ_L + B}{CZ_L + D} = \frac{\cos(\theta)Z_L + jZ_c \sin(\theta)}{j[\sin(\theta)Z_L/Z_c] + \cos(\theta)} = Z_c \left[\frac{Z_L + jZ_c \tan(\theta)}{Z_c + jZ_L \tan(\theta)} \right]$$

Note that this more general form could have been used to derive both stub forms. Now, however, we focus on a special case: that for which $\theta = 90°$. Of course, $\tan(\theta)$ becomes infinite, so the impedance becomes

$$Z_1 = Z_c \frac{jZ_c \tan(\theta)}{jZ_L \tan(\theta)} = \frac{Z_c^2}{Z_L}$$

There are two features to note about this result. First, Z_1 is, except for a scale factor, the functional inverse of Z_L. This will be useful in making transmission line high-pass and bandpass filters. The transmission line will be pressed into service as either an impedance inverter or an admittance inverter, depending upon the type of resonator. Second, the impedance level can be controlled through the use of the impedance of

the line. This finds use in basic microwave circuit theory in matching two resistors of different levels to have good match. In the filters done later, however, this will serve to adjust impedance levels internally to the filter.

6.4.1 Semilumped Low-Pass Filters

Consider a single piece of transmission line with characteristic impedance Z_c and electrical length θ terminated at either end in 50 Ω. The *ABCD* parameters for this element can be derived as follows.

If we normalize the impedance and admittance terms of the *ABCD* matrix, it becomes

$$
A = \begin{bmatrix} \cos\theta & j\dfrac{Z_c}{Z_0}\sin\theta \\ j\dfrac{Z_0}{Z_c}\sin\theta & \cos\theta \end{bmatrix}
$$

Consider two limiting applications, each with the common condition that $\theta \ll \pi/8$. Figure 6.11a shows the first case, with $Z_c \gg Z_0$. This would correspond to a transmission line with a very thin center conductor. Then, $C \cong 0$. For a first approximation, $B \cong jZ_c/Z_0 = jX_L$. The *ABCD* matrix now becomes

$$
A = \begin{bmatrix} 1 & jX_L \\ 0 & 1 \end{bmatrix}
$$

This is identical to the *ABCD* matrix of a series element of reactance X_L. In fact, this appears to be a series inductor.

For the second case, consider the opposite condition of $Z_c \ll Z_0$. This corresponds to a transmission line with a very wide center conductor. Now, $B \cong 0$ and $C \cong jZ_0/Z_c = jB_C$. The *ABCD* matrix for this element is

$$
A = \begin{bmatrix} 1 & 0 \\ jB_C & 1 \end{bmatrix}
$$

This is the form of an *ABCD* matrix of a parallel inductor, indeed a parallel capacitor.
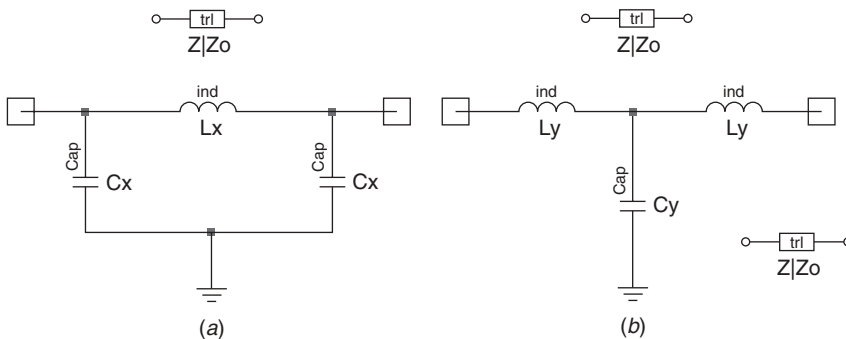
FIGURE 6.11   (*a*) Short high-impedance transmission line. (*b*) Short low-impedance transmission line.

The overall conclusion of this exercise is that short pieces of transmission lines can be used in place of lumped inductors and capacitors. Instead of having to purchase parts and have them soldered in place, we can etch a circuit pattern and get the same result. There is much truth to this conclusion, but there are some caveats and some work to do before we have a good design method.

The first thing to notice is that the supposedly vanishing term in each matrix above does not become zero. In fact, we could improve our model by including a little parallel C with each series L and a little series L with each parallel C. In fact, Figure 6.11 shows approximate models for these two cases. For the high-impedance line in Figure 6.11a, the main element is the inductor Lx with the capacitance being split into two capacitors of value Cx. The low-impedance line in Figure 6.11b follows the same pattern, with Cy being the main element and the inductance split into two inductors with value Ly.

The second thing to be concerned about is the assumption of "zero"-length transmission line segments. This turns out to be pretty good for a few cases, but most semilumped low-pass filters are a compromise in this area. Even more disturbing, the stopband of the semilumped filter breaks up when the electrical length becomes close to a quarter wavelength.

The first problem of the "parasitic" elements can actually be solved by absorbing them into the adjacent elements. This means that the adjacent elements must be reduced by the amount of the parasitic terms, but this is easy to do. In fact, usually one or two iterations will suffice to yield an accurate design. The second problem has no such simple adjustment and limits the extent of the stopband.

Example 6.2   Semilumped LPF   Specifications:

$$f_c = 2 \text{ GHz} \qquad N = 5 \qquad \text{Ripple} = 0.1 \text{ dB}$$
$$\text{Rejection} = 20 \text{ dB} \qquad \text{at 4 GHz}$$

From the transformed response, the rejection point will be $x = \frac{4}{2} = 2$, giving a rejection of 34.7 dB. This is more than enough, but, as we shall see, the extra margin will be helpful.

The g values for the filter are

$$g_1 = g_5 = 1.1468 \qquad g_2 = g_4 = 1.3712 \qquad g_3 = 1.9750$$

Scaling the element values to 50 Ω and 2 GHz, the lumped circuit would have element values

$$C_1 = C_5 = 1.825 \text{ pF} \qquad L_2 = L_4 = 5.456 \text{ nH} \qquad C_3 = 3.143 \text{ pF}$$

The next step is to choose impedance values for the low- and high-impedance sections. In general, one wants the most extreme values possible, since that will keep the line lengths short. In practice, the choices are limited by the medium in which the filter appears. For most microstrip configurations, 100 and 20 Ω are feasible, so we will choose these values. Note that the impedances can be varied from section to section, but the extremes are usually preferred.

The next step is to calculate the line length of each section to simulate the lumped values. One useful way to do this is to calculate the electrical length at the cutoff frequency. For the values at hand, the lengths are

$$\theta_1 = \theta_5 = 26.3° \qquad \theta_2 = \theta_4 = 39.3° \qquad \theta_3 = 45.3°$$

The third section is getting a bit long and will degrade the stopband performance. Calculating the parasitic terms,

$$L_1 = L_5 = 0.705 \text{ nH} \qquad C_2 = C_4 = 0.504 \text{ nH} \qquad L_3 = 1.131 \text{ nH}$$

Subtracting the parasitics from the nominal elements leads to a revised set of lengths:

$$\theta_1 = \theta_5 = 22.7° \qquad \theta_2 = \theta_4 = 32.7° \qquad \theta_3 = 38°$$

This has improved the lengths, especially of the third section. Figure 6.12 shows schematics for both the lumped and the semilumped circuits and their response. The
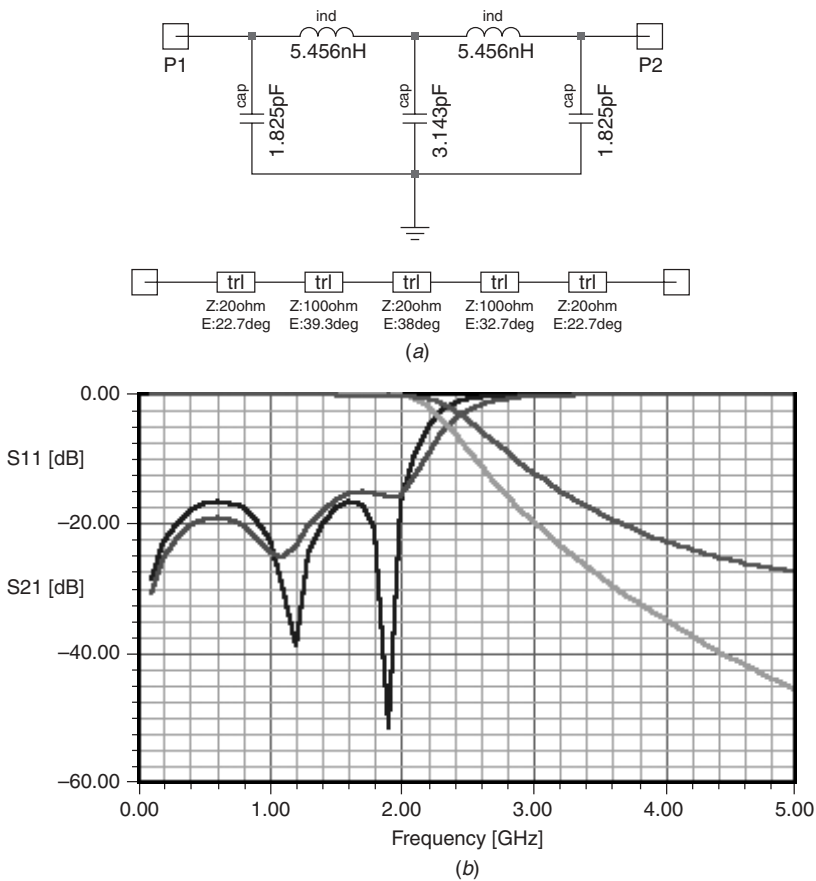
FIGURE 6.12   Semilumped low-pass filter: (*a*) example circuit; (*b*) response.

passband response is acceptable, although not perfect. The stopband is fine near the passband but degrades as the long sections approach a quarter wavelength. This type of circuit is a good candidate for optimization to improve both passband and stopband.

6.4.2 Richards Transformation

Most classical transmission line filters are designed on the basis of one of the fundamental properties of the transmission line. Consider a length of transmission line with characteristic impedance Z_t and electrical length θ short circuited at one end. The impedance at the input will be

$$Z_{\text{in}} = j Z_t \tan(\theta)$$

Define a new frequency variable, $\lambda = \Sigma + j\Omega = \tanh(sT)$, where $s = \sigma + j\omega$ is the standard complex-frequency variable and T is the time delay through the transmission line. Along the imaginary frequency axis, $\lambda = j\Omega = \tan(\theta)$. Now, we can express the impedance of the shorted stub in the new frequency variable,

$$Z_{\text{in}} = j\Omega Z_t$$

In this new frequency variable, the shorted stub takes on the appearance of an inductor. By a similar process, an open-circuited stub is a capacitor. The transformation used to establish λ is known as the Richards transformation, after its author [6.6]. The new complex-frequency variable, λ, is often known as the Richards variable. Circuits designed to take advantage of this analogy consist of assemblages of shorted stubs (inductors), open stubs (capacitors), and cascaded transmission lines (unit elements) all having the same phase length. Formally, these are *commensurate transmission line networks* and form the basis of much transmission line theory.

Transmission Line Low-Pass Filters A very simple application of this process is to use the analogy and make low-pass filters using series shorted stubs and parallel open stubs. (There are some practical realization issues with this simple approach, which we shall resolve in the next section.) The following points of analogy will show how we transform lumped-element (LE) prototype filters into transmission line (TL) filters. Our starting point is the normalized prototype, with 1 rad/s cutoff frequency and 1 Ω source and load impedance.

1. Inductances in the LE circuit transfer to characteristic impedances of the shorted stub in the TL circuit.
2. Capacitances in the LE circuit become characteristic admittances of open stubs in the TL circuit.
3. TL filter behavior at dc will be the same as that in the LE circuit.
4. When the LE filter approaches infinite frequency, the TL filter approaches its infinite point, which occurs for $\theta = 90°$. (Note that this implies a repeating process as θ becomes greater that $90°$. In fact, this is theoretically an infinitely repeating characteristic.)

5. At first glance, the condition at cutoff seems simple: In the normalized filter, $x_c = 1$ implies $\theta = 45°$. However, it is more flexible to adjust the cutoff by scaling the prototype circuit as follows. Let f_c be the desired cutoff frequency, the edge of the passband. Then, calculate the desired cutoff in the Richards variable $\Omega_c = \tan(\pi f_c / 2 f_d)$, where f_d is the quarter-wavelength frequency. When calculating the transmission line impedances from the prototype, scale the circuit by Ω_c.

Example 6.3   Transmisson Line Low-Pass Filter   Specifications:

$$f_c = 2 \text{ GHz} \qquad f_d = 5 \text{ GHz} \qquad N = 3 \qquad \text{Ripple} = 0.1 \text{ dB}$$

We start with the prototype element values:

$$g_1 = g_3 = 1.0316 \qquad g_2 = 1.1474$$

The cutoff frequency scales as follows:

$$\Omega_c = \tan\left(\frac{f_c}{f_d}\frac{\pi}{2}\right) = 0.7265$$

If we choose the end elements to be inductors, their line impedances become

$$Z_1 = Z_0 \frac{g_1}{\Omega_c} = 70.99 \ \Omega = Z_3$$

The center stub has impedance

$$Z_2 = Z_0 \frac{1}{g_2 \Omega_c} = 31.66 \ \Omega$$

The lengths of the transmission lines can be determined from the phase length at cutoff. For example, a Teflon-filled coaxial line will have lengths

$$L_{\text{coax}} = \frac{c_o}{4 f_d} = 679 \text{ mil}$$

There is only one problem left: How to deal with a series shorted stub. Of course, pieces of coaxial line can be soldered in place to do this. However, this kind of realization is not very convenient in printed configurations. There is, however, a solution using one more theoretical piece, known as the Kuroda transform. Once we have put this in place, we will resume this example with a more realizable result.

Kuroda Transforms   Consider the two circuits shown in Figure 6.13. The first is a cascaded line (unit element, or UE) with characteristic impedance Z_1 followed by a series shorted stub with characteristic impedance L, represented by an inductor in the Richards variable λ. The *ABCD* matrix for this collection expressed in λ is

$$\frac{1}{\sqrt{1+\lambda^2}}\begin{bmatrix} 1 & \lambda Z_1 \\ \dfrac{\lambda}{Z_1} & 1 \end{bmatrix}\begin{bmatrix} 1 & \lambda L \\ 0 & 1 \end{bmatrix} = \frac{1}{\sqrt{1+\lambda^2}}\begin{bmatrix} 1 & \lambda(Z_1 + L) \\ \dfrac{\lambda}{Z_1} & 1 + \lambda^2 \dfrac{L}{Z_1} \end{bmatrix}$$
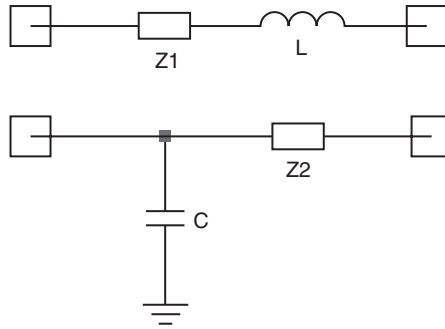
FIGURE 6.13   Circuits for Kuroda's transform.

The second circuit is a parallel open stub with characteristic admittance C, represented by a capacitor in λ, followed by a cascaded line with impedance Z_2. The overall $ABCD$ matrix will be

$$\begin{bmatrix} 1 & 0 \\ \lambda C & 1 \end{bmatrix} \frac{1}{\sqrt{1+\lambda^2}} \begin{bmatrix} 1 & \lambda Z_2 \\ \dfrac{\lambda}{Z_2} & 1 \end{bmatrix} = \frac{1}{\sqrt{1+\lambda^2}} \begin{bmatrix} 1 & \lambda Z_2 \\ \lambda\left(C+\dfrac{1}{Z_2}\right) & 1+\lambda^2 C Z_2 \end{bmatrix}$$

Note that each of the elements of the two matrices have the same functional form in the variable λ. Thus, if a noncontradictory set of relationships between corresponding elements of each matrix can be established, the two networks will have the same frequency response. Taking each term by its degree of λ, there are five relationships to be satisfied. Two of them are trivial $(1 = 1)$, and the remaining three are

$$C + \frac{1}{Z_2} = \frac{1}{Z_1} \qquad Z_2 = Z_1 + L \qquad \frac{L}{Z_1} = C Z_2$$

Since the goal from the previous section is to get rid of the problematic series shorted stub, let us restate these in terms of calculating C and Z_2 from L and Z_1:

$$Z_2 = Z_1 + L \qquad C = \frac{1}{Z_1} - \frac{1}{Z_2} = \frac{1}{Z_1} - \frac{1}{Z_1 + L} = \frac{L}{Z_1(Z_1 + L)}$$

Such circuit manipulations are known as Kuroda transforms or Kuroda identities after their originator [6.6]. There are actually many such transforms available for special purposes. We will see two more later in this section.

Now, let us apply this to the unfinished example of the previous section.

Example Revisited   The use of series stubs has two problems. The first, as we have noted, is that they can be inconvenient to realize, especially in some printed-circuit forms. The second is that the series and parallel stubs need to be connected to a common junction. This can have some problems for even two elements, but the situation becomes hopeless for $N > 2$. The Kuroda transform, however, gives a method to eliminate series
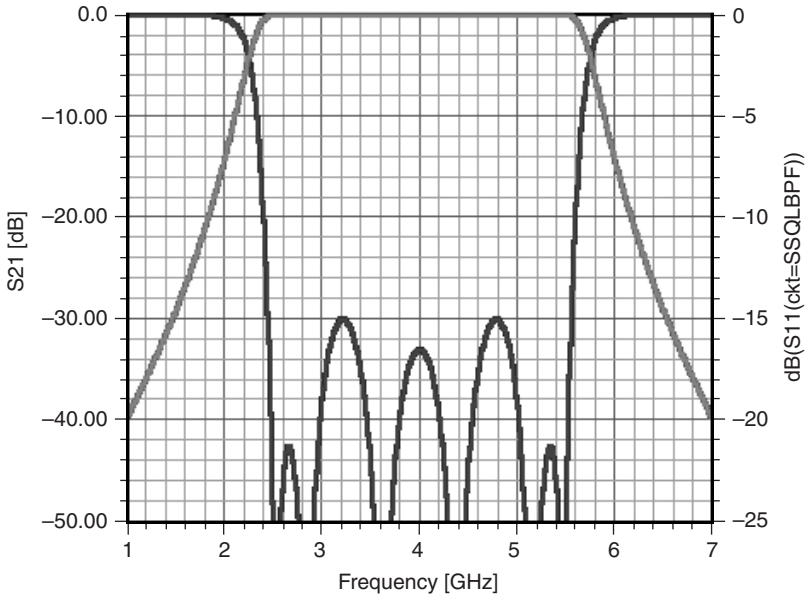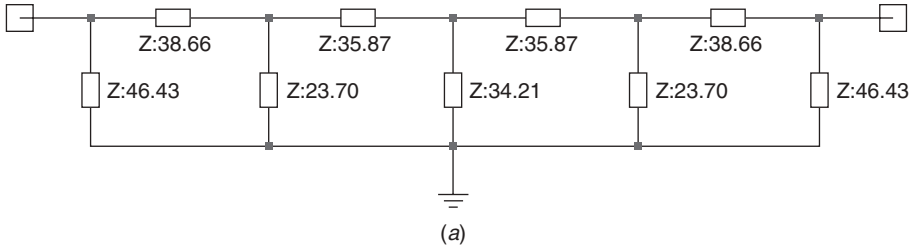
FIGURE 6.14 Stub bandpass filter: (*a*) schematic; (*b*) response.

stubs and separate the connections of stubs with a quarter-wavelength line. The scheme, as shown in Figure 6.14, proceeds as follows:

1. Insert a unit element between the source resistor and the filter with impedance equal to that of the source resistance. This will affect the phase of the response but not its amplitude response. Repeat at the load.
2. Use Kuroda's identity to transform the UE *L* structure into a UE *C* circuit.
3. For structures larger that $N = 3$, more transforms will be needed. In fact, there may be more than one possibility.

With a 50-Ω source and load, we insert a UE of $Z_0 = 50$ Ω. The new UE becomes

$$Z_1 + Z_0 = 70.99 + 50 = 120.99 \ \Omega$$

The parallel open stub on each end then becomes

$$\frac{Z_0(Z_1 + Z_0)}{Z_1} = \frac{50(70.99 + 50)}{50} = 85.22 \ \Omega$$

Transmission Line High-Pass Filters   As with lumped filters, it is possible to design transmission line filters using the transformation

$$\lambda = \frac{\Omega_c}{\tanh(sT)}$$

One can envision the same sort of circuit transformation as with lumped elements. Series shorted stubs become series open stubs and parallel open stubs become parallel shorted stubs. In fact, this can be done. However, it will be closer to practical design procedures to follow another approach.

Consider a two-section low-pass filter consisting of an open and a shorted stub. Suppose now that we wanted to have a filter with only parallel open stubs. One way to do that would be to place a quarter-wavelength transformer between the two stubs and replace the series shorted stub with a parallel open stub. Now we have two stubs of the same type separated by a transmission line, making realization much simpler. In addition, we have some freedom about the adjustment of impedance levels.

Now the transformation to a high-pass filter can be done as in the lumped-element design, using the frequency transformation above. Our parallel open stubs become parallel shorted stubs, which are similar in connection. Note the response of the filter, however. At zero frequency, there is perfect (infinite) attenuation. At $\theta = 90°$, the frequency variable becomes infinite, and the filter passes without attenuation. As frequency increases, the response repeats, and the attenuation again becomes infinite at $\theta = 180°$. To the user of this filter, it appears to have a passband flanked by two stopbands and could reasonably be called a bandpass filter. In fact, most microwave bandpass filters are really, from the network theory standpoint, high-pass filters. (An important exception to this is the comb-line filter, which we will discuss in the next section.)

At this point, we need to consider what should appear to be a glaring problem. The approach used here assumes a perfect admittance inverter, but the quarter-wavelength transformer is such only at one frequency. The first set of high-pass (bandpass) designs will assume narrow bandwidth. They are generally good for 10 to 15% bandwidths. The second set will include an adjustment at the band edge, giving good approximate designs for large bandwidths. Finally, in Section 6.5, we will suggest some paths to pursue to make exact designs for any bandwidth.

The details of these designs are complicated and beyond the intent of this brief introduction to filter design. Many of the details are available in the literature, especially in Refs. 6.1 and 6.11. We will adopt a pragmatic approach here, realizing that the following things are being done:

1. Our starting point is the low-pass prototype network.
2. The low-pass design is transformed to a high-pass one using narrow-band and corrected narrow-band transforms.
3. Impedance scaling is applied, and, in most cases, impedance levels are adjustable within a range internal to the filters. A parameter to adjust these levels to make resonators more realizable is often provided.
4. Frequency responses can be estimated prior to design using frequency transformations consistent with the network transformations. The traditional approximate

transformations are presented along with more accurate transformations using the Richards variable.

Before proceeding with the designs themselves, a few common terms will be defined.

f_1 Lower edge of the passband
f_2 Upper edge of the passband
BW   Bandwidth: $\text{BW} = f_2 - f_1$.
f_0 Center frequency: $f_0 = (f_2 + f_1)/2$
w Fractional bandwidth: $w = (f_2 - f_1)/f_0 = \text{BW}/f_0; \theta_1 = (\pi/2)(1 - w/2)$

Shorted-Stub Bandpass Filters   This design is practical for fractional bandwidths from 40 to 70%. First, the admittance inverter values are calculated. Initially, a parameter d is defined which can be used to modify impedance levels internal to the filter. A default is $d = 1.0$. If values for a particular design are not satisfactory, it is useful to build a spreadsheet or program to watch the variation of impedances as d is varied. The source and load impedances are taken to be Y_0. (It is usually satisfactory to start with $Y_0 = 1$ and scale impedances at the end. The examples will be done in this manner using a MathCAD spreadsheet to display the results.) The calculations proceed as follows. First, calculate

$$\theta_1 = \frac{\pi}{2}\left(1 - \frac{w}{2}\right)$$

Then,

$$C_a = 2dg_1$$

$$\frac{J_{12}}{Y_0} = g_0\sqrt{\frac{C_a}{g_2}}$$

$$\frac{J_{n-1,n}}{Y_0} = g_0\sqrt{\frac{C_a g_{n+1}}{g_0 g_{n-1}}}$$

$$\left.\frac{J_{k,k+1}}{Y_0}\right|_{k=2,\dots,n-2} = \frac{g_0 C_a}{\sqrt{g_k g_{k+1}}}$$

A set of intermediate variables are defined,

$$N_{k,k+1}|_{k=1,\dots,n-1} = \sqrt{\left(\frac{J_{k,k+1}}{Y_0}\right)^2 + \left(\frac{g_0 C_a \tan(\theta_1)}{2}\right)^2}$$

Then, the stub characteristic admittances are

$$\frac{Y_1}{Y_0} = g_0(1-d)g_1 \tan(\theta_1) + \left(N_{12} - \frac{J_{12}}{Y_0}\right)$$

$$\frac{Y_n}{Y_0} = (g_n g_{n+1} - dg_0 g_1)\tan(\theta_1) + \left(N_{n-1,n} - \frac{J_{n-1,n}}{Y_0}\right)$$

$$\left.\frac{Y_k}{Y_0}\right|_{k=2,\dots,n-1} = \left(N_{k-1,k} + N_{k,k+1} - \frac{J_{k-1,k}}{Y_0} - \frac{J_{k,k+1}}{Y_0}\right)$$

The lines connecting the stubs have characteristic admittances equal to those of the admittance inverters:

$$\left.\frac{Y_{k,k+1}}{Y_0}\right|_{k=1,\dots,n-1} = \frac{J_{k,k+1}}{Y_0}$$

All stubs and lines are a quarter-wavelength long at the midband frequency f_0. For truly TEM media (coaxial lines, stripline), all lengths are the same. For non-TEM media (microstrip), line length will depend on impedance. For example:

$n = 6$
0.1 dB ripple

Parallel-Coupled-Line Bandpass Filters   A very useful design is the use of parallel-coupled line sections. (See Figure 6.15.) The design procedure will be similar to

(a)

(b)
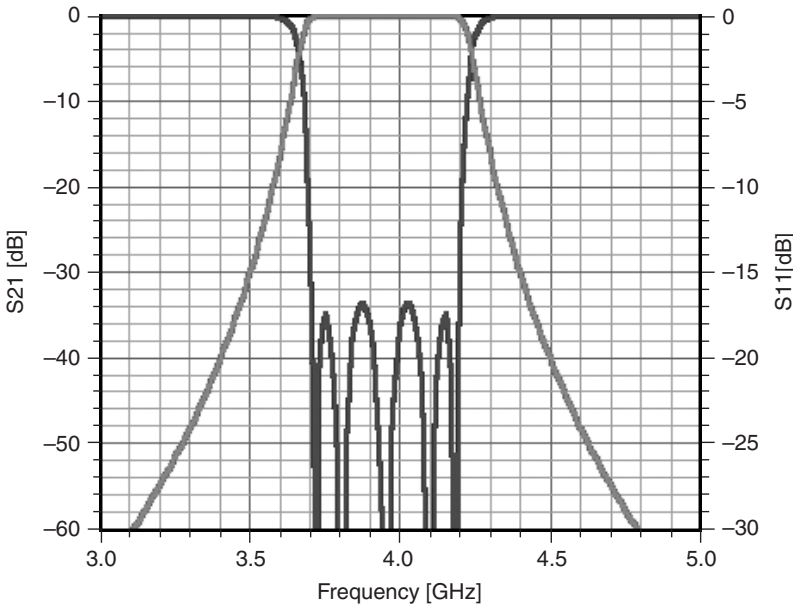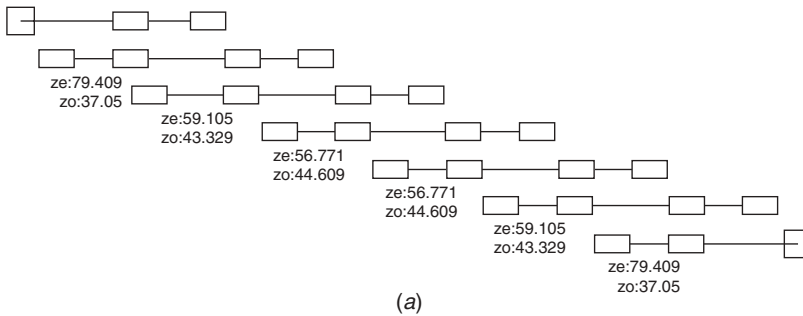
FIGURE 6.15   Coupled-line bandpass filter: (a) example circuit; (b) response.

the shorted stubs, but the results of the calculations are the even- and odd-mode impedances. An additional step of converting these impedances into dimensions is dependent on the medium and will be left to the designer. It is usually convenient to rely on one of the large number of excellent software tools available for this purpose. Many simulators come with a utility for this purpose.

The starting point (assuming the fractional bandwidth and g values are known) is the admittance inverters:

$$\frac{J_{01}}{Y_0} = \sqrt{\frac{\pi w}{2 g_0 g_1}}$$

$$\frac{J_{n,n+1}}{Y_0} = \sqrt{\frac{\pi w}{2 g_n g_{n+1}}}$$

$$\left. \frac{J_{k,k+1}}{Y_0} \right|_{k=1,\ldots,n-1} = \frac{\pi w}{2} \frac{1}{\sqrt{g_k g_{k+1}}}$$

There are $n + 1$ sections, from o to n, with even- and odd-mode impedances:

$$\left. \frac{Z_0 e_{k,k+1}}{Z_0} \right|_k = \left[1 + \frac{J_{k,k+1}}{Y_0} + \left(\frac{J_{k,k+1}}{Y_0} \right)^2 \right]$$

$$\left. \frac{Z_0 o_{k,k+1}}{Z_0} \right|_k = \left[1 - \frac{J_{k,k+1}}{Y_0} + \left(\frac{J_{k,k+1}}{Y_0} \right)^2 \right]$$

where $Z_0 = 1/Y_0$. For example:

> It contains a good set of operations with transmission line filters, including the major standard design realizations, and is one of the first of a new generation of true synthesis programs for filters useful in microwave systems. It ranges from lumped to transmission line designs and has a large set of circuit manipulation capabilities.

Although the filter synthesis programs have improved remarkably in recent years, some caution is recommended. One really needs to know the basic principles of circuit synthesis and, in particular transmission line synthesis, to use the software. There are some excellent university programs that provide this, but they are not universal.

Finally, a word about optimization is in order. It is pretty well established now that optimization programs are not suitable for design. On the other hand, even a perfectly worked-out design process must confront the realities of element parasitics and approximate realizations of theoretically perfect filters. (A good example of this is the comb-line filter, which is usually used with a lumped tuning capacitor instead of the exact design with an open stub.) Further, when filters are connected in multiplexer configurations, there is degradation in the pure filter response. For things such as this, optimizers are essential tools.

6.5   EXACT DESIGNS AND CAD TOOLS

Although the designs presented here are suitable for all but the most exacting purposes, there are times when an exact design is desirable. The process of building transfer functions to realize a particular filter topology is known as *synthesis*. There is a remaining process, that of determining the actual element values for the topology being designed. Technically, that is known as *extraction* or *element extraction*, although it is often lumped with the transfer function design under the heading of "synthesis." The drawback to this is a complicated mathematical procedure, including the need to pay careful attention to errors which can crop up, especially in larger filters. The payoff can be more accurate designs and, in some cases, topologies which are novel and particularly suited to a certain application.

The exact design of lumped-element filters is covered in a number of books on synthesis going back to the 1960s. A classic book with a lot of information and extensive tables is the book by Zverev [6.2]. A more recent text, for example, is the one by Temes and LaPatra [6.6]. Many others abound. A book which leads into broadband matching is the venerable but still viable book by W. K. Chen [6.7].

The sources of information for synthesis of transmission line filters is a bit more diffuse. An excellent starting point is a pair of articles by H. J. Carlin [6.8, 6.9] and the text by Carlin and Civalleri [6.10], which also goes into the important area of matching networks. There are a number of texts which have treated the topic and gone out of print, for example Malherbe [6.11] and Baher [6.12].

This process is complicated enough that most people doing exact design will need to use some kind of software. There are three basic levels of such software:

1. Computer programs written is some language capable of dealing with high accuracy and the mathematical operations used in filter synthesis. This is a lot of work and is useful only in the cases for which a specially tailored design tool is needed.
2. Programs such as MATLAB, MathCAD, and Mathematica can be used effectually to do much of the heavy lifting. Polynomial operations are particularly helpful. One is still left, however, with a lot of work organizing the procedures. This approach is helpful in cases for which a limited scope of designs is needed.
3. Commercial synthesis software is a viable alternative to writing one's own code. New synthesis programs are appearing with much flexibility for circuit manipulation. Some examples are:
   - S/Filsyn [6.13–6.15] is a general-purpose program that will design exact filters for cases ranging from lumped element through digital and including active cases. If more than just transmission line filters are needed, this is a tool with broad capability.

6.6   REAL-LIFE FILTERS

The purpose of this chapter has been to spell out practical design procedures for filters of various kinds. In closing, a brief discussion of the kinds of elements used to make physical filters is presented. A very interesting new medium is sketched in slightly more detail to suggest directions for modern filter design.

6.6.1 Lumped Elements

The ideal inductors and capacitors shown in the sections on lumped-element filter design can be realized by high-quality chip inductors and capacitors in microwave circuits at lower frequencies. Capacitors of increasingly small size can be used up to 10 to 15 GHz, depending on the design and the medium of realization. Inductors usually become problematic at somewhat lower frequencies. In any case, it is always a good rule to minimize the number of inductors in a filter design. For both components, the chief enemies are element Q (quality factor due to losses) and resonant frequencies. Vendor data specifications include the resonant frequency, and it is usually best to stay below the lowest point of resonance.

As was intimated in Section 6.4.1, transmission lines can be used as lumped elements. It is often possible to use simple lumped models for design, but most situations require taking the transmission line properties into account.

6.6.2 Transmission Line Elements

Transmission line elements can be realized in coaxial, waveguide, stripline, microstrip, slotline, and numerous other structures. A number of current books treat specific realizations, but Ref. 6.1 gives a good starting point for the first three media.

6.6.3 Cavity Resonators

A major workhorse for very selective filters and diplexers has been the coaxial cavity. These are realized by making fairly large cavities in blocks of metal (usually, but not exclusively, aluminum) and coupling them to form coupled-resonator bandpass filters. These filters can be highly selective and are used in many cellular base-station applications, usually as diplexers.

A variation on the cavity is the use of ceramic dielectric resonators. The materials used have dielectric constants ranging from 20 to 100 and can have intrinsic quality factors of 10,000 to 30,000. The materials are usually shaped into cylinders to form a cavity. The high dielectric constant means that fields will reside mostly in the cylinders, making the surrounding structure of less effect on performance. They are used in a manner similar to the cavities discussed above, being coupled together to form very selective narrow-band filters.

6.6.4 Coaxial Dielectric Resonators

The materials used in dielectric resonators can be shaped into rectangular elements with a conducting center to form a modestly high quality (100 to 300) resonator. These have found applications in portable electronic devices, such as pagers and cell phones. They are coupled together using a lumped element or other coupling structures to form narrow-band bandpass filters. They can be relatively small and light.

6.6.5 Thin-Film Bulk-Wave Acoustic Resonator (FBAR)

An interesting, relatively new technology is the subject of the last form of realization developed by Agilent Technologies in the early 1990s [6.15]. The process consists of making resonators from a thin silicon film. Figure 6.16 shows a sketch of the physical

Physical Representation   Electrical Analog

Thin Film Bulk-Wave
Acoustic Resonator

FBAR   One Port Resonator
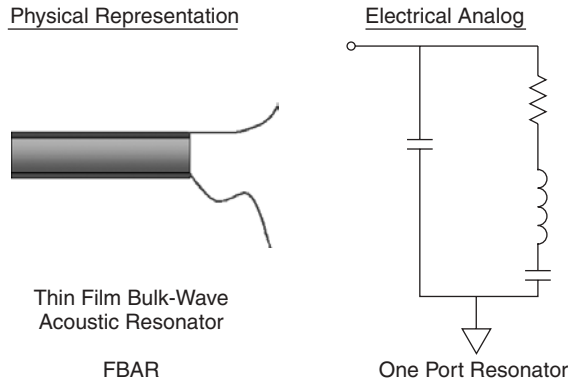
FIGURE 6.16 FBAR basics.
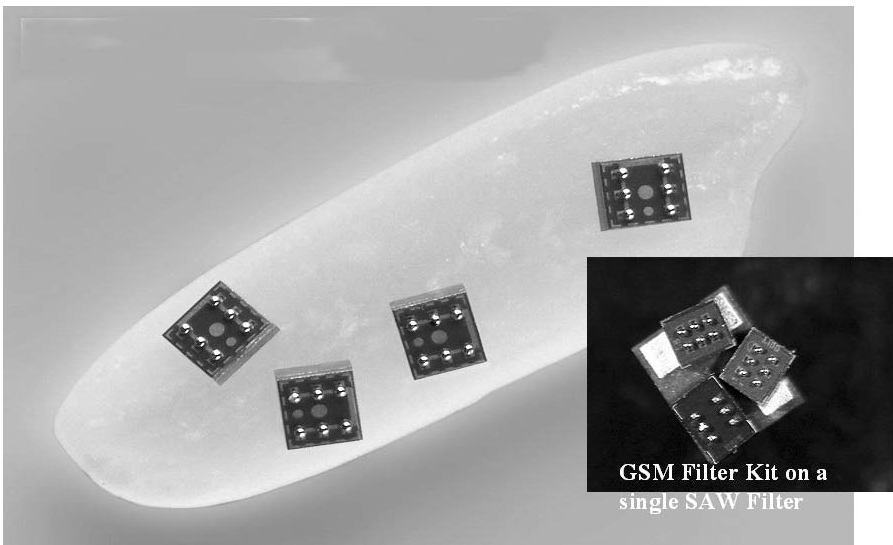
FIGURE 6.17 Size comparison of FBAR filters.

realization and a starting equivalent circuit. The circuit consists of a more complicated model than the traditional *LC* resonator, but the design approach is similar. Using a set of these resonators coupled together, filters can be built which are extremely small in size. Figure 6.17 shows four FBAR filters on a grain of rice which is about 6 to 7 mm in length. However, the startling result is in the resonator performance, shown in Figure 6.18. Note the resonator *Q*'s of 2500.

For comparison, dielectric resonators (DRs) are as much as an order of magnitude more, but a DR is around an inch in diameter, depending on the material involved. Lumped elements and transmission line elements have *Q* values that range from tens to 100 or 200, as do coaxial dielectric resonators. This technology, currently in volume production (30 million per year), shows much promise for efficient filtering in hand-held electronic devices.

Qs ~ 2500
Qp ~ 2500
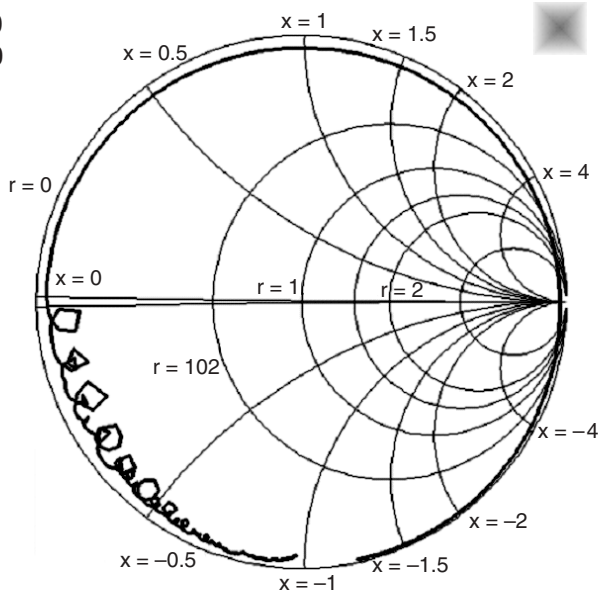
FIGURE 6.18   FBAR performance.

40 Units of the latest Tx FullBand Filter
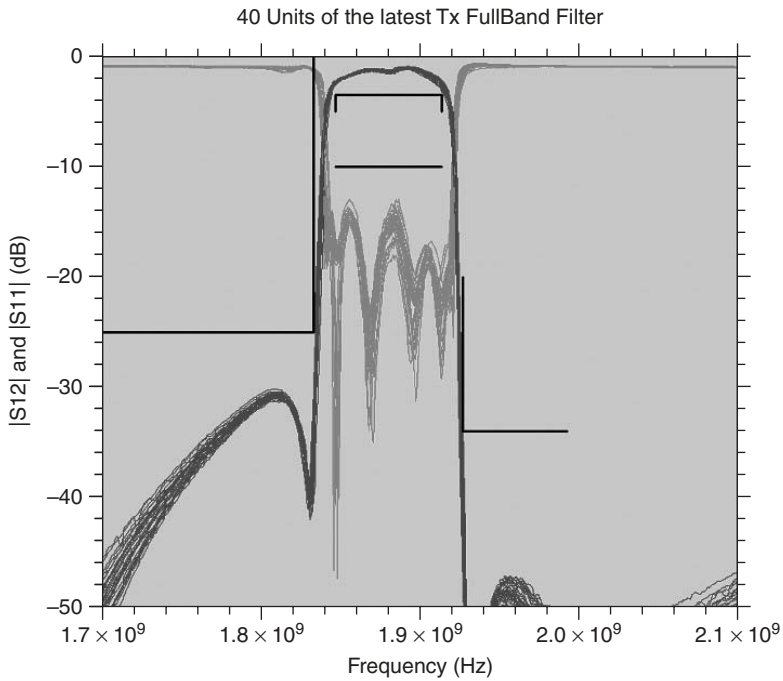
FIGURE 6.19   Performance of 1.88 GHz FBAR filter.

The proof of the filter is in the final performance. Figure 6.19 shows the response of a transmit filter in one of the cellular bands. The filter consists of four sections and a pair of finite transmission zeros. (That topic will be discussed briefly in the next paragraph.) Note the steep slope going from the passband with a nominal loss of about 1.5 dB down to a rejection of over 30 dB in a few megahertz.

Finally a parenthetical word about finite transmission zeros. The filter designs given in this book all have zeros of transmission (frequencies at which S_{21} goes to zero) at either dc or infinite frequency. (Infinite frequency for commensurate transmission line filters is actually at odd multiples of the quarter-wavelength frequency.) When more rejection is needed, there are two choices. The simplest is to increase the number of sections of the filter. However, this has a cost in terms of fabrication and can actually be a less than helpful trade-off when loss effects are considered. The second choice is to introduce zeros of transmission at critical frequencies. In the FBAR filter above, sharp drops just above and just below the passband show the presence of finite zeros. How this is achieved and the design are beyond the scope of this chapter.

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PROBLEMS

6.1 Design a lumped low-pass filter with the following specifications: cutoff frequency = 3 GHz, Chebyshev response with ripple = 0.05 dB, rejection at 6 GHz = 50 dB, source and load impedance = 50 Ω.

    (a) Determine the minimum number of elements to achieve the specified rejection.

    (b) Calculate the inductor and capacitor values for the specified cutoff and impedance. If there is a choice, minimize the number of inductors.

6.2 Design a lumped bandpass filter with the following specifications: passband = 824 to 849 MHz, Chebyshev response with return loss = 20 dB, rejection = 60 dB from 869 to 894 MHz, source and load impedance = 50 Ω.

    (a) Determine the minimum number of elements to achieve the specified rejection.

    (b) Using capacitive coupling, design a narrow-band coupled-resonator circuit.

    (c) Estimate the passband insertion loss and the time delay at band center.

6.3 Design a lumped-element high-pass filter with the following specifications: cutoff frequency = 10 GHz, rejection = 50 dB minimum at 2 GHz, Ripple = 0.1 dB.

6.4 Design a lumped-element band-stop filter to notch out the band from 1 to 2 GHz: $N = 5$, Ripple = 0.5 dB.

6.5 Design a semilumped low-pass filter using transmission line elements to meet the same requirements as the filter in problem 6.1. Use 100 and 20 Ω, respectively, for the high and low impedances.

6.6 Design a transmission line stub low-pass filter for the same requirements as problem 6.1. Use a quarter-wavelength frequency to keep impedances between 20 and 100 Ω.

6.7 Design a transmission line stub high-pass (bandpass) filter to pass 1 to 2 GHz. Use five sections and 0.1 dB ripple.

6.8 Design a transmission line coupled-line bandpass filter from 3.7 to 4.2 GHz. Determine the number of sections to give 30 dB rejection at 5.9 GHz. Find the even- and odd-mode impedances for the coupled lines.

CHAPTER 7

NOISE IN LINEAR TWO-PORTS

7.1 INTRODUCTION

In Chapters 4 and 5 we learned that a linear two-port requires four complex *S* parameters to describe the gain. In this chapter we find that four additional parameters are required to describe the noise; many equivalent representations are described.

Even when a two-port is linear, the output waveform may differ from the input, because of the failure to transmit all spectral components with equal gain (or attenuation) and delay. By careful design of the two-port or by limitation of the bandwidth of the input waveform, such distortions can largely be avoided. However, noise generated within the two-port can still change the waveform of the output signal. In a linear passive two-port, noise arises only from the losses in the two-port; thermodynamic considerations indicate that such losses result in the random changes that we call noise. When the two-port contains active devices, such as transistors, there are other noise mechanisms that are present. A very important consideration in a system is the amount of noise that it adds to the transmitted signal. This is often judged by the ratio of the output signal power to the output noise power (*S/N*). The ratio of signal plus noise power to noise power [(*S* + *N*)/*N*] is generally easier to measure and approaches *S/N* when the signal is large.

In the evaluation of a two-port it is important to know the amount of noise added to a signal passing through it. An important parameter for expressing this characteristic is the noise factor. The signal energy coming from a generator or antenna is amplified or attenuated in passing from the input to the output of a two-port, as is the noise that accompanies the input signal energy. A system generally includes a cascade of two-port networks which constitute one overall two-port which amplifies the signal to a high-enough power level for its intended use. The noise factor of a system is defined

as the ratio of signal-to-noise ratios available at input and output:

$$F = \frac{(S/N)_{\text{input}}}{(S/N)_{\text{output}}} \geq 1 \tag{7.1}$$

The noise figure (or factor) of a receiver is an easily measured quantity that describes the signal-to-noise ratio reduction of that receiver.

When this ratio of powers is converted to decibels, it is generally referred to as the noise figure rather than the noise factor. Various conventions are used to distinguish the symbols used for noise factor and noise symbol. Here we use F to represent the noise factor and NF to represent the noise figure, although the terms are usually used interchangeably.

For an amplifier with the power gain G, the noise factor can be rearranged as

$$F = \frac{S_i/N_i}{GS_i/G(N_i + N_a)} \tag{7.2}$$

where N_a is the additional noise power added by the amplifier referred to the input. This can be computed to be

$$F = 1 + \frac{N_a}{N_i} \tag{7.3}$$

The noise factor is often replaced by the noise figure (NF), which is defined in decibels as

$$\text{NF} = 10 \log_{10} F \tag{7.4}$$

In applications such as satellite receivers the noise factor becomes such a small number that it is inconvenient to work with. Many people have adopted the use of an equivalent noise temperature for a circuit to remedy this situation. Since the thermal noise power available from a resistor at temperature T_e is

$$N = kT_e B \tag{7.5}$$

where k is Boltzmann's constant (1.38×10^{-23} J/K), T_e is the effective temperature in kelvin, and B is the bandwidth in hertz. The equation above may be used to associate an effective noise temperature with circuits containing more than just thermal noise sources. This allows (7.3) to be written as

$$F = 1 + \frac{kT_e B}{kT_0 B} = 1 + \frac{T_e}{T_0} \tag{7.6}$$

where T_e is the effective noise temperature of the circuit and T_0 is the temperature of the generator resistor in kelvin. The noise temperature T_e now characterizes our circuit noise contribution and can be directly related to the noise factor.

Assuming a reference noise temperature of 290 K ($-273 + 290 = 17°C$), let us determine the noise temperature of the system with a noise factor of 2.6 (4.15 dB):

$$T_e = (2.6 - 1)(290) = 464 \text{ K}$$

This temperature T_e should not be confused with the environmental operating temperature T_0. It is quite common to operate low-noise amplifiers with T_e below 100 K at an ambient temperature of 290 K.

7.2 SIGNAL-TO-NOISE RATIO

Let us consider the signal-to-noise ratio of power delivered from a generator to a load as shown in Figure 7.1. The signal power delivered to the input is given by

$$S_{\text{in}} = P_{\text{in}} = \frac{E_g^2 \, \text{Re}(Z_{\text{in}})}{|Z_g + Z_{\text{in}}|^2} \tag{7.7}$$

where E_g is the rms voltage of the input signal supplied to the system and the noise power supplied to the input is expressed by

$$N_{\text{in}} = \frac{\overline{v_n^2} \, \text{Re}(Z_{\text{in}})}{|Z_g + Z_{\text{in}}|^2} \tag{7.8}$$

where the noise power at the input is provided by the noise energy of the real part of Z_g. The input impedance Z of the system in the form $Z = R_{\text{in}} + jX_{\text{in}}$ is assumed to be complex.

The Johnson noise of a resistor [here $\text{Re}(Z_g)$] is given by the mean-square voltage

$$\overline{v_n^2} = 4kTRB \tag{7.9}$$

with Boltzmann's constant $k = 1.38 \times 10^{-23}$ J/K, T is the absolute temperature of the resistor, and the bandwidth B is sufficiently small that the resistive component of impedance does not change. The available signal power from the generator has a lower limit, even if the signal is attenuated by the highest possible attenuation. The generator resistor acts as a Johnson noise generator, its power being

$$P_A = \frac{4kTRB}{4R} = kTB \tag{7.10}$$
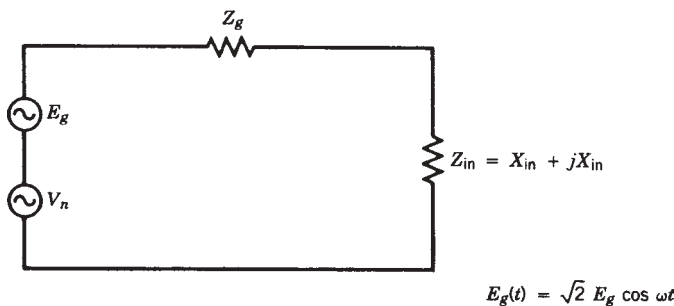
FIGURE 7.1 Combination of signal and noise voltages supplied to a complex termination.

with k the Boltzmann constant, T the absolute temperature, and B the bandwidth. This power is the maximum available output power.

For an ambient temperature of 290 K, $kT = 4 \times 10^{-21}$ W/Hz. This expression is also given as $kT = -204$ dBW/Hz $= -174$ dBm/Hz $= -114$ dBm/MHz. We can combine (7.7) to (7.9) to obtain

$$\left(\frac{S}{N}\right)_{\text{in}} = \frac{E_g^2}{4kT \ \text{Re}(Z_g)B} \tag{7.11}$$

This is the value of S/N contributed by the generator, which does not include the noise generated by the load, in this case $\text{Re}(Z_{\text{in}})$, which would need to be included in the measurement of the total S/N across the input impedance.

A critical parameter is the noise bandwidth B_n, which is defined as the equivalent bandwidth, as shown in Figure 7.2. For reasons of group delay correction, most practical filters have round rather than sharp corners. The noise figure measurements shown later can be used to determine the "integrated" bandwidth, which is B_n.

An active system such as a combination of amplifiers and mixers will add noise to the input signals, and the noise factor that describes this is defined as the S/N ratio at the input to the S/N ratio at the output, which is always greater than unity [7.1]. In practice, a certain minimum signal-to-noise ratio is required for operation. For example, in a communication system such a minimum is required for intelligible transmission, either voice or data. For high-performance TV reception, to provide a noise-free picture to the eye, a typical requirement is for a 60-dB S/N. In the case of a TV system, a
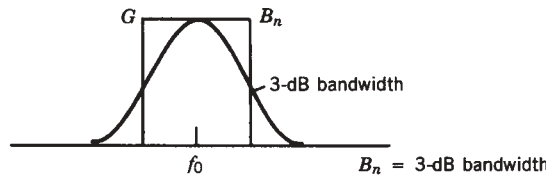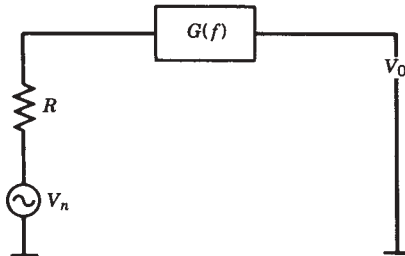
FIGURE 7.2   Graphical and mathematical explanation of the noise bandwidth from a comparison of the Gaussian-shaped bandwidth to the rectangular filter response.

large dynamic range is required as well as a very large bandwidth to reproduce all colors truthfully and all shades from high-intensity white to black. Good systems will have 8 MHz bandwidth or more.

7.3   NOISE FIGURE MEASUREMENTS

Some of the noise equations are based on mathematical models and physics. To understand some of these expressions, it is useful to look at a practical case of a system with amplifiers which is to be evaluated.

Let us look at Figure 7.3, which consists of a signal generator, the system or device under test (DUT), and a selective receiver with a build-in root-mean-square (rms) voltmeter to determine the signal and the noise voltage. It is necessary that the system have enough gain so that the noise voltage supplied by the generator will be indicated [7.2].

If we assume that our selective receiver is a video noise meter calibrated in rms voltage levels, we can perform two measurements. With an input termination connected to the TV system (typically, 75 Ω for cable TV, 50 Ω for satellite TV), the noise receiver/meter will read a value for proper termination which can easily be calculated. Since one-half of the mean-square noise voltage appears across the input,

$$v_{\text{in}} = \frac{v_n}{2} = \frac{\sqrt{4kTRB}}{2} \tag{7.12}$$

With $B = 10$ MHz, $T = 290$ K (T is always expressed in absolute temperature; $T_0 = -273°$C), and $k = 1.38 \times 10^{-23}$ J/K, for $R = 75$ Ω,

$$v_{\text{in}} = \frac{v_n}{2} = 1.73 \ \mu\text{V} \tag{7.13}$$

where the rms noise voltage has been referred to the input port. We can verify this with our first measurement.

Now we increase the input voltage of the signal generator to a value that indicates a 60-dB S/N ratio at the output port. This should be about

$$E_g = \frac{v_n}{2} \sqrt{F} \times 1000 = 1.73\sqrt{F} \qquad \text{mV}$$
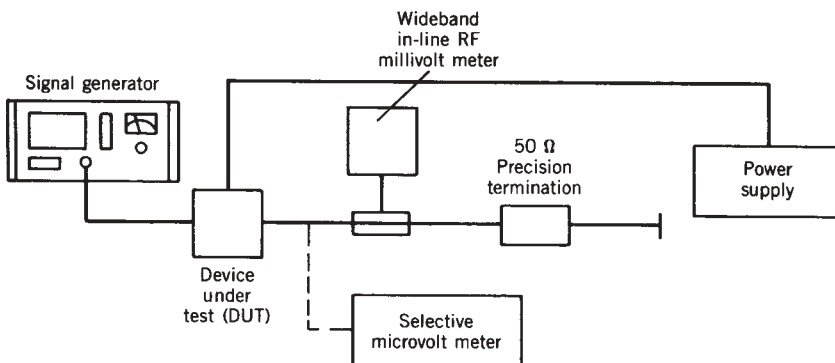
FIGURE 7.3   Test setup to measure signal-to-noise ratio.

where F is the noise factor of the receiver. For a receiver noise factor of 10 we would obtain $E_g = 5.48$ mV (rms value). If the noise energy equivalent to a noise factor of F is assumed, we need $\sqrt{F}$ times more voltage. For a 60-dB ratio, this means that $E_g = 1000 \times (v_n/2) \times \sqrt{F}$.

As they are done here, over a power range of 60 dB, the measurements can be performed over such a wide range only if special equipment is available. In cases where the internal detector of a piece of communications equipment is used, the signal-to-noise ratio measurements are performed over much smaller power ranges.

Let us assume that for the above-mentioned case ($F = 10$) we find a S/N ratio of 10 dB at the output for an input signal of 5.47 μV. By rewriting (7.6) as

$$E_g = \frac{v_n}{2}\sqrt{F} = \sqrt{kTRBF} \tag{7.14}$$

with F being the noise factor, we can solve for F with

$$F = \frac{P_s}{P_n} = \frac{E_g^2/R}{kTB} \tag{7.15}$$

While the input power from the thermal energy of the input termination resistor was $kTB = 4 \times 10^{-14}$ W, the input power required for the 10-dB S/N ratio was

$$P_s = \frac{(5.47 \times 10^{-6})^2}{75} = 3.98 \times 10^{-13} \text{ W} \tag{7.16}$$

The noise factor is defined as the ratio P_s/P_n:

$$F = \frac{3.98 \times 10^{-13}}{4 \times 10^{-14}} = 10 \tag{7.17}$$

which is the proof.

This method is used more frequently at the 3-dB point, or double the input power if the dynamic range of the detector is small or only a linear indicator is available. Because of hum and other pickup, this is not an easy measurement. Using a signal generator is very expensive because in a laboratory or production environment a wide frequency range requires several generators.

Another method is the use of a wide-band noise generator. Modern gas discharge diodes or avalanche diodes are available which provide essentially white-noise energy over a large frequency range. These microwave diodes typically have an output of 30 dB above kT when switched on and kT when switched off. To provide good matching at microwave frequencies, a 15-dB attenuator is cascaded. This means that the noise power of the source in the on condition is about 15 dB above kT.

In the early 1960s, low-cost noise figure test equipment was built around vacuum diodes whose operating range was limited to 1200 MHz due to the resonate effects of the structure. The automatic noise gain analyzer offered currently by Hewlett-Packard and Eaton/AIL uses calibrated solid-state noise sources up to 26.5 GHz. It appears that the upper frequency limit has to do with matching and the lower frequency limit with $1/f$ noise.

7.4 NOISE PARAMETERS AND NOISE CORRELATION MATRIX

The noise correlation matrices form a general technique for calculating noise in n-port networks. This method is useful because it forms a base from which we can rigorously calculate the noise of linear two-ports combined in arbitrary ways. For many representations, the method of combining the noise parameters is as simple as that for combining the circuit element matrices.

A linear, noisy two-port can be modeled as a noise-free two-port with two additional noise sources as shown in Figures 7.4a and 7.4b. The matrix representation is

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} i_{n1} \\ i_{n2} \end{bmatrix} \tag{7.18}$$

where i_{n1} and i_{n2} are noise sources at the input and output ports of admittance form.

Since i_{n1} and i_{n2} (noise vectors) are random variables, is convenient to work with the noise correlation matrix because the correlation matrix gives a deterministic number to calculate. The above two-port example can be extended to n-ports in a straightforward way, as a matrix chain representation.

7.4.1 Correlation Matrix

The correlation matrix is defined as the mean value of the outer product of the noise vector, which is equivalent to multiplying the noise vector by its adjoint (complex conjugate transpose; identical to Hermitian matrix) and averaging the result.

Consider the Y-parameter noise correlation matrix $[C_y]$; it can be given as [7.22]

$$\langle \bar{i}\,\bar{i}^+ \rangle = \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \begin{bmatrix} i_1^* & i_2^* \end{bmatrix} = \begin{bmatrix} \langle i_1 \ i_1^* \rangle & \langle i_1 \ i_2^* \rangle \\ \langle i_1^* \ i_2 \rangle & \langle i_2 \ i_2^* \rangle \end{bmatrix} = [C_y] \tag{7.19}$$

The diagonal term represents the power spectrum of each noise source and the off-diagonal terms are the cross-power spectrum of the noise source. Angular brackets denote the average value.
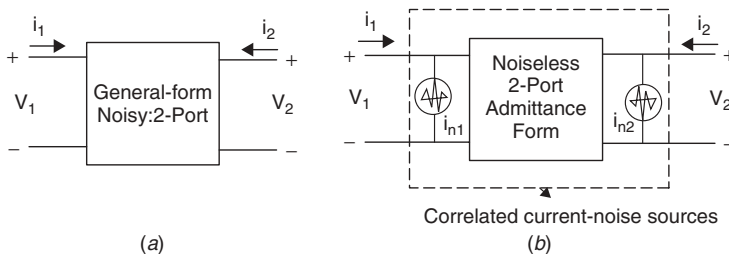
FIGURE 7.4 General form of noise two-port: (a) noisy two-port; (b) noiseless two-port with two noise current sources at input and output.
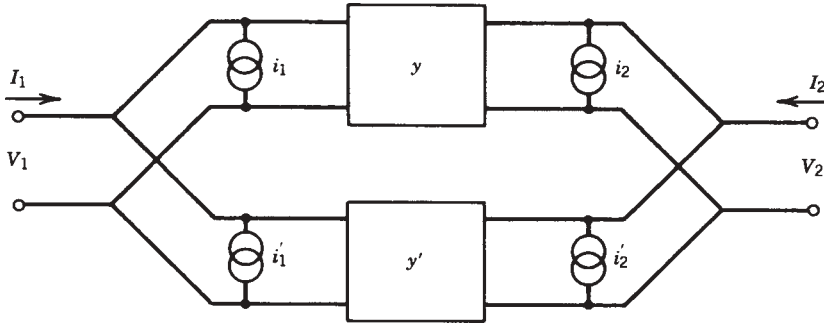
FIGURE 7.5 Parallel combination of two-ports using Y parameters.

7.4.2 Method of Combining Two-Port Matrix

If we parallel the two matrices y and y', we have the same port voltages, and the terminal currents add as shown in Figure 7.5:

$$I_1 = y_{11}V_1 + y_{12}V_2 + y'_{11}V_1 + y'_{12}V_2 + i_1 + i'_1$$
$$I_2 = y_{21}V_1 + y_{22}V_2 + y'_{21}V_1 + y'_{22}V_2 + i_2 + i'_2 \tag{7.20}$$

In matrix form

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} + y'_{11} & y_{12} + y'_{12} \\ y_{21} + y'_{21} & y_{22} + y'_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} i_1 + i'_1 \\ i_2 + i'_2 \end{bmatrix} \tag{7.21}$$

Here we can see that the noise current vectors add just as the y parameters add. Converting the new noise vector to a correlation matrix yields

$$\langle \bar{i}_{\text{new}} \bar{i}^+_{\text{new}} \rangle = \left\langle \begin{bmatrix} i_1 + i'_1 \\ i_2 + i'_2 \end{bmatrix} [\, i^*_1 + i'^*_1 \quad i_2 i'^*_2 \,] \right\rangle \tag{7.22}$$

$$= \begin{bmatrix} \langle i_1 i^*_1 \rangle + \langle i'_1 i'^*_1 \rangle & \langle i_1 i^*_2 \rangle + \langle i'_1 i'^*_2 \rangle \\ \langle i_2 i^*_1 \rangle + \langle i'_2 i'^*_1 \rangle & \langle i_2 i^*_2 \rangle + \langle i'_2 i'^*_2 \rangle \end{bmatrix} \tag{7.23}$$

The noise sources from different two-ports must be uncorrelated, so there are no cross products of different two ports. By inspection it can be seen it is just the addition of the correlation matrices for the individual two-ports, which is given as

$$[C_{y,\text{new}}] = [C_y] + [C'_y] \tag{7.24}$$

7.4.3 Noise Transformation Using the [ABCD] Noise Correlation Matrices

Figure 7.6 shows the noise transformation using the $[ABCD]$ matrix, where $[C_A]$ and $[C'_A]$ are correlation matrices respectively for a noise free two-port system:

$$[C_A] = \begin{bmatrix} \overline{v_A v^{\bullet}_A} & \overline{v_A i^{\bullet}_A} \\ \overline{i_A v^{\bullet}_A} & \overline{i_A i^{\bullet}_A} \end{bmatrix} \tag{7.25}$$
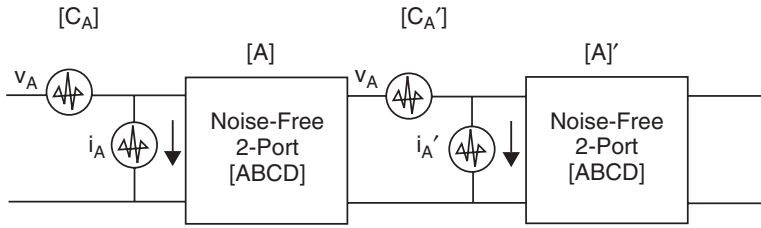
FIGURE 7.6 Noise transformation using the [*ABCD*] matrix.

$$[A_{\text{new}}] = [A][A]^{'} \tag{7.26}$$

The corresponding correlation matrix is given as

$$[C_{A,\text{new}}] = [C_A] + [A][C'_A][A]^{'} \tag{7.27}$$

7.4.4 Relation Between the Noise Parameter and [*C$_A$*]

Figure 7.7 shows the generator current and noise sources for the derivation of noise parameters, where I_G is generator current, Y_G is generator admittance, and i_G, i_A, v_A are noise sources. Using the noise correlation matrix representation, the correlated noise voltage and current are located at the input of the circuit, supporting a direct relation with the noise parameters (R_n, Γ_{opt}, F_{min}).

From the matrix properties, i_A can be written as

$$i_A = Y_{\text{cor}}v_A + i_u \tag{7.28}$$

$$\overline{i_A} = \overline{(Y_{\text{cor}}v_A + i_u)} \tag{7.29}$$

$$\overline{v_A i_A^{\bullet}} = Y_{\text{cor}}v_A^2 \tag{7.30}$$

$$Y_{\text{cor}} = \frac{\overline{v_A i_A^{\bullet}}}{v_A^2} \tag{7.31}$$

where i_u represents the uncorrelated port, Y_{cor} represents the correlation factor, and i_u and v_A are uncorrelated.
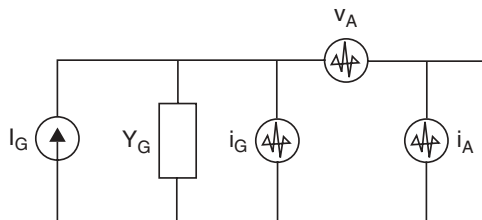
FIGURE 7.7 Generator current with noise sources.

The noise factor F is now given as

$$F = \left|\frac{i_G}{i_G}\right|^2 + \left|\frac{i_A + Y_G v_A}{i_G}\right|^2 = 1 + \left|\frac{Y_{cor}v_A + i_u + Y_G v_A}{i_G}\right|^2$$

$$= 1 + \left|\frac{v_A(Y_{cor} + Y_G) + i_u}{i_G}\right|^2 \tag{7.32}$$

$$= 1 + \left|\frac{i_u}{i_G}\right|^2 + \left|\frac{v_A(Y_{cor} + Y_G)}{i_G}\right|^2$$

$$= 1 + \frac{G_u}{G_G} + \frac{R_n}{G_G}[(G_G + G_{cor})^2 + (B_G + B_{cor})^2] \tag{7.33}$$

$$i_G^2 = 4kTBG_G \tag{7.34}$$

$$i_u^2 = 4kTBG_u \tag{7.35}$$

$$v_A^2 = 4kTBR_n \tag{7.36}$$

$$Y_{cor} = G_{cor} + jB_{cor} \tag{7.37}$$

where

$$G_u = \frac{1}{R_u} \qquad R_n = \frac{1}{G_n} \qquad Y_{cor} = \frac{1}{Z_{cor}} \tag{7.38}$$

$$F = 1 + \frac{R_u}{R_G} + \frac{G_n}{G_G}[(R_G + R_{cor})^2 + (X_G + X_{cor})^2] \tag{7.39}$$

The minimum noise factor F_{min} and corresponding optimum noise source impedance $Z_{opt} = R_{opt} + jX_{opt}$ are found by differentiating F with respect to source resistance (R_G) and susceptance (X_G):

$$\left.\frac{dF}{dR_G}\right|_{Rg,opt} = 0 \tag{7.40}$$

$$\left.\frac{dF}{dX_G}\right|_{Xg,opt} = 0 \tag{7.41}$$

$$R_{opt} = \sqrt{\frac{R_u}{G_n} + R_{cor}^2} \tag{7.42}$$

$$X_{opt} = -X_{cor} \tag{7.43}$$

$$F_{min} = 1 + 2G_n R_{cor} + 2\sqrt{R_u G_n + (G_n R_{cor})^2} \tag{7.44}$$

$$F = F_{min} + \frac{G_n}{R_G}|Z_G - Z_{opt}|^2 \tag{7.45}$$

$$= F_{min} + \frac{4r_n|\Gamma_G - \Gamma_{opt}|^2}{(1 - |\Gamma_G|^2)|1 + \Gamma_{opt}|^2} \tag{7.46}$$

The noise factor of a linear two-port as a function of the source admittance can be expressed as

$$F = F_{\min} + \frac{R_n}{G_g}[(G_{\text{opt}} - G_g)^2 + (B_{\text{opt}} - B_G)^2] \tag{7.47}$$

where Y_g = generator admittance, $= G_g + jB_G$
$\quad Y_{\text{opt}}$ = optimum noise admittance, $= G_{\text{opt}} + jB_{\text{opt}}$
$\quad F_{\min}$ = minimum achievable noise factor when $Y_{\text{opt}} = Y_g$
$\quad R_n$ = noise resistance and gives sensitivity of NF to source admittance

7.4.5 Representation of the *ABCD* Correlation Matrix in Terms of Noise Parameters [7.22]:

$$[C_A] = \begin{bmatrix} \overline{v_A v_A^\bullet} & \overline{v_A i_A^\bullet} \\ \overline{i_A v_A^\bullet} & \overline{i_A i_A^\bullet} \end{bmatrix} = \begin{bmatrix} C_{uu}{}^\bullet & C_{ui}{}^\bullet \\ C_{u}{}^\bullet{}_i & C_{ii}{}^\bullet \end{bmatrix}$$

$$= \begin{bmatrix} R_n & \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}}^\bullet \\ \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}} & R_n |Y_{\text{opt}}|^2 \end{bmatrix} \tag{7.48}$$

$$Y_{\text{opt}} = \sqrt{\frac{C_{ii}{}^\bullet}{C_{uu}{}^\bullet} - \left[\text{Im}\left(\frac{C_{ui}{}^\bullet}{C_{uu}{}^\bullet}\right)\right]^2} + j\,\text{Im}\left(\frac{C_{ui}{}^\bullet}{C_{uu}{}^\bullet}\right) \tag{7.49}$$

$$F_{\min} = 1 + \frac{C_{ui}{}^\bullet + C_{uu}{}^\bullet Y_{\text{opt}}^\bullet}{kT} \tag{7.50}$$

$$R_n = \frac{C_{uu}{}^\bullet}{kT} \tag{7.51}$$

7.4.6 Noise Correlation Matrix Transformations

For simplification of the analysis of the noise parameters of the correlation matrix, it is often needed to transform between admittance to impedance and vice versa. Two-port currents for the admittance form can be written as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = [Y]\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{7.52}$$

Writing in terms of voltage (we can move the noise vector to the left side and invert y),

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = [Y^{-1}]\begin{bmatrix} I_1 - i_1 \\ I_2 - i_2 \end{bmatrix} = [Y^{-1}]\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} + [Y^{-1}]\begin{bmatrix} -i_1 \\ -i_2 \end{bmatrix} \tag{7.53}$$

Since $(Y)^{-1} = (Z)$, we have

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = [Z]\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} + [Z]\begin{bmatrix} -i_1 \\ -i_2 \end{bmatrix} \tag{7.54}$$

Considering only noise source,

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = [Z] \begin{bmatrix} -i_1 \\ -i_2 \end{bmatrix} = [T_{yz}] \begin{bmatrix} -i_1 \\ -i_2 \end{bmatrix} \tag{7.55}$$

Here the signs of i_1 and i_2 are superfluous since they will cancel when the correlation matrix is formed and the transformation of the Y noise current vector to the Z noise voltage vector is done simply by multiplying $[Z]$. Other transformations are given in Table 7.1 for ready reference.

To form the noise correlation matrix, we again form the mean of the outer product:

$$\langle vv^+ \rangle = \begin{bmatrix} \langle v_1 v_1^* \rangle & \langle v_1 v_2^* \rangle \\ \langle v_1^* v_2 \rangle & \langle v_2 v_2^* \rangle \end{bmatrix} = [Z] \left\langle \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} [i_1^* \quad i_2^*] \right\rangle [Z]^+ \tag{7.56}$$

which is identical to

$$[C_z] = [Z][C_y][Z]^+ \tag{7.57}$$

$$v^+ = [i_1^* \quad i_2^*][Z]^+ \tag{7.58}$$

This is called a congruence transformation. The key to all of these derivations is the construction of the correlation matrix from the noise vector. For passive circuit noise the correlation matrix can be determined with only thermal noise sources. The $2kT$ factor comes from the double-sided spectrum of thermal noise:

$$[C_z] = 2kT \ \Delta f \ \mathrm{Re}([Z]) \tag{7.59}$$

and

$$[C_y] = 2kT \ \Delta f \ \mathrm{Re}([Y]) \tag{7.60}$$

for example, transformation of the noise correlation matrix $[C_A]$ to $[C_Z]$:

$$[C_A] = \begin{bmatrix} 1 & -Z_{11} \\ 0 & -Z_{22} \end{bmatrix} [C_A] = \begin{bmatrix} 1 & 0 \\ -Z_{11}^{\bullet} & -Z_{22}^{\bullet} \end{bmatrix} \tag{7.61}$$

TABLE 7.1   Noise Correlation Matrix Transformations

		Original form (α form)					
		Y		Z		A	
Resulting form (β form)	Y	1	0	y_{11}	y_{12}	$-y_{11}$	1
		0	1	y_{21}	y_{22}	$-y_{21}$	0
	Z	z_{11}	z_{12}	1	0	1	$-z_{11}$
		z_{21}	z_{22}	0	1	0	$-z_{21}$
	A	0	A_{12}	1	$-A_{11}$	1	0
		1	A_{22}	0	$-A_{21}$	0	1
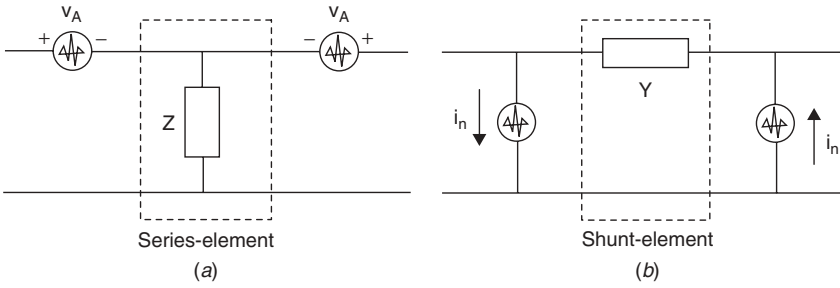
FIGURE 7.8   (*a*) Series element for the calculation of noise parameters. (*b*) Shunt element for the calculation of the noise parameters.

7.4.7   Matrix Definitions of Series and Shunt Element

Figures 7.8*a* and 7.8*b* show series and shunt elements for the calculation of noise parameters:

$$[Z]_{\text{series}} = \begin{bmatrix} Z & Z \\ Z & Z \end{bmatrix} \tag{7.62}$$

$$[C_Z]_{\text{series}} = 2kT \ \Delta f \ \text{Re}([z]_{\text{series}}) \tag{7.63}$$

$$[Y]_{\text{shunt}} = \begin{bmatrix} Y & -Y \\ -Y & Y \end{bmatrix} \tag{7.64}$$

$$[C_Y]_{\text{shunt}} = 2kT \ \Delta f \ \text{Re}([Y]_{\text{shunt}}) \tag{7.65}$$

7.4.8   Transferring All Noise Sources to the Input

For easier calculation of the noise parameters, all the noise sources are transferred to the input with the help of the *ABCD* matrix.

Before going into the detailed analysis of the noise parameters, some useful transformations using the *ABCD* matrix are discussed. They will be used later in forming the correlation matrices.

Figure 7.9 shows the two-port [*ABCD*] parameter representation of a noise-free system.

The general expression of the two-port *ABCD* matrix is given as

$$V_i = AV_0 + BI_o \tag{7.66}$$

$$I_i = CV_0 + DI_o \tag{7.67}$$
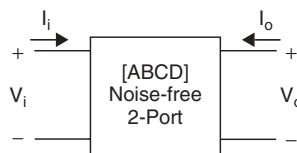
FIGURE 7.9   Two-port [*ABCD*] parameter representation of a noise-free system.

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} V_0 \\ I_0 \end{bmatrix} \tag{7.68}$$

With the addition of the noise source at the output as shown in Figure 7.10, the matrix shown above can be expressed as in [7.22]. The expression of a two-port *ABCD* matrix with noise sources connected at the output can be given as

$$V_i = AV_0 + BI_o - AV_n - BI_n \tag{7.69}$$

$$I_i = CV_0 + DI_o - CV_n - DI_n \tag{7.70}$$

7.4.9   Transformation of the Noise Sources

Figure 7.11 shows the noise sources transformed to the input, where current and voltage noise sources are correlated.

The modified matrix is expressed as

$$V_i + AV_n + BI_n = AV_0 + BI_o \tag{7.71}$$

$$I_i + CV_n + DI_n = CV_0 + DI_o \tag{7.72}$$

7.4.10   *ABCD* Parameters for CE, CC, and CB Configurations

Figures 7.12*a* and 7.12*b* show the grounded emitter configuration of the noise-free transistor and with the current and voltage noise sources at the input of the transistor:
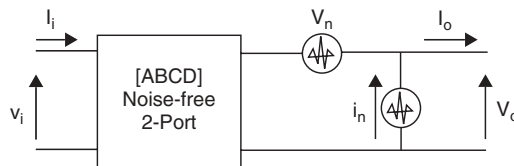
FIGURE 7.10   Two-port [*ABCD*] parameter representation with noise source connected at output.
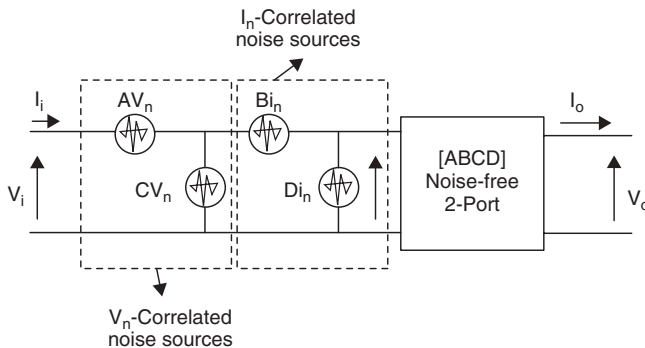
FIGURE 7.11   Noise source transformed to the input.
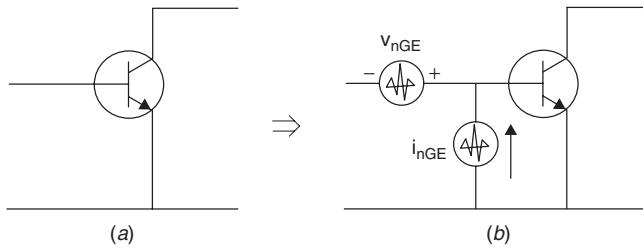
FIGURE 7.12 (*a*) CE configuration of noise-free transistor. (*b*) CE configuration with the noise sources at the input of the transistor.

Common emitter (CE):

$$[ABCD]_{CE} = \begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix} \tag{7.73}$$

$$\begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix} \Rightarrow \begin{matrix} v_{nCE} = v_{bn} + B_{CE}i_{cn} \\ i_{nCE} = i_{bn} + D_{CE}i_{cn} \end{matrix} \tag{7.74}$$

Common collector (CC):

$$[ABCD]_{CC} = \begin{bmatrix} A_{CC} & B_{CC} \\ C_{CC} & D_{CC} \end{bmatrix} \tag{7.75}$$

Figures 7.13*a* through 7.13*d* show the grounded-collector configuration of the noise-free transistor and with the current and voltage noise sources at the input of the transistor.
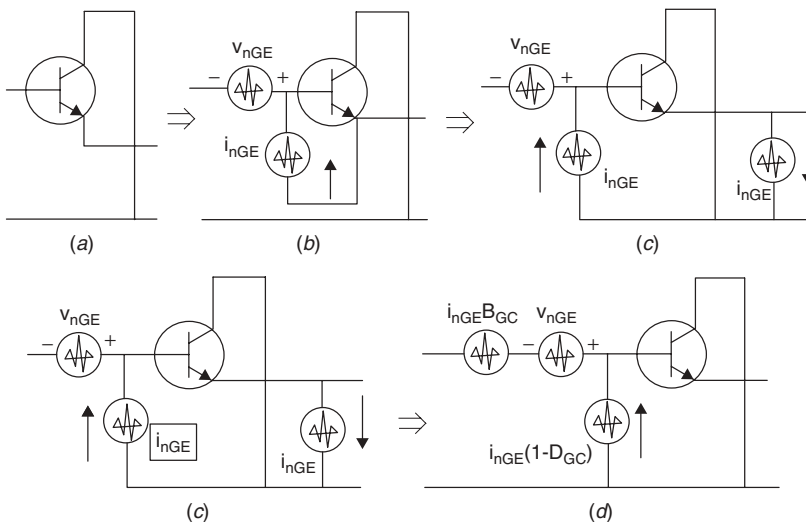
FIGURE 7.13 (*a*) CC configuration. (*b*) CC with input noise sources. (*c*) CC noise current splitting. (*d*) Output current noise source transferred to the input.

The parameters B_{CC} and D_{CC} are very small for the CC configuration because trans-admittance ($1/B_{CC}$ and the current gain $1/D_{CC}$ are large; therefore, the noise performance/parameters of the CC configuration are similar to the CE configuration.

Figures 7.14*a* through 7.14*f* show the grounded-base configuration of the noise-free transistor and the transformation of all noise sources to the input. The common-base (CB) configuration is given as

$$[ABCD]_{CB} = \begin{bmatrix} A_{CB} & B_{CB} \\ C_{CB} & D_{CB} \end{bmatrix} \tag{7.76}$$

Here, A_{CB} and C_{CB} are very small for the CB stage because the trans-impedance $[1/C_{CB} = (v_o/i_i)|_{io} = 0]$ and the voltage gain $(1/A_{CB} = v_o/v_i|_{io} = 0)$ are very larger. With comparable bias conditions the noise performance is similar to that of the CE stage configuration.

7.5 NOISY TWO-PORT DESCRIPTION

Based on the convention by Rothe and Dahlke [7.3], any linear two-port can be in the form shown in Figure 7.15. This general case of a noisy two-port can be redrawn showing noise sources at the input and at the output. Figure 7.15*b* shows this in admittance form and Figure 7.15*c* in impedance form. The internal noise sources are assumed to produce very small currents and voltages, and we assume that linear two-port equations are valid. From the set of equations from the γ parameters in Table 4.1, we can describe the general case. The internal noise contributions have been expressed by using external noise sources:

$$I_1 = y_{11}V_1 + y_{12}V_2 + I_{K1}$$
$$I_2 = y_{21}V_1 + y_{22}V_2 + I_{K2} \tag{7.77}$$
$$V_1 = z_{11}I_1 + z_{12}I_2 + V_{L1}$$
$$V_2 = z_{21}I_1 + z_{22}I_2 + V_{L2} \tag{7.78}$$

where the external noise sources are I_{K1}, I_{K2}, V_{L1}, and V_{L2}.

Since we want to describe our noisy circuit in terms of the noise figure, the *ABCD*-matrix description will be more convenient since it refers both noise sources to the input of the two-port [7.4]. This representation is given below (note the change in direction of I_2):

$$V_1 = AV_2 + BI_2 + V_A$$
$$I_1 = CV_2 + DI_2 + I_A \tag{7.79}$$

where V_A and I_A are the external noise sources.

It is important to remember that all of these matrix representations are interrelated. For example, the noise sources for the *ABCD*-matrix description can be obtained from the *z*-matrix representation shown in (7.78). This transformation is

$$V_A = -\frac{I_{K2}}{y_{21}} = V_{L1} - \frac{V_{L2}Z_{11}}{z_{21}} \tag{7.80}$$
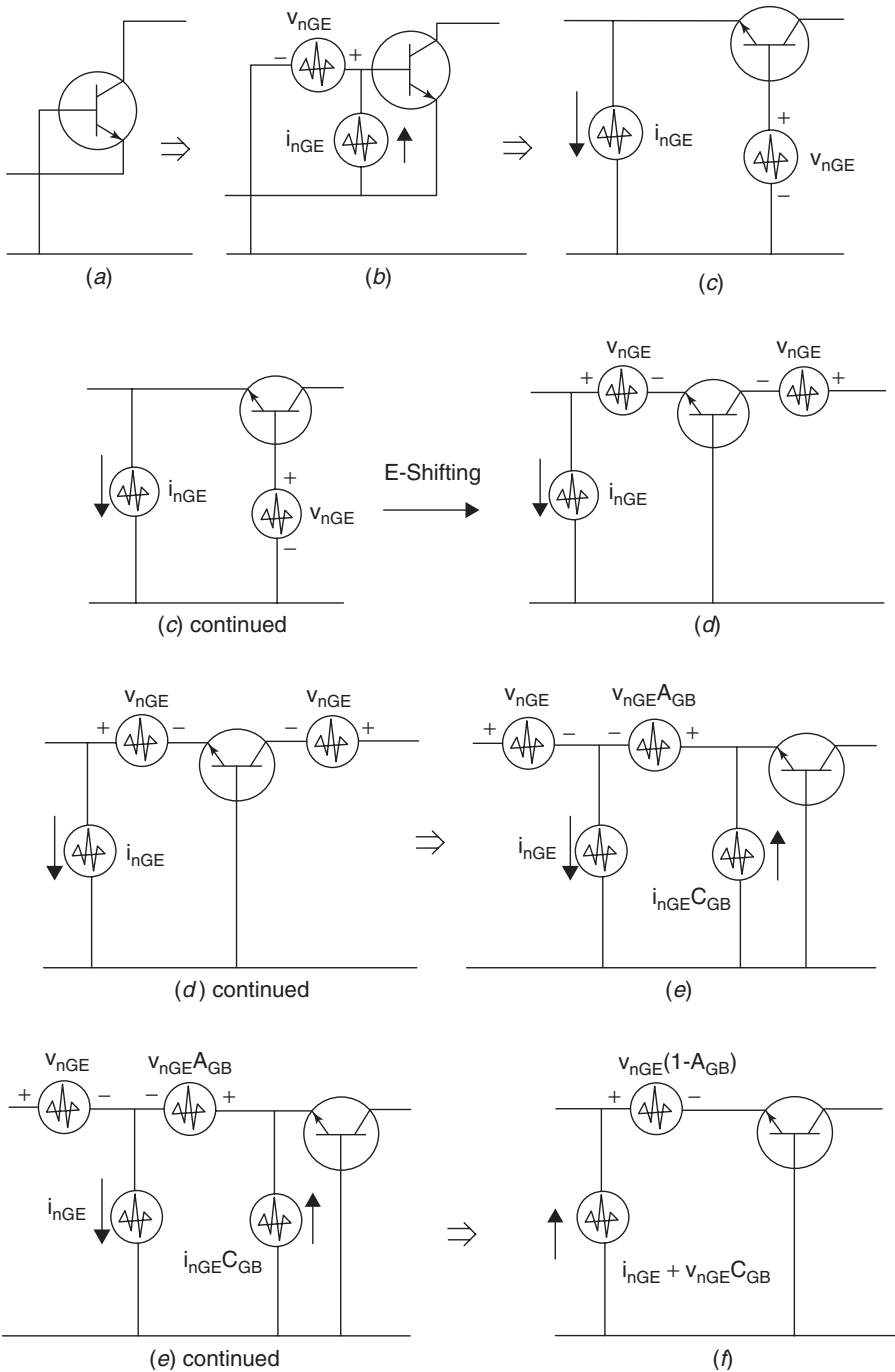
FIGURE 7.14   (*a*) CB configuration. (*b*) CB with input noise sources. (*c*) Orientation of noise sources. (*d*) Noise sources e-shift. (*e*) Noise transformation from output to input. (*f*) Orientation of noise sources at the input.
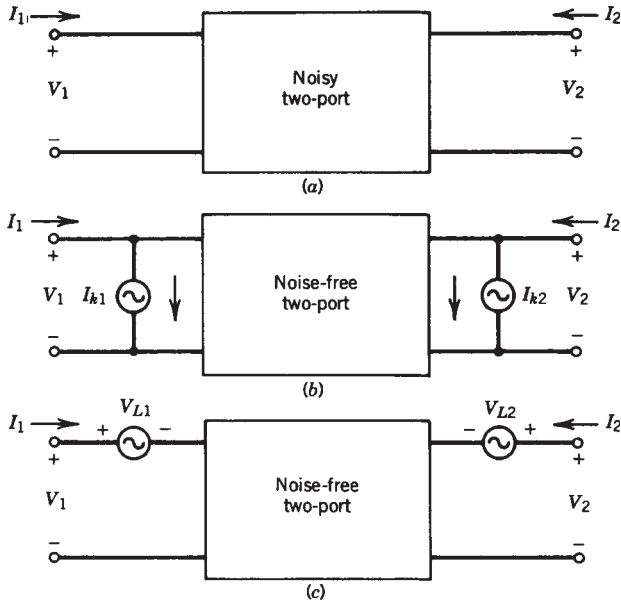
FIGURE 7.15   Noisy linear two-ports: (*a*) general form; (*b*) admittance form; (*c*) impedance form.
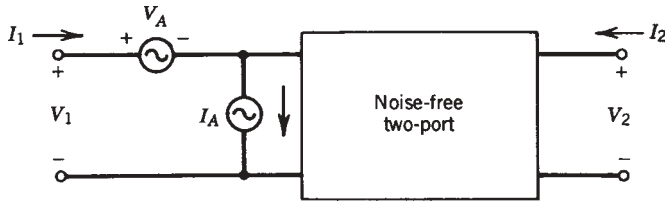
FIGURE 7.16   Chain matrix form of linear noisy two-port.

$$I_A = I_{K1} - \frac{I_{K2}y_{11}}{y_{21}} = -\frac{V_{L2}}{z_{21}} \tag{7.81}$$

The *ABCD* representation is particularly useful based on the fact that it allows us to define a noise temperature for the two-port referenced to its input. The two-port itself (shown in Fig. 7.16) is assumed to be noise free.

In the past, *z* and *y* parameters have been used, but in microwave applications it has become common to use *S*-parameter definitions. This is shown in Figure 7.17. The previous equations can be rewritten in their new form using *S* parameters:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} + \begin{bmatrix} b_{n1} \\ b_{n2} \end{bmatrix} \tag{7.82}$$

There are different physical origins for the various sources of noise. Typically, thermal noise is generated by resistances and loss in the circuit or transistor, whereas
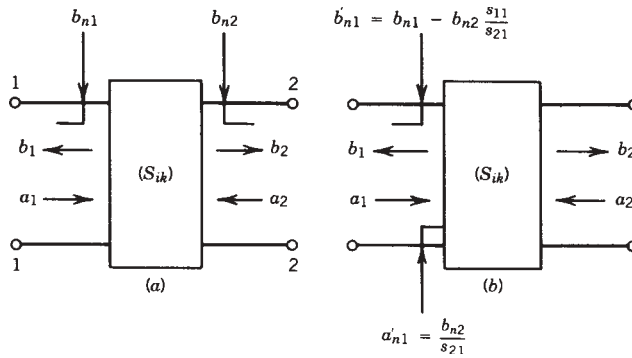
FIGURE 7.17   *S*-parameter form of linear noisy two-ports.

shot noise is generated by current flowing through semiconductor junctions and vacuum tubes. Since these many sources of noise are represented by only two noise sources at the device input, the two equivalent input noise sources are often a complicated combination of the circuit internal noise sources. Often, some fraction of V_A and I_A is related to the same noise source. This means that V_A and I_A are not independent in general. Before we can use V_A and I_A to calculate the noise figure of the two-port, we must calculate the correlation between the V_A and I_A shown in Figure 7.16.

The noise source V_A represents all of the device noise referred to the input when the generator impedance is zero; that is, the input is short circuited. The noise source I_A represents all of the device noise referred to the input when the generator admittance is zero; that is, the input is open circuited.

The correlation of these two noise sources considerably complicates the analysis. By defining a correlation admittance, we can simplify the mathematics and get some physical intuition for the relationship between noise figure and generator admittance. Since some fraction of I_A will be correlated with V_A, we split I_A into correlated and uncorrelated parts as follows:

$$I_A = I_n + I_u \tag{7.83}$$

where I_u is the part of I_A uncorrelated with V_A. Since I_n is correlated with V_A, we can say that I_n is proportional to V_A and the constant of proportionality is the correlation admittance:

$$I_n = Y_{\text{cor}} V_A \tag{7.84}$$

This leads us to

$$I_A = Y_{\text{cor}} V_A + I_u \tag{7.85}$$

The following derivation of noise figure will use the correlation admittance. The admittance Y_{cor} is not a physical component located somewhere in the circuit. It is a complex number derived by correlating the random variables I_A and V_A. To calculate Y_{cor}, we multiply each side of (7.85) by V_A^* and average the result. This gives

$$\overline{V_A^* I_A} = Y_{\text{cor}} \overline{V_A^2} \tag{7.86}$$

where the I_u term averaged to zero since it was uncorrelated with V_A. The correlation admittance is thus given by

$$Y_{\text{cor}} = \frac{\overline{V_A^* I_A}}{\overline{V_A^2}} \tag{7.87}$$

Often, people use the term "correlation coefficient." This normalized quantity is defined as

$$c = \frac{\overline{V_A^* I_A}}{\sqrt{\overline{V_A^2 I_A^2}}} = Y_{\text{cor}} \sqrt{\frac{\overline{V_A^2}}{\overline{I_A^2}}} \tag{7.88}$$

Note that the dual of this admittance description is the impedance description. Thus the impedance representation has the same equations as above with Y replaced by Z, I replaced by V, and V replaced by I.

The parameters V_A and I_A represent internal noise sources in the form of a voltage source acting in series with the input voltage and a source of current flowing in parallel with the input current. This representation conveniently leads to the four noise parameters needed to describe the noise performance of the two-port. Again using the Nyquist formula, the open-circuit voltage of a resistor at the temperature T is

$$\overline{V_A^2} = 4kTRB \tag{7.89}$$

This voltage is a mean-square fluctuation (or spectral density). It is the method used to calculate the noise density. We could also define a noise equivalent resistance for a noise voltage as

$$R_n = \frac{\overline{V_A^2}}{4kTB} \tag{7.90}$$

The resistor R_n is not a physical resistor but can be used to simulate different portions of the noise equivalent circuit.

In a similar manner a mean-square current fluctuation can be represented in terms of an equivalent noise conductance G_n, which is defined by

$$G_n = \frac{\overline{I_A^2}}{4kTB} \tag{7.91}$$

and

$$G_u = \frac{\overline{I_u^2}}{4kTB} \tag{7.92}$$

for the case of the uncorrelated noise component. The input generator to the two-port has a similar contribution:

$$G_G = \frac{I_G^2}{4kTB} \tag{7.93}$$

with Y_G being the generator admittance and G_G being the real part. With the definition of F above, we can write

$$F = 1 + \left| \frac{I_A + Y_G V_A}{I_G} \right|^2 \tag{7.94}$$

The use of the voltage V_A and the current I_A has allowed us to combine all the effects of the internal noise sources.

We can use the previously defined (7.87) correlation admittance, $Y_{\text{cor}} = G_{\text{cor}} + jB_{\text{cor}}$, to simplify (7.94). First, we determine the total noise current:

$$\overline{I_A^2} = 4kT(Y_{\text{cor}}/R_n^2 + G_u)B \tag{7.95}$$

where R_n and G_u are as defined in (7.90) and (7.91). The noise factor can now be determined:

$$F = 1 + \frac{G_u}{G_g} + \frac{R_n}{G_g}[(G_G + G_{\text{cor}})^2 + (B_G + B_{\text{cor}})^2] \tag{7.96}$$

$$= 1 + \frac{R_u}{R_g} + \frac{G_n}{R_g}[(R_G + R_{\text{cor}})^2 + (X_G + X_{\text{cor}})^2] \tag{7.97}$$

The noise factor is a function of various elements, and the optimum impedance for the best noise figure can be determined by minimizing F with respect to generator reactance and resistance. This gives[†]

$$R_{on} = \sqrt{\frac{R_u}{G_n} + R_{\text{cor}}^2} \tag{7.98}$$

$$X_{on} = -X_{\text{cor}} \tag{7.99}$$

and

$$F_{\min} = 1 + 2G_n R_{\text{cor}} + 2\sqrt{R_u G_n + (G_n R_{\text{cor}})^2} \tag{7.100}$$

At this point we see that the optimum condition for the minimum noise figure is not a conjugate power match at the input port. We can explain this by recognizing that the noise source V_A and I_A represent all the two-port noise, not just the thermal noise of the input port. We should observe that the optimum generator susceptance, $-X_{\text{cor}}$, will minimize the noise contribution of the two noise generators.

In rearranging for conversion to S parameters, we write

$$F = F_{\min} + \frac{G_n}{R_G}|Z_G - Z_{on}|^2 \tag{7.101}$$

$$= F_{\min} + \frac{R_n}{G_G}|Y_G - Y_{on}|^2 \tag{7.102}$$

From the definition of the reflection coefficient,

$$\Gamma_G = \frac{Y_0 - Y_G}{Y_0 + Y_G} \tag{7.103}$$

and with

$$r_n = \frac{R_n}{Z_0} \tag{7.104}$$

[†] To distinguish between optimum noise and optimum power, we have introduced the conventional on instead of the more familiar abbreviation opt.

the normalized equivalent noise resistance

$$F = F_{\min} + \frac{4r_n|\Gamma_G - \Gamma_{on}|^2}{(1 - |\Gamma_G|^2)|1 + \Gamma_{on}|^2} \tag{7.105}$$

$$r_n = (F_{50} - F_{\min})\frac{|1 + \Gamma_{on}|^2}{4|\Gamma_{on}|^2} \tag{7.106}$$

$$\Gamma_{on} = \frac{Z_{on} - Z_0}{Z_{on} + Z_0} \tag{7.107}$$

The noise performance of any linear two-port can now be determined if the values of the four noise parameters $F_{\min}$, $r_n = R_n/50$, and Γ_{on} are known.

7.6   NOISE FIGURE OF CASCADED NETWORKS

In a system with many circuits connected in cascade (Fig. 7.18), we must consider the contributions of the various circuits. In considering the equivalent noise resistor R_n in series with the input circuit,

$$F = \frac{R_G + R_n}{R_G} \tag{7.108}$$

$$= 1 + \frac{R_n}{R_G} \tag{7.109}$$

The excess noise added by the circuit is R_n/R_G.

   In considering two cascaded circuits a and b, by definition, the available noise at the output of b is

$$N_{ab} = F_{ab}G_{ab}kTB \tag{7.110}$$

with B the equivalent noise bandwidth in which the noise is measured. The total available gain G is the product of the individual available gains, so

$$N_{ab} = F_{ab}G_aG_bkTB \tag{7.111}$$
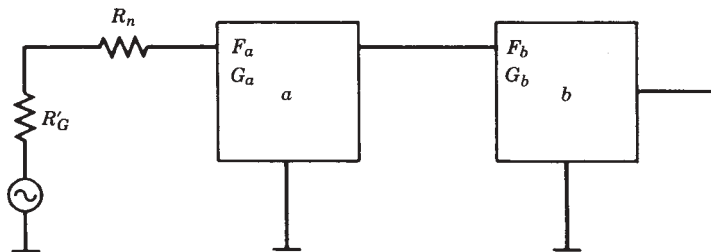
FIGURE 7.18   Cascaded noisy two-ports with noise figures F_a and F_b and gain figures G_a and G_b.

The available noise from network a at the output of network b is

$$N_{a/b} = N_a G_b = F_a G_a G_b kTB \tag{7.112}$$

The available noise added by network b (its excess noise) is

$$N_{b/b} = (F_b - 1)G_b kTB \tag{7.113}$$

The total available noise N_{ab} is the sum of the available noise contributed by the two networks:

$$N_{ab} = N_{a/b} + N_{b/b} = F_a G_a G_b kTB + (F_b - 1)G_b kTB$$

$$= \left(F_a + \frac{F_b - 1}{G_a} \right) G_a G_b kTB \tag{7.114}$$

$$F_{ab} = F_a + \frac{F_b - 1}{G_a} \tag{7.115}$$

For any number of circuits, this can be extended to be

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots \tag{7.116}$$

When considering a long chain of cascaded amplifiers there will be a minimum noise figure achievable for this chain. This is a figure of merit and was proposed by Haus and Adler [7.5]. It is calculated by rearranging (7.116). If all stages are designed for a minimum noise figure, we find that, for an infinite chain of identical stages,

$$(F_{\text{tot}})_{\min} = (F_{\min} - 1) + \frac{F_{\min} - 1}{G_A} + \frac{F_{\min} - 1}{G_A^2} + \cdots + 1 \tag{7.117}$$

where $F_{\min}$ is the minimum noise figure for each stage and G_A is the available power gain of the identical stages. Using

$$\frac{1}{1 - X} = 1 + X + X^2 + \cdots \tag{7.118}$$

we find a quantity $(F_{\text{tot}} - 1)$, which is defined as noise measure M. The minimum noise measure

$$(F_{\text{tot}})_{\min} - 1 = \frac{F_{\min} - 1}{1 - 1/G_A} = M_{\min} \tag{7.119}$$

refers to the noise of an infinite chain of optimum-tuned, low-noise stages, so it represents a lower limit on the noise of an amplifier.

The minimum noise measure $M_{\min}$ is an invariant parameter and is not affected by lossless feedback. It is somewhat similar to a gain–bandwidth product in its use as a system invariant. The minimum noise measure is achieved when the amplifier is tuned for the available power gain and $\Gamma_G = \Gamma_{on}$, given by (7.107).

7.7   INFLUENCE OF EXTERNAL PARASITIC ELEMENTS

Mounting an active two-port such as a transistor usually adds stray capacitance and lead inductance to the device, as shown in Figure 7.19. These external components, consisting of transmission lines and parasitic reactances, modify the noise parameters and the gain. Some researchers have published the results of these parasitic effects and have made manual computations or used some limited computer programs.

In a paper by Fukui [7.6] an attempt was made to determine the necessary equations, but the formulas are too involved even for pocket calculators. A more generic study by Iversen [7.7] is also very involved because of the various matrix manipulations and is more suitable for a computer. Besser's paper in the IEEE MTT-S in 1975 [7.8] and Vendelin's paper [7.9] in the same issue have shown for the first time some practical results using computers and even optimization methods using an early version of Compact. The intention of these investigations was to find feedback that modifies the device noise and scattering parameters such that a noise match could also provide a low-input VSWR. It can be seen from these discussions that some feedback, besides resulting in some gain reduction, may improve the noise matching at the input for a limited frequency range. The derivation of these matrix methods is presented in Section 7.9.

A more recent paper by Suter [7.10] based on a report by Hartman and Strutt [7.11] has given a simple transformation starting from the S parameters and the noise parameters from common-source (or common-emitter) measurements. The noise parameters for the "packaged" device are calculated. This means that the parameters for the "new" device, including the common-gate (or common-base) case, are calculated. The equations are device independent. They are valid for any active two-port.

A transformation matrix, n, may be used to combine the noise sources of the various circuit configurations. The transformation matrix parameters are given in Table 7.2 for series feedback, shunt feedback, and the common-gate (base) case, which will be
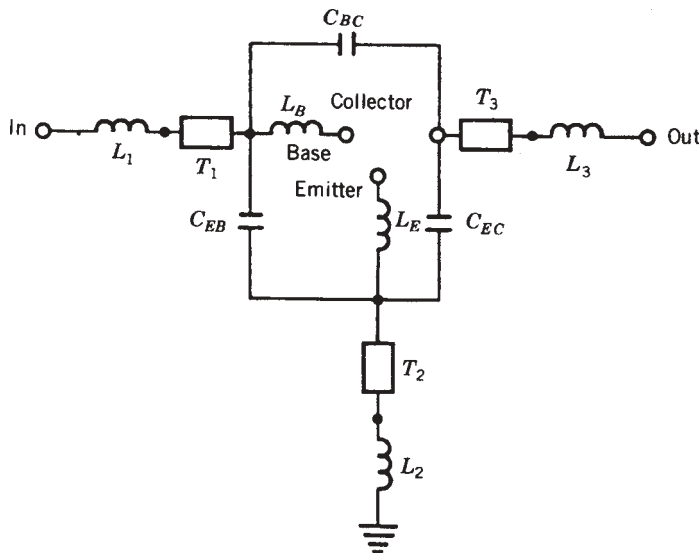
FIGURE 7.19   Equivalent circuit of the transistor package.

TABLE 7.2   Transformation of Noise Parameters

Series Feedback
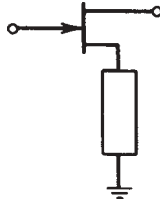
$$Z_s = R_s + jX_s = Z_s$$

$$[n] = \begin{bmatrix} n_{11} = 1 & n_{12} = Z_0 \dfrac{S_{21}M - S'_{21}N}{S_{21}C'_1 + S'_{21}C_1} & \Omega \\[3mm] n_{21} = 0 & n_{22} = \dfrac{S_{21}C'_1}{S_{21}C'_1 + S'_{21}C_1} \end{bmatrix}$$

where

$$S'_{11} = S'_{22} = \frac{-1}{1 + 2Z_S}$$

$$S'_{12} = S'_{21} = \frac{2Z_S}{1 + 2Z_S}$$

$$M = (1 + S'_{11})(1 - S'_{22}) + S'_{12}S'_{21}$$

$$N = (1 + S_{11})(1 - S_{22}) + S_{12}S_{21}$$

$$C_1 = (1 - S_{11})(1 - S_{22}) - S_{12}S_{21}$$

$$C'_1 = (1 + S'_{11})(1 - S'_{22}) - S'_{12}S'_{21}$$

$$[S]_{\text{DEVICE}} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

Shunt Feedback
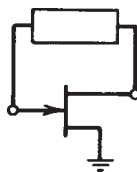
$$Z_p = R_p + jX_p = Z_p$$

$$[n] = \begin{bmatrix} n_{11} = \dfrac{S_{21}C'_2}{S_{21}C'_2 + S'_{21}C_2} & n_{12} = 0 \ \Omega \\[3mm] n_{21} = \dfrac{1}{Z_0}\dfrac{S_{21}P - S'_{21}Q}{S_{21}C'_2 + S'_{21}C_2}S & n_{22} = 1 \end{bmatrix}$$

where

$$S'_{11} = S'_{22} = \frac{Z_p}{2 + Z_p}$$

$$S'_{12} = S'_{21} = \frac{2}{2 + Z_p}$$

TABLE 7.2   Transformation of Noise Parameters (*continued*)

$$P = (1 - S'_{11})(1 + S'_{22}) + S'_{12}S'_{21}$$

$$Q = (1 - S_{11})(1 + S_{22}) + S_{12}S_{21}$$

$$C_2 = (1 + S_{11})(1 + S_{22}) - S_{12}S_{21}$$

$$C'_2 = (1 + S'_{11})(1 + S'_{22}) - S'_{12}S'_{21}$$

$$[S]_{\text{DEVICE}} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

Common Gate
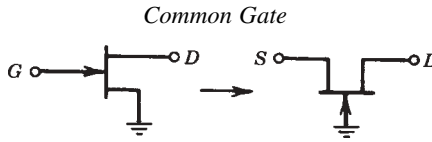
$$[n] = \begin{bmatrix} n_{11} = \dfrac{2S_{21}}{-2S_{21} + C_4} & n_{12} = 0 \ \Omega \\[2mm] n_{21} = \dfrac{1}{Z_0} \dfrac{C_3 C_4 - 4 S_{12} S_{21}}{V(-2S_{21} + C_4)} S & n_{22} = -1 \end{bmatrix}$$

where

$$V = (1 + S_{11})(1 + S_{22}) - S_{12}S_{21}$$

$$C_3 = (1 - S_{11})(1 + S_{22}) + S_{12}S_{21}$$

$$C_4 = (1 + S_{11})(1 - S_{22}) + S_{12}S_{21}$$

$$[S]_{\text{DEVICE}} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \text{common-source } S \text{ parameters}$$

important for oscillator analysis. The transformation matrix gives the new four noise parameters as follows:

$$R'_n = R_n|n_{11} + n_{12}Y_{\text{cor}}|^2 + G_n|n_{12}|^2 \tag{7.120}$$

$$G'_n = \frac{G_n R_n}{R'_n}|n_{11}n_{22} - n_{12}n_{21}|^2 \tag{7.121}$$

$$Y'_{\text{cor}} = \frac{R_n}{R'_n}(n_{21} + n_{22}Y_{\text{cor}})(n^*_{11} + n^*_{12}Y^*_{\text{cor}}) + \frac{G_n}{R'_n}n_{22}n^*_{12} \tag{7.122}$$

A final transformation to the more common noise parameter format given by (7.102) is still needed [7.9]:

$$F_{\min} = 1 + 2R'_n(G'_{\text{cor}} + G'_{on}) \tag{7.123}$$

$$R_n = R'_n \tag{7.124}$$

$$G_{on} = \sqrt{\frac{G'_n}{R'_n} + G'^2_{cor}} \qquad (7.125)$$

$$B_{on} = -B'_{cor} \qquad (7.126)$$

In Chapter 3 we will see examples of the different noise parameters for bipolar and field-effect transistors. Figure 7.20 shows the noise figure as a function of external
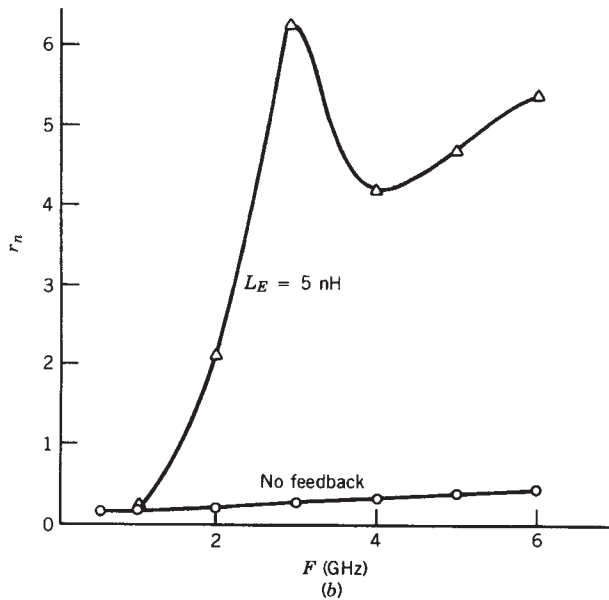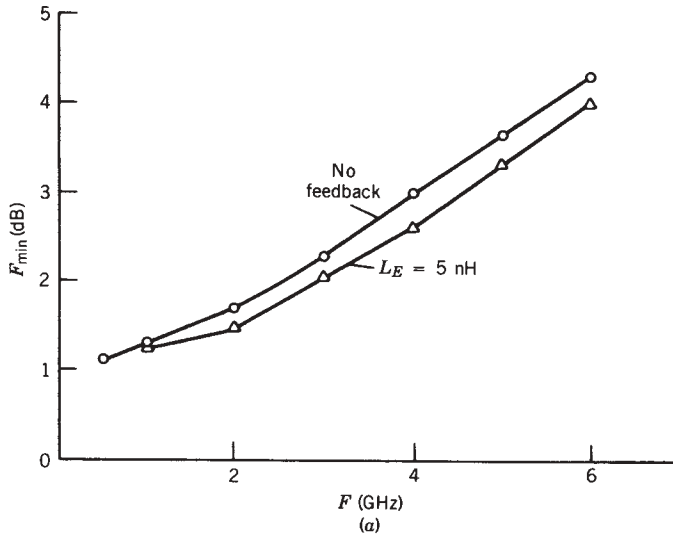
FIGURE 7.20 Noise parameters versus feedback for AT-41435 silicon bipolar transistor: (a) F_{min} for AT-41435 versus frequency and feedback; (b) r_n for AT-41435 versus frequency and feedback; (c) Γ_{on} for AT-41435 versus frequency and feedback.
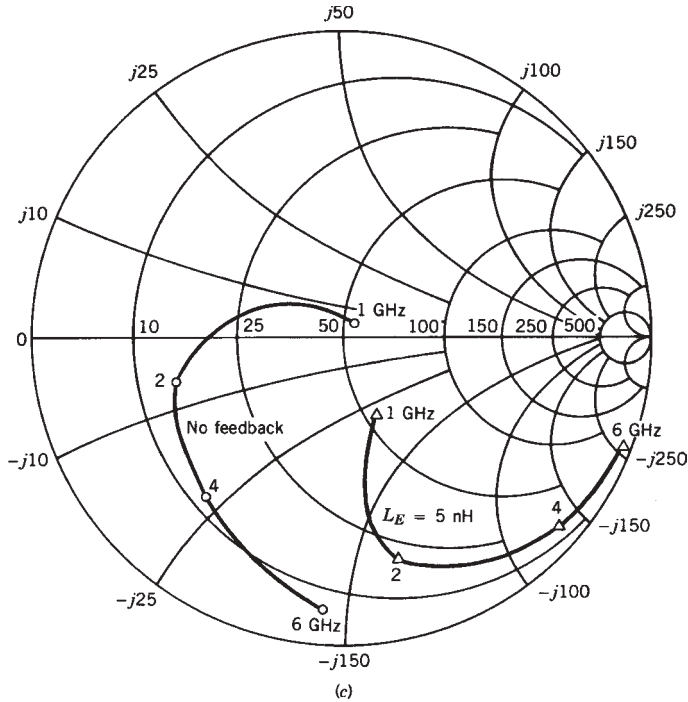
FIGURE 7.20   (*continued*)

feedback for a low-noise microwave bipolar transistor that is discussed in Chapter 3, the AT-41435.

7.8 NOISE CIRCLES

From Section 7.7 we see that the noise factor is a strong function of the generator admittance (or impedance) presented to the input terminals of the noisy two-port. Noise tuning is the method to change the values of the input admittance to obtain the best noise performance. There is a range of values of input reflection coefficients over which the noise figure is constant. In plotting these points of constant noise figure, we obtain the so-called noise circles, which can be drawn on the Smith chart Γ_G plane [7.12]. Using similar techniques as were used to calculate the gain circles [7.12] and starting with the noise equation [see (7.105)] for a 50-Ω generator impedance, we find that

$$F_{50} = F_{\min} + 4r_n \frac{|\Gamma_{on}|^2}{|1 + \Gamma_{on}|^2} \tag{7.127}$$

We want to find the position of the reflection coefficient on the Smith chart, as in the case of the gain circles, for which $F = $ constant. First we rearrange (7.124) to read

$$r_n = (F_{50} - F_{\min}) \frac{|1 + \Gamma_{on}|^2}{4|\Gamma_{on}|^2} \tag{7.128}$$

By introducing

$$N_i = \frac{F_i - F_{\min}}{4r_n}|1 + \Gamma_{on}|^2 \qquad (7.129)$$

we can find an expression for a circle of constant noise figure as introduced by Rothe and Dahlke [7.3, 7.12]. The center for the noise circle is

$$C_i = \frac{\Gamma_{on}}{1 + N_i} \qquad (7.130)$$

and the radius

$$r_i = \frac{\sqrt{N_i^2 + N_i(1 - |\Gamma_{on}|^2)}}{1 + N_i} \qquad (7.131)$$

with the definition of N used previously. Examples of noise circles are shown in the literature and in Figure 7.21. However, if we only consider the minimum noise figure for a given device, we will not obtain the minimum noise figure for the multistage amplifier system. This was explained when the noise measure was introduced. (See Fig. 7.21.) Therefore, a better way to design the amplifier would be to use circles of constant noise measure instead of circles of constant noise figure. The noise measure circles are a function of S parameters, noise parameters, and Γ_G, using

$$G_A = \frac{|S_{21}|^2(1 - |\Gamma_G|^2)}{(1 - |S_{22}|^2) + |\Gamma_G|^2(|S_{11}|^2 - |\Delta|^2) - 2\,\mathrm{Re}(\Gamma_G C_1)} \qquad (7.132)$$
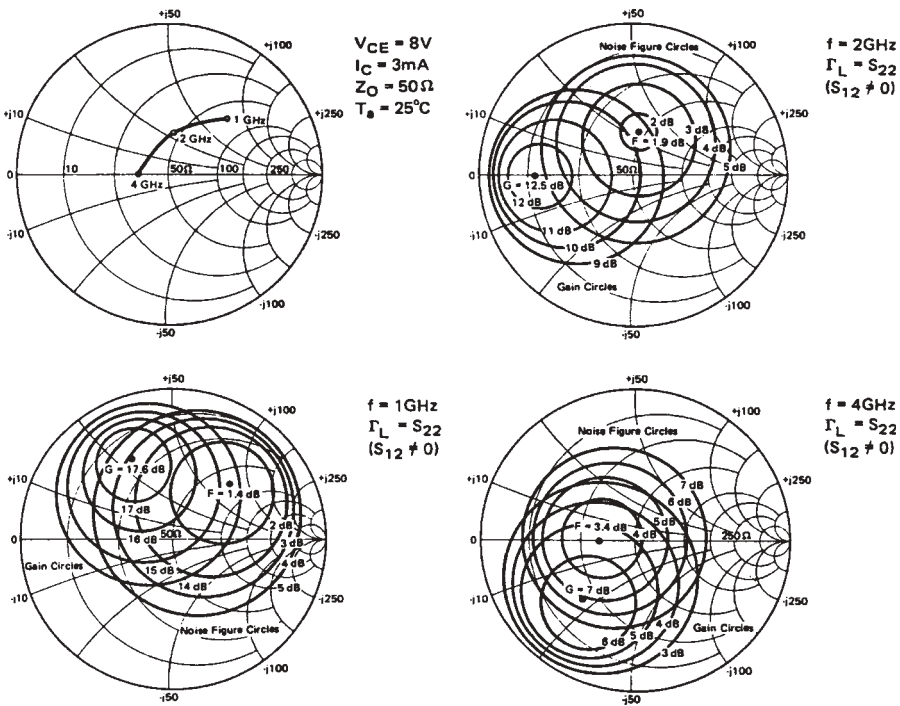
FIGURE 7.21 Typical noise figure circles and gain circles.

where

$$C_1 = S_{11} - S_{22}^* \Delta \qquad \Delta = S_{11} S_{22} - S_{12} S_{11}$$

7.9   NOISE CORRELATION IN LINEAR TWO-PORTS USING CORRELATION MATRICES

In the introduction to two-port noise theory, it was indicated that noise correlation matrices form a general technique for calculating noise in n-port networks. Haus and Adler have described the theory behind this technique [7.5]. In 1976, Hillbrand and Russer published equations and transformations that aid in supplying this method to two-port CAD [7.13].

This method is useful because it forms a base from which we can rigorously calculate the noise of linear two-ports combined in arbitrary ways. For many representations, the method of combining the noise parameters is as simple as that for combining the circuit element matrices. In addition, noise correlation matrices can be used to calculate the noise in linear frequency conversion circuits. The following is an introduction to this subject.

Linear, noisy two-ports can be modeled as a noise-free two-port with two additional noise sources. These noise sources must be chosen so that they add directly to the resulting vector of the representation, as shown in (7.133) and (7.134) and Figure 7.15:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{7.133}$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} + \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{7.134}$$

where the i and v vectors indicate noise sources for the y and z representations, respectively. This two-port example can be extended to n-ports in a straightforward, obvious way.

Since the noise vector for any representation is a random variable, it is much more convenient to work with the noise correlation matrix. The correlation matrix gives us deterministic numbers to calculate with. The correlation matrix is formed by taking the mean value of the outer product of the noise vector. This is equivalent to multiplying the noise vector by its adjoint (complex conjugate transpose) and averaging the result:

$$\langle \bar{i}\ \bar{i}^+ \rangle = \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \begin{bmatrix} i_1^* & i_2^* \end{bmatrix} = \begin{bmatrix} \langle i_1 i_1^* \rangle & \langle i_1 i_2^* \rangle \\ \langle i_1^* i_2 \rangle & \langle i_2 i_2^* \rangle \end{bmatrix} = [C_y] \tag{7.135}$$

where the angular brackets denote the average value.

Note that the diagonal terms are the "power" spectrum of each noise source and the off-diagonal terms are complex conjugates of each other and represent the cross "power" spectrums of the noise sources. "Power" is used because these magnitude-squared quantities are proportional to power.

To use these correlation matrices in circuit analysis, we must know how to combine them and how to convert them between various representations. An example using y matrices will illustrate the method for combining two-ports and their correlation
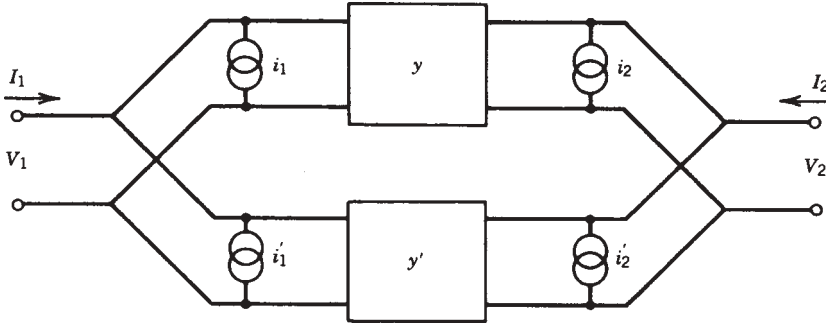
FIGURE 7.22 Parallel combination of two-ports using Y parameters.

matrices. Given two matrices y and y', when we parallel them, we have the same port voltages, and the terminal currents add (Fig. 7.22):

$$I_1 = y_{11}V_1 + y_{12}V_2 + y'_{11}V_1 + y'_{12}V_2 + i_1 + i'_1$$
$$I_2 = y_{21}V_1 + y_{22}V_2 + y'_{21}V_1 + y'_{22}V_2 + i_2 + i'_2 \tag{7.136}$$

or

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} + y'_{11} & y_{12} + y'_{12} \\ y_{21} + y'_{21} & y_{22} + y'_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} i_1 + i'_1 \\ i_2 + i'_2 \end{bmatrix} \tag{7.137}$$

Here we can see that the noise current vectors add just as the y parameters add. Converting the new noise vector to a correlation matrix yields

$$\langle \vec{i}_{\text{new}} \vec{i}_{\text{new}}^+ \rangle = \left\langle \begin{bmatrix} i_1 + i'_1 \\ i_2 + i'_2 \end{bmatrix} \begin{bmatrix} i_1^* + i'^*_1 & i_2 i'^*_2 \end{bmatrix} \right\rangle \tag{7.138}$$

$$= \begin{bmatrix} \langle i_1 i_1^* \rangle + \langle i'_1 i'^*_1 \rangle & \langle i_1 i_2^* \rangle + \langle i'_1 i'^*_2 \rangle \\ \langle i_2 i_1^* \rangle + \langle i'_2 i'^*_1 \rangle & \langle i_2 i_2^* \rangle + \langle i'_2 i'^*_2 \rangle \end{bmatrix} \tag{7.139}$$

The noise sources from different two-ports must be uncorrelated, so there are no cross products of different two-ports. By inspection (7.139) is just the addition of the correlation matrices for the individual two-ports, so

$$[C_{y,\text{new}}] = [C_y] + [C'_y] \tag{7.140}$$

The same form holds true for g, h, and z parameters, but $ABCD$ parameters have the more complicated form shown below. If

$$[A_{\text{new}}] = [A][A'] \tag{7.141}$$

then

$$[C_{A,\text{new}}] = [C_A] + [A][C_{A'}][A]^+ \tag{7.142}$$

The transformation of one representation to another is best illustrated by an example. Let us transform the correlation matrix for a Y representation to a Z representation. Starting with

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = [Y] \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{7.143}$$

we can move the noise vector to the left side and invert y:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = [Y^{-1}] \begin{bmatrix} I_1 - i_1 \\ I_2 - i_2 \end{bmatrix} = [Y^{-1}] \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} + [Y^{-1}] \begin{bmatrix} -i_1 \\ -i_2 \end{bmatrix} \tag{7.144}$$

Since $(Y)^{-1} = (Z)$, we have

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = [Z] \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} + [Z] \begin{bmatrix} -i_1 \\ -i_2 \end{bmatrix} \tag{7.145}$$

so

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = [Z] \begin{bmatrix} -i_1 \\ -i_2 \end{bmatrix} = [T_{yz}] \begin{bmatrix} -i_1 \\ -i_2 \end{bmatrix} \tag{7.146}$$

where the signs of i_1 and i_2 are superfluous since they will cancel when the correlation matrix is formed. Here the transformation of the Y noise current vector to the Z noise voltage vector is done simply by multiplying by (Z). Other transformations were given in Table 7.1.

To form the noise correlation matrix, we again form the mean of the outer product:

$$\langle vv^+ \rangle = \begin{bmatrix} \langle v_1 v_1^* \rangle & \langle v_1 v_2^* \rangle \\ \langle v_1^* v_2 \rangle & \langle v_2 v_2^* \rangle \end{bmatrix} = [Z] \quad \left\langle \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \begin{bmatrix} i_1^* & i_2^* \end{bmatrix} \right\rangle \quad [Z]^+ \tag{7.147}$$

or

$$[C_z] = [Z][C_y][Z]^+ \tag{7.148}$$

where

$$v^+ = \begin{bmatrix} i_1^* & i_2^* \end{bmatrix} [Z]^+$$

This is called a congruence transformation. The key to all of these derivations is the construction of the correlation matrix from the noise vector, as shown in (7.139).

These correlation matrices may easily be derived from the circuit matrices of passive circuits with only thermal noise sources. For example,

$$[C_z] = 2kT \ \Delta f \ \text{Re}([Z]) \tag{7.149}$$

$$[C_y] = 2kT \ \Delta f \ \text{Re}([Y]) \tag{7.150}$$

The $2kT$ factor comes from the double-sided spectrum of thermal noise. The correlation matrix for the $ABCD$ matrix may be related to the noise figure, as shown by Hillbrand and Russer [7.13]. We have

$$F = 1 + \frac{\overline{Y}[C_a]\overline{Y}^+}{2kT \ \text{Re}(Y_G)} \tag{7.151}$$

where

$$\overline{Y} = \begin{bmatrix} Y_G \\ 1 \end{bmatrix}$$

The *ABCD* correlation matrix can be written in terms of the noise figure parameters as

$$[C_a] = 2kT \begin{bmatrix} R_n & \dfrac{F_0 - 1}{2} - R_n Y_{on}^* \\ \dfrac{F_0 - 1}{2} - R_n Y_{on} & R_n |Y_{on}|^2 \end{bmatrix} \tag{7.152}$$

The noise correlation matrix method forms an easy and rigorous technique for handling noise in networks. This technique allows us to calculate the total noise for complicated networks by combining the noise matrices of subcircuits. It should be remembered that although noise correlation matrices apply to *n*-port networks, noise figure calculations apply only to pairs of ports. The parameters of the C_a matrix can be used to give the noise parameters:

$$Y_{on} = \sqrt{\frac{C_{ii^*}}{C_{uu^*}} - \left[\text{Im} \left(\frac{C_{ui^*}}{C_{uu^*}} \right) \right]^2} + j \, \text{Im} \left(\frac{C_{ui^*}}{C_{uu^*}} \right) \tag{7.153}$$

$$F_0 = 1 + \frac{C_{ui^*} + C_{uu^*} Y_{on}^*}{kT} \tag{7.154}$$

$$R_n = C_{uu^*} \tag{7.155}$$

7.10 NOISE FIGURE TEST EQUIPMENT

Figure 7.23 shows the block diagram of a noise test setup. It includes the noise source and the other components. The metering unit has a special detector which is linear and over a certain dynamic range measures linear power. The tunable receiver covers a wide frequency range (e.g., 10 to 1800 MHz) and controls the noise source. The receiver is a double-conversion superheterodyne configuration with sufficient image rejection to avoid double-sideband noise measurements that would give the wrong results.
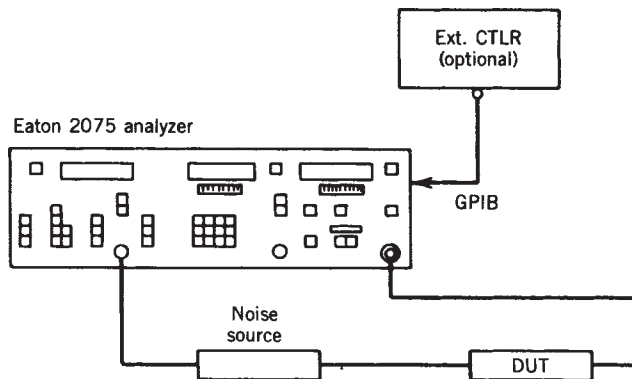
FIGURE 7.23 Noise figure measurement.

These receivers are microprocessor controlled and the measurement is a two-step procedure. The first is a calibration step that measures the noise figure of the receiver system and a reference power level. Then the DUT is inserted and the system noise figure and total output power are measured. The noise factor is calculated by

$$F_1 = F_{\text{system}} - \frac{F_2 - 1}{G_1} \tag{7.156}$$

and the gain is given by the change in output power from the reference level [7.14]. The noise of the system is calculated by measuring the total noise power with the noise source on and off. With the ENR (excess-noise ratio) known [7.14],

$$F_{\text{system}} = \frac{\text{ENR}}{Y - 1} \tag{7.157}$$

The noise bandwidth is usually set by the bandwidth of the receiver, which is assumed to be constant over the linear range. The ENR of the noise source is given by

$$\text{ENR} = \frac{T_{\text{hot}}}{T_{\text{cold}}} - 1 \tag{7.158}$$

where T_{cold} is usually room temperature (290 K). This ENR number is about 15 dB for noise sources with a 15-dB pad and 5 dB for noise sources with a 25-dB pad. Since both gain and noise were stored in the initial calibration, a noise/gain sweep can be performed.

For frequencies above 1800 MHz we can extend the range with the help of the external signal generators, as shown in Figure 7.24. As shown, a filter ahead of the external mixer reduces the noise energy in the image band. If the DUT has a very broad frequency range and has flat gain and noise over that range, a double sideband (DSB) measurement is possible, with the image rejection filter removed. However, a SSB (single-sideband) measurement is always more accurate [7.15].
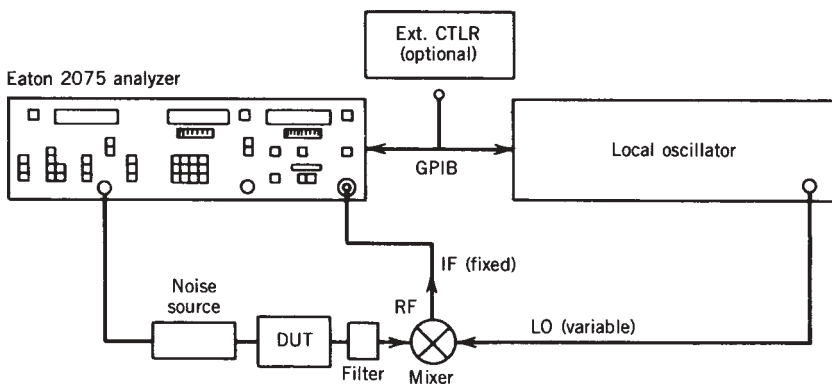
FIGURE 7.24   Single-sideband noise figure measurement using an external mixer.

7.11   HOW TO DETERMINE NOISE PARAMETERS

The noise figure of a linear two-port network as a function of source admittance may be represented by

$$F = F_{\min} + \frac{R_n}{G_G}[(G_{on} - G_G)^2 + (B_{on} - B_G)^2] \tag{7.159}$$

where $G_G + jB_G$ = generator admittance presented to input of two-port

$G_{on} + jB_{on}$ = generator admittance at which optimum noise figure occurs

R_n = empirical constant relating sensitivity of noise figure to generator admittance, with dimensions of resistance

It may be noted that for an arbitrary noise figure measurement with a known generator admittance, Eq. (7.159) has four unknowns, $F_{\min}$, R_n, G_{on}, and B_{on}. By choosing four known values of generator admittance, a set of four linear equations are formed and the solution of the four unknowns can be found [7.16, 7.17]. Equation (7.159) may be transformed to

$$F = F_{\min} + \frac{R_n|Y_{on}|^2}{G_G} - 2R_n G_{on} + \frac{R_n|Y_G|^2}{G_G} - 2R_n B_{on}\frac{B_G}{G_G} \tag{7.160}$$

or

$$F = F_{\min} + \frac{R_n}{G_G}|Y_G - Y_{on}|^2 \tag{7.161}$$

Let

$$X_1 = F_{\min} - 2R_n G_{on} \qquad X_2 = R_n|Y_{on}|^2 \qquad X_3 = R_n \qquad X_4 = R_n B_{on}$$

Then the generalized equation may be written as

$$F_i = X_1 + \frac{1}{G_{si}}X_2 + \frac{|Y_{si}|^2}{G_{si}}X_3 - 2\frac{G_{si}}{B_{si}}X_4 \tag{7.162}$$

or, in matrix form,

$$[F] = [A][X] \tag{7.163}$$

and the solution becomes

$$[X] = [A]^{-1}[F] \tag{7.164}$$

These parameters completely characterize the noise behavior of the linear two-port network. Direct measurement of these noise parameters by this method would be possible only if the receiver on the output of the two-port were noiseless and insensitive to its input admittance. In practice, the receiver itself behaves as a noisy two-port network and can be characterized in the same manner. What is actually being measured is the system noise figure of the two-port and the receiver.

The two-port noise figure can, however, be calculated using the system formula (7.156). It is important to note that F_2 is assumed to be independent of the impedance of the first-stage two-port, which means that an isolator should be inserted

between the first-stage two-port and the receiver. Thus it becomes apparent that to do a complete two-port noise characterization, the system noise characterization, the receiver noise characterization, and the gain of the two-port must be measured [7.18]. In addition, any losses in the input-matching networks must be carefully accounted for, because they add directly to the measured noise figure reading [7.19].

7.12   CALCULATION OF NOISE PROPERTIES OF BIPOLAR AND FETS

7.12.1   Hybrid-Π Configuration [7.22]

Figure 7.25 shows the equivalent schematic of the bipolar transistor in the grounded-emitter configuration. The high-frequency or microwave noise of a silicon bipolar transistor in the common-emitter configuration can be modeled by using the three noise sources as shown in the equivalent schematic (hybrid-Π) in Figure 7.26. The emitter junction in this case is conductive and this generates shot noise on the emitter. The emitter current is divided into a base (I_b) and a collector current (I_c) and both these currents generate shot noise.

There is the collector reverse current (I_{cob}), which also generates shot noise. The emitter, base, and collector are made of semiconductor material and have finite values of resistance associated with them, which generates thermal noise.

The value of the base resistor is relatively high in comparison to the resistance associated with the emitter and collector, so the noise contribution of these resistors can be neglected.

For noise analysis three sources are introduced in a noiseless transistor, and these noise generators are due to fluctuation in dc bias current (i_{bn}), dc collector current (i_{cn}), and the thermal noise of the base resistance.

For the evaluation of the noise performances, the signal-driving source should also be taken into consideration because its internal conductance generates noise and its susceptance affects the noise figure through noise tuning.

In silicon transistors the collector reverse current (I_{cob}) is very small and noise (i_{con}) generated due to this can be neglected.
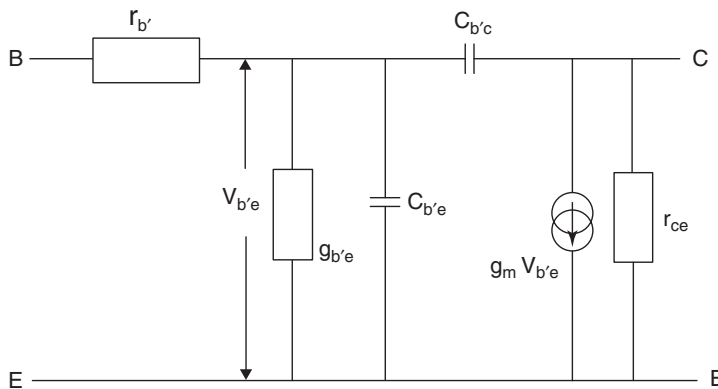
FIGURE 7.25   Π configuration of the CE bipolar transistor.
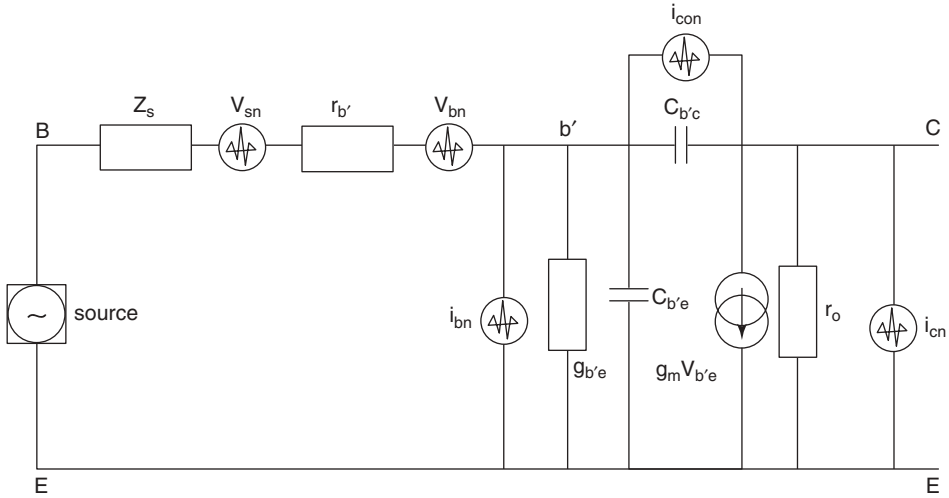
FIGURE 7.26 Π configuration of CE bipolar transistor with noise sources.

The mean-square values of the above noise generators in a narrow frequency interval Δf are given by

$$\overline{i_{bn}^2} = 2qI_b \ \Delta f \tag{7.165}$$

$$\overline{i_{cn}^2} = 2qI_c \ \Delta f \tag{7.166}$$

$$\overline{i_{con}^2} = 2qI_{cob} \ \Delta f \tag{7.167}$$

$$\overline{v_{bn}^2} = 4kTR_b \ \Delta f \tag{7.168}$$

$$\overline{v_{sn}^2} = 4kTR_s \ \Delta f \tag{7.169}$$

where I_b, I_c, and I_{cob} are average dc current over Δf noise bandwidth. The noise power spectral densities due to the noise sources are given as

$$S(i_{cn}) = \frac{\overline{i_{cn}^2}}{\Delta f} = 2qI_c = 2KTg_m \tag{7.170}$$

$$S(i_{bn}) = \frac{\overline{i_{bn}^2}}{\Delta f} = 2qI_b = \frac{2KTg_m}{\beta} \tag{7.171}$$

$$S(v_{bn}) = \frac{\overline{v_{bn}^2}}{\Delta f} = 4KTR_b \tag{7.172}$$

$$S(v_{sn}) = \frac{\overline{v_{sn}^2}}{\Delta f} = 4KTR_s \tag{7.173}$$

where R_b and R_s are base and source resistances and Z_s is the complex source impedance.

(a)

(b)
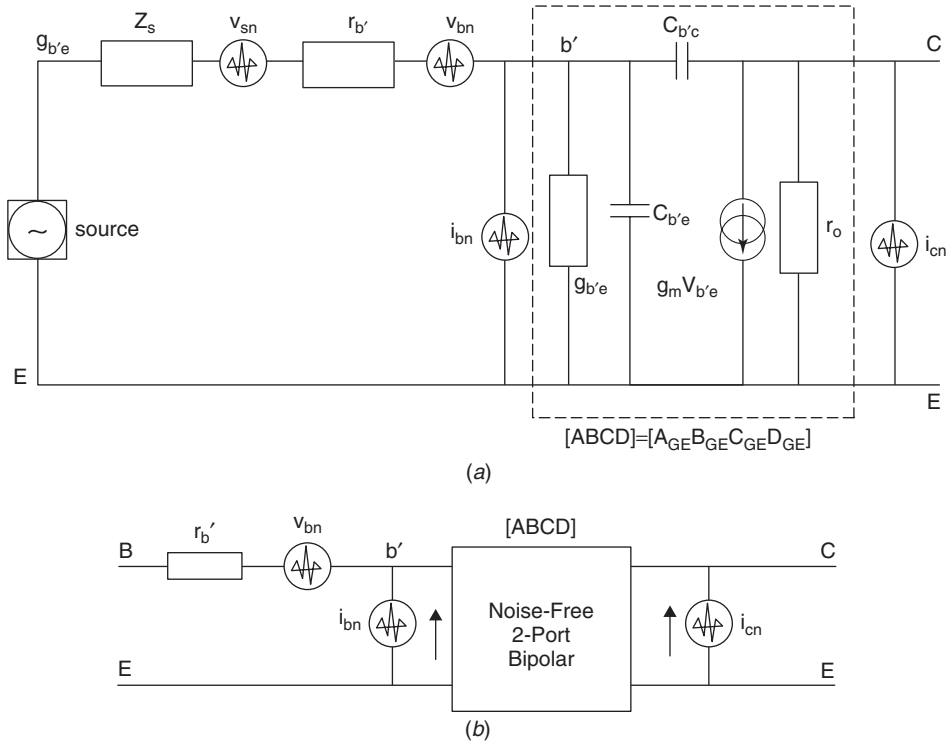
FIGURE 7.27 (a) Π configuration of the bipolar transistor with noise sources. (b) Equivalent [*ABCD*] representation of the intrinsic transistor.

7.12.2 Transformation of Noise Current Source to Input of CE Bipolar Transistor

Figure 7.27a shows the grounded-emitter Π configuration with the noise sources. In a silicon transistor the collector reverse current (I_{cob}) is very small and the noise (i_{con}) generated due to this can be neglected.

Figure 7.27b shows the equivalent [*ABCD*] representation of the intrinsic transistor in terms of the two-port noise-free parameters A_{CE}, B_{CE}, C_{CE}, and D_{CE} [7.22]:

$$[ABCD] = \begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ g_{b'e} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sc_{b'e} & 0 \end{bmatrix}$$

$$\times \begin{bmatrix} \dfrac{sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{1}{sc_{b'c} - g_m} \\ \dfrac{g_m sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{sc_{b'c}}{sc_{b'c} - g_m} \end{bmatrix} \tag{7.174}$$

$$\begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ (g_{b'e} + sc_{b'e}) & 0 \end{bmatrix} \begin{bmatrix} \dfrac{sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{1}{sc_{b'c} - g_m} \\ \dfrac{g_m sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{sc_{b'c}}{sc_{b'c} - g_m} \end{bmatrix} \tag{7.175}$$

$$\begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix} = \begin{bmatrix} \dfrac{sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{1}{sc_{b'c} - g_m} \\ \dfrac{sc_{b'c}(g_m + g_{b'e} + sc_{b'e})}{sc_{b'c} - g_m} & \dfrac{(g_{b'e} + sc_{b'e} + sc_{b'c})}{sc_{b'c} - g_m} \end{bmatrix} \tag{7.176}$$

$$A_{CE} = \frac{sc_{b'c}}{sc_{b'c} - g_m} = \frac{1}{1 - g_m/sc_{b'c}} \tag{7.177}$$

$$B_{CE} = \frac{1}{sc_{b'c} - g_m} = \frac{-1}{g_m - jwc_{b'c}} = -r_e$$

$$= -\frac{1}{g_m} \qquad (wr_e c_{b'c} \ll 1) \tag{7.178}$$

$$C_{CE} = \frac{sc_{b'c}(g_m + g_{b'e} + sc_{b'e})}{sc_{b'c} - g_m} \tag{7.179}$$

$$D_{CE} = \frac{g_{b'e} + sc_{b'e} + sc_{b'c}}{sc_{b'c} - g_m}$$

$$= \left[\frac{(1 + jwr_{b'e}c_{b'e})/r_{b'e} + jwc_{b'c}}{g_m - jwc_{b'c}} \right] \tag{7.180}$$

$$D_{CE} = -\left[\frac{1}{\beta} + j\frac{f}{f_T} \right] \qquad \text{if } (wr_e c_{b'c} \ll 1) \tag{7.181}$$

where

$$\beta = \beta(f) = g_e(f)r_{b'e} \tag{7.182}$$

$$f_T = \left[\frac{g_e}{2\pi(C_{b'c} + C_{b'e})} \right] \tag{7.183}$$

Here, r_0 is normally very large and can be neglected for ease in analysis.

7.12.3 Noise Factor

Figures 7.28*a* and 7.28*b* show the two-port [*ABCD*] and the CE bipolar transistor presentation for the calculation of the noise figure.

The resulting noise voltage $V_{n(\text{network})}$, combining all the noise contribution, is expressed in terms of the chain parameters:

$$V_{n(\text{network})} = V_{bn} + I_{cn}B_{ce} + (I_{bn} + D_{ce}I_{cn})(Z_s + r_b') \tag{7.184}$$

$$V_{n(\text{network})} = V_{bn} + I_{bn}(R_s + r_b') + I_{cn}[B_{ce} + D_{ce}(R_s + r_b')]$$
$$+ j(I_{bn}X_s + I_{cn}D_{ce}) \tag{7.185}$$

$$V_{n(\text{network})} = V_{bn} + I_{bn}(R_s + r_b') + I_{cn}(-r_e)$$
$$+ \left[\frac{1}{\beta} + j\frac{f}{f_T} \right](R_s + r_b') + j(I_{bn}X_s) + j\left[\frac{1}{\beta} + j\frac{f}{f_T} \right]I_{cn} \tag{7.186}$$
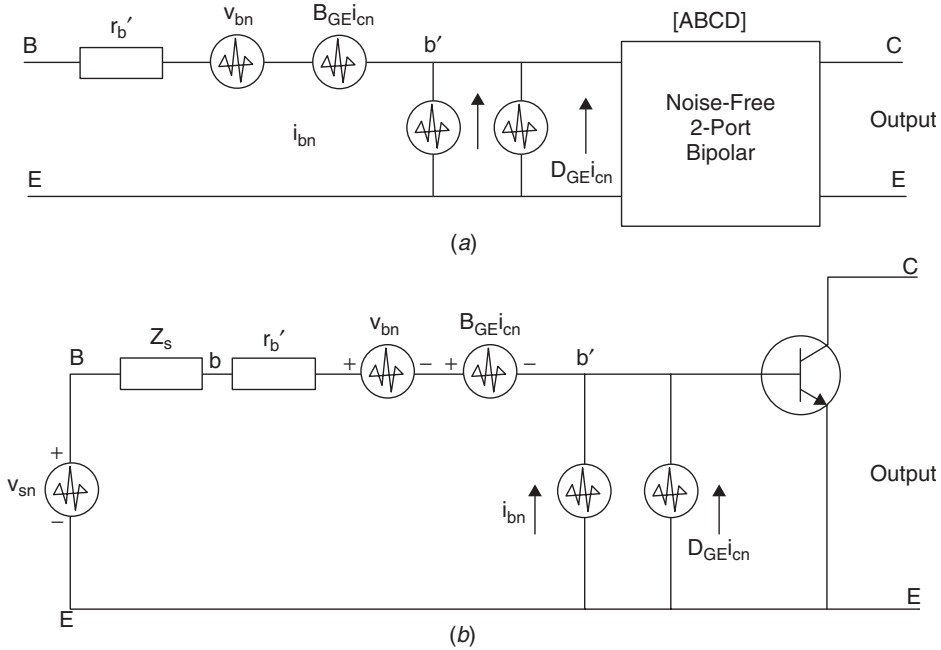
FIGURE 7.28 (*a*) Two-port [*ABCD*] with noise sources transferred to the input. (*b*) CE bipolar with transferred noise sources to the input.

$$V_{n(\text{total})} = V_{sn} + V_{n(\text{network})} \tag{7.187}$$

where $V_{n(\text{total})}$ = total noise voltage
V_{sn} = noise due to source
$V_{n(\text{network})}$ = noise due to network

The noise factor F is the ratio of the total mean-square noise current and the thermal noise generated from the source resistance:

$$F = \frac{\overline{v_{n(\text{total})}^2}}{\overline{v_{sn}^2}} = \frac{\overline{V_{sn}^2} + \overline{V_{\text{network}}^2}}{\overline{V_{sn}^2}} \tag{7.188}$$

$$= \frac{\overline{V_{sn}^2}}{\overline{V_{sn}^2}} + \frac{\overline{V_{\text{network}}^2}}{\overline{V_{sn}^2}} = 1 + \frac{\overline{V_{\text{network}}^2}}{\overline{V_{sn}^2}} \tag{7.189}$$

After substituting the values of V_{sn} and $V_{n(\text{network})}$, noise factor F can be expressed as

$$F = 1 + \frac{\overline{V_{\text{network}}^2}}{\overline{V_{ns}^2}} = \frac{\overline{\left\{ V_{bn} + I_{bn}(R_s + r_b') - r_e I_{cn} - [1/\beta + j(f/f_T)] \atop \times (R_s + r_b')I_{cn} + jI_{bn}X_s + jI_{cn}[1/\beta + j(f/f_T)] \right\}^2}}{4kT \, \Delta f \, R_s} \tag{7.190}$$

$$
\begin{aligned}
&= 1 + \left[\frac{
\begin{array}{c}
\overline{V_{bn}^2} + \overline{I_{bn}^2}(R_s + r_b')^2 + \overline{I_{cn}^2}r_e^2 + \overline{I_{cn}^2}(R_s + r_b')^2(f^2/f_T^2) \\
+ \overline{I_{cn}^2}(R_s + r_b')^2(1/\beta^2) + \overline{I_{bn}^2}(R_s + r_b')(R_s + r_b' + 2r_e)
\end{array}
}{4kT\ \Delta f\ R_s} \right] \\
&\quad + \left[\frac{\overline{I_{bn}^2}X_s^2 + \overline{I_{cn}^2}(1/\beta^2) - \overline{I_{cn}^2}(f^2/f_T^2)}{4kT\ \Delta f\ R_s} \right]
\end{aligned}
\tag{7.191}
$$

7.12.4 Case of Real Source Impedance

In the case of a real source impedance, $X_s = 0$, and noise factor F can be expressed as

$$
F = 1 + \frac{r_b'}{R_s} + \frac{r_e}{2R_s} + \frac{(r_b' + R_s)(r_b' + R_s + 2r_e)}{2r_e\beta R_s} + \frac{(r_b' + R_s)^2}{2r_e R_s \beta^2} + \frac{(r_b' + R_s)^2}{2r_e R_s}\left(\frac{f}{f_T}\right)^2
\tag{7.192}
$$

If $wr_e C_{b'c} \ll 1$ and $\beta \gg 1$, then the noise factor can be further simplified as

$$
F = 1 + \frac{1}{R_s}\left[r_b' + \frac{(r_b' + R_s)^2}{2r_e\beta} + \frac{r_e}{2} + \frac{(r_b' + R_s)^2}{2r_e}\left(\frac{f^2}{f_T^2}\right) \right]
\tag{7.193}
$$

$$
= 1 + \frac{1}{R_s}\left[\langle r_b' \rangle + \left\langle \frac{(r_b' + R_s)^2}{2r_e\beta} \right\rangle + \left\langle \frac{r_e}{2} + \frac{(r_b' + R_s)^2}{2r_e}\left(\frac{f^2}{f_T^2}\right) \right\rangle \right]
\tag{7.194}
$$

where the contribution of the first term is due to the base resistance, the second term is due to the base current, and the last term is due to the collector current.

7.12.5 Formation of Noise Correlation Matrix of CE Bipolar Transistor

Figures 7.29a and 7.29b show the steps for the calculation of the noise correlation matrix [7.22].

Figure 7.29c shows the noise transformation from the output to the input for the calculation of noise parameters:

$$
\begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ g_{b'e} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sc_{b'e} & 0 \end{bmatrix} \begin{bmatrix} \dfrac{sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{1}{sc_{b'c} - g_m} \\ \dfrac{g_m sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{sc_{b'c}}{sc_{b'c} - g_m} \end{bmatrix}
\tag{7.195}
$$

$$
\begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ (g_{b'e} + sc_{b'e}) & 0 \end{bmatrix} \begin{bmatrix} \dfrac{sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{1}{sc_{b'c} - g_m} \\ \dfrac{g_m sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{sc_{b'c}}{sc_{b'c} - g_m} \end{bmatrix}
\tag{7.196}
$$

$$
\begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix} = \begin{bmatrix} \dfrac{sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{1}{sc_{b'c} - g_m} \\ \dfrac{sc_{b'c}(g_m + g_{b'e} + sc_{b'e})}{sc_{b'c} - g_m} & \dfrac{(g_{b'e} + sc_{b'e} + sc_{b'c})}{sc_{b'c} - g_m} \end{bmatrix}
\tag{7.197}
$$
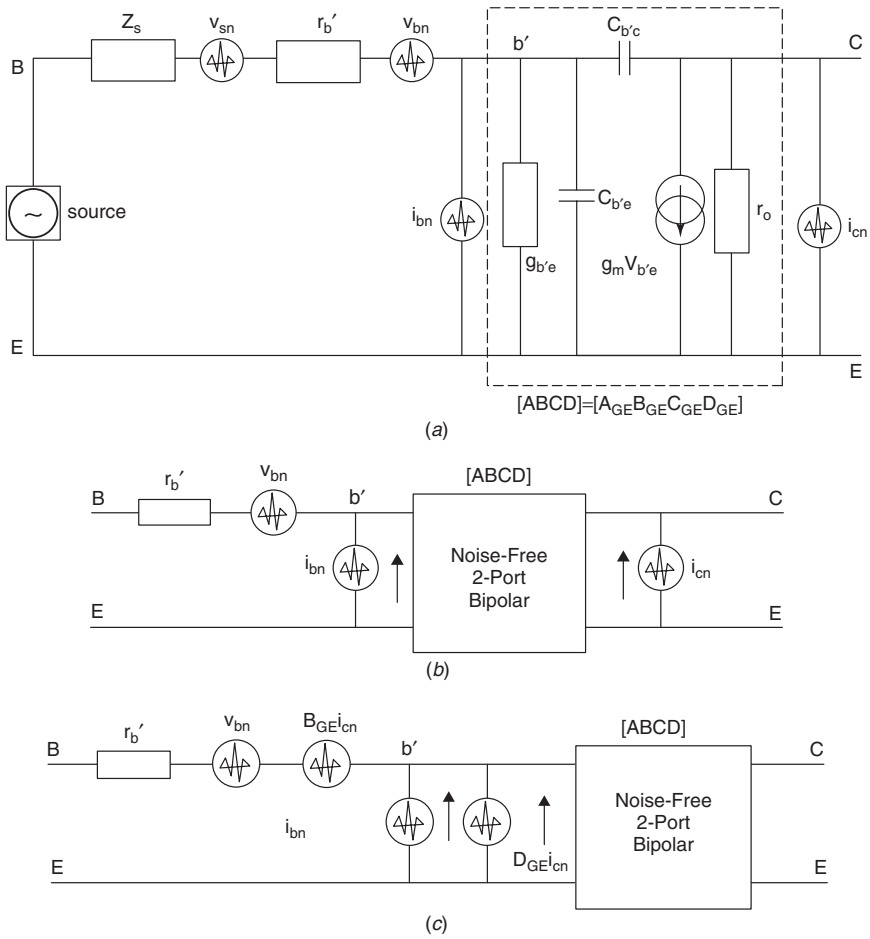
FIGURE 7.29 (*a*) Π configuration of bipolar transistor with noise sources. (*b*) Two-port [*ABCD*] with transferred noise sources to the input. (*c*) Noise transformation from output to input.

$$A_{CE} = \frac{sc_{b'c}}{sc_{b'c} - g_m} = \frac{1}{1 - g_m/sc_{b'c}} \tag{7.198}$$

$$B_{CE} = \frac{1}{sc_{b'c} - g_m} = \frac{-1}{g_m - jwc_{b'c}} = -r_e \tag{7.199}$$

$$= -\frac{1}{g_m} \qquad (wr_ec_{b'c} \ll 1) \tag{7.200}$$

$$C_{CE} = \frac{sc_{b'c}(g_m + g_{b'e} + sc_{b'e})}{sc_{b'c} - g_m} \tag{7.201}$$

$$D_{CE} = \frac{(g_{b'e} + sc_{b'e} + sc_{b'c})}{sc_{b'c} - g_m} = \left[\frac{(1 + jwr_{b'e}c_{b'e})/r_{b'e} + jwc_{b'c}}{g_m - jwc_{b'c}} \right]$$

$$= -\left[\frac{1}{\beta} + j\frac{f}{f_T} \right] \qquad (wr_ec_{b'c} \ll 1) \tag{7.202}$$

$$\beta = \beta(f) = g_e(f)r_{b'e} \qquad f_T = \left[\frac{g_e}{2\pi(C_{b'c} + C_{b'e})}\right]$$

$$r_0 \gg \text{(neglected)} \tag{7.203}$$

The noise transformation to the input using the chain matrix is shown in Figure 7.30. The [ABCD] parameters of the noiseless transistor are given as A_{CE}, B_{CE}, C_{CE}, and D_{CE}. Because only i_{cn} is being transformed from the output port to the input port of the noiseless transistor two-port, A_{CE} and C_{CE} can be ignored.

7.12.6 Calculation of Noise Parameter Ignoring Base Resistance [7.22]

Figures 7.31a and 7.31b show the two uncorrelated noise sources located at its input (i_{bn}) and output (i_{cn}) terminals of the bipolar transistor. This equivalent circuit is analogous to the y representation, so converting the [ABCD] parameter into a [Y] parameter for formation of a noise correlation matrix is as follows:
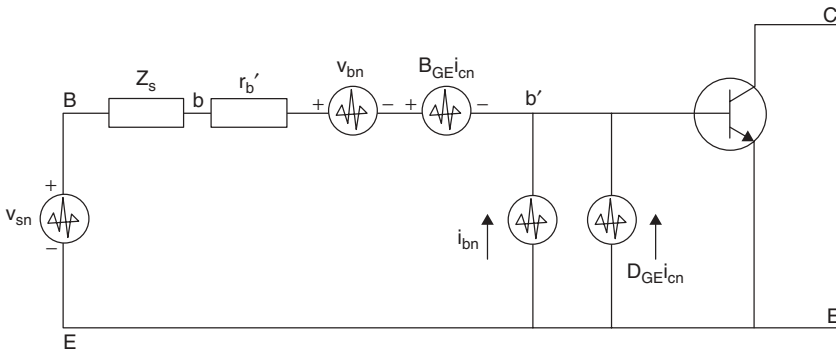
FIGURE 7.30 CE bipolar with transferred noise sources to the input.
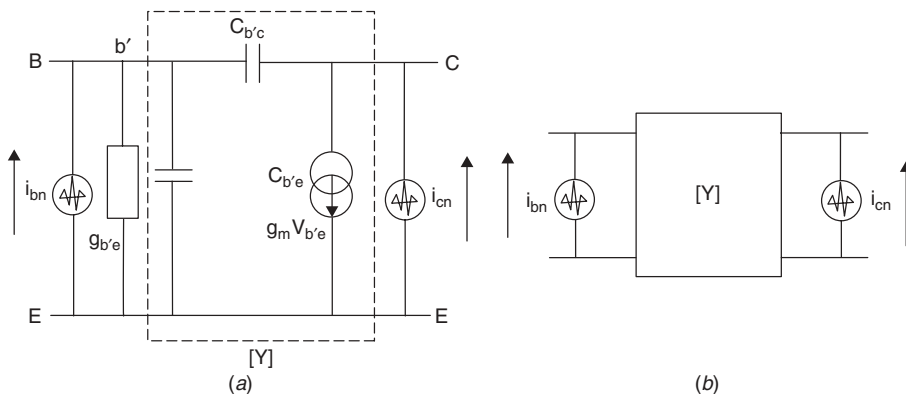
FIGURE 7.31 (a) [Y] representation of intrinsic bipolar. (b) Two-port [Y] representation of intrinsic bipolar transistor.

$$[Y]_{tr} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \tag{7.204}$$

$$y_{11} = \frac{D}{B} = g_{b'e} + s(C_{b'e} + C_{b'c}) \tag{7.205}$$

$$y_{12} = C - \frac{AD}{B} = -sC_{b'c} \tag{7.206}$$

$$y_{21} = -\frac{1}{B} = g_m - sC_{b'c} \tag{7.207}$$

$$y_{22} = \frac{A}{B} = sC_{b'c} \tag{7.208}$$

$$[Y]_{tr} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \tag{7.209}$$

$$[Y]_{tr} = \begin{bmatrix} g_{b'e} + s(C_{b'e} + C_{b'c}) & -sC_{b'c} \\ g_m - sC_{b'c} & sC_{b'c} \end{bmatrix} \tag{7.210}$$

$$[C_Y]_{tr} = [N]_{\text{noise matrix}} = \begin{bmatrix} \overline{i_{bn}i_{bn}^{\bullet}} & \overline{i_{cn}i_{bn}^{\bullet}} \\ \overline{i_{bn}i_{cn}^{\bullet}} & \overline{i_{cn}i_{cn}^{\bullet}} \end{bmatrix} \tag{7.211}$$

$$\overline{i_{bn}i_{cn}^{\bullet}} = 0 \tag{7.212}$$

$$\overline{i_{cn}i_{bn}^{\bullet}} = 0 \tag{7.213}$$

$$\overline{i_{bn}i_{bn}^{\bullet}} = kTg_m\,\Delta f \tag{7.214}$$

$$\overline{i_{cn}i_{cn}^{\bullet}} = \frac{kTg_m\,\Delta f}{\beta} \tag{7.215}$$

$$S(i_{cn}) = qI_c = kTg_m \tag{7.216}$$

$$S(i_{bn}) = qI_b = \frac{kTg_m}{\beta} \tag{7.217}$$

$$[C_Y]_{tr} = [N]_{\text{noise matrix}} = \begin{bmatrix} \overline{i_{bn}i_{bn}^{\bullet}} & \overline{i_{cn}i_{bn}^{\bullet}} \\ \overline{i_{bn}i_{cn}^{\bullet}} & \overline{i_{cn}i_{cn}^{\bullet}} \end{bmatrix} \tag{7.218}$$

$$[C_Y]_{tr} = kT \begin{bmatrix} \dfrac{g_m}{\beta} & 0 \\ 0 & g_m \end{bmatrix} \tag{7.219}$$

$$[C_a]_{tr} = [A][C_Y]_{tr}[A]^+ \tag{7.220}$$

$$[C_a]_{tr} = \begin{bmatrix} 0 & B_{CE} \\ 1 & D_{CE} \end{bmatrix} [C_Y]_{tr} \begin{bmatrix} 0 & 1 \\ B_{CE}^{\bullet} & D_{CE}^{\bullet} \end{bmatrix} \tag{7.221}$$

$$B_{ce} = \frac{-1}{g_m - jwc_{b'c}} = -r_e = -\frac{1}{g_m} \qquad (wr_ec_{b'c} \ll 1) \tag{7.222}$$

$$D_{ce} \to -\left[\frac{1}{\beta} + j\frac{f}{f_T} \right] \qquad (wr_{b'e}c_{b'e} \ll 1) \tag{7.223}$$

$$[C_Y]_{\text{tr}} = kT \begin{bmatrix} \dfrac{g_m}{\beta} & 0 \\ 0 & g_m \end{bmatrix} \tag{7.224}$$

$$[C_a]_{\text{tr}} = kT \begin{bmatrix} \dfrac{1}{g_m} & \dfrac{1}{\beta} + j\dfrac{f}{f_T} \\ \dfrac{1}{\beta} - j\dfrac{f}{f_T} & g_m\left(\dfrac{1}{\beta} + \dfrac{1}{\beta^2} + \dfrac{f^2}{f_T^2}\right) \end{bmatrix} \tag{7.225}$$

$$g_m = Y_{21} + sC_{b'c} \tag{7.226}$$

$$\beta \cong \dfrac{Y_{21}}{Y_{11}} \tag{7.227}$$

$$[C_a]_{\text{tr}} = kT \begin{bmatrix} \dfrac{1}{Y_{21} + sC_{b'c}} & \dfrac{Y_{11}}{Y_{21}} + j\dfrac{f}{f_T} \\ \dfrac{Y_{11}}{Y_{21}} - j\dfrac{f}{f_T} & Y_{21}\left(\dfrac{Y_{11}}{Y_{21}} + \dfrac{Y_{11}^{\,2}}{Y_{21}^{\,2}} + \dfrac{f^2}{f_T^2}\right) \end{bmatrix} \tag{7.228}$$

$$[C_a]_{\text{tr}} = \begin{bmatrix} 0 & -\dfrac{1}{g_m} \\ 1 & -\left(\dfrac{1}{\beta} + j\dfrac{f}{f_T}\right) \end{bmatrix} kT \begin{bmatrix} \dfrac{g_m}{\beta} & 0 \\ 0 & g_m \end{bmatrix}$$

$$\begin{bmatrix} 0 & 1 \\ -\dfrac{1}{g_m} & -\left(\dfrac{1}{\beta} - j\dfrac{f}{f_T}\right) \end{bmatrix} \tag{7.229}$$

From $[C_a]_{\text{tr}}$, the noise parameters are given as

$$[C_a]_{\text{tr}} = \begin{bmatrix} C_{uu^\bullet} & C_{ui^\bullet} \\ C_{u^\bullet i} & C_{ii^\bullet} \end{bmatrix} = \begin{bmatrix} R_n & \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}}^\bullet \\ \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}} & R_n |Y_{\text{opt}}|^2 \end{bmatrix} \tag{7.230}$$

$$R_n = \dfrac{C_{uu^\bullet}}{2kT} = \dfrac{1}{2g_m} \tag{7.231}$$

$$Y_{\text{opt}} = \sqrt{\dfrac{C_{ii^\bullet}}{C_{uu^\bullet}} - \left[\text{Im}\left(\dfrac{C_{ui^\bullet}}{C_{uu^\bullet}}\right)\right]^2} + j\,\text{Im}\left(\dfrac{C_{ui^\bullet}}{C_{uu^\bullet}}\right) \tag{7.232}$$

$$Y_{\text{opt}} = g_m\left(\dfrac{\sqrt{\beta + 1}}{\beta} + j\dfrac{f}{f_T}\right) \Rightarrow g_m\left(\sqrt{\dfrac{1}{\beta}} + j\dfrac{f}{f_T}\right) \qquad \beta \gg 1 \tag{7.233}$$

$$F_{\min} = 1 + \dfrac{C_{ui^\bullet} + C_{uu^\bullet}Y_{\text{opt}}}{kT} \tag{7.234}$$

$$F_{\min} = 1 + \dfrac{1}{\beta} + \dfrac{\sqrt{\beta + 1}}{\beta} \Rightarrow 1 + \dfrac{1}{\sqrt{\beta}} \qquad \beta \gg 1 \tag{7.235}$$

The noise factor F is given as

$$F = 1 + \frac{1}{\beta} + \frac{G_s}{2g_m} + \frac{g_m}{2G_s\beta} + \frac{g_m}{2G_s\beta^2} + \frac{g_m w^2}{2G_s w_T^2} \tag{7.236}$$

$$= F_{\min} + \frac{R_n}{G_g}[(G_{\mathrm{opt}} - G_g)^2 + (B_{\mathrm{opt}} - B_G)^2] \tag{7.237}$$

$$R_b \to 0 \tag{7.238}$$

where Y_g = generator admittance, $= G_g + jB_G$

Y_{opt} = optimum noise admittance, $= G_{\mathrm{opt}} + jB_{\mathrm{opt}}$

$F_{\min}$ = minimum achievable noise figure, $F = F_{\min}$ when $Y_{\mathrm{opt}} = Y_g$

R_n = noise resistance and gives sensitivity of NF to source admittance

For $r_b' > 0$ the resulting $[ABCD]$ matrix is given as

$$\begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix}$$

$$= \begin{bmatrix} 1 & r_b' \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ g_{b'e} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sc_{b'e} & 0 \end{bmatrix} \begin{bmatrix} \dfrac{sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{1}{sc_{b'c} - g_m} \\ \dfrac{g_m sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{sc_{b'c}}{sc_{b'c} - g_m} \end{bmatrix} \tag{7.239}$$

$$\begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix}$$

$$= \begin{bmatrix} 1 & r_b' \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ g_{b'e} + sc_{b'e} & 0 \end{bmatrix} \begin{bmatrix} \dfrac{sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{1}{sc_{b'c} - g_m} \\ \dfrac{g_m sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{sc_{b'c}}{sc_{b'c} - g_m} \end{bmatrix} \tag{7.240}$$

$$\begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix}$$

$$= \begin{bmatrix} 1 & r_b' \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \dfrac{sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{1}{sc_{b'c} - g_m} \\ \dfrac{sc_{b'c}(g_m + g_{b'e} + sc_{b'e})}{sc_{b'c} - g_m} & \dfrac{g_{b'e} + sc_{b'e} + sc_{b'c}}{sc_{b'c} - g_m} \end{bmatrix} \tag{7.241}$$

$$\begin{bmatrix} A_{CE} & B_{CE} \\ C_{CE} & D_{CE} \end{bmatrix}$$

$$= \begin{bmatrix} \dfrac{sc_{b'c}}{sc_{b'c} - g_m} & \dfrac{1}{sc_{b'c} - g_m} \\ + \dfrac{r_b' sc_{b'c}(g_m + g_{b'e} + sc_{b'e})}{sc_{b'c} - g_m} & + \dfrac{r_b'(g_{b'e} + sc_{b'e} + sc_{b'c})}{(sc_{b'c} - g_m)} \\[2mm] \dfrac{sc_{b'c}(g_m + g_{b'e} + sc_{b'e})}{sc_{b'c} - g_m} & \dfrac{g_{b'e} + sc_{b'e} + sc_{b'c}}{(sc_{b'c} - g_m)} \end{bmatrix} \tag{7.242}$$

$$[C_Y]_{\text{tr}} = kT \begin{bmatrix} \dfrac{g_m}{\beta} & 0 \\ 0 & g_m \end{bmatrix} \tag{7.243}$$

$$[C_a]_{\text{tr}} = \begin{bmatrix} 0 & \dfrac{1}{sc_{b'c} - g_m} + \dfrac{r_b'(g_{b'e} + sc_{b'e} + sc_{b'c})}{sc_{b'c} - g_m} \\ 1 & \dfrac{g_{b'e} + sc_{b'e} + sc_{b'c}}{sc_{b'c} - g_m} \end{bmatrix} kT \begin{bmatrix} \dfrac{g_m}{\beta} & 0 \\ 0 & g_m \end{bmatrix} \tag{7.244}$$

$$\times \begin{bmatrix} 0 & 1 \\ \left(\dfrac{1}{sc_{b'c} - g_m} + \dfrac{r_b'(g_{b'e} + sc_{b'e} + sc_{b'c})}{sc_{b'c} - g_m} \right)^{\bullet} & \left(\dfrac{g_{b'e} + sc_{b'e} + sc_{b'c}}{sc_{b'c} - g_m} \right)^{\bullet} \end{bmatrix} \tag{7.245}$$

$$[C_a]_{\text{tr}} = \begin{bmatrix} C_{uu^{\bullet}} & C_{ui^{\bullet}} \\ C_{u^{\bullet}i} & C_{ii^{\bullet}} \end{bmatrix} = \begin{bmatrix} R_n & \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}}^{\bullet} \\ \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}} & R_n |Y_{\text{opt}}|^2 \end{bmatrix} \tag{7.246}$$

$$C_{uu^{\bullet}} = kT \left[2r_b' \left(1 + \frac{1}{\beta} \right) + \frac{1}{g_m} + g_m (r_b')^2 \left(\frac{1}{\beta^2} + \frac{f^2}{f_T^2} \right) \right] \tag{7.247}$$

$$C_{ui^{\bullet}} = kT \left[\frac{1}{\beta} + g_m r_b' \left(\frac{1}{\beta^2} + \frac{f^2}{f_T^2} \right) - j \frac{f}{f_T} \right] \tag{7.248}$$

$$C_{u^{\bullet}i} = kT \left[\left\{ 1 + \frac{g_m r_b'}{\beta} + \frac{1}{g_m \beta} + r_b' \left(\frac{1}{\beta^2} + \frac{f^2}{f_T^2} \right) \right\} \right.$$

$$\left. - j \left\{ g_m r_b' \frac{f}{f_T} - \frac{f}{g_m f_T} \right\} \right] \tag{7.249}$$

$$C_{ii^{\bullet}} = kT \left[\frac{g_m}{\beta} + g_m \left(\frac{1}{\beta^2} + \frac{f^2}{f_T^2} \right) \right] \tag{7.250}$$

$$[C_a]_{\text{tr}} = [A][C_Y]_{\text{tr}}[A]^+ \tag{7.251}$$

$$[C_a]_{\text{tr}} = \begin{bmatrix} 0 & B_{CE} \\ 1 & D_{CE} \end{bmatrix} [C_Y]_{\text{tr}} \begin{bmatrix} 0 & 1 \\ B_{CE}^{\bullet} & D_{CE}^{\bullet} \end{bmatrix} \tag{7.252}$$

$$R_n = \frac{C_{uu^{\bullet}}}{2kT} \tag{7.253}$$

$$R_n = r_b' \left(1 + \frac{1}{\beta} \right) + \frac{1}{2g_m} + \frac{g_m (r_b')^2}{2} \left(\frac{1}{\beta^2} + \frac{f^2}{f_T^2} \right)$$

$$= R_b \left(1 + \frac{1}{\beta} \right) + \frac{kT}{2qI_C} + \frac{qI_C (r_b')^2}{2kT} \left(\frac{1}{\beta^2} + \frac{f^2}{f_T^2} \right) \tag{7.254}$$

$$Y_{\text{opt}} = \sqrt{\frac{C_{ii\bullet}}{C_{uu\bullet}} - \left[\text{Im}\left(\frac{C_{ui\bullet}}{C_{uu\bullet}}\right)\right]^2} + j \, \text{Im}\left(\frac{C_{ui\bullet}}{C_{uu\bullet}}\right) \tag{7.255}$$

$$Y_{\text{opt}} = G_{\text{opt}} + jB_{\text{opt}} \tag{7.256}$$

$$Y_{\text{opt}} = \frac{\begin{array}{c}[1/\beta^2 + 2g_m r_b'(1+1/\beta)(1/\beta^2 + f^2/f_T^2) \\ + (g_m r_b')^2(1/\beta^2 + f^2/f_T^2)^2]^{1/2} + j(f/f_T)\end{array}}{1/g_m + 2r_b'(1+1/\beta) + g_m(r_b')^2(1/\beta^2 + f^2/f_T^2)} \tag{7.257}$$

$$G_{\text{opt}} = \frac{\begin{array}{c}[1/\beta^2 + 2g_m r_b'(1+1/\beta)(1/\beta^2 + f^2/f_T^2) \\ + (g_m r_b')^2(1/\beta^2 + f^2/f_T^2)^2]^{1/2}\end{array}}{1/g_m + 2r_b'(1+1/\beta) + g_m(r_b')^2(1/\beta^2 + f^2/f_T^2)} \tag{7.258}$$

$$B_{\text{opt}} = \frac{f/f_T}{1/g_m + 2r_b'(1+1/\beta) + g_m(r_b')^2(1/\beta^2 + f^2/f_T^2)} \tag{7.259}$$

$$Z_{\text{opt}} = \frac{1}{Y_{\text{opt}}} = \frac{1/g_m + 2r_b'(1+1/\beta) + g_m(r_b')^2(1/\beta^2 + f^2/f_T^2)}{\begin{array}{c}[1/\beta^2 + 2g_m r_b'(1+1/\beta)(1/\beta^2 + f^2/f_T^2) \\ + (g_m r_b')^2(1/\beta^2 + f^2/f_T^2)^2]^{1/2} + j(f/f_T)\end{array}} \tag{7.260}$$

$$Z_{\text{opt}} = R_{\text{opt}} + jX_{\text{opt}} \tag{7.261}$$

$$Z_{\text{opt}} = \frac{\begin{array}{c}[1/g_m + 2r_b'(1+1/\beta) + g_m(r_b')^2(1/\beta^2 + f^2/f_T^2)] \\ \times \{[1/\beta^2 + 2g_m r_b'(1+1/\beta)(1/\beta^2 + f^2/f_T^2) \\ + (g_m r_b')^2(1/\beta^2 + f^2/f_T^2)^2]^{1/2} - j(f/f_T)\}\end{array}}{\begin{array}{c}1/\beta^2 + 2g_m r_b'(1+1/\beta)(1/\beta^2 + f^2/f_T^2) \\ + (g_m r_b')^2(1/\beta^2 + f^2/f_T^2)^2 + (f/f_T)^2\end{array}} \tag{7.262}$$

$$R_{\text{opt}} = \frac{\begin{array}{c}[1/g_m + 2r_b'(1+1/\beta) + g_m(r_b')^2(1/\beta^2 + f^2/f_T^2)] \\ \times [1/\beta^2 + 2g_m r_b'(1+1/\beta)(1/\beta^2 + f^2/f_T^2) \\ + (g_m r_b')^2(1/\beta^2 + f^2/f_T^2)^2]^{1/2}\end{array}}{\begin{array}{c}1/\beta^2 + 2g_m r_b'(1+1/\beta)(1/\beta^2 + f^2/f_T^2) \\ + (g_m r_b'^2(1/\beta^2 + f^2/f_T^2)^2 + (f/f_T)^2\end{array}} \tag{7.263}$$

$$X_{\text{opt}} = \frac{(f/f_T)[1/g_m + 2r_b'(1+1/\beta) + g_m(r_b')^2(1/\beta^2 + f^2/f_T^2)]}{\begin{array}{c}1/\beta^2 + 2g_m r_b'(1+1/\beta)(1/\beta^2 + f^2/f_T^2) \\ + (g_m r_b')^2(1/\beta^2 + f^2/f_T^2)^2 + (f/f_T)^2\end{array}} \tag{7.264}$$

$$\Gamma_{\text{opt}} = \frac{Z_{\text{opt}} - Z_0}{Z_{\text{opt}} + Z_0} \qquad \Gamma_{\text{opt}} = \frac{Y_{\text{opt}} - Y_0}{Y_{\text{opt}} + Y_0} \tag{7.265}$$

$$F = F_{\min} + \frac{R_n}{G_g}[(G_{\text{opt}} - G_g)^2 + (B_{\text{opt}} - B_G)^2] \tag{7.266}$$

$$F_{\min} = 1 + \frac{C_{ui\bullet} + C_{uu\bullet}Y_{\text{opt}}}{kT} \tag{7.267}$$

$$= \left(1 + \frac{1}{\beta}\right)(1 + r_b'G_s) + \frac{G_s}{2g_m} + \frac{g_m G_s}{2}\left(r_b' + \frac{1}{G_s}\right)^2\left(\frac{1}{\beta^2} + \frac{f^2}{f_T^2}\right) \tag{7.268}$$

$$F = 1 + \frac{1}{R_s}\left[R_b + \frac{r_e}{2} + \frac{(R_b + R_s)(R_b + R_s + 2r_e)}{2r_e\beta} + \frac{(R_b + R_s)^2}{2r_e\beta^2}\right.$$
$$\left. + \frac{(R_b + R_s)^2}{2r_e}\left(\frac{f^2}{f_T^2}\right)\right] \tag{7.269}$$

If $wr_eC_{b'c} \ll 1$ and $\beta \gg 1$, then the noise factor can be further simplified to

$$F = 1 + \frac{1}{R_s}\left[R_b + \frac{(R_b + R_s)^2}{2r_e\beta} + \frac{r_e}{2} + \frac{(R_b + R_s)^2}{2r_e}\left(\frac{f^2}{f_T^2}\right)\right] \tag{7.270}$$

$$F_{\min} = \left(1 + \frac{1}{\beta}\right)(1 + r_b'G_s) + \frac{G_s}{2g_m} + \frac{g_mG_s}{2}\left(r_b' + \frac{1}{G_s}\right)^2\left(\frac{1}{\beta^2} + \frac{f^2}{f_T^2}\right)$$

$$\Rightarrow 1 + \frac{1}{\sqrt{\beta}} \qquad \beta \gg 1 \tag{7.271}$$

where

$$\beta = \beta(f) = g_e(f)r_{b'e} \tag{7.272}$$

$$= \frac{\alpha}{1 - \alpha} = \frac{\alpha_0 \exp(-jw\tau)}{1 + j(f/f_\alpha) - \alpha_0 \exp(-jw\tau)}$$

$$= \frac{1}{(1/\alpha_0)\exp(jw\tau) + j(f/\alpha_0 f_\alpha)\exp(jw\tau) - 1} \tag{7.273}$$

$$= \frac{\beta_0}{1 + j\beta_0(f/f_T)} \tag{7.274}$$

$$\alpha = \frac{\alpha_0\exp(-jw\tau)}{1 + j(f/f_\alpha)} \qquad \beta_0 = \frac{\alpha_0}{1 - \alpha_0} \tag{7.275}$$

$$g_e(f \rightarrow \text{low freq.}) = g_{e0} \qquad g_{e0} = \frac{1}{r_{e0}} \tag{7.276}$$

$$r_{e0} = \left(\frac{\partial I_E}{\partial V_{EB}}\right)^{-1} = \left(\frac{KT}{qI_E}\right)\left(\frac{\alpha_0}{\alpha_{DC}}\right) = \left(\frac{KT}{qI_C}\right)\alpha_0 \tag{7.277}$$

$$f_T = \frac{g_e}{2\pi(C_{b'c} + C_{b'e})} \tag{7.278}$$

7.13   BIPOLAR TRANSISTOR NOISE MODEL IN T CONFIGURATION

Figure 7.32 shows the T-equivalent circuit of the bipolar noise model with C_{Te} the emitter junction capacitance and Z_g is the complex source impedance [7.22].

For the calculation of the minimum noise figure, the T configuration is simpler than the hybrid-Π. For the formation of the noise correlation matrix with the base collector capacitance, the C_{bc}, the hybrid-Π topology is an easier approach for analysis. The noise of a silicon bipolar transistor can be modeled by the three noise sources shown
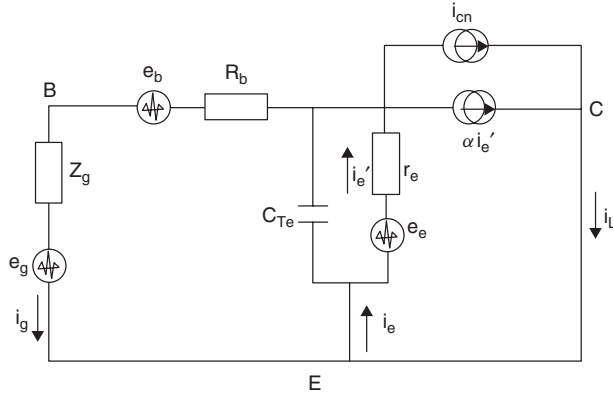
FIGURE 7.32   T-equivalent circuit of bipolar noise model.

in Figure 7.26. The mean-square values of noise sources in a narrow frequency range Δf are given as

$$\overline{e_e e_e^*} = \overline{e_e^2} = 2KTr_e \ \Delta f \tag{7.279}$$

$$\overline{e_g e_g^*} = \overline{e_g^2} = 4KTR_g \ \Delta f \tag{7.280}$$

$$\overline{e_b e_b^*} = \overline{e_b^2} = 4KTR_b \ \Delta f \tag{7.281}$$

$$\overline{i_{cp} e_e^*} = 0 \tag{7.282}$$

$$\alpha = \frac{\alpha_0}{1 + j(f/f_b)} \tag{7.283}$$

$$\beta = \frac{\alpha}{1 - \alpha} \tag{7.284}$$

$$r_e = \frac{KT}{qI_e} \tag{7.285}$$

$$g_e = \frac{1}{r_e} \tag{7.286}$$

where the thermal noise voltage source due to base resistance is e_b, the shot noise voltage source e_e is generated by the forward-biased emitter–base junction r_e, and the collector noise current source i_{cp} comes from the collector partition, which is strongly correlated to the emitter–base shot noise.

The definition of the noise factor is the ratio of the output noise power to that from a noiseless but otherwise identical device:

The noise factor F is given by

$$F = \frac{\overline{i_L^2}}{\overline{i_{L0}^2}} \tag{7.287}$$

where i_{L0} is the value of i_L due to the source generator e_g alone. From KVL, for the loop containing Z_g, r_b, and r_e, the loop equations can be expressed as

$$i_g(Z_g + r_b) + i'_e r_e = e_g + e_b + e_e \tag{7.288}$$

$$i_L = \alpha i'_e + i_{cp} \tag{7.289}$$

$$i'_e = \frac{i_L - i_{cp}}{\alpha} \tag{7.290}$$

$$i_e = i'_e(1 + jwC_{Te}) - jwC_{Te}e_e \tag{7.291}$$

$$i_g = i_e - i_L \tag{7.292}$$

$$i_g = i'_e(1 + jwC_{Te}r_e) - jwC_{Te}e_e - i_L \tag{7.293}$$

$$i_g = \frac{i_L - i_{cp}}{\alpha}(1 + jwC_{Te}r_e) - jwC_{Te}e_e - i_L \tag{7.294}$$

$$i_g(Z_g + r_b) + i'_e r_e = e_g + e_b + e_e \tag{7.295}$$

$$\left(\frac{i_L - i_{cp}}{\alpha}(1 + jwC_{Te}r_e) - jwC_{Te}e_e - i_L\right)(Z_g + r_b) + \left(\frac{i_L - i_{cp}}{\alpha}\right)r_e$$
$$= e_g + e_b + e_e \tag{7.296}$$

$$\frac{i_L}{\alpha}[(1 - \alpha + jwC_{Te}r_e)(Z_g + r_b) + r_e]$$
$$= e_g + e_b + e_e[1 + jwC_{Te}(Z_g + r_b)]$$
$$+ \frac{i_{cp}}{\alpha}[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e] \tag{7.297}$$

$$i_L = \alpha \left[\frac{\begin{array}{c} e_g + e_b + e_e[1 + jwC_{Te}(Z_g + r_b)] \\ + \dfrac{i_{cp}}{\alpha}[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e] \end{array}}{(1 - \alpha + jwC_{Te}r_e)(Z_g + r_b) + r_e} \right] \tag{7.298}$$

where i_L is the total load current or collector current (ac short-circuited current) due to all the generators such as e_e, e_b, e_g, and i_{cp}.

Let i_{L0} be the value of i_L due to the source generator e_g alone and other noise generators (e_e, e_b, e_g, and i_{cp}) are zero:

$$i_{L0} = \alpha \left[\frac{e_g}{(1 - \alpha + jwC_{Te}r_e)(Z_g + r_b) + r_e} \right] \tag{7.299}$$

$$F = \frac{\overline{i_L^2}}{\overline{i_{L0}^2}} = \frac{\overline{\left\{ \begin{array}{c} e_g + e_b + e_e[1 + jwC_{Te}(Z_g + r_b)\cdots] \\ +(i_{cp}/\alpha)[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e] \end{array} \right\}^2}}{\overline{e_g^2}} \tag{7.300}$$

$$= \frac{\overline{e_g^2} + \overline{e_b^2} + \overline{e_e^2[1 + jwC_{Te}(Z_g + r_b)]^2}}{\overline{e_g^2}} \tag{7.301}$$
$$\frac{+(i_{cp}^2/|\alpha|^2)[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e]^2}{\overline{e_g^2}}$$

$$
\begin{aligned}
= \frac{\begin{array}{l} 4KTR_g + 4KTr_b + 2KTr_e\overline{[1 + jwC_{Te}(Z_g + r_b)]^2} \\ +[2KT(\alpha_0 - |\alpha|^2)/|\alpha|^2 r_e]\overline{[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e]^2} \end{array}}{4KTR_g}
\end{aligned}
\tag{7.302}
$$

$$
\begin{aligned}
= 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}\overline{[1 + jwC_{Te}(Z_g + r_b)]^2} \\
+ \frac{(\alpha_0 - |\alpha|^2)}{2R_g|\alpha|^2 r_e}\overline{[(1 + jwC_{Te}r_e)(Z_g + r_b) + r_e]^2}
\end{aligned}
\tag{7.303}
$$

$$
\begin{aligned}
= 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}|1 + jwC_{Te}(R_g + r_b + jX_g)|^2 \\
+ \left(\frac{\alpha_0}{|\alpha|^2} - 1\right)\frac{|(1 + jwC_{Te}r_e)(R_g + r_b + jX_g) + r_e|^2}{2R_g r_e}
\end{aligned}
\tag{7.304}
$$

$$
\begin{aligned}
= 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}|1 + jwC_{Te}(R_g + r_b) - wC_{Te}X_g|^2 \\
+ \left(\frac{\alpha_0}{|\alpha|^2} - 1\right)\frac{|R_g + r_b + r_e - wC_{Te}X_g r_e + jwC_{Te}r_e(R_g + r_b + X_g)|^2}{2R_g r_e}
\end{aligned}
\tag{7.305}
$$

$$
\begin{aligned}
= 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}[(1 - wC_{Te}X_g)^2 + w^2C_{Te}^2(R_g + r_b)^2] \\
+ \left(\frac{\alpha_0}{|\alpha|^2} - 1\right)\frac{[R_g + r_b + r_e(1 - wC_{Te}X_g)]^2 + [(X_g + wC_{Te}e_e(R_g + r_b)]^2}{2R_g r_e}
\end{aligned}
\tag{7.306}
$$

$$
\begin{aligned}
= 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g} + \left(\frac{\alpha_0}{|\alpha|^2} - 1\right)\frac{(R_g + r_b + r_e)^2 + X_g^2}{2R_g r_e} \\
+ \left(\frac{\alpha_0}{|\alpha|^2}\right)\left(\frac{r_e}{2R_g}\right)[w^2C_{Te}^2X_g^2 - 2wC_{Te}X_g + w^2C_{Te}^2(R_g + r_b)^2]
\end{aligned}
\tag{7.307}
$$

The noise terms and the generator thermal noise are given as ($\Delta f = 1$ Hz)

$$
\overline{e_e^2} = 2KTr_e
\tag{7.308}
$$

$$
\overline{e_g^2} = 4KTR_g
\tag{7.309}
$$

$$
\overline{e_b^2} = 4KTR_b
\tag{7.310}
$$

$$
\overline{i_{cp}^2} = \frac{2KT(\alpha_0 - |\alpha|^2)}{r_e}
\tag{7.311}
$$

$$
r_e = \frac{KT}{qI_e}
\tag{7.312}
$$

$$
\alpha = \frac{\alpha_0}{1 + j\dfrac{f}{f_b}}
\tag{7.313}
$$

7.13.1 Real Source Impedance

In the case of a real source impedance, rather than a complex one, for example, $R_g = 50\ \Omega$, $X_g = 0$, the equation of the noise factor becomes [7.22]

$$F = 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g} + + \left(\frac{\alpha_0}{|\alpha|^2} - 1\right) \frac{(R_g + r_b + r_e)^2}{2R_g r_e} + \frac{\alpha_0}{|\alpha|^2} w^2 C_{Te}^2 r_e^2 \frac{(R_g + r_b)^2}{2R_g r_e}$$
(7.314)

Substituting the value of α where f_b is the cutoff frequency of the base alone and introducing an emitter cutoff frequency $f_e = 1/2\pi C T_e r_e$,

$$F = 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g} + + \left(1 - \alpha_0 + \frac{f^2}{f_b^2}\right) \frac{(R_g + r_b + r_e)^2}{2R_g r_e \alpha_0}$$
$$+ \left(1 + \frac{f^2}{f_b^2}\right) \frac{f^2}{f_e^2} \frac{(R_g + r_b)^2}{2R_g r_e \alpha_0}$$
(7.315)

Simplifying the equation above by f_e',

$$f_e' = f_e \frac{R_g + r_b + r_e}{R_g + r_b} = \frac{R_g + r_b + r_e}{2\pi C_{Te} r_e (R_g + r_b)}$$
(7.316)

The simplified equation of the noise factor for the real source impedance is given by

$$F = 1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g} + \left[\left(1 + \frac{f^2}{f_b^2}\right)\left(1 + \frac{f^2}{f_e'^2}\right) - \alpha_0\right] \frac{(R_g + r_b + r_e)^2}{2R_g r_e \alpha_0}$$
(7.317)

7.13.2 Minimum Noise Factor

The minimum noise factor $F_{\min}$ and the corresponding optimum source impedance $Z_{\mathrm{opt}} = R_{\mathrm{opt}} + jX_{\mathrm{opt}}$ are found by differentiating the general equation of the noise figure with respect to X_g and then R_g [7.22].

The equation of the noise factor can be expressed as

$$F = A + BX_g + CX_g^2$$
(7.318)

We determine

$$a = \left(1 - \frac{|\alpha|^2}{\alpha_0} + w^2 C_{Te}^2 r_e^2\right) \frac{\alpha_0}{|\alpha|^2}$$
(7.319)

The coefficients A, B, and C can be expressed as

$$A = a\frac{(R_g + r_b)^2}{2R_g r_e} + \frac{\alpha_0}{|\alpha|^2}\left(1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}\right)$$
(7.320)

$$B = -\frac{\alpha_0}{|\alpha|^2} \frac{wC_{Te} r_e}{R_g}$$
(7.321)

$$C = \frac{a}{2r_e R_g}$$
(7.322)

Differentiating with respect to X_g for the optimum source reactance,

$$\left.\frac{dF}{dX_g}\right|_{X_{\text{opt}}} = B + 2CX_{\text{opt}} \tag{7.323}$$

$$X_{\text{opt}} = \frac{-B}{2C} = \frac{\alpha_0}{|\alpha|^2}\frac{wC_{Te}r_e}{a} \tag{7.324}$$

The corresponding noise factor is

$$F_{X_{\text{opt}}} = A - CX_{\text{opt}}^2 \tag{7.325}$$

$$F_{X_{\text{opt}}} = a\frac{(R_g + r_b)^2}{2R_g r_e} + \frac{\alpha_0}{|\alpha|^2}\left(1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}\right) - \frac{aX_{\text{opt}}^2}{2r_e R_g} \tag{7.326}$$

This must be further optimized with respect to the source resistance to get F_{min}.

Differentiating $F_{X_{\text{opt}}}$ with respect to the source resistance, we get

$$F_{X_{\text{opt}}} = a\frac{(R_g + r_b)^2}{2R_g r_e} + \frac{\alpha_0}{|\alpha|^2}\left(1 + \frac{r_b}{R_g} + \frac{r_e}{2R_g}\right) - \frac{aX_{\text{opt}}^2}{2r_e R_g} \tag{7.327}$$

$$= A_1 + \frac{B_1}{R_g} + C_1 R_g \tag{7.328}$$

where

$$A_1 = a\frac{r_b}{r_e} + \frac{\alpha_0}{|\alpha|^2} \tag{7.329}$$

$$B_1 = a\frac{r_b^2 - X_{\text{opt}}^2}{2r_e} + \frac{\alpha_0}{|\alpha|^2}\left(r_b + \frac{r_e}{2}\right) \tag{7.330}$$

$$C_1 = \frac{a}{2r_e} \tag{7.331}$$

Differentiating the noise factor with respect to R_g to obtain the minimum noise figure yields

$$\left.\frac{dF}{dR_g}\right|_{R_{\text{opt}}} = 0 = \frac{-B_1}{R_{\text{opt}}^2} + C_1 \tag{7.332}$$

$$R_{\text{opt}}^2 = \frac{B_1}{C_1} = r_b^2 - X_{\text{opt}}^2\frac{\alpha_0}{|\alpha|^2}\frac{r_e(2r_b + r_e)}{a} \tag{7.333}$$

$$F_{\text{min}} = A_1 + 2C_1 R_{\text{opt}} = a\frac{r_b + R_{\text{opt}}}{r_e} + \frac{\alpha_0}{|\alpha|^2} \tag{7.334}$$

The factor a can be simplified in terms of a simple symmetrical function of f_e and f_b:

$$a = \left(1 - \frac{|\alpha|^2}{\alpha_0} + w^2 C_{Te}^2 r_e^2\right)\frac{\alpha_0}{|\alpha|^2} \tag{7.335}$$

$$= \left[1 + \frac{f^2}{f_b^2} - \alpha_0 + \left(1 + \frac{f^2}{f_b^2} \right) \frac{f^2}{f_e^2} \right] \frac{1}{\alpha_0} \tag{7.336}$$

$$= \left[\left(1 + \frac{f^2}{f_b^2} \right) \left(1 + \frac{f^2}{f_b^2} \right) - \alpha_0 \right] \frac{1}{\alpha_0} \tag{7.337}$$

If C_{Te} and X_{opt} are assumed to be zero, then the modified factor a can be given as

$$a = \left(1 + \frac{f^2}{f_b^2} - \alpha_0 \right) \frac{1}{\alpha_0} \tag{7.338}$$

$$R_{opt}^2 = \frac{B_1}{C_1} = r_b^2 + \frac{1 + f^2/f_b^2}{1 + f^2/f_b^2 - \alpha_0} \frac{r_e(2r_b + r_e)}{a} \tag{7.339}$$

$$F_{min} = A_1 + 2C_1 R_{opt} = a \frac{r_b + R_{opt}}{r_e} + \frac{\alpha_0}{|\alpha|^2} \tag{7.340}$$

$$= \left(1 + \frac{f^2}{f_b^2} - \alpha_0 \right) \frac{(r_b + R_{opt})}{\alpha_0 r_e} + \left(1 + \frac{f^2}{f_b^2} \right) \frac{1}{\alpha_0} \tag{7.341}$$

7.13.3   Noise Correlation Matrix of Bipolar Transistor in T-Equivalent Configuration

Figure 7.33 shows the T-equivalent configuration of the common-emitter circuit for the transistor. To apply the noise correlation matrix approach, we transform the noise model to an equivalent one consisting of two noise sources, a voltage source and a current source of a noiseless transistor [7.22].

The new bipolar transistor noise model from Figure 7.27 now takes the form shown in Figure 7.34. Since the system is linear, the two noise sources can be expressed in terms of three original noise sources by a linear transformation:

$$[Y]_{tr} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \tag{7.342}$$

$$= \begin{bmatrix} [(1 - \alpha)g_e + jwC_e + Y_c] & -Y_c \\ \alpha g_e - Y_c & Y_c \end{bmatrix} \tag{7.343}$$

Now for easier representation, the matrix for the intrinsic device is defined as $[N]$ and for the transformed noise circuit as $[C]$:

$$[N]_{intrinsic} = \frac{1}{4KT \ \Delta f} \begin{bmatrix} \overline{e_e e_e^*} & \overline{e_e i_{cp}^*} \\ \overline{i_{cp} e_e^*} & \overline{i_{cp} i_{cp}^*} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{2g_e} & 0 \\ 0 & \dfrac{g_e(\alpha_0 - |\alpha|^2)}{2} \end{bmatrix} \tag{7.344}$$

$$[C]_{transformed} = \frac{1}{4KT \ \Delta f} \begin{bmatrix} \overline{e_n e_n^*} & \overline{e_n i_n^*} \\ \overline{i_n e_n^*} & \overline{i_n i_n^*} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \tag{7.345}$$
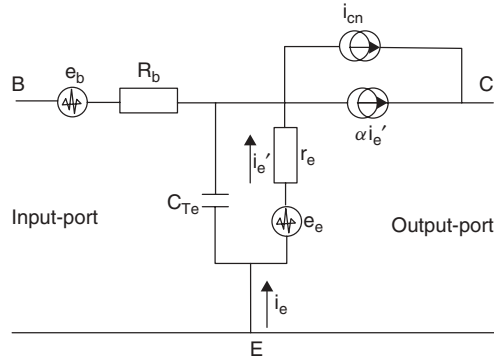
FIGURE 7.33   T-equivalent configuration of common emitter transistor.
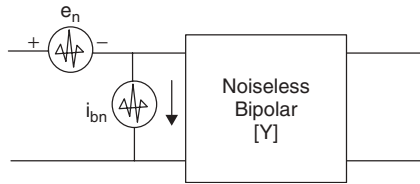
FIGURE 7.34   Transformed bipolar transistor noise model represented as a two-port admittance matrix.

The noise correlation matrix C in terms of N can be obtained by a straightforward application of the steps outlined as

$$C = AZTN\,(AZT)^{\oplus} + ARA^{\oplus} \tag{7.346}$$

where the sign $\oplus$ denotes the Hermitian conjugate.

The matrix Z is the inverse of the admittance matrix Y for the intrinsic portion of the model and T is a transformation matrix, which converts the noise sources e_e and i_{cp} to shunt current sources, respectively, across the base–emitter and collector–emitter ports of the transistor:

$$T = \begin{bmatrix} -(1-\alpha)g_e & 1 \\ -\alpha g_e & -1 \end{bmatrix} \tag{7.347}$$

$$A = \begin{bmatrix} 1 & \dfrac{Z_{11} + r_b}{Z_{21}} \\ 0 & -\dfrac{1}{Z_{11}} \end{bmatrix} \tag{7.348}$$

$$R = \frac{1}{4KT\ \Delta f} \begin{bmatrix} \overline{e_b e_b^*} & 0 \\ 0 & 0 \end{bmatrix} = \begin{bmatrix} r_b & 0 \\ 0 & 0 \end{bmatrix} \tag{7.349}$$

Here Y_c is added as a fictitious admittance across the α-current generator to overcome the singularity of the actual Z matrix. However, in the final evaluation of C, Y_c is set to zero. The matrix A is a circuit transformation matrix and the matrix R is a noise correlation matrix representing the thermal noise of the extrinsic base resistance:

$$
C = \begin{bmatrix} C_{uu^\bullet} & C_{ui^\bullet} \\ C_{u^\bullet i} & C_{ii^\bullet} \end{bmatrix} = \begin{bmatrix} R_n & \dfrac{F_{\min} - 1}{2} - R_n Y_{\mathrm{opt}}^\bullet \\ \dfrac{F_{\min} - 1}{2} - R_n Y_{\mathrm{opt}} & R_n |Y_{\mathrm{opt}}|^2 \end{bmatrix} \tag{7.350}
$$

$$
R_n = \frac{C_{uu^\bullet}}{2kT} \tag{7.351}
$$

$$
Y_{\mathrm{opt}} = \sqrt{\frac{C_{ii^\bullet}}{C_{uu^\bullet}} - \left[\mathrm{Im}\left(\frac{C_{ui^\bullet}}{C_{uu^\bullet}} \right) \right]^2} + j \, \mathrm{Im}\left(\frac{C_{ui^\bullet}}{C_{uu^\bullet}} \right) \tag{7.352}
$$

$$
Y_{\mathrm{opt}} = G_{\mathrm{opt}} + jB_{\mathrm{opt}} \tag{7.353}
$$

The element of the noise correlation matrix C contains all necessary information about the four extrinsic noise parameters $F_{\min}$, $R_{g,\mathrm{opt}}$, $X_{g,\mathrm{opt}}$, and R_n of the bipolar. The expression for $F_{\min}$, $R_{g,\mathrm{opt}}$, $X_{g,\mathrm{opt}}$ are already derived above except the expression for R_n:

$$
R_n = \frac{C_{uu^\bullet}}{2kT} \tag{7.354}
$$

$$
= r_b \left(\frac{1 + (f/f_b)^2}{\alpha_0^2} - \frac{1}{\beta_0} \right) + \frac{r_e}{2} \left[\frac{1 + (f/f_b)^2}{\alpha_0^2} \right.
$$
$$
\left. + (g_e r_b)^2 \left\{ 1 - \alpha_0 + \left(\frac{f}{f_b} \right)^2 + \left(\frac{f}{f_e} \right)^2 + \left[\frac{1}{\beta_0} - \left(\frac{f}{f_b} \right) \left(\frac{f}{f_e} \right) \right]^2 \right\} \right] \tag{7.355}
$$

7.14 THE GaAs FET NOISE MODEL

7.14.1 Model at Room Temperature

Figures 7.35a and 7.35b show a noise model of a grounded-source FET with noise source at the input and the output [7.22].

The mean-square value of the noise sources in the narrow frequency range Δf are given by

$$
\overline{i_d^2} = 4kTg_m P \ \Delta f \tag{7.356}
$$

$$
\overline{i_g^2} = \frac{4kT(wC_{gs})^2 R}{g_m} \Delta f \tag{7.357}
$$

$$
\overline{i_g i_d^\bullet} = -jwC_{gs} 4kT C \sqrt{PR} \ \Delta f \tag{7.358}
$$

$$
S(i_d) = \frac{\overline{i_d^2}}{\Delta f} = \left\langle |i_d^2| \right\rangle = 4kTg_m P \tag{7.359}
$$
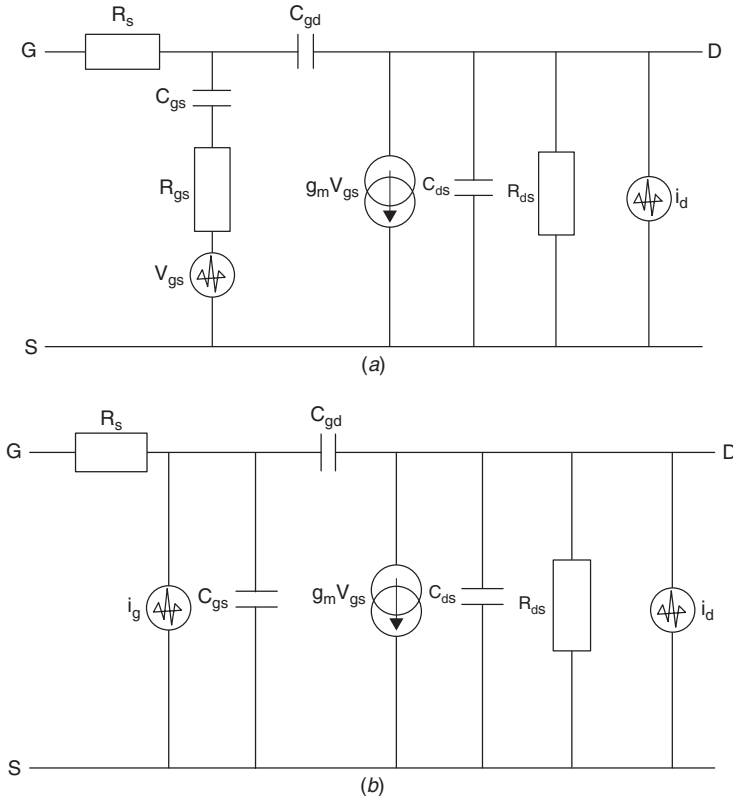
FIGURE 7.35 (*a*) Noise model of FET with voltage noise source at input and the current noise at output. (*b*) Noise model of FET with current noise source at input and output.

$$S(i_g) = \frac{\overline{i_g^2}}{\Delta f} = \left\langle \overline{|i_g^2|} \right\rangle = \frac{4kT(wC_{gs})^2 R}{g_m} \tag{7.360}$$

$$S(i_g i_d^\bullet) = \left\langle \overline{|i_g i_d^\bullet|} \right\rangle = -jwC_{gs}4kTC\sqrt{PR} \tag{7.361}$$

where P, R, and C are the FET noise coefficients and can be given as

$$P = \left[\frac{1}{4kTg_m} \right] \overline{i_d^2} \quad (\mathrm{Hz}^{-1}), 0.67 \text{ for JFETs and } 1.2 \text{ for MESFETs}$$

$$R = \left[\frac{g_m}{4kTw^2 C_{gs}^2} \right] \overline{i_g^2} \quad (\mathrm{Hz}^{-1}), 0.2 \text{ for JFETs and } 0.4 \text{ for MESFETs}$$

$$C = -j \left[\frac{\overline{i_g i_d^\bullet}}{\sqrt{[\overline{i_d^2 i_g^2}]}} \right], 0.4 \text{ for JFETs and } 0.6\text{--}0.9 \text{ for MESFETs}$$
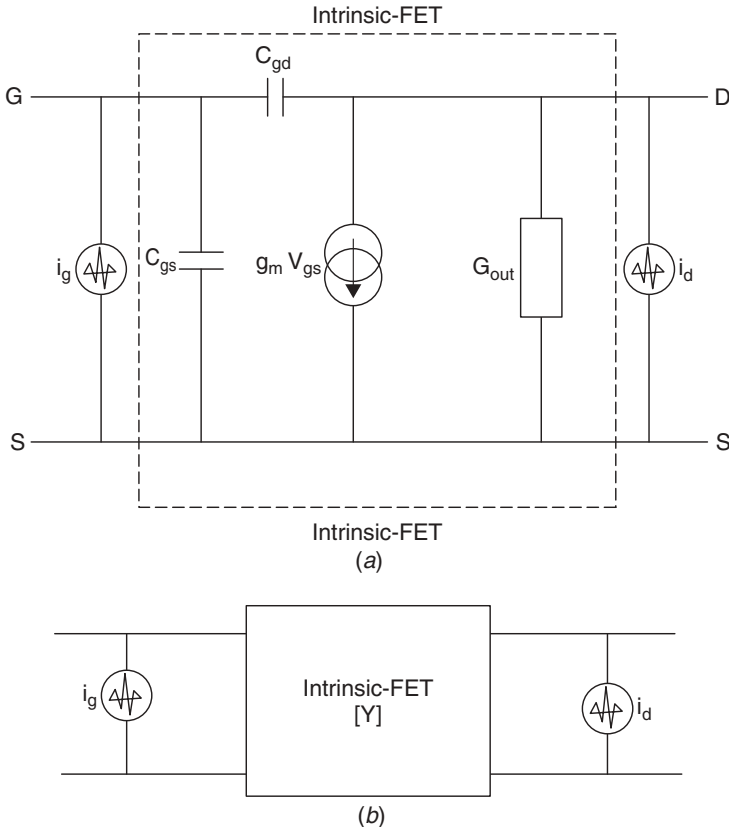
FIGURE 7.36 (*a*) Intrinsic FET with noise sources at input and output. (*b*) Intrinsic FET with noise sources at input and output.

7.14.2   Calculation of Noise Parameters

Figures 7.36*a* and 7.36*b* show the intrinsic FET with noise sources at the input and output [7.22]:

$$[Y]_{\text{FET intrinsic}} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \tag{7.362}$$

$$[C_Y] = [N]_{\text{noise matrix}} = \begin{bmatrix} \overline{i_g i_g^\bullet} & \overline{i_g i_d^\bullet} \\ \overline{i_d i_g^\bullet} & \overline{i_d i_d^\bullet} \end{bmatrix} \tag{7.363}$$

$$[C_Y]_{\text{FET}} = 4kT \begin{bmatrix} \dfrac{w^2 c_{gs}^2 R}{g_m} & -jw c_{gs} C\sqrt{PR} \\ jw c_{gs} C\sqrt{PR} & g_m P \end{bmatrix} \tag{7.364}$$

The noise transformation from the output to the input can be done to calculate the noise parameters:
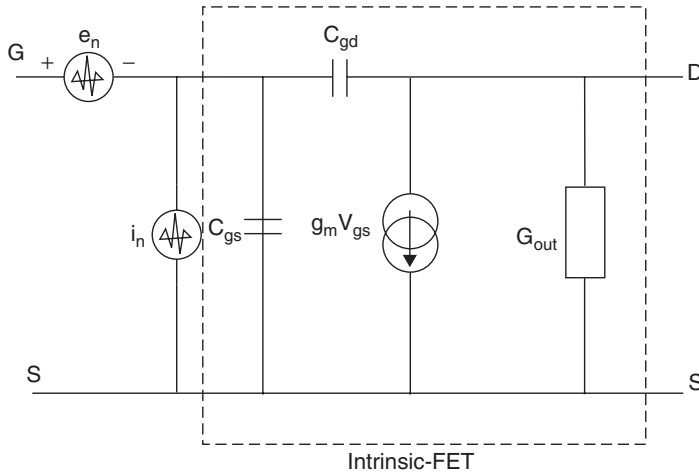
FIGURE 7.37 Equivalent circuit representation of FET with noise sources at input.

Figure 7.37 shows the equivalent FET circuit with the noise source transferred to the input side:

$$[C_a]_{\text{tr}} = \begin{bmatrix} \overline{e_n e_n^\bullet} & \overline{e_n i_n^\bullet} \\ \overline{i_n e_n^\bullet} & \overline{i_n i_n^\bullet} \end{bmatrix} \tag{7.365}$$

$$[C_a]_{\text{tr}} = [T][C_Y]_{\text{tr}}[T]^+ \tag{7.366}$$

$$[T] = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix} \tag{7.367}$$

$$[C_a]_{\text{tr}} = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix} [C_Y]_{\text{tr}} \begin{bmatrix} 0 & 1 \\ B_{CS}^\bullet & D_{CS}^\bullet \end{bmatrix} \tag{7.368}$$

$[ABCD]_{\text{FET}}$

$$= \begin{bmatrix} A_{CS} & B_{CS} \\ C_{CS} & D_{CS} \end{bmatrix} = \begin{bmatrix} 1 & R_s \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sc_{gs} & 1 \end{bmatrix} \begin{bmatrix} \dfrac{sc_{gd}}{sc_{gd} - g_m} & \dfrac{1}{sc_{gd} - g_m} \\ \dfrac{g_m sc_{gd}}{sc_{gd} - g_m} & \dfrac{sc_{gd}}{sc_{gd} - g_m} \end{bmatrix}$$

$$\times \begin{bmatrix} 1 & 0 \\ g_{ds} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sc_{ds} & 1 \end{bmatrix} \tag{7.369}$$

$[ABCD]_{\text{FET}}$

$$= \begin{bmatrix} 1 & R_s \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \dfrac{sc_{gd}}{sc_{gd} - g_m} & \dfrac{1}{sc_{gd} - g_m} \\ \dfrac{sc_{gd}(g_m + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} & \dfrac{sc_{gd} + g_{ds} + sc_{gs} + sc_{ds}}{sc_{gd} - g_m} \end{bmatrix}$$

$$\tag{7.370}$$

$[ABCD]_{\text{FET}}$

$$= \begin{bmatrix} \dfrac{sc_{gd}}{sc_{gd} - g_m} & \dfrac{1}{sc_{gd} - g_m} \\[2mm] +\dfrac{R_s sc_{gd}(g_m + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} & +\dfrac{R_s(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \\[4mm] \dfrac{sc_{gd}(g_m + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} & \dfrac{sc_{gd} + g_{ds} + sc_{gs} + sc_{ds}}{sc_{gd} - g_m} \end{bmatrix}$$

(7.371)

$$[C_Y]_{\text{FET}} = 4kT \begin{bmatrix} \dfrac{w^2 c_{gs}^2 R}{g_m} & -jwc_{gs}C\sqrt{PR} \\[4mm] jwc_{gs}C\sqrt{PR} & g_m P \end{bmatrix}$$

(7.372)

$$[C_a]_{\text{FET}} = [T][C_Y]_{\text{tr}}[T]^+$$

(7.373)

$$[C_a]_{\text{FET}} = \begin{bmatrix} 0 & \dfrac{1}{sc_{gd} - g_m} + \dfrac{R_s(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \\[4mm] 1 & \dfrac{sc_{gd} + g_{ds} + sc_{gs} + sc_{ds}}{sc_{gd} - g_m} \end{bmatrix}$$

$$\times 4kT \begin{bmatrix} \dfrac{w^2 c_{gs}^2 R}{g_m} & -jwc_{gs}C\sqrt{PR} \\[4mm] jwc_{gs}C\sqrt{PR} & g_m P \end{bmatrix} \times K_1$$

(7.374)

$$K_1 = \begin{bmatrix} 0 & 1 \\[4mm] \left(\dfrac{\dfrac{1}{sc_{gd} - g_m}}{+\dfrac{R_s(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m}} \right)^{\bullet} & \left(\dfrac{(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right)^{\bullet} \end{bmatrix}$$

(7.375)

$$= 4kT \begin{bmatrix} \dfrac{sc_{gs}C\sqrt{PR}}{sc_{gd} - g_m} & \dfrac{g_m P}{sc_{gd} - g_m} \\[2mm] +\dfrac{sc_{gs}R_s C\sqrt{PR}(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} & +\dfrac{g_m P R_s(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \\[6mm] \dfrac{\dfrac{w^2 c_{gs}^2 R}{g_m}(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{} & -jwc_{gs}C\sqrt{PR}(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds}) \\[2mm] +\dfrac{sc_{gs}C\sqrt{PR}}{sc_{gd} - g_m} & +\dfrac{g_m P}{sc_{gd} - g_m} \end{bmatrix} \times K_2$$

(7.376)

$$K_2 = \begin{bmatrix} 0 & 1 \\ \left(\dfrac{\dfrac{1}{sc_{gd} - g_m}}{+ \dfrac{R_s(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m}} \right)^{\bullet} & \left(\dfrac{(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right)^{\bullet} \end{bmatrix}$$

(7.377)

$$[C_a]_{\text{FET}} = \begin{bmatrix} C_{uu^{\bullet}} & C_{ui^{\bullet}} \\ C_{u^{\bullet}i} & C_{ii^{\bullet}} \end{bmatrix} = 4kT \begin{bmatrix} R_n & \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}}^{\bullet} \\ \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}} & R_n |Y_{\text{opt}}|^2 \end{bmatrix}$$

(7.378)

$$C_{uu^{\bullet}} = 4kT \left[\left(\frac{g_m P}{sc_{gd} - g_m} + \frac{g_m P R_s(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right) \right.$$
$$\left. \times \left(\frac{1}{sc_{gd} - g_m} + \frac{R_s(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right)^{\bullet} \right]$$

(7.379)

$$C_{ui^{\bullet}} = 4kT \left[\frac{sc_{gs} C \sqrt{PR}}{sc_{gd} - g_m} + \frac{sc_{gs} R_s C \sqrt{PR}(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right] + A_1$$

(7.380)

$$A_1 = \left[\left(\frac{g_m P}{sc_{gd} - g_m} + \frac{g_m P R_s(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right) \right.$$
$$\left. \times \left(\frac{(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right)^{\bullet} \right]$$

(7.381)

$$C_{u^{\bullet}i} = 4kT \left[\left(-jwc_{gs} C \sqrt{PR} + \frac{(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds}) g_m P}{sc_{gd} - g_m} \right) \right.$$
$$\left. \times \left(\frac{1}{sc_{gd} - g_m} + \frac{R_s(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right)^{\bullet} \right]$$

(7.382)

$$C_{ii^{\bullet}} = 4kT \left[\left(\frac{w^2 c_{gs}^2 R}{g_m} + \frac{(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds}) sc_{gs} C \sqrt{PR}}{sc_{gd} - g_m} \right) + B_1 \right]$$ (7.383)

$$B_1 = \left(-jwc_{gs} C \sqrt{PR} + \frac{(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds}) g_m P}{sc_{gd} - g_m} \right)$$
$$\times \left(\frac{(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right)^{\bullet}$$

(7.384)

After substituting the values of $C_{uu^{\bullet}}$, $C_{ui^{\bullet}}$, $C_{u^{\bullet}i}$, and $C_{ii^{\bullet}}$, we get the noise parameters

$$R_n = \frac{C_{uu^{\bullet}}}{2kT}$$

(7.385)

$$F_{\min} = 1 + \frac{C_{ui^{\bullet}} + C_{uu^{\bullet}} Y_{\text{opt}}}{kT}$$

(7.386)

$$Y_{\text{opt}} = \sqrt{\frac{C_{ii^\bullet}}{C_{uu^\bullet}} - \left[\text{Im}\left(\frac{C_{ui^\bullet}}{C_{uu^\bullet}}\right)\right]^2} + j \text{ Im}\left(\frac{C_{ui^\bullet}}{C_{uu^\bullet}}\right) \tag{7.387}$$

$$Y_{\text{opt}} = G_{\text{opt}} + jB_{\text{opt}} \tag{7.388}$$

$$\Gamma_{\text{opt}} = \frac{Z_{\text{opt}} - Z_0}{Z_{\text{opt}} + Z_0} \Rightarrow \frac{Y_{\text{opt}} - Y_0}{Y_{\text{opt}} + Y_0} \tag{7.389}$$

Neglecting the effect of gate leakage current I_{gd} and gate-to-drain capacitance C_{gd}, the models above will be further simplified as shown below.

Figures 7.38a and 7.38b show the equivalent configuration of the FET without gate–drain capacitance:

$$[C_a]_{\text{tr}} = \begin{bmatrix} \overline{e_n e_n^\bullet} & \overline{e_n i_n^\bullet} \\ \overline{i_n e_n^\bullet} & \overline{i_n i_n^\bullet} \end{bmatrix} \tag{7.390}$$

$$[C_a]_{\text{FET}} = [T][C_Y]_{\text{FET}}[T]^+ \tag{7.391}$$

$$[T] = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix}_{\text{FET}} \tag{7.392}$$

$$[C_a]_{\text{FET}} = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix} [C_Y]_{\text{FET}} \begin{bmatrix} 0 & 1 \\ B_{CS}^\bullet & D_{CS}^\bullet \end{bmatrix} \tag{7.393}$$

The transformation matrix T comes from the $ABCD$ matrix of the intrinsic FET:

$$[Y]_{\text{FET}} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} sc_{gs} & 0 \\ g_m & G_{\text{out}} \end{bmatrix} \tag{7.394}$$
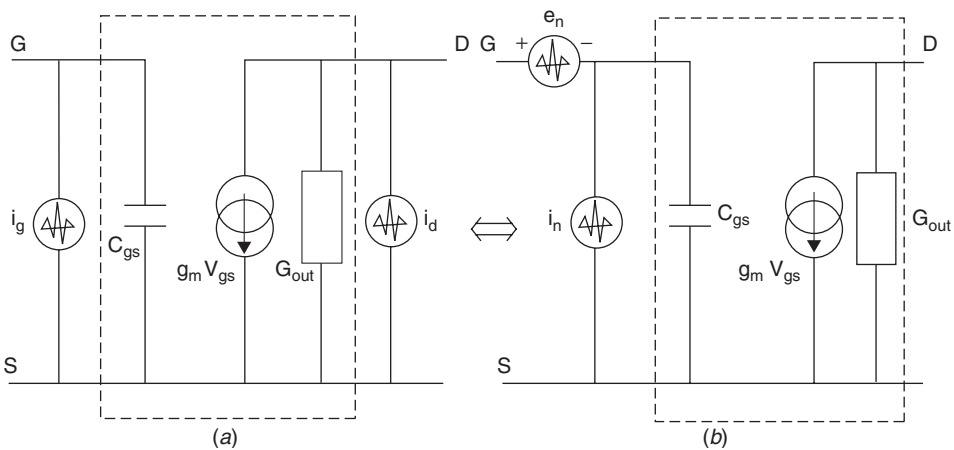
FIGURE 7.38 Equivalent configuration of FET without gate–drain capacitance: intrinsic FET with (a) current noise sources at input and output and (b) voltage and current noise sources at input.

$$[ABCD]_{\text{FET}} = \begin{bmatrix} A_{CS} & B_{CS} \\ C_{CS} & D_{CS} \end{bmatrix} = \begin{bmatrix} -\dfrac{y_{22}}{y_{11}} & \dfrac{1}{-y_{21}} \\ \dfrac{\Delta}{y_{21}} & \dfrac{-y_{11}}{y_{21}} \end{bmatrix}$$

$$= \begin{bmatrix} -\dfrac{G_{\text{out}}}{g_m} & \dfrac{-1}{g_m} \\ \dfrac{sc_{gs}G_{\text{out}}}{g_m} & \dfrac{-sc_{gs}}{g_m} \end{bmatrix} \tag{7.395}$$

$$[T] = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{-1}{g_m} \\ 1 & \dfrac{-sc_{gs}}{g_m} \end{bmatrix} \tag{7.396}$$

$$[T]^+ = \begin{bmatrix} 0 & 1 \\ B_{CS}^\bullet & D_{CS}^\bullet \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ \dfrac{1}{-g_m} & \dfrac{sc_{gs}}{-g_m} \end{bmatrix} \tag{7.397}$$

$$[C_a]_{\text{FET}} = [T][C_Y]_{\text{FET}}[T]^+ \tag{7.398}$$

$$[C_a]_{\text{FET}} = \begin{bmatrix} 0 & \dfrac{1}{-g_m} \\ 1 & \dfrac{sc_{gs}}{-g_m} \end{bmatrix} \times 4kT \begin{bmatrix} \dfrac{w^2 c_{gs}^2 R}{g_m} & -jwc_{gs}C\sqrt{PR} \\ jwc_{gs}C\sqrt{PR} & g_m P \end{bmatrix}$$

$$\times \begin{bmatrix} 0 & 1 \\ \dfrac{1}{-g_m} & \dfrac{sc_{gs}}{-g_m} \end{bmatrix} \tag{7.399}$$

$$[C_a]_{\text{FET}} = \dfrac{4kT}{g_m} \begin{bmatrix} P & -jwc_{gs}(P + C\sqrt{PR}) \\ jwc_{gs}(P + C\sqrt{PR}) & w^2 c_{gs}^2 (P + R + 2C\sqrt{PR}) \end{bmatrix} \tag{7.400}$$

$$[C_a]_{\text{FET}} = \begin{bmatrix} C_{uu}^\bullet & C_{ui}^\bullet \\ C_{u^\bullet i} & C_{ii}^\bullet \end{bmatrix}$$

$$= 4kT \begin{bmatrix} R_n & \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}}^\bullet \\ \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}} & R_n |Y_{\text{opt}}|^2 \end{bmatrix} \tag{7.401}$$

After substituting the values of $C_{uu}^\bullet$, $C_{ui}^\bullet$, $C_{u^\bullet i}$, and $C_{ii}^\bullet$, we get the noise parameters

$$R_n = \dfrac{C_{uu}^\bullet}{4kT} = \dfrac{P}{g_m} \tag{7.402}$$

$$Y_{\text{opt}} = \sqrt{\dfrac{C_{ii}^\bullet}{C_{uu}^\bullet} - \left[\text{Im}\left(\dfrac{C_{ui}^\bullet}{C_{uu}^\bullet}\right)\right]^2} + j\ \text{Im}\left(\dfrac{C_{ui}^\bullet}{C_{uu}^\bullet}\right) \tag{7.403}$$

$$Y_{\text{opt}} = G_{\text{opt}} + jB_{\text{opt}} \tag{7.404}$$

$$G_{\text{opt}} = \frac{wc_{gs}}{P}\sqrt{PR(1 - C^2)} \tag{7.405}$$

$$B_{\text{opt}} = -wc_{gs}\left(1 + C\sqrt{\frac{R}{P}}\right) \tag{7.406}$$

$$F_{\text{min}} = 1 + \frac{C_{ui\bullet} + C_{uu\bullet}Y_{\text{opt}}}{kT} = 1 + \frac{2wc_{gs}}{g_m}\sqrt{PR(1 - C^2)} \tag{7.407}$$

7.14.3   Influence of C_{gd}, R_{gs}, and R_s on Noise Parameters

$$[C_a]_{\text{FET}} = \begin{bmatrix} \overline{e_n e_n^\bullet} & \overline{e_n i_n^\bullet} \\ \overline{i_n e_n^\bullet} & \overline{i_n i_n^\bullet} \end{bmatrix} \tag{7.408}$$

$$[C_a]_{\text{FET}} = \begin{bmatrix} C_{uu\bullet} & C_{ui\bullet} \\ C_{u\bullet i} & C_{ii\bullet} \end{bmatrix} \tag{7.409}$$

$$C_{uu\bullet} = \left|\frac{g_m}{g_m - jwc_{gd}}\right|^2 \left(\frac{P + R - 2C_r\sqrt{PR}}{g_m}\right) + (R_s + R_{gs}) \tag{7.410}$$

$$C_{ui\bullet} = \left|\frac{g_m}{g_m - jwc_{gd}}\right|^2 \left[\left(\frac{w^2 C_{gs}^2 C_{gd}^2}{g_m^2} + \frac{jwc_{gd}}{g_m}\right) \right.$$
$$\left. (R - C\sqrt{PR}) - \frac{jwc_{gd}}{g_m}(P - C^\bullet\sqrt{PR})\right] \tag{7.411}$$

$$C_{ii\bullet} = \left|\frac{g_m}{g_m - jwc_{gd}}\right|^2 \left(\left|\frac{w^2 C_{gs}^2 C_{gd}^2}{g_m^2} + \frac{jwc_{gd}}{g_m}\right|^2 \frac{R}{g_m} + \left|\frac{jwc_{gs}}{g_m}\right|^2 Pg_m\right) \tag{7.412}$$

$$+ \left|\frac{g_m}{g_m - jwc_{gd}}\right|^2 \left\{2 \operatorname{Re}\left[\left(\frac{w^2 C_{gs}^2 C_{gd}^2}{g_m^2} + \frac{jwc_{gd}}{g_m}\right) \right.\right.$$
$$\left.\left. \times \left(\frac{jwc_{gs}}{g_m}\right) C\sqrt{PR}\right]\right\} \tag{7.413}$$

$$C_{u\bullet i} = \left\{\left|\frac{g_m}{g_m - jwc_{gd}}\right|^2 \left[\left(\frac{w^2 C_{gs}^2 C_{gd}^2}{g_m^2} + \frac{jwc_{gd}}{g_m}\right) \right.\right.$$
$$\left.\left. \times (R - C\sqrt{PR}) - \frac{jwc_{gd}}{g_m}(P - C^\bullet\sqrt{PR})\right]\right\}^\bullet \tag{7.414}$$

where

$$\frac{R}{g_m} = \overline{e_n e_n^\bullet} \tag{7.415}$$

$$Pg_m = \overline{i_n i_n^\bullet} \tag{7.416}$$

$$C = \frac{\overline{|e_n i_n^\bullet|}}{\sqrt{(\overline{e_n e_n^\bullet})(\overline{i_n i_n^\bullet})}} = \frac{\overline{|e_n i_n^\bullet|}}{\sqrt{|e_n^2||i_n^2|}} \tag{7.417}$$

$$[C_a]_{\text{FET}} = \begin{bmatrix} C_{uu^\bullet} & C_{ui^\bullet} \\ C_{u^\bullet i} & C_{ii^\bullet} \end{bmatrix} = \begin{bmatrix} R_n & \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}}^\bullet \\ \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}} & R_n |Y_{\text{opt}}|^2 \end{bmatrix} \tag{7.418}$$

The modified expressions for the noise parameters are now [7.22]:

$$R_n = C_{uu^\bullet} \tag{7.419}$$

$$Y_{\text{opt}} = \sqrt{\frac{C_{ii^\bullet}}{C_{uu^\bullet}} - \left[\text{Im}\left(\frac{C_{ui^\bullet}}{C_{ii^\bullet}}\right)\right]^2} + j\,\text{Im}\left(\frac{C_{ui^\bullet}}{C_{uu^\bullet}}\right) \tag{7.420}$$

$$Z_{\text{opt}} = \sqrt{\frac{C_{uu^\bullet}}{C_{ii^\bullet}} - \left(\frac{\text{Im }C_{ui^\bullet}}{C_{ii^\bullet}}\right)^2} - j\left(\frac{\text{Im }C_{ui^\bullet}}{C_{ii^\bullet}}\right) \tag{7.421}$$

$$Y_{\text{opt}} = G_{\text{opt}} + jB_{\text{opt}} \tag{7.422}$$

$$F_{\min} = 1 + 2\lfloor \text{Re}(C_{ui^\bullet}) + C_{ii^\bullet}\text{Re}(Z_{\text{opt}})\rfloor \tag{7.423}$$

$$F_{\min} = 1 + 2\left[\left(\frac{w^2 c_{gs}^2}{g_m^2}\right)(R_{gs} + R_s)Pg_m \right.$$
$$\left. + \sqrt{\frac{w^4 c_{gs}^4}{g_m^4}(R_{gs} + R_s)^2 P^2 g_m^2 + \left(\frac{w^2 c_{gs}^2}{g_m^2}\right)[PR(1 - C^2) - Pg_m R_{gs}]}\right] \tag{7.424}$$

$$R_n = \left|\frac{g_m}{g_m - jwc_{gd}}\right|^2 \left(\frac{P + R - 2C_r\sqrt{RP}}{g_m}\right) + (R_{gs} + R_s) \tag{7.425}$$

$$R_{\text{opt}} = \frac{1}{wc_{gs}}\sqrt{\frac{g_m(R_s + R_{gs}) + R(1 - C_r^2)}{P} + w^2 c_{gs}^2 (R_s + R_{gs})^2} \tag{7.426}$$

$$X_{\text{opt}} = \frac{1}{wc_{gs}}\left(1 - C_r\sqrt{\frac{R}{P}}\right) \tag{7.427}$$

7.14.4 Temperature Dependence of Noise Parameters of an FET [7.22]

We now introduce a minimum noise temperature $T_{\min}$ and modify the noise parameters previously derived. This equation now will have temperature dependence factors.

For the use of FETs in amplifiers used in huge dishes scanning the universe, in evaluating signals coming from outer space, extreme low noise temperatures are needed. These amplifiers are being cooled cryogenically to temperatures close to 0 K. Since there are no measurements available, the following method allows for the prediction of
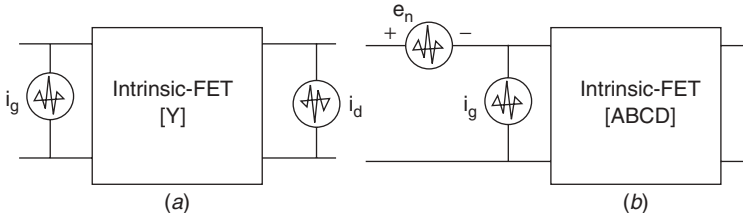
FIGURE 7.39 Noise representation in linear two-port: (*a*) current noise source at input and output; (*b*) current and voltage noise sources at input.

noise performance of FETs under the "cooled" conditions. The following is a derivation showing how to calculate the temperature-dependent noise performance.

Figures 7.39*a* and 7.39*b* are the familiar two-port noise representation of the intrinsic FET in admittance and *ABCD* matrix form.

The admittance representation of the noise parameter of an intrinsic FET is expressed as

$$G_1 = \frac{\overline{|i_g^2|}}{4kT_0 \, \Delta f} \tag{7.428}$$

$$G_2 = \frac{\overline{|i_d^2|}}{4kT_0 \, \Delta f} \tag{7.429}$$

$$C_r = \frac{\overline{|i_g i_d^\bullet|}}{\sqrt{|i_d^2||i_g^2|}} \tag{7.430}$$

Where k is Boltzmann's constant ($k = 1.38 \times 10^{-23}$ J/K), T_0 is standard room temperature (290 K), and Δf is the reference bandwidth.

The *ABCD* matrix representation and the corresponding noise parameters are

$$R_n = \frac{\overline{|e_n^2|}}{4kT_0 \, \Delta f} \tag{7.431}$$

$$g_n = \frac{\overline{|i_n^2|}}{4kT_0 \, \Delta f} \tag{7.432}$$

$$C_r = \frac{\overline{|e_n i_n^\bullet|}}{\sqrt{|e_n^2||i_n^2|}} \tag{7.433}$$

$$N = R_{\text{opt}}g_n \tag{7.434}$$

where g_n is noise conductance.

The expression for the noise temperature T_n and a noise measure M of a two-port driven by generator impedance Z_g is expressed as

$$T_n = T_{\min} + T_0 \frac{g_n}{R_g}|Z_g - Z_{\text{opt}}|^2 \tag{7.435}$$

$$= T_{\min} + NT_0 \frac{|Z_g - Z_{\text{opt}}|^2}{R_g R_{\text{opt}}} \tag{7.436}$$

$$= T_{\min} + 4NT_0 \frac{|T_g - T_{\text{opt}}|^2}{(1 - |T_{\text{opt}}|^2)(1 - |T_g|^2)} \tag{7.437}$$

$$T_{\text{opt}} = \frac{Z_{\text{opt}} - Z_0}{Z_{\text{opt}} + Z_0} \tag{7.438}$$

$$M = \frac{T_n}{T_0} \left(\frac{1}{1 - 1/G_a} \right) \tag{7.439}$$

where Z_0 is the reference impedance and G_a is the available gain.

An example of an extrinsic FET with parasitic resistances is shown in Figure 7.40. They contribute thermal noise, and their influence can be calculated based on the ambient temperature T_a:

$$G_1 = \frac{T_g}{T_0} \frac{R_{gs}(wC_{gs})^2}{(1 + w^2 C_{gs}^2 R_{gs}^2)} \tag{7.440}$$

$$G_2 = \frac{T_g}{T_0} \frac{g_m^2 R_{gs}}{(1 + w^2 C_{gs}^2 R_{gs}^2)} + \frac{T_d}{T_0} g_{gs} \tag{7.441}$$

$$C_{r_c} = C_r \frac{\overline{|i_g i_d^\bullet|}}{\sqrt{|i_d^2||i_g^2|}} = \frac{-jwg_m C_{gs} R_{gs}}{(1 + w^2 C_{gs}^2 R_{gs}^2)} \frac{T_g}{T_0} \tag{7.442}$$

The noise properties of the intrinsic FET are treated by assigning equivalent temperatures T_g and T_d to R_{gs} and g_{ds}.

No correlation is assumed between the noise sources represented by the equivalent temperatures T_g and T_d in Figure 7.41.

The modified noise parameters are expressed as

$$Z_{\text{opt}} = R_{\text{opt}} + jX_{\text{opt}} \tag{7.443}$$
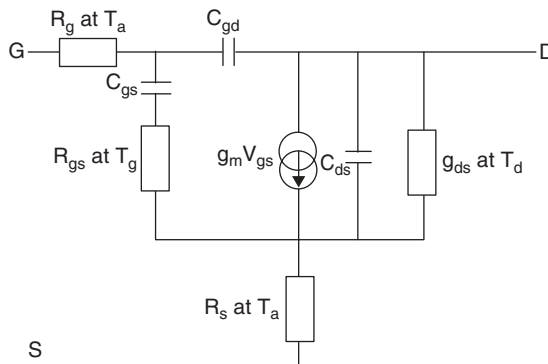
FIGURE 7.40 Extrinsic FET with parasitic resistances.
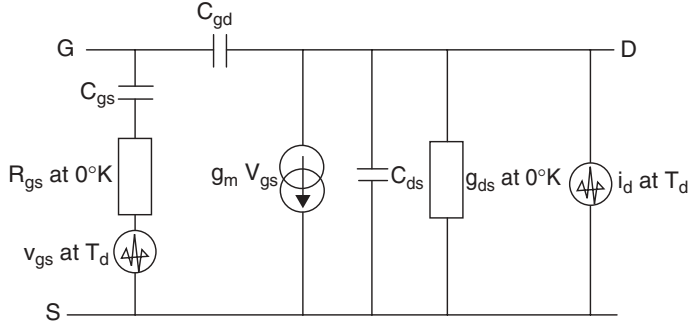
FIGURE 7.41   Intrinsic FET with assigned equivalent temperature.

$$R_{\mathrm{opt}} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{R_{gs}}{R_{ds}} \frac{T_g}{T_d} + R_{gs}^2} \tag{7.444}$$

$$X_{\mathrm{opt}} = \frac{1}{w C_{gs}} \tag{7.445}$$

$$T_{\min} = 2\frac{f}{f_T}\sqrt{R_{gs}g_{ds}T_gT_d + \left(\frac{f_T}{f}\right)^2 R_{gs}^2 g_{ds}^2 T_d^2} + 2\left(\frac{f_T}{f}\right)^2 R_{gs}g_{ds}T_d \tag{7.446}$$

$$T_{\min} = (F_{\min} - 1)T_0 \tag{7.447}$$

$$g_n = \left(\frac{f_T}{f}\right)^2 \frac{g_{ds}T_d}{T_0} \tag{7.448}$$

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{7.449}$$

$$\frac{4NT_0}{T_{\min}} = \frac{2}{1 + R_{gs}/R_{\mathrm{opt}}} \tag{7.450}$$

$$R_n = \frac{T_g}{T_0}R_{gs} + \frac{T_d}{T_0}\frac{g_{ds}}{g_m^2}(1 + w^2 C_{gs}^2 R_{gs}^2) \tag{7.451}$$

$$C_r = C\sqrt{R_n g_n} = \frac{T_d}{T_0}\frac{g_{ds}}{g_m^2}(w^2 C_{gs}^2 R_{gs} + jw C_{gs}) \tag{7.452}$$

7.14.5 Approximation and Discussion

With some reasonable approximation, the expression of the noise parameters becomes much simpler (by introducing the following approximation, the obtained values from the calculation typically vary less than 5% from the exact one):

$$if \frac{f}{f_T} \le \sqrt{\frac{R_{gs}}{R_{ds}} \frac{T_g}{T_d}} \tag{7.453}$$

and $R_{\text{opt}} \geq R_{gs}$. Then

$$R_{\text{opt}} \cong \left(\frac{f_T}{f}\right) \sqrt{\frac{r_{gs}}{r_{ds}} \frac{T_g}{T_d}} \tag{7.454}$$

$$X_{\text{opt}} \cong \frac{1}{w C_{gs}} \tag{7.455}$$

$$T_{\text{min}} \cong 2 \frac{f}{f_T} \sqrt{r_{gs} g_{ds} T_g T_d} \tag{7.456}$$

$$g_n \cong \left(\frac{f_T}{f}\right)^2 \frac{g_{ds} T_d}{T_0} \tag{7.457}$$

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{7.458}$$

$$\frac{4 N T_0}{T_{\text{min}}} \cong 2 \tag{7.459}$$

Example 7.1   A linear FET model with the following intrinsic parameters is assumed:

$$
\begin{aligned}
R_{gs} &= 2.5 \ \Omega & C_{gd} &= 0.042 \ \text{pF} \\
r_{ds} &= 400 \ \Omega & g_m &= 57 \ \text{mS} \\
C_{gs} &= 0.28 \ \text{pF} & f &= 8.5 \ \text{GHz} \\
C_{ds} &= 0.067 \ \text{pF}
\end{aligned}
$$

The temperature-dependent noise parameters for the intrinsic FET are now calculated for two cases (room temperature):

1. Assume $T_a = 297$ K, $T_g = 304$ K, $T_d = 5514$ K, $V_{ds} = 2$ V, $I_{ds} = 10$ mA:

$$f_T = \frac{g_m}{2\pi C_{gs}} = 32.39 \ \text{GHz} \tag{7.460}$$

$$R_{\text{opt}} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{r_{gs}}{g_{ds}} \frac{T_g}{T_d} + r_{gs}^2} = 28.42 \ \Omega \tag{7.461}$$

$$X_{\text{opt}} = \frac{1}{w C_{gs}} = 66.91 \ \Omega \tag{7.462}$$

$$T_{\text{min}} = 2 \frac{f}{f_T} \sqrt{r_{gs} g_{ds} T_g T_d + \left(\frac{f_T}{f}\right)^2 r_{gs}^2 g_{ds}^2 T_d^2}$$
$$+ 2 \left(\frac{f_T}{f}\right)^2 r_{gs} g_{ds} T_d = 58.74 \ \text{K} \tag{7.463}$$

$$g_n = \left(\frac{f_T}{f}\right)^2 \frac{g_{ds} T_d}{T_0} = 3.27 \ \text{mS} \tag{7.464}$$

$$F_{\min} = \frac{T_{\min}}{T_0} + 1 = \frac{58.7}{290} + 1 = 1.59 \text{ dB} \tag{7.465}$$

$$R_n = \frac{T_g r_{gs}}{T_0} + \frac{g_{ds} T_d}{T_0 g_m^2}(1 + w^2 r_{gs}^2 c_{gs}^2) = 17.27 \ \Omega \tag{7.466}$$

2. Assume $T_a = 12.5$ K, $T_g = 14.5$ K, $T_d = 1406$ K, $V_{ds} = 2$ V, $I_{ds} = 5$ mA (cooled down to 14.5 K!):

$$f_T = \frac{g_m}{2\pi C_{gs}} = 32.39 \text{ GHz} \tag{7.467}$$

$$R_{\text{opt}} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{r_{gs}}{g_{ds}} \frac{T_g}{T_d} + r_{gs}^2} = 12.34 \ \Omega \tag{7.468}$$

$$X_{\text{opt}} = \frac{1}{w C_{gs}} = 66.9 \ \Omega \tag{7.469}$$

$$T_{\min} = 2\frac{f}{f_T}\sqrt{r_{gs} g_{ds} T_g T_d + \left(\frac{f_T}{f}\right)^2 r_{gs}^2 g_{ds}^2 T_d^2}$$

$$+ 2\left(\frac{f_T}{f}\right)^2 r_{gs} g_{ds} T_d = 7.4 \text{ K} \tag{7.470}$$

$$g_n = \left(\frac{f_T}{f}\right)^2 \frac{g_{ds} T_d}{T_0} = 0.87 \text{ mS} \tag{7.471}$$

$$F_{\min} = \frac{T_{\min}}{T_0} + 1 = \frac{7.4}{290} + 1 = 0.21 \text{ dB} \tag{7.472}$$

$$R_n = \frac{T_g r_{gs}}{T_0} + \frac{g_{ds} T_d}{T_0 g_m^2}(1 + w^2 r_{gs}^2 c_{gs}^2) = 3.86 \ \Omega \tag{7.473}$$

These results are consistent with results published by Pospieszalski [7.20] and Pucel et al. [7.21] [See also 7.22].

One final point for noise data is the inequalities derived in Eq. (4.95), which is repeated here:

$$1 \le \frac{4NT_0}{T_{\min}} < 2 \tag{7.474}$$

where the first equality occurs if the noise sources (at the input) are fully correlated and the second inequality occurs if the noise sources are totally uncorrelated. This is a valuable check on the data (or model) to ensure the numbers are physically possible.

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PROBLEMS

7.1 For a passive element, show that the noise figure is given by

$$F = \frac{1}{G_A}$$

where G_A is the available power gain. For an ideal generator ($\Gamma_G = 0$), show that this reduces to

$$F = \frac{1 - |S_{22}|^2}{|S_{21}|^2}$$

What is the noise figure of an ideal 3-dB attenuator? What is the noise temperature?

7.2 Consider the following resistive network, which has a noise figure given by problem 7.1. Find the values of R_1 and R_2 for

(a) $F = 6$ dB (use Chapter 4)

(b) $F = 0$ dB
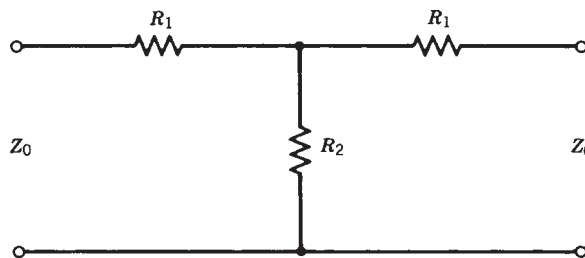
7.3 For a bandwidth of 1 MHz and room temperature (290 K), calculate the root-mean-square noise voltage V_n for the following resistors:

(a) $R = 1 \text{ k}\Omega$

(b) $R = 1 \text{ M}\Omega$

7.4 Derive a table for the equivalence between noise temperature and noise figure for 0 to 100 K for every 10 K. Plot the Y axis as the noise figure in decibels versus the X axis as temperature in kelvin. For a noise figure of 3 dB, what is the noise temperature?

7.5 What is the minimum system noise figure for a transistor with a 1.0-dB noise figure and 8 dB gain? What is the minimum noise temperature?

7.6 Give the S parameters and noise parameters of a GaAs FET at 12 GHz, ATF-13135:

$$S = \begin{bmatrix} 0.16\underline{/37^\circ} & 0.144\underline{/-89^\circ} \\ 2.34\underline{/-84^\circ} & 0.15\underline{/46^\circ} \end{bmatrix}$$

$$F_{\min} = 1.2 \text{ dB} \qquad \Gamma_{on} = 0.47\underline{/-65^\circ} \qquad R_n = 40 \ \Omega$$

(a) Find Y_{on} and Z_{on}.

(b) Calculate the available gain for a noise match in the input, $G_A(\Gamma_{on})$ in decibels.

(c) Using Table 7.2, calculate the four noise parameters for a 10-Ω source resistor.

(d) Calculate the noise figure circles in the Γ_G plane.

7.7 For the transistor of problem 7.6, calculate the common-gate noise parameters (see Table 7.2).

7.8 For a three-stage amplifier, calculate the total noise figure and noise temperature.

$$F_1 = 1.2 \text{ dB} \qquad G_{A1} = 9 \text{ dB}$$

$$F_2 = 1.4 \text{ dB} \qquad G_{A2} = 9 \text{ dB}$$

$$F_3 = 1.8 \text{ dB} \qquad G_{A3} = 9 \text{ dB}$$

7.9 The noise figure data for a low-noise transistor gives $\Gamma_{on} = 0.5\underline{/45^\circ}$ at the reference plane of the test fixture. What is the device Γ_{on} if the test fixture has an electrical length of 1.65 cm at 10 GHz? (Given: The velocity of light $= c = 3.0 \times 10^{10}$ cm/s. Electrical length is defined as βl in the air line.)
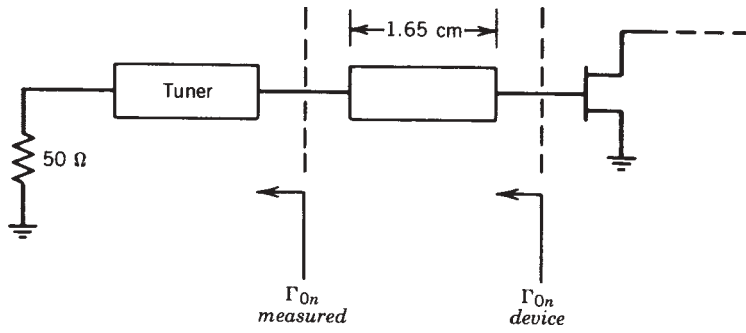
7.10   A one-stage low-noise amplifier has $F = F_{\min} = 1.4$ dB and $G = G_A = 7$ dB. By adding source feedback, the noise figure is improved until $F = 1.2$ dB and $G = 5$ dB. Show the noise measure has not changed.

CHAPTER 8

SMALL- AND LARGE-SIGNAL AMPLIFIER DESIGN

8.1 INTRODUCTION

This chapter describes the design of small-signal amplifiers using S parameters, including high-gain amplifiers (HGAs), low-noise amplifiers (LNAs), and high-power or large-signal amplifiers (HPAs); broadband amplifiers; balanced amplifiers; feedback, cascode, multistage, traveling-wave or distributed amplifiers; and millimeter-wave amplifiers. The conditions for stability and its limitations are also included in this chapter. Amplifier design should be considered a three-step process:

1. A dc design
2. An RF design
3. Total schematic layout

The first step is often treated too lightly, leading to nonworking amplifiers as the transistor is not turned on properly because the engineer is clumsy with Ohm's law. The second step uses the concepts in Chapters 4 and 5, and the third step is necessary to lay out the circuit mask. It is this step that requires some design experience as computers during the process of unrestrained optimization easily come up with transmission line elements that cannot be realized, for example, with lines where lengths are approaching the widths or are even shorter. The junction effects of joined transmission lines must also be included in the CAD calculations, tee, cross, and so on.

The dc bias circuits for a BJT and a MESFET are given in Figures 8.1 and 8.2. The curve tracer responses are helpful to understand the biasing of the transistor [8.1]. The BJT (and HBT) bias circuit consists of four resistors, where some of the resistances may be arbitrarily set to zero. The essential idea is to forward bias the base–emitter junction
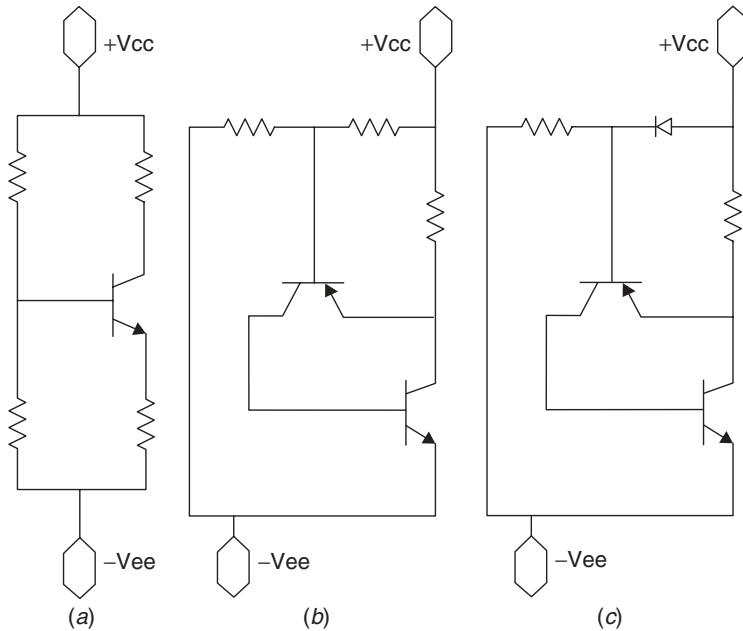
FIGURE 8.1 A dc bias circuit for BJT/HBT: (*a*) four-resistor network; (*b*) active bias; (*c*) active bias with diode.

of a silicon BJT to about 0.7 V; for a GaAs HBT this is 1.0 to 1.2 V, depending on the materials used for the emitter and base; it may be much lower (0.6 to 0.9 V) for Si–Ge HBTs.

For the MESFET, an examination of the curve tracer response of a depletion-mode device will set the negative V_{gs} dc value by

$$V_{gs} = -I_d R_s \tag{8.1}$$

For enhancement-mode devices, a positive value of V_{gs} is required. Some examples of dc biasing will be included in this chapter for common-source or common-emitter transistors and the HBT cascode connection, which is an essential step in design. The dc biasing of common-base and common-collector transistors may be accomplished by common-emitter dc biasing.

Also included in Figure 8.1 are active bias circuits for BJTs and FETs. The value of I_1 is about 1 mA, and it is set by the minimum value of h_{FE}, which is typically 30. The reference voltage, which is at the forward-biased emitter–base junction of the *pnp* transistor, remains essentially constant over temperature (-2.5 mV/$^\circ$C); the collector current is set by R_c, and V_{CE} is set by the voltage dividers R_1 and R_2. The same principles hold for the FET, where active bias with *pnp* BJTs can also be used.

Some improvement in the temperature response can be achieved by adding diodes to this active bias scheme. An example using the AT41400 BJT is shown in Table 8.1 and Figure 8.2, with the transistor biased at $I_c = 30$ mA and $V_{ce} = 8.0$ V. The idea is to compensate for the -2.5 mV/$^\circ$C of the *pnp* base–emitter junction with the same factor introduced appropriately into the active bias circuit.

TABLE 8.1   Temperature Properties of Active Bias Circuits

Circuits	ΔV_{ce} (V) $(T = -100 - 150°\text{C})$	ΔI_c (mA) $(T = -100 - 150°\text{C})$
Four-resistor bias	−0.679	4
Active bias using 2907 *pnp*	−0.494	4
Active bias with second 2907 *pnp* to ground	−0.276	2
Active bias with 1206 diode	−0.206	0.96
Active bias with 1183 diode	−0.173	0.7
Active bias with 4006 diode	−0.135	0.42
Active bias with 3900 diode	−0.107	0.21

Note: All resistors have temperature coefficient of 100 ppm.
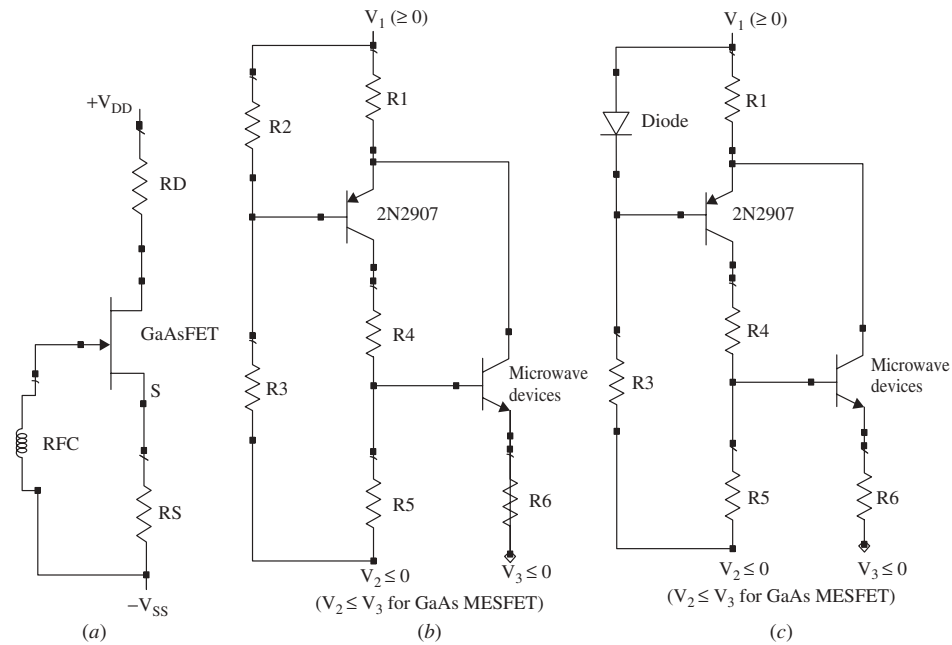
FIGURE 8.2   Bias circuits for MESFET/PHEMT: (*a*) simple circuit; (*b*) active bias; (*c*) active bias with diode.

8.2   SINGLE-STAGE AMPLIFIER DESIGN

8.2.1   High Gain

The design of a HGA depends upon the value of k, the stability factor. If $k > 1$, both ports of the transistor may be conjugately matched to achieve G_{ma}, the maximum available gain. If $k < 1$, more care must be exercised to obtain approximately G_{ms} and stability at all frequencies. When $k < 1$, the two-port may oscillate if the terminations fall into the unstable regions at any frequency. The definition of k was presented in Chapter 4 [Eq. (4.7)]. When more gain is needed, it is best to use multistage amplifiers

and guarantee each stage is stable. Another approach is to consider unilateral amplifiers, which have 4 to 6 dB more gain than a G_{ma}/G_{ms} amplifier.

A common misconception is the belief that if $k < 1$ the maximum gain is G_{ms}; no, it is infinity, since the transistor may oscillate and deliver output RF power with no input RF power other than noise. A helpful way to interpret G_{ms} is to consider loading the transistor resistively until $k = 1$; then, if the two-port is simultaneously matched, the gain is G_{ms}. This is not the recommended way to design the amplifier, since the transistor may be made stable by designing $\Gamma_G(f)$ and $\Gamma_L(f)$ to be in the stable regions without the addition of any resistors.

8.2.2   Maximum Available Gain and Unilateral Gain

The material in this section was previously published in Ref. 8.2. Notice there is very little published on the realization of unilateral amplifiers, but this should change soon, since the gain is much higher and the stability can be made to be excellent. The most difficult part of this design is to guarantee stability at all frequencies.

Introduction   For amplifier design, various power gains of a stable circuit have been defined in the past 50 years [8.1]. Unilateral gain (U), defined by Mason [8.3], is the highest gain of these definitions and is realized by the unilateralization technique, which is to make the reverse gain (S_{12}) zero using only lossless feedback elements. The techniques discussed by Cheng [8.4] show several different networks to unilateralize a circuit. An approach to measure unilateral gain was proposed by Lange [8.5] which reveals that it is possible to build a stable amplifier with a gain of U. A more recent review paper about unilateral gain was published by Gupta [8.6]. To design a stable unilateral amplifier, an exact analysis of the gain and the active device is necessary.

The S-parameter analysis method deduces the following:

1. The maximum available gain, G_{ma}, when the stability factor $k > 1$ and the input and output ports are simultaneously matched:

$$G_{ma} = \left| \frac{S_{21}}{S_{12}} \right| (k - \sqrt{k^2 - 1}) \qquad (8.2)$$

   The S-parameter matrix has two zeroes for this amplifier.
2. The Mason unilateral gain, U, which is the highest possible gain obtained by achieving G_{ma} and unilateralizing the two-port network with lossless feedback [8.1, 8.3]:

$$U = \frac{|(S_{21}/S_{12}) - 1|^2}{2[k|S_{21}/S_{12}| - \mathrm{Re}(S_{21}/S_{12})]} \qquad (8.3)$$

   The S-parameter matrix has three zeroes for this amplifier, and U is considered the highest achievable stable gain at this frequency, independent of the ground terminal.

Equations (8.2) and (8.3) give the gain and are used to evaluate the performance of an active device [8.6]. The gain formulas, G_{ma} and U, only provide the magnitude. The phase angle of S_{21} is not available from the analysis, but this omission will be

removed in the following discussion. Since there are many circuits that will achieve a simultaneous match when $k > 1$, the resulting phase angle of S_{21} is dependent on the particular matching circuits. Therefore, there is no unique answer for the phase angle of S_{21} in many circuits for G_{ma}.

In the following discussion, exact G_{ma} and U amplifier design equations with the phase angle of S_{21} are derived. Further study of the amplifiers with unilateral gain has shown that a phase angle of S_{21} approaching $180°$ is possible, which allows a perfect inverter. A $180°$ phase shift signal has many future applications at frequencies of 18 GHz or higher. The high-frequency limitation depends on the stability of the amplifier. The design of the G_{ma} amplifier and five different types of stable unilateral amplifiers will be presented and verified by commercially available simulation software such as Agilent Advanced Design System, Applied Wave Research Microwave Office, and Ansoft Serenade or Design Suite.

Another point for discussion is the commonly accepted fact that the frequency where $|h_{21}|^2$ is unity is f_t and f_{max} is the frequency where the U is unity. The discussion in Ref. 8.7 would argue that f_{max} is the same for U, G_{ma}, and G_{ms}, a rather controversial conclusion. The conventional theory is that f_t is the frequency where current gain reaches unity and a higher frequency is where U is unity, the f_{max} for the transistor. Above f_{max} the transistor is a passive component; f_{max} is invariant to the common lead, and it is also called the maximum frequency of oscillation.

Maximum Available Gain   The following analysis is based upon problem 1.17 of Ref. 8.1. If two two-ports S_m and S_n are cascaded, the resulting two-port has the following S parameters (Fig. 8.3):

$$S_{11} = S_{m11} + \frac{S_{m12}S_{m21}S_{n11}}{1 - S_{m22}S_{n11}} \tag{8.4}$$

$$S_{12} = \frac{S_{n12}S_{m12}}{1 - S_{m22}S_{n11}} \tag{8.5}$$

$$S_{21} = \frac{S_{n21}S_{m21}}{1 - S_{m22}S_{n11}} \tag{8.6}$$

$$S_{22} = S_{n22} + \frac{S_{n12}S_{n21}S_{m22}}{1 - S_{m22}S_{n11}} \tag{8.7}$$

The G_{ma} amplifier is the cascade of three two-ports (Fig. 8.4). By the above formulas and the assumption of a perfect input and output match, the result shown is

$$S_{21} = \frac{S_{g21}S_{m21}S_{n21}}{(1 - S_{g22}S_{m11})(1 - S_{m22}S_{n11}) - S_{g22}S_{m21}S_{m12}S_{n11}} \tag{8.8}$$

$$S_{12} = \frac{S_{g12}S_{m12}S_{n12}}{(1 - S_{g22}S_{m11})(1 - S_{m22}S_{n11}) - S_{g22}S_{m21}S_{m12}S_{n11}} \tag{8.9}$$

$$S_{11} = S_{22} = 0 \tag{8.10}$$

FIGURE 8.3   Cascade circuit of two-ports S_m and S_n.

FIGURE 8.4   Typical G_{ma} amplifier.

This result gives both the gain and phase of S_{21}, but the phase depends on the particular matching structure. These formulas for S_{21} and S_{12} have been verified in Advanced Design System, Microwave Office, and Serenade. Notice (8.8) for S_{21} bears a startling resemblance to the transducer gain equation, G_T [8.1].

Unilateral Gain   The unilateral gain, which is defined by Mason, has usually been used as a design criterion for transistors because the gain is invariant to the common terminal for an active device. To achieve the unilateral gain, S_{12}, S_{11}, and S_{22} of the four S parameters are reduced to zero using lossless feedback and lossless matching regardless of the value of k. The first method of unilateralizing an amplifier is to use two lossless feedback elements to cancel the real and imaginary parts of S_{12}. This method will turn out an arbitrary angle of S_{21}. Three calculated examples of this method in ADS (Advanced Design System) are given in Figure 8.5 for the MWT-7 MESFET biased at $V_{DS} = 5$ V and $I_D = 28$ mA. The two-port network of circuit A includes two types of feedback interconnection, shunt–shunt and series–series. Circuit B consists of a series–shunt feedback at the input, and circuit C is made up of a shunt–series feedback at the output [8.4]. The resulting performance is shown in Table 8.2.
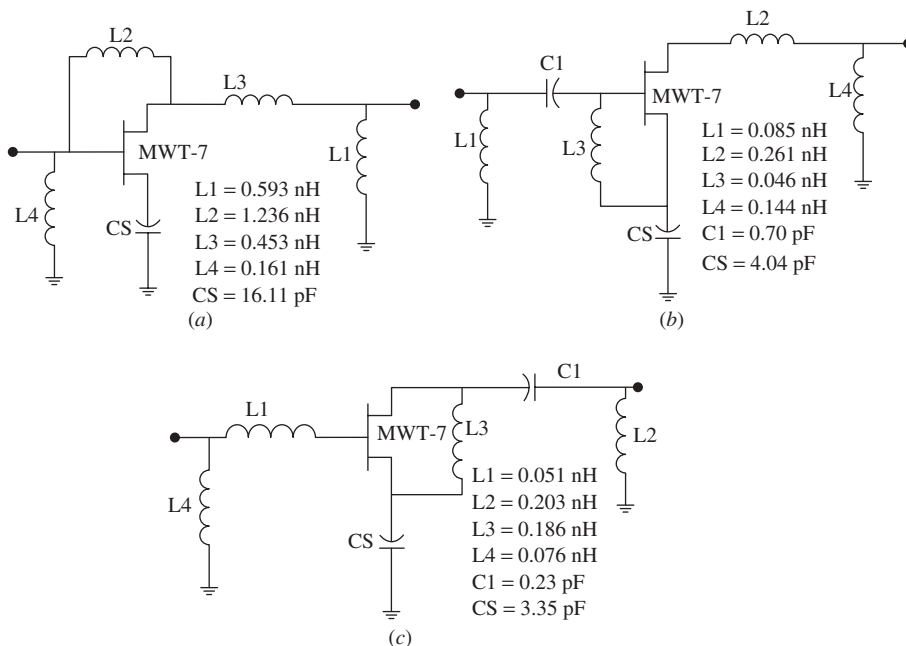
FIGURE 8.5   (*a*) RF schematic of circuit A. (*b*) RF schematic of circuit B. (*c*) RF schematic of circuit C.

TABLE 8.2   *S* Parameters of MWT-7: Circuits A, B, and C at 18 GHz

	S_{11} (dB/deg)	S_{12} (dB/deg)	S_{21} (dB/deg)	S_{22} (dB/deg)
MWT-7	$-2.81/-155.90°$	$-20.00/15.50°$	$4.81/42°$	$-8.57/-89.60°$
Circuit A	$-28.33/0.14°$	$-50.99/-86.95°$	$15.61/91.77°$	$-60.01/-21.80°$
Circuit B	$-59.81/-170.09°$	$-50.99/87.97°$	$15.62/-91.98°$	$-53.91/148.37°$
Circuit C	$-41.80/69.84°$	$-50.99/82.61°$	$15.62/-96.95°$	$-59.94/-69.17°$
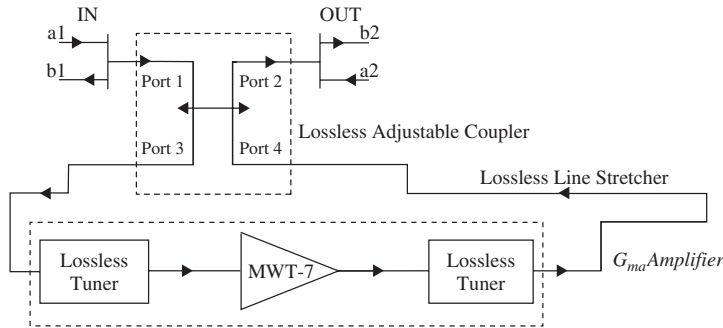
FIGURE 8.6   Unilateral amplifier using a variable coupler and a variable line stretcher.

Another unilateralizing method that uses a variable 90° coupler for the lossless feedback, as proposed by Lange [8.5], is given in Fig. 8.6, which consists of a unilateralizing variable coupler, a line stretcher, and an internal amplifier that is a G_{ma} amplifier. The *S* parameters are given in the following:

1. The *S* parameters of an ideal directional coupler are

$$
S_{lc} = \begin{bmatrix} 0 & C & -jT & 0 \\ C & 0 & 0 & -jT \\ -jT & 0 & 0 & C \\ 0 & -jT & C & 0 \end{bmatrix}
$$

$$
= \begin{bmatrix} 0 & C & T\underline{/-90°} & 0 \\ C & 0 & 0 & T\underline{/-90°} \\ T\underline{/-90°} & 0 & 0 & C \\ 0 & T\underline{/-90°} & C & 0 \end{bmatrix} \tag{8.11}
$$

with $C^2 = 1 - T^2$ and where port 3 is the through port and port 2 is the coupled port.

2. The *S* parameters of a G_{ma} amplifier [Eqs. (8.4) to (8.7)] are defined by

$$
S_{ma} = \begin{bmatrix} S_{11\_ma}\underline{/\theta_3} & S_{12\_ma}\underline{/\theta_2} S_{21\_ma}\underline{/\theta_1} & S_{22\_ma}\underline{/\theta_4} \end{bmatrix}, |S_{21\_ma}|
$$

$$
= \sqrt{G_{ma}} > 1 \text{ and } |S_{12\_ma}| = \sqrt{G_{maR}} < 1 \tag{8.12}
$$

where $G_{maR} = \left| \dfrac{S_{12}}{S_{21}} \right| (k - \sqrt{k^2 - 1})$, G_{maR} being the reverse G_{ma}.

3. The S_{12} and S_{21} of the lossless line stretcher are

$$S_{ls\_12} = 1 \underline{/\phi} \qquad S_{ls\_21} = 1 \underline{/\phi}$$

4. The derivations of S parameters of a unilateral amplifier with $90°$ directional coupler (Fig. 8.6) are given in Appendix D. The results are

$$S_{11} = \frac{b_1}{a_1} = T^2 S_{11\_ma} \underline{/(-180° + \theta_3)} \tag{8.13}$$

$$S_{12} = \frac{b_1}{a_2} = \frac{C \underline{/0°} - \sqrt{G_{maR}} \underline{/(\phi + \theta_2)}}{1 - C\sqrt{G_{maR}} \underline{/(\phi + \theta_2)}} \tag{8.14}$$

$$S_{21} = \frac{b_2}{a_1} = \frac{C \underline{/0°} - \sqrt{G_{ma}} \underline{/(\phi + \theta_1)}}{1 - C\sqrt{G_{ma}} \underline{/(\phi + \theta_1)}} \tag{8.15}$$

$$S_{22} = \frac{b_2}{a_2} = T^2 S_{22\_ma} \underline{/(-180° + \theta_4 + 2\phi)} \tag{8.16}$$

Consider the measurement of S_{12} using Figure 8.6, where the input signal is a_2 at the output port and the reflected signal is b_1 at the input port. For S_{12}, the line stretcher varies the phase such that the coupled portion of a_2 is $180°$ out of phase with the portion of a_2 from the transistor amplifier and the line stretcher. As S_{12} approaches zero to achieve unilateralization, the value of S_{21} is that of the unilateral gain of the transistor amplifier. The derivation of unilateralization is given in Appendix D and the results are

$$S_{12} = 0 \qquad \text{only if} \qquad \phi + \theta_2 = 0° \qquad \text{and} \qquad C = \sqrt{G_{maR}} \tag{8.17}$$

This approach of unilateralization will also produce an arbitrary phase angle of S_{21}. Circuit D in Figure 8.7 uses this approach, and the simulation results are listed in
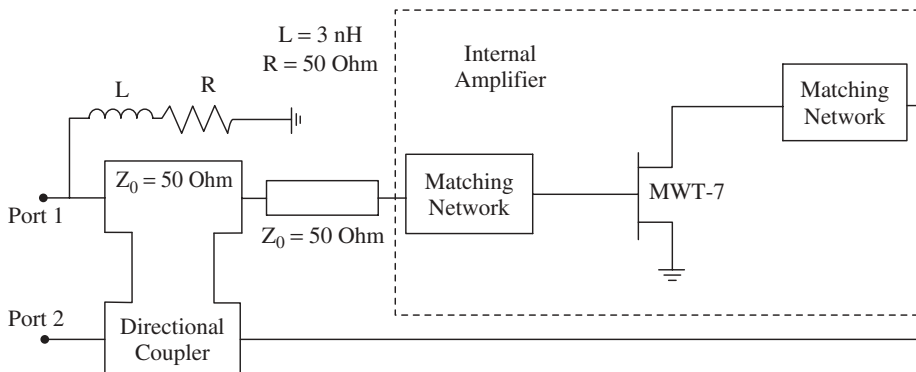
FIGURE 8.7 RF schematic of circuit D.

TABLE 8.3   Performance of Circuits D and E at 18 GHz

	Circuit D		Circuit E	
	Without Parallel R and L at Port 1	With Parallel R and L at Port 1	Without Parallel R and L at Port 2	With Parallel R and L at Port 2
C (dB/deg)	$-14.49/0°$	$-14.50/0°$	$-32.92/0°$	$-33.69/0°$
ϕ (deg)	$-122.00°$	$-120.92°$	$-100.30°$	$105.70°$
S_{11} (dB/deg)	$-30.04/-30.01°$	$-30.20/72.95°$	$-28.68/-19.88°$	$-26.54/-38.01°$
S_{12} (dB/deg)	$-84.00/-54.38°$	$-67.88/-132.45°$	$-80.00/163.14°$	$-70.10/143.23°$
S_{21} (dB/deg)	$15.47/-120.21°$	$15.35/-116.04°$	$15.46/-179.94°$	$15.35/-179.48°$
S_{22} (dB/deg)	$-30.03/104.96°$	$-30.66/137.19°$	$-34.04/26.21°$	$-29.94/38.76°$
Internal amplifier's S_{12}/θ_2 (dB/deg)	$-14.49/121.99°$	$-14.50/121.97°$	$-32.89/100.26°$	$-33.58/105.29°$
Internal amplifier's S_{21}/θ_1 (dB/deg)	$10.32/148.49°$	$10.32/147.47°$	$14.40/100.39°$	$14.46/102.37°$

Table 8.3. The 3-dB bandwidth of S_{21} is typically 10%. Equation (8.17) is a general analysis for this kind of unilateralization technique shown in Figure 8.6.

Now a special condition is discussed as follows. From Eq. (D.10) in Appendix D,

$$S_{21} = -\sqrt{U} \qquad \text{if} \qquad \phi + \theta_1 = 0° \qquad (8.18)$$

Consequently, a perfect inverter at microwave frequencies can be built when the circuits satisfy Eqs. (8.14), (8.15), (8.17), and (8.18), which means $\theta_1 = \theta_2$. A novel circuit topology that fulfills (8.17) and (8.18) is proposed here to achieve a unilateral amplifier with 180° of S_{21}. Circuit E shown in Figure 8.8 is an example for the new topology. The feedback amplifier consists of a CS transistor, matching networks, and a parallel–parallel feedback network, which makes the phase angles of S_{21} and S_{12} of the internal amplifier the same. This result also includes both magnitude and phase for the unilateral gain, which was verified on ADS.
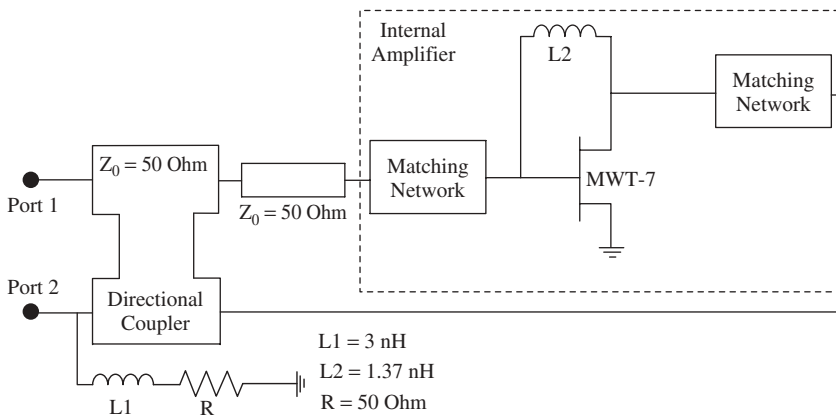
FIGURE 8.8   RF schematic of circuit E.

Verification The MWT-7 MESFET from Microwave Technology, where the bias conditions are $V_{DS} = 5$ V and $I_D = 28$ mA, is used in circuits A, B, C, D, and E for the same operational frequency, 18 GHz. The k factor is 1.117 and the G_{ma} [(8.2)], is 10.32 dB. The theoretical U is 15.47 dB from Mason's equation,(8.3). Using the loss-less feedback elements to unilateralize the MESFET, the three topologies in Figure 8.5 give the required unilateral gain and various phase angles of S_{12} and S_{21}. The results are shown in Table 8.2. The three values of S_{21} in decibels, which are equal to the unilateral gains, approach the theoretical values. All three circuits are designed to be stable by the topology of the shunt inductor (low-frequency stability) of the input and output matching networks. Using the stability circles to check these three cases, circuits A, B, and C are stable from 1 to 18 GHz, even where $k < 1$, which means the circuits are conditionally stable.

Using the topology recommended in Ref. 8.5, the resulting circuit for unilateral gain is given in Figure 8.7. The internal amplifier of circuit D is a G_{ma} amplifier. Table 8.3 illustrates the simulation results of circuit D that satisfies (8.11) to (8.17) and is a typical unilateral amplifier. For circuit D, θ_1 is not equal to θ_2. Therefore, the phase angle of S_{21} is not 180°. The internal amplifier of circuit E is a feedback amplifier and its results are also listed in Table 8.3. The phase angle of S_{12} of the amplifier and line stretcher is 180°, so it will cancel the coupled signal from the out port to the in port precisely. Circuit E's θ_1 is equal to θ_2. The phase angle for circuit E is 180° for S_{21}, which fits (8.18).

In Figures 8.7 and 8.8, the parallel resistors in ports 1 and port 2 are used to make the two circuits stable at low frequencies and have no significant effect on gain. For these resistors, the S_{21} of the two circuits will decrease 0.1 dB compared to the S_{21} without resistors. Using the stability circle method to verify the stability, both circuits D and E are stable.

The material presented for the design procedure of a unilateral amplifier may be summarized by three different procedures:

1. For circuits A to C, try various forms of lossless feedback using two elements to reduce $|S_{12}|$ to below −50 dB, which will bring k above 1. Then match the input and output with standard lossless matching structures, M_1 and M_2.
2. For circuit D, the k must be greater than unity, so you design a G_{ma} amplifier with M_1 and M_2 in the usual way. Then you adjust the variable coupler and the line stretcher to cancel $|S_{12}|$ to below −50 dB. This will produce an S-parameter matrix with three zeroes, and the angle of S_{21} will often approach 180°.
3. Beginning with circuit D, an additional form of feedback is added to the G_{ma} amplifier to produce circuit E. For the example in this section, this was an inductor which produces an angle of 180° for both S_{21} and S_{12}, which becomes a perfect inverter at 18 GHz. This can be used to produce an active balun, an important component for many circuits. Due to low-frequency considerations, a stabilizing network may be necessary which has a very small effect on the resulting gain.

Hopefully, some realizations of these amplifiers will be reported soon with band-widths of about 10% and gains of 4 to 6 dB higher than other conventional approaches.

Conclusions The design of amplifiers for G_{ma} and U has been presented in a new form, where the G_{ma} amplifier design has many phase solutions determined by the form

of the lossless matching circuits. Once the internal amplifier design is determined, the unilateralized amplifier may be achieved with a coupler and line stretcher, which is demonstrated by circuit D. The value of the coupling factor of the coupler is simply the $|S_{12}|$ of the G_{ma} amplifier. A new topology is proposed (circuit E) which makes the phase angle of U approximately $180°$, which is the same value for the low-frequency S_{21} of the CE or CS transistor, which will have many applications in microwave circuits (e.g., active baluns). The equations for the specified topology of a variable coupler and a line stretcher give both the magnitude and phase of S_{21}, which is another new feature in this discussion. From the results of this section, it is possible to design an amplifier with unilateral gain and an arbitrary phase angle of S_{21}.

8.2.3 Low-Noise Amplifier

The key to this design is the lossless input matching circuit, which must present Γ_{on} to the input of the transistor. This will result in an imperfect match at the input but the lowest noise figure. The output is conjugately matched for highest gain. A low-noise design must be stable, so stability considerations in the operating band may be ignored for the first-order design, but stability should be checked in all bands before the amplifier is realized.

Noise circles in the Γ_g plane will determine the effects of mismatching on the resulting noise figure, given as

$$F_x = F_{\min} + \frac{R_n/R_x[(R_x - R_{on})^2 + (X_x - X_{on})^2]}{|Z_{on}|^2} \tag{8.19}$$

where F_x = noise figure at generator impedance of Z_x

$\quad Z_x = R_x + jX_x$

$\quad F_{\min}$ = NF at generator impedance of $Z_{on}(Z_{opt})$

$\quad Z_{on} = R_{on} + jX_{on}$

The gain is the available gain G_A, sometimes called the associated gain, since the amplifier output is always conjugately matched, so $S_{22} = 0$ for the amplifier.

The noise circle equations are

$$\text{Center} = C_F = \frac{\Gamma_{on}}{1 + N} \tag{8.20}$$

$$\text{Radius} = R_F = \frac{\sqrt{N^2 + N(1 - |\Gamma_{on}|^2)}}{1 + N} \tag{8.21}$$

where

$$N = \frac{|1 + \Gamma_{on}|^2(F - F_{\min})}{4r_n} \tag{8.22}$$

$$r_n = \frac{R_n}{Z_0} \tag{8.23}$$

$$F = F_{\min} + \frac{4R_n|\Gamma_G - \Gamma_{on}|^2}{|1 + \Gamma_{on}|^2(1 - |\Gamma_G|^2)} \tag{8.24}$$

Numerous examples of this description of noise circles are found in the literature [8.1]. Since all CAD packages will plot noise circles, further discussion is unnecessary. See Ref. 8.8 for further discussion of these concepts.

The problem of an imperfectly matched input port may be solved by using a balanced amplifier configuration, first suggested by Bell Labs in 1965 [8.9, 8.10]. The balanced amplifier is used in many applications where cascading individual stages are required and of course stability is also required. In microstripline, the Lange coupler [8.11] is used to provide the required 3-dB coupler.

The balanced amplifier configuration is shown in Figure 8.9 along with two alternate design procedures. The basic concept is to use two identical amplifiers inserted between two 3-dB couplers. If the amplifier stages are identical (Fig. 8.10),

$$S_{11} = \frac{1}{2}(S_{11a} - S_{11b}) = 0 \tag{8.25}$$
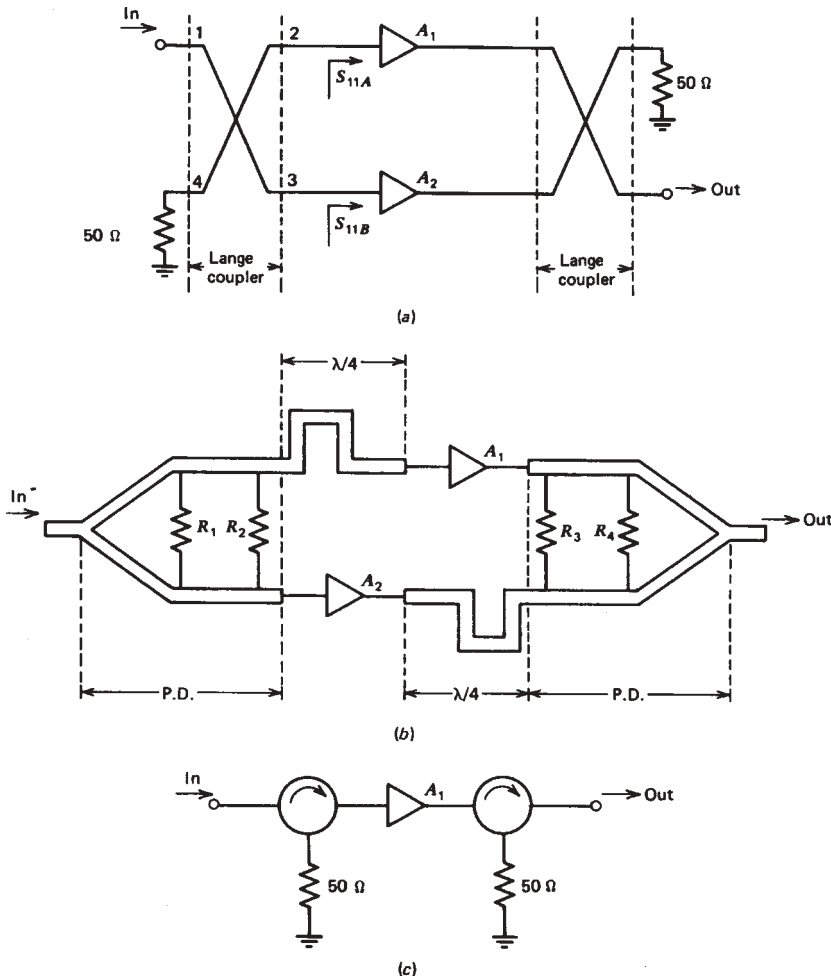
FIGURE 8.9 Low-VSWR amplifiers: (*a*) balanced amplifier using 3-dB Lange coupler; (*b*) balanced amplifier using 3-dB Wilkinson power divider (P.D.); (*c*) isolator amplifier.
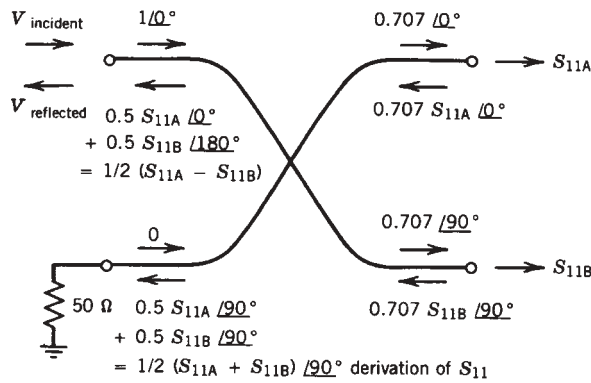
FIGURE 8.10   Analysis of 3-dB directional coupler.

$$S_{21} = \frac{1}{2}(S_{21a} + S_{21b}) = S_{21a} = S_{21b} \tag{8.26}$$

$$S_{22} = \frac{1}{2}(S_{22a} - S_{22b}) = 0 \tag{8.27}$$

$$F = \frac{1}{2}(F_a + F_b) \tag{8.28}$$

The gain is the average gain and the noise figure is the average value. If one stage is open circuited, the gain will decrease by 6 dB, so-called graceful degradation. The reflected power ends up at the 50-Ω termination of the coupler. This is shown in Figure 8.10 for an ideal, lossless 3-dB coupler. Two back-to-back lossless couplers may be considered a "0-dB gain amplifier," which is the first step in the design of balanced amplifiers. For larger bandwidths, an overcoupled design is needed, that is, 1.5 to 2.5 dB, which introduces ripple but increases the bandwidth significantly.

Another way to solve the input mismatch is the use of Wilkinson in-phase power splitters. In this case, a quarter-wavelength phase shift is introduced into the input of one stage and the output of the other stage. The resulting reflections are absorbed by the 100-Ω termination of the Wilkinson; see Figure 8.9b. The third choice is using isolators (Fig. 8.9c).

Still another way of designing LNAs with good input match is the use of lossless feedback, where Γ_{on} is made equal to $S_{11}^{'*}$, as discussed in Refs. 8.12, 8.12a, and 8.13. The usual solution is to use a common-source inductor to resonate the C_{gs} capacitor; this results in a LNA with a noise figure of F_{min} and an input reflection coefficient of $S_{11} = 0$.

8.2.4   High-Power Amplifier

This type of amplifier should be considered the dual of the LNA. Instead of matching M_1 for best noise figure, we match M_2 for best output power. If the data sheet does not provide the value of Γ_{0p}, we can estimate the value from the dc curve tracer response [8.14].

In analogy to noise circles, the output power ellipses (or roughly circles) may be plotted in the Γ_L plane to determine the effects of mismatching in the output. This

is only an intuitive way of understanding the design, and a more accurate procedure requires using the nonlinear device model and a harmonic balance calculation for the dynamic load line (see Fig. 1.25) and the output power spectrum at the load. Because the HPA is the dual of the LNA, we can find lossless feedback circuits which will make Γ_{0p} become $S_{22}^{'*}$; in other words, maximum power will be given with $S_{22} = 0$ for the total amplifier structure, which can be a difficult task without the use of lossless feedback. A feedback resistor may be required to raise the third order intercept (TOI) which will surely lower gain slightly. Gain can be easily achieved, but the TOI is often the main criterion.

The analogous equation to (8.19) for HPA is

$$G_x = G_{\max} - \frac{R_p/R_x[(R_x - R_{0p})^2 + (X_x - X_{0p})^2]}{|Z_{0p}|^2} \tag{8.29}$$

where G_x = large-signal power gain at load impedance of Z_x
  $Z_x = R_x + jX_x$
  $G_{\max}$ = large-signal power gain at load impedance of $Z_{0p}(Z_{\text{opt}})$
  $Z_{0p} = R_{0p} + jX_{0p}$

This describes the large-signal gain circles in the Γ_L plane. Since this is really determined by the nonlinear model of the transistor, however useful, this linear approach is only a first-order approximation.

We must also pay attention to the thermal impedance of the transistor and the maximum junction or channel temperature of the transistor, which is normally considered to be $200°C$ for Si, $175°C$ for GaAs, and $155°C$ for SiGe, in order to ensure long-term reliability.

Another consideration for power amplifier design is the difference between balanced stages using $90°$ couplers and push–pull amplifiers using $180°$ baluns. For some unknown reason, microwave designers tend to use the former, while RF designers use the latter. Recent studies at 2 GHz using MESFETs show the difference is very small. The balanced amplifiers gave better output match due to coupler performance, but push–pull amplifiers were only 6 dB worse in the output match. The primary difference in these two approaches has to do with which harmonics and intermodulation products are canceled [8.15].

The large-signal effects of MESFETs may be described by AM/AM and AM/PM measurements [8.16], which are illustrated in Figure 8.11 for a 1-W MESFET at 6 GHz, the MWT-17 from *Microwave Technology*. This transistor has a gate geometry of about $1 \, \mu m \times 2400 \, \mu m$, which was found to be optimum for about 1.5- to 2.5-GHz wireless applications. The AM/AM distortion is described by changes in $|S_{21}|$ versus P_{in}, and the AM/PM is described by changes in $<S_{21}$ versus P_{in}. The chip was measured in a 50-Ω system with tuners added to tune the device to the maximum power and gain point. The small-signal gain was 7.5 dB with a phase angle of zero; as the input power increases beyond 19 dBm (the P_1dBc point), the gain drops rapidly and the phase angle increases nonlinearly. Finding nonlinear models which also behave in this fashion is a challenging and necessary part of the design; the Angelov model mentioned in Chapter 3 seems to also produce these large-signal effects.

(a)

(b)
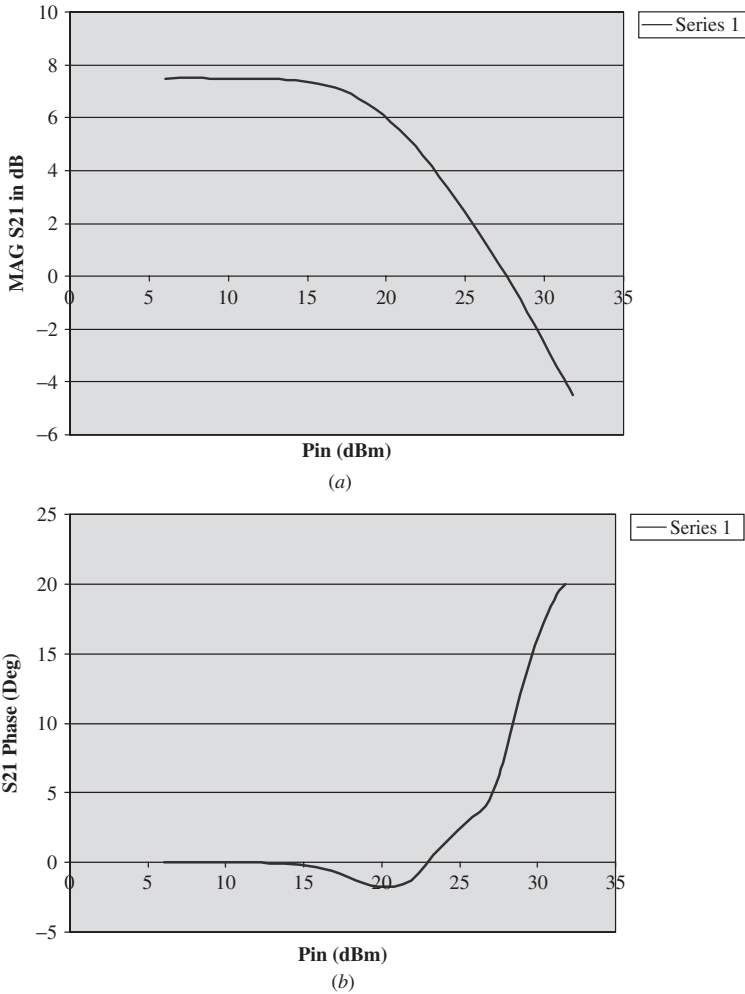
FIGURE 8.11   Large-signal distortion of MWT-17 MESFET.

8.2.5 Broadband Amplifier

For this type of amplifier, the highest possible gain at f_2 is required and the gain must be made flat by mismatch at the input and output. This is usually accomplished on the computer with either S parameters or the nonlinear model.

In Chapter 5 we discussed a 6- to 18-GHz MESFET amplifier design using distributed matching elements. There are numerous solutions to this type of design, but be sure the design is stable at all frequencies.

Resistive feedback may also be used for broadband amplifiers with reduced gain.

8.2.6 Feedback Amplifier

By using resistive feedback, broadband amplifiers with reduced gain and good matches are produced in high quantity today. In this case engineers do not have to use the Smith

chart. These amplifiers are unconditionally stable at all frequencies, and they can be easily cascaded for higher gain. The first microwave feedback amplifier was developed by Avantek [8.17].

This design began with the compound feedback circuit with RE and RF chosen for $S_{11} = S_{22} = 0$ at low frequencies using silicon BJTs. Then about 1982 the MODAMP (Monolithic Darlington Amplifier) [8.18] followed and was in full-scale production by 1985. This configuration is shown in Figure 8.12. The basic idea is to extend compound feedback to a higher gain configuration with broadband performance but forget about gain flatness, which is not always important. This type of silicon MMIC (available from Agilent and Mini-Circuits) is produced in high volume and sells for less than $1 in high quantity. This type of stable amplifier is very popular among engineers who do not understand Smith charts but need to test some prototype system which needs gain with low cost. The MODAMP fulfills this need very nicely.

The detailed derivations of the compound feedback circuit are found in Ref. 8.1, and the derivations of the MODAMP have never been published. The MODAMPs were all designed using PSPICE and a modified Gummel–Poon model for the BJT devices. Notice that the bias circuit cannot be separated from the RF circuit because monolithic capacitors would occupy far too much real estate; the dc blocking capacitors are used external from the monolithic circuit. This series of amplifiers basically provides different output powers at P_1dBc, up to 1 W output power. The biasing is primarily determined by the current, where the voltage is relatively unimportant.

Another view of lossless feedback amplifiers is presented here. There are basically three types of useful lossless feedback amplifiers:

1. High-gain unilateralized amplifiers [8.3, 8.15]
2. LNA amplifiers designed for $S'_{11} = 0$ [8.11, 8.12]
3. HPA amplifiers designed for $S'_{22} = 0$ (the dual of 2)

The third group may have lower power gain, and $S'_{22} = 0$ is unnecessary for most applications. It can always be achieved by a balanced configuration if needed.

The effect of feedback in amplifier circuits can be expressed by series elements in the nonfeedback circuit of Figure 8.13 for series feedback and by parallel elements for
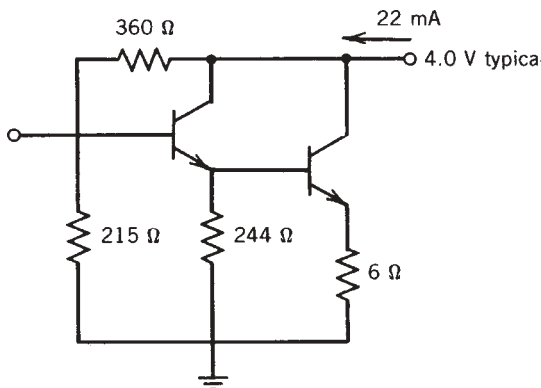
FIGURE 8.12   MODAMP schematic (MSA 07).
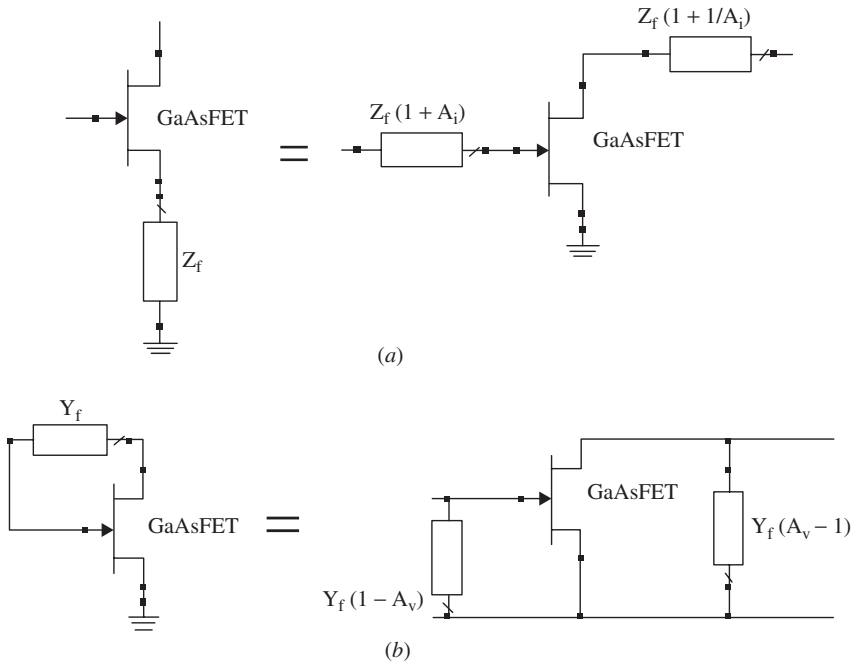
FIGURE 8.13   Feedback circuits.

the parallel feedback, also shown in Figure 8.13. The analysis for the series feedback case follows.

Consider the series combination of Z_f and the two-port Z. This is equivalent to the two-port with two series elements, one on the input with a voltage drop of $(1 + A_i)Z_f$ and one on the output with a voltage drop of $(1 + 1/A_i)Z_f$. This is simple to show since

$$I_1 + I_2 = I_1(1 + A_i) \tag{8.30}$$

$$I_1 + I_2 = I_2(1 + 1/A_i) \tag{8.31}$$

and the laws of linear superposition apply.

For the parallel feedback case, consider the parallel combination of Y_f and the two-port Y. This is equivalent to the two-port with two parallel elements, one on the input and one on the output, with values given by

$$Y_1 = \frac{I_1}{V_1} = Y_f(1 - A_v) \tag{8.32}$$

$$Y_2 = \frac{I_2}{V_2} = Y_f(A_v - 1) \tag{8.33}$$

Thus the equivalence in Figure 8.13 has been shown.

The case of a parallel resistor is of interest since the input and output power lost can be easily calculated and is small if the resistor is large.

8.2.7 Cascode Amplifier

In 1948 MIT researchers investigated the best configuration for low-noise figure from a two-stage vacuum tube amplifier [8.19]. They found that a common cathode–common grid configuration gave the best noise figure from the nine possibilities and named it the cascode. This name is still used today, especially for the common source–common gate FET configuration, which is widely used for high-gain applications.

An example using this concept is the design of an HBT amplifier using the BFP 620 SiGe HBT from Siemens/Infineon for a 1- to 4-GHz amplifier using the library nonlinear model in Serenade. Lumped-element Π-networks were used for the matching. The individual HBTs were biased at $I_C = 14$ mA and $V_{CE} = 2$ V (approximately). The gain is 22 ± 2 dB and the noise figure is less than 3 dB. The input/output match is poor, but this can be solved by the techniques given in Chapter 4 (balancing, feedback, etc.). The matching circuits are low-pass Π networks, where often one capacitor is essentially zero. The initial design was for a narrow-band 4-GHz amplifier which turned out to be a relatively flat gain design over 1 to 4 GHz with a gain of about 22 dB.

After optimization of the input and output circuits over 1 to 5 GHz, the performance improved to (Fig. 8.14)

$$\text{Gain} = 22.0 \pm 1 \text{ dB}$$

$$\text{NF} = 2.9 \text{ dB maximum}$$

$$|S_{11}| = -2.5 \text{ dB typical}$$

$$|S_{22}| = -2.5 \text{ dB typical}$$

(a)
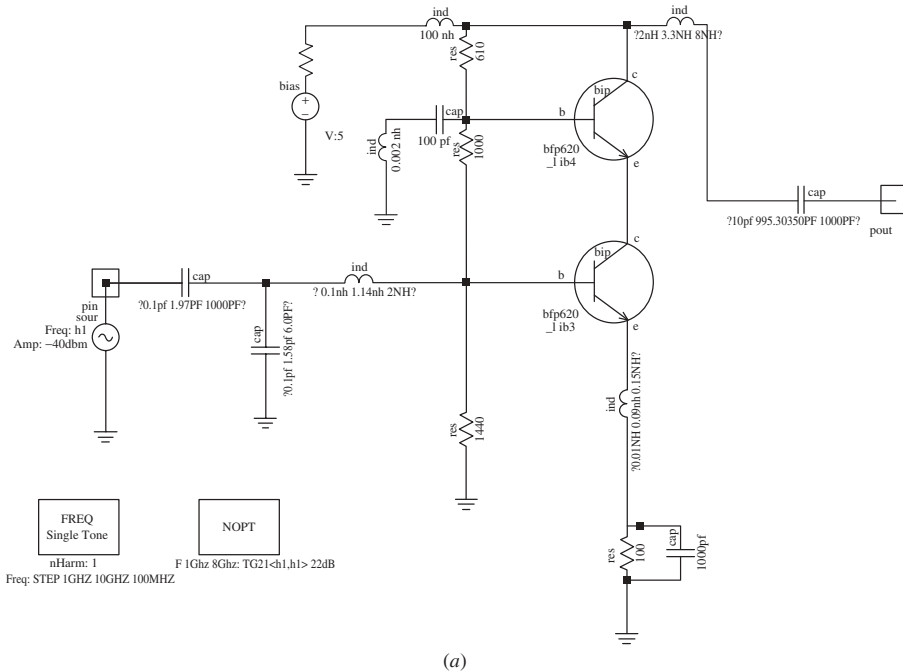
FIGURE 8.14 A 1- to 5-GHz cascode amplifier: (a) schematic; (b) gain; (c) noise figure.

Ansoft Corporation - Harmonica ® v8.7
opt8ghz_cascode01.ckt

(*b*)

Ansoft Corporation - Harmonica ® v8.7
opt8ghz_cascode01.ckt

(*c*)
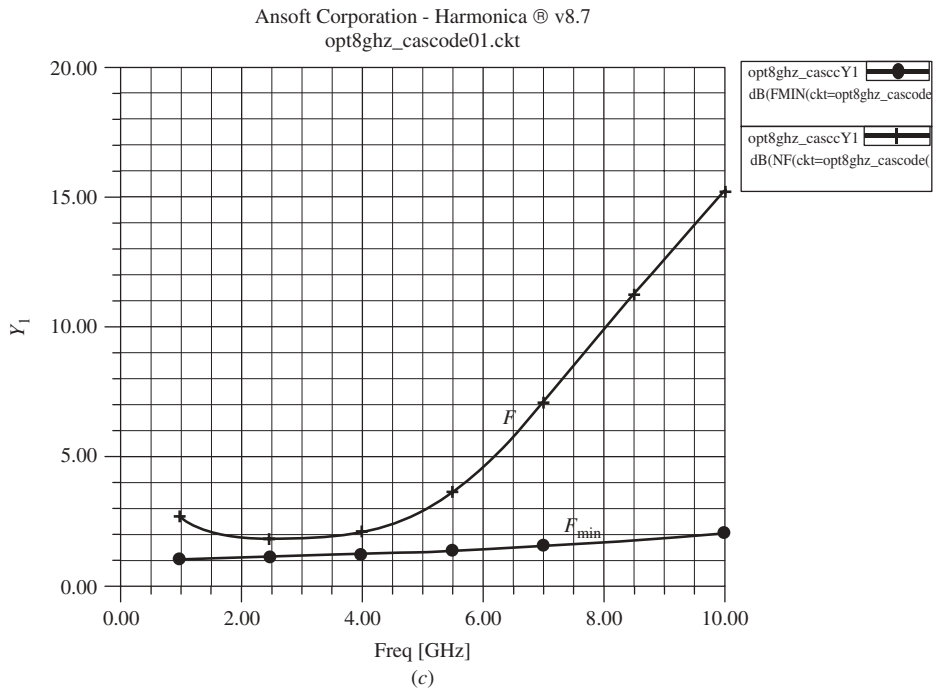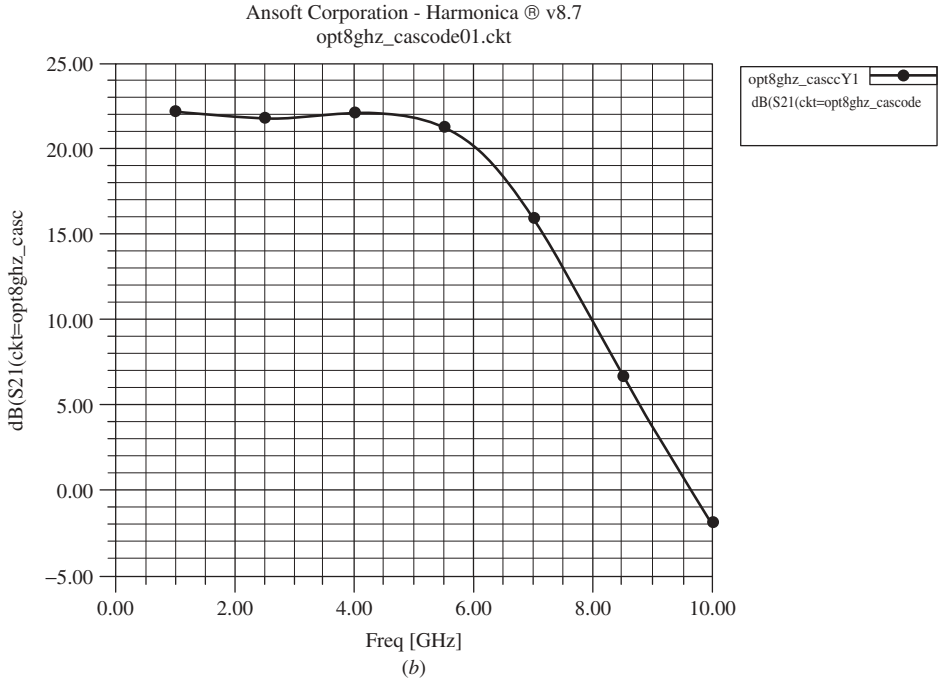
FIGURE 8.14 (*continued*)

After optimization over 1 to 8 GHz, the performance improved to (Fig. 8.15)

$$\text{Gain} = 22.0 \pm 0.3 \text{ dB}$$

$$\text{NF} = 2.0 \text{ dB maximum (2--8 GHz)}$$

$$|S_{11}| = -4.0 \text{ dB typical}$$

$$|S_{22}| = -5.0 \text{ dB typical}$$

The dc biasing circuit is given in Figure 8.16 for a supply voltage of $V_{CC} = 5.0$ V. The transistors are biased as follows:

	Q_1 (bottom)	Q_2 (top)
V_{BE}	0.853 V	0.853 V
V_{CE}	1.63 V	1.89 V
I_B	89 μA	88 μA
I_C	14.0 mA	13.9 mA

Thus the current gain β is about 157 for these transistors. The base-current feed is about 1 mA, or more than 10 times the base current.

The total Serenade-derived schematic and performance are given in Figure 8.17 for the 1- to 8-GHz design. The values for three designs are given in Table 8.4, showing the decrease of parameter values as frequency is increased.

(*a*)
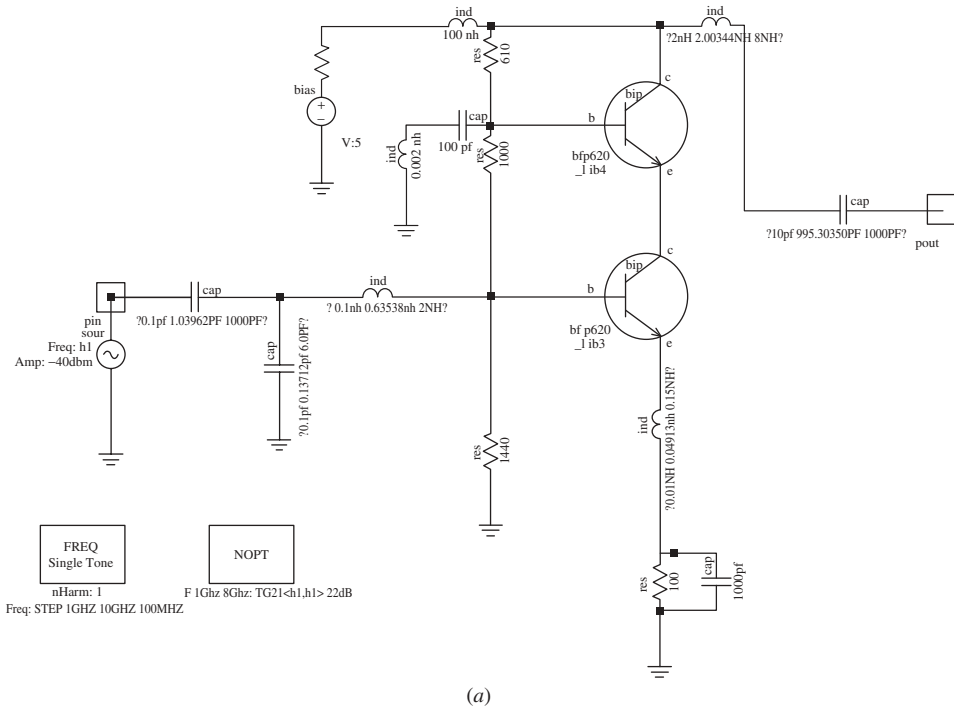
FIGURE 8.15 A 1- to 8-GHz cascode amplifier: (*a*) schematic; (*b*) gain; (*c*) noise figure.

(b)

(c)
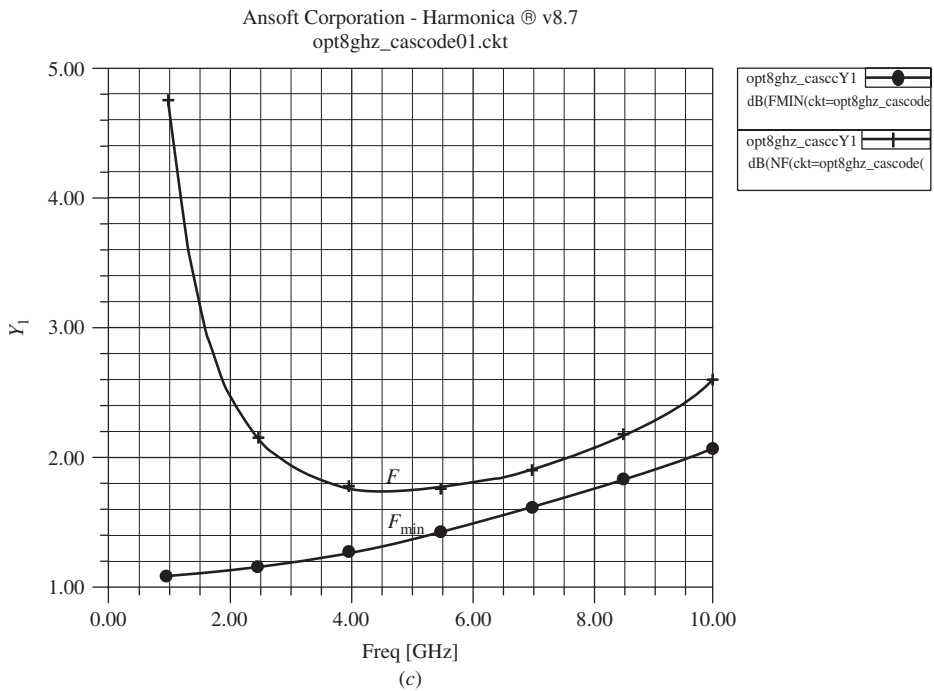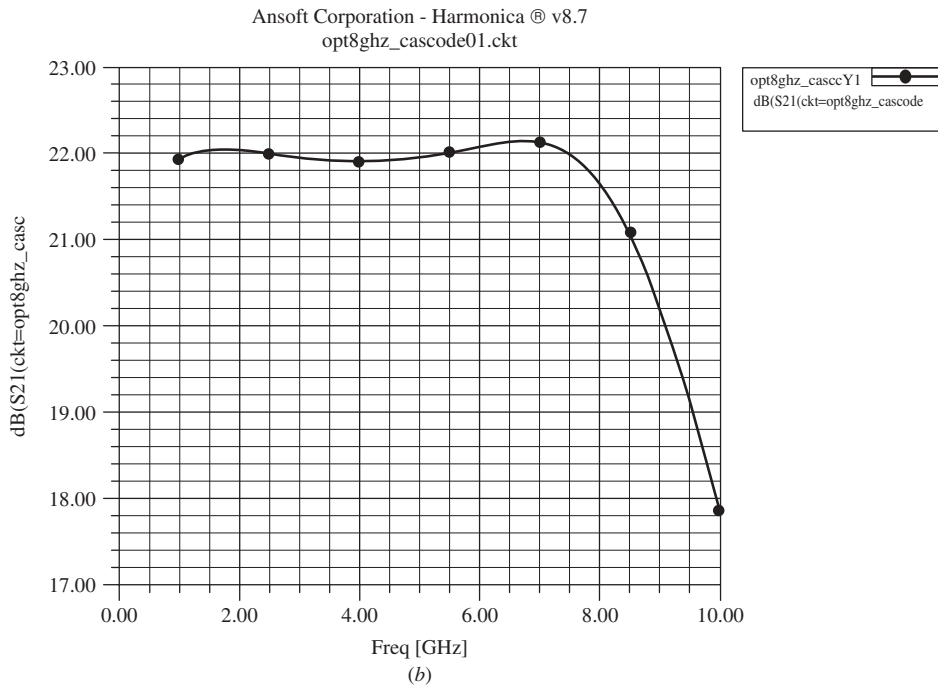
FIGURE 8.15   (*continued*)
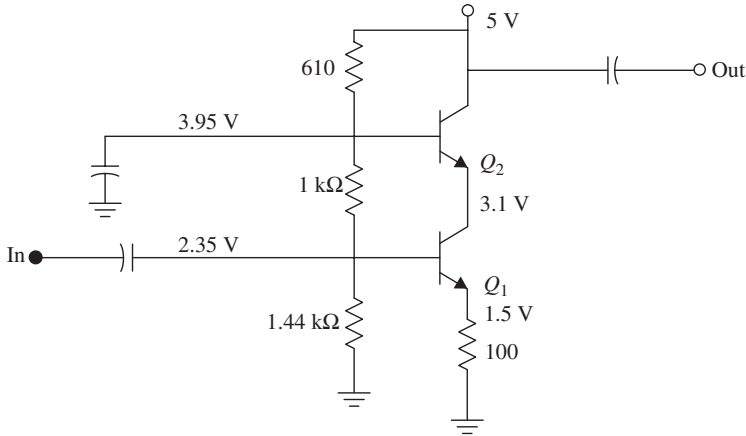
FIGURE 8.16   Bipolar cascode dc bias schematic.
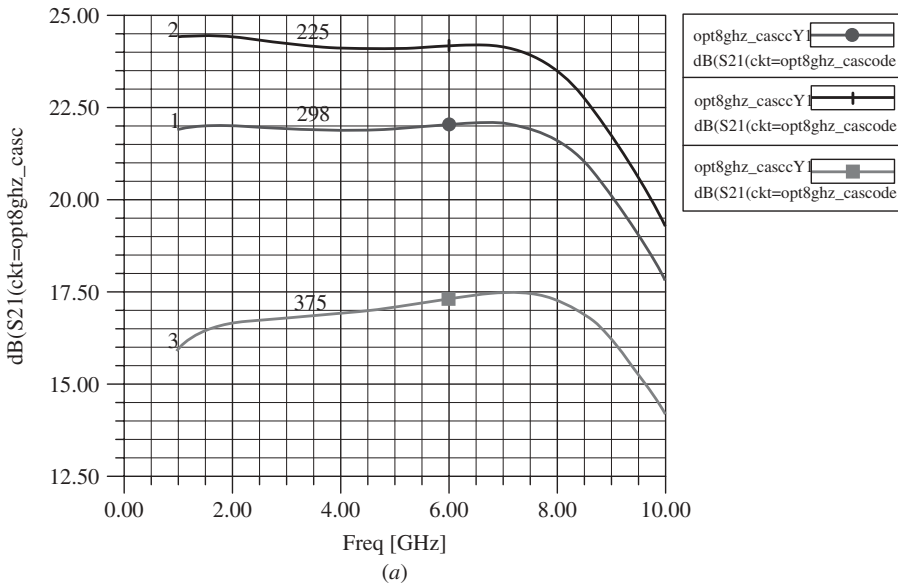
FIGURE 8.17   A 1- to 8-GHz cascode amplifier including temperature effects.

The noise figure of the third design is within 0.2 dB of F_{min} at 8 GHz, but it rises rapidly below 2 GHz, probably due to the input blocking capacitor (C_1), which helps to flatten the gain at low frequencies. All of the optimization was based upon gain using the nonlinear model of this very advanced Si–Ge HBT. The data sheet nonlinear Gummel–Poon model for BFP 620 is given in Table 8.5.

After further optimization a nominal gain of 24 dB was achieved over 1 to 8 GHz. This performance is given in Figure 8.17, which includes the temperature response of this amplifier. Circuits for temperature compensating the gain are found in Refs. 8.20 and 8.21. Also, *pnp* active bias circuits may be used to perform this temperature
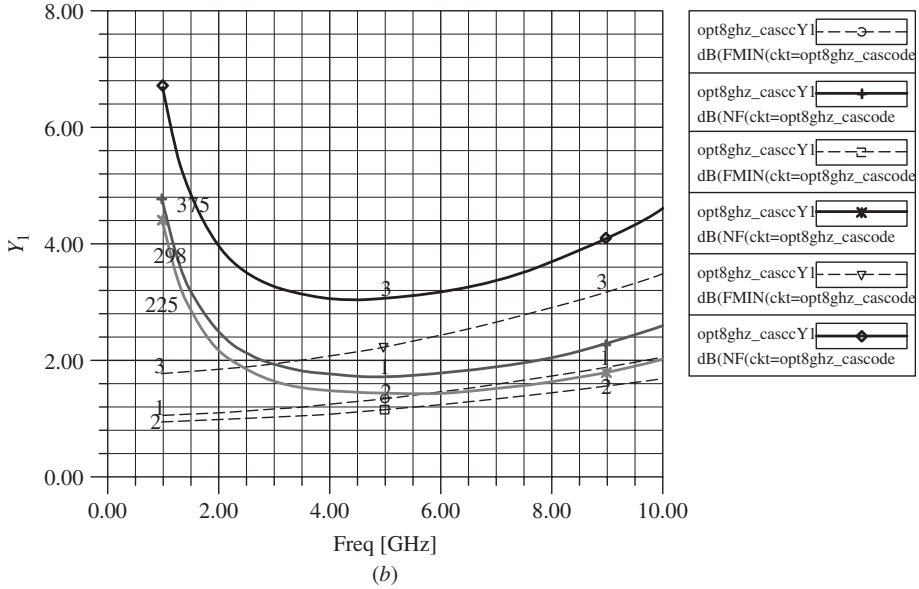
FIGURE 8.17 (*continued*)

TABLE 8.4   Cascode Amplifier Circuit Parameters

Design	C_1 (pF)	C_2 (pF)	L_1 (nH)	C_3 (pF)	L_2 (nH)	C_5 (pF)	L_S (nH)
Unoptimized, 1–5 GHz	1000	3.4	1.0	1.0	4.0	0.03	0.12
Optimized, 1–5 GHz	1.97	1.58	1.14	—	3.30	—	0.09
Optimized, 1–8 GHz	1.04	0.14	0.64	—	2.00	—	0.05

TABLE 8.5   Gummel–Poon Model for Siemens BFP620: Transitor Chip Data

IS = 0.22 fA	BF = 425	NF = 1.025
VAF = 1000 V	IKF = 0.25 A	ISE = 21 fA
NE = 2	BR = 50	NR = 1
VAR = 2 V	IKR = 10 mA	ISC = 18 pA
NC = 2	RB = 3.129 Ω	IRB = 1.522 mA
RBM = 2.707 Ω	RE = 0.6	RC = 2.364 Ω
CJE = 250.7 fF	VJE = 0.75 V	MJE = 0.3
TF = 1.43 ps	XTF = 10	VTF = 1.5 V
ITF = 2.4 A	PTF = 0°	CJC = 124.9 fF
VJC = 0.6 V	MJC = 0.5	XCJC = 1
TR = 0.2 ns	CJS = 128.1 fF	VJS = 0.52 V
MJS = 0.5	NK = −1.42	EG = 1.078 eV
XTI = 3	FC = 0.8	TNOM = 298 K
AF = 2	KF = 7.291×10^{-11}	
TITF1 −0.0065	TITF2 1.0×10^{-5}	

Note: All parameters are ready to use; no scalling is necessary.

TABLE 8.6   Temperature Response of Cascode Amplifier (1–8 GHz)

Temperature (K)	I_C (mA)	Gain (dB)	NF (dB)
225	18.4	25.2	1.5 (max)
298	15	24	1.55 (max)
375	12.7	23	1.6 (max)

compensation function [8.1] for both BJT and FET circuits, which was discussed in the first part of this chapter.

The idea of active bias is to keep the collector/drain current constant over temperature. These circuits were given earlier in this chapter. Another common technique is to build a *pin* diode attenuator which can give a gain–temperature characteristic opposite to that of the amplifier gain versus temperature (see Table 8.6). Both circuits need to have flat gain over the operating bandwidth.

We must also consider the junction temperature of the transistor by using the thermal impedance:

$$R_{\text{th}} = R_{\text{th},JS} + R_{\text{th},JA} = 300 + 100 = 400 \text{ K/W}$$

where $R_{\text{th},JS}$ is the junction-to-substrate thermal impedance (taken from the data sheet) and $R_{\text{th},JA}$ is the additional thermal impedance to the ambient (which is estimated here on the low side).

At 375 K ambient, $T_{\max} = R_{\text{th}} P_{\text{dc}} = 400 \times (1.75 \times 0.0127) = 8.89$ K, so the junction temperature is 384 K, or 111°C, well below the maximum value of 150°C given on the data sheet.

8.2.8   Multistage Amplifier

When more gain is needed, a multistage amplifier is required. The interstage design may be realized with two lossless elements, or four lossless elements if the 50 Ω reference impedance is in the middle of the network. Examples of the interstage network are shown in Figure 8.18 for HGAs, LNAs, and HPAs. A recommended matching technique is to locate the larger $|\Gamma|$ (or its conjugate) and move it toward the smaller $|\Gamma|$.

The stability of a multistage amplifier is more difficult to guarantee, since both stages must be independently checked for stability at all frequencies. Therefore, four Smith charts of stability must be examined for a two-stage amplifier.

Another problem with multistage amplifiers (or for all amplifiers) is the gain variation over temperature. This is usually accomplished by inserting a variable-gain *pin* diode attenuator which has the opposite temperature behavior to that of the rest of the amplifier.

There are at least three types of multistage amplifiers:

Cascaded stages where the gain multiplies (or adds, in decibels)

Distributed stages where the gain is additive

Matrix stages where the gain is both additive and multiplicative
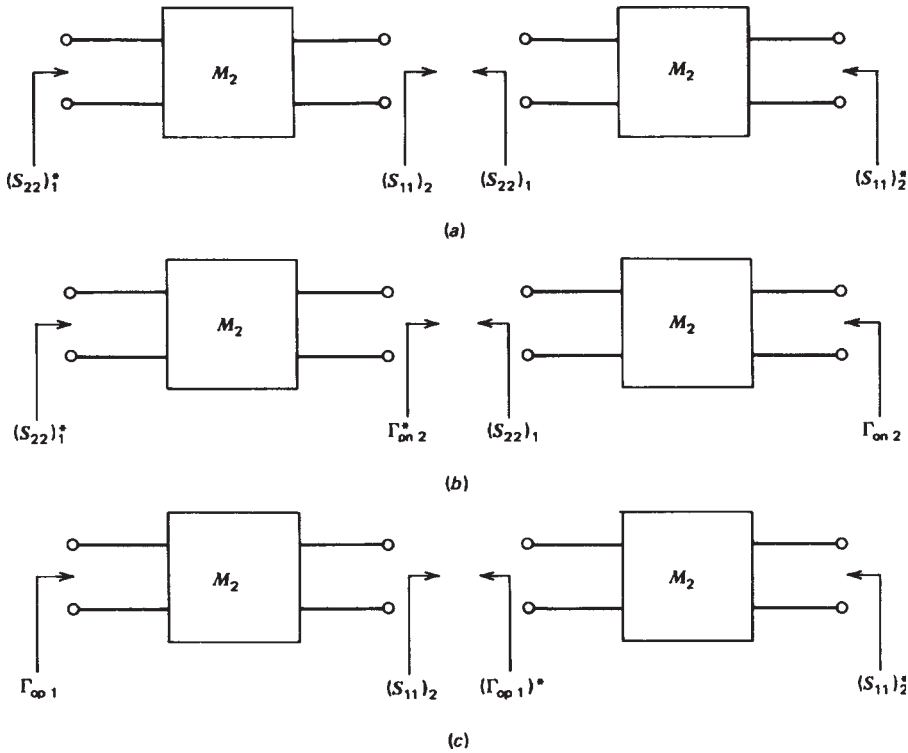
FIGURE 8.18   Interstage designs (assuming $S_{12} = 0$): (*a*) high-gain interstage; (*b*) low-noise interstage; (*c*) high-power interstage.

The formation of these three types of amplifiers is easily demonstrated and the last two types are discussed in the next section, but usually we build cascaded stages which could be balanced for ease in final assembly. Another type of multistage amplifier is the Darlington MODAMP discussed in the feedback section of this chapter.

8.2.9   Distributed Amplifier and Matrix Amplifier

The idea for the distributed (or traveling-wave) amplifier was disclosed in 1937 [8.22]. It has been widely applied since 1948 [8.23] using vacuum tubes to build wide-band amplifiers using lumped-element terminated transmission lines, where FETs or BJTs can also be used to provide the capacitance of the line. Lumped inductors or at higher frequencies transmission lines are being used to create an artificial transmission line which neutralizes the band-limiting effects of the tube's grid–cathode capacitance or the transistor's input gate–source capacitance. If the phase velocities on the input and output transmission lines are equal, the gain is additive; as more stages are added to the amplifier, the gain and output power increase, and the noise figure reduces. Elementary distributed- or traveling-wave amplifiers are found everywhere in the literature [8.1].

The upper frequency may be predicted from the cutoff frequency of the transmission line:

$$f_c = \frac{1}{\pi \sqrt{L_{\text{in}} C_{gs}}} \tag{8.34}$$

and the gain is approximately

$$A_v = \frac{1}{2}n \ g_m R_L \tag{8.35}$$

so higher frequencies may be achieved by simply reducing C_{gs}. The voltage gain is divided by 2 because 1/2 of the output wave travels to the drain terminating resistor where it is absorbed. A Smith chart of the input impedance of a lumped-element transmission line terminated in Z_0 is given in Figure 8.19 versus frequency; if the first series element is an inductor, the impedance approaches infinity at high frequencies above f_c, the cutoff frequency of the line. On the other hand, if the first element is a shunt capacitor, the input impedance approaches a short circuit at high frequencies.

Cascode FET devices are particularly well suited for this type of amplifier [8.24–8.26]. Bipolars generally have high C_{EB}, which would limit the upper frequency, but with HBT devices, this does not seem to be a problem.

Several additional forms of this amplifier have been disclosed. The distributed-matrix amplifier (Fig 8.20) consists of several distributed amplifiers inductively coupled in parallel, which gives very good noise figure, higher gain, and a very small circuit size. The distributed-matrix amplifier is a component that combines the additive process of the distributed and the multiplicative process of the cascaded multistage amplifier. The schematics given in Figure 8.21 clarify these two types of amplification. In

$$f_c = \frac{1}{\pi\sqrt{10^{-9}\cdot 0.17\cdot 10^{-12}}} = 24.4 \ GHz$$

$$Z_0 = \sqrt{\frac{10^{-9}}{0.17\cdot 10^{-12}}} = 76.84 \ \Omega$$

m1
freq=24.40 GHz
S(1,1)=0.924/152.382
impedance = Z0 * (0.042 + j0.245)

freq (1.000GHz to 200.0GHz)
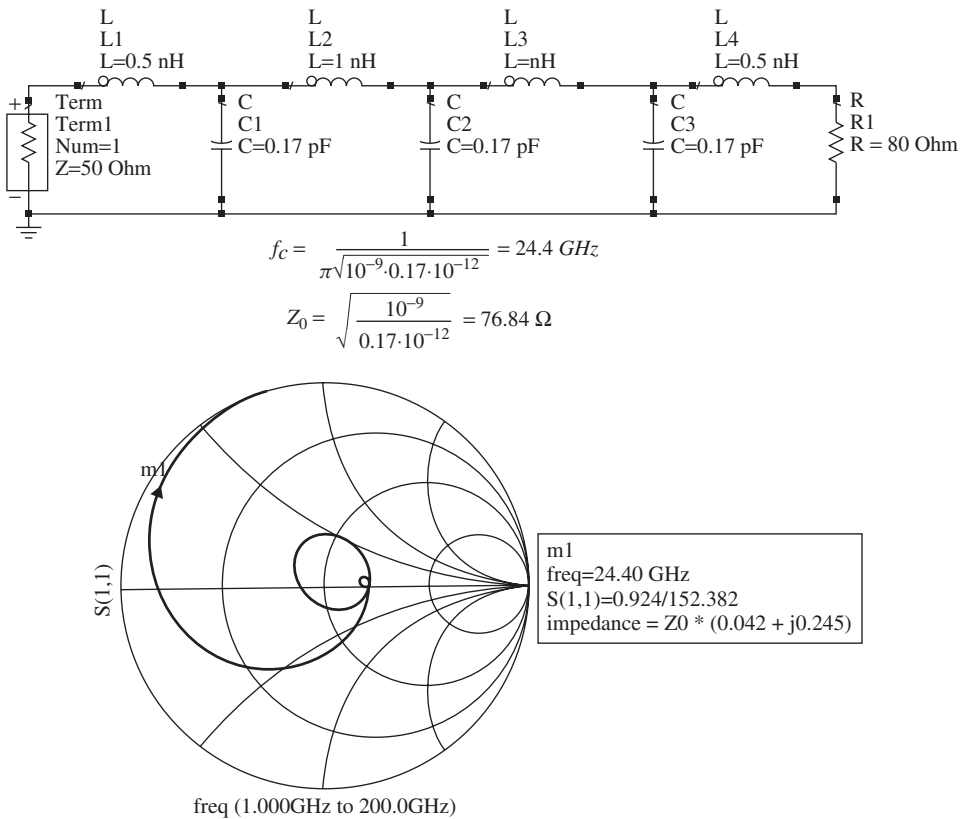
FIGURE 8.19   Smith chart impedance of lumped-element transmission lines versus frequency.

(*a*) Distributed
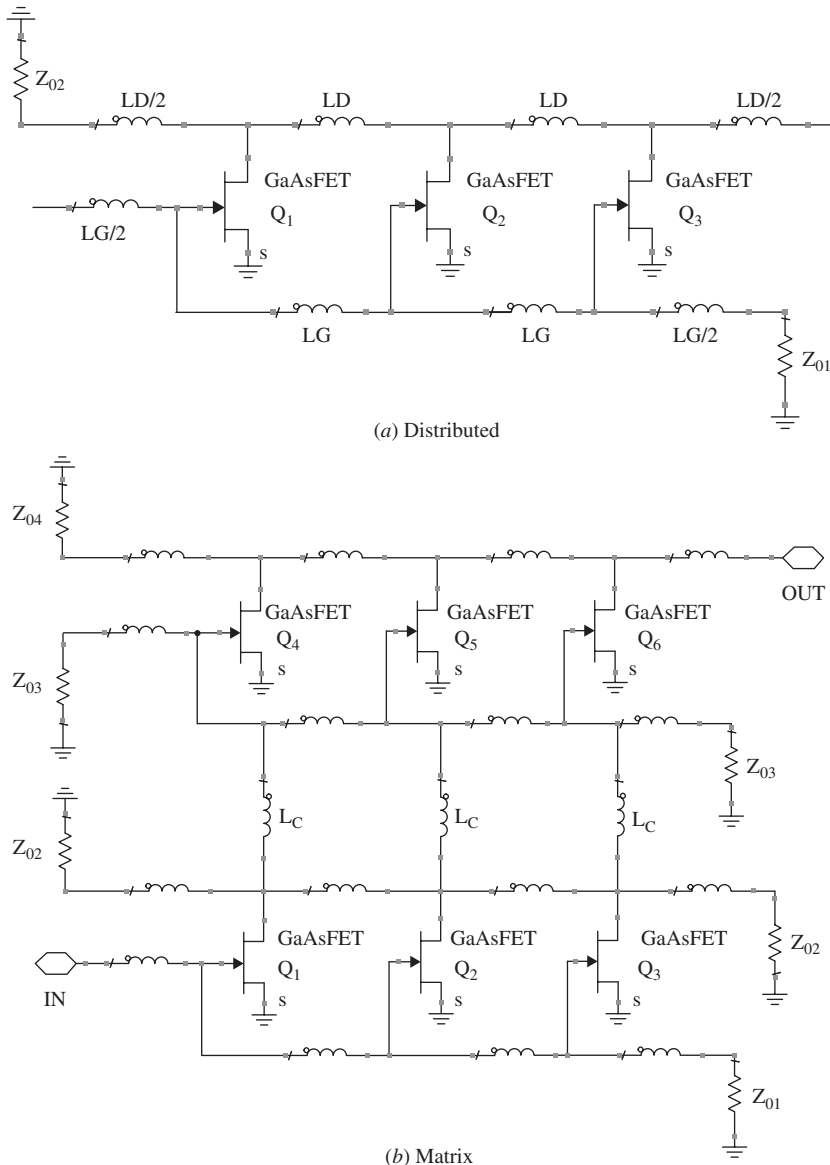
(*b*) Matrix

FIGURE 8.20   Distributed matrix amplifiers. (L_C is coupling inductance).

Figure 8.21*a* a three-stage cascaded amplifier is shown consisting of three transistors separated by the interstage matching circuits M_2 and M_3. The input matching circuit M_1 precedes the first and the output matching M_4 follows the last transistor. The total gain of the chain equals the product of the numerical gains of the individual stages, a multiplicative result. Figure 8.21*b* is a schematic of a three-transistor distributed amplifier. In this case the gain is based on the sum of the output powers of the three transistors representing the additive amplification process. For the 2×3 matrix amplifier whose schematic is shown in Figure 8.21*c* the above principles are combined in a
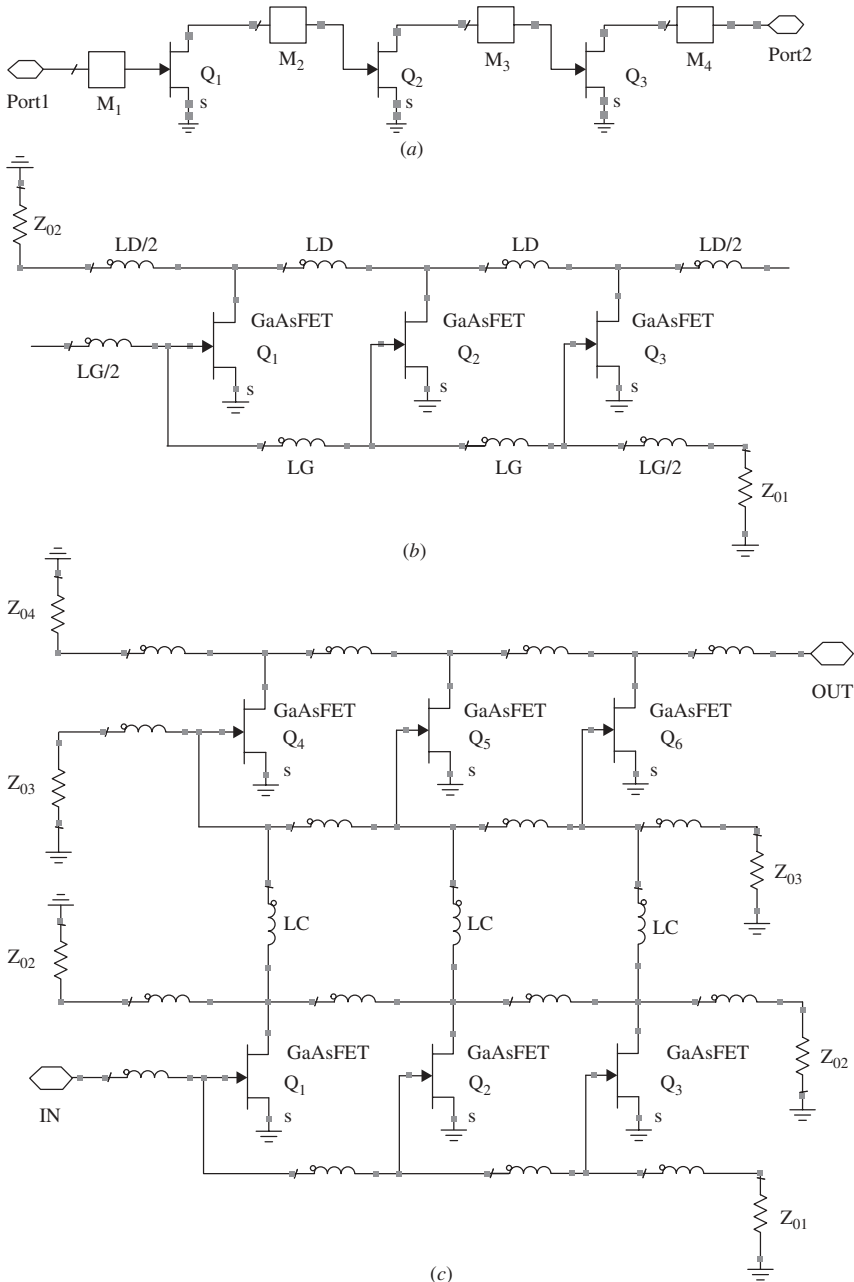
FIGURE 8.21   Three types of three-stage amplifiers.

unique way forming a matrix-shaped network. The additive process proceeds in both tiers from left to right in the horizontal direction and the multiplicative process from the bottom to the top in the vertical direction. The matrix amplifier delivers higher gain in addition to very good noise figures and a very small circuit size but uses six transistors.

The first monolithic version of a matrix amplifier with a gain of 15.5 ± 0.9 dB and a minimum P_1dBc of 15.5 dBm covering the 2- to 18-GHz band was reported in 1989 [8.26]. In addition, very good bandwidth has been demonstrated in a distributed amplifier by varying the characteristic impedance and line length of the transmission lines; for example, 2 to 26.5 GHz has been obtained [8.27] using a declining drain line length concept. Another variation on this concept is the cascode-delay-matched distributed amplifier for efficient broadband power amplification, achieving 30% efficiency over 1 to 4 GHz [8.28]. More recently, nonuniform stages of increasing device size allow higher output powers over very wide bandwidths [8.29]. One-watt amplifiers have been reported with 8 dB gain over 1 to 10 GHz. The highest frequency distributed amplifier in 1990 came from Varian Associates [8.30], where a bandwidth of 5 to 100 GHz was reported with InGaAs technology; the gain was 5 dB and the noise figure was 5 dB at 100 GHz. This paper won the MTT Applications Award in 1990. Another paper on a 2×3 HEMT matrix distributed amplifier for 6 to 21 GHz also won the MTT Applications Award in 1994 [8.31].

8.2.10   Millimeter-Wave Amplifiers

Monolithic millimeter-wave integrated circuits were first reported in 1968 by Texas Instruments [8.32]. The first circuits were a balanced Schottky barrier mixer using a branch line coupler with a Gunn diode local oscillator at 94 GHz with an IF of 2 GHz. The principles of design are no different from the 1-GHz design. With the advent of better transistors, amplifiers are now possible at frequencies greater than 100 GHz.

For example, Ref. 8.33 presents a three-stage InAlAs/InGaAs/InP PHEMT amplifier at 153 to 156 GHz with 10 to 12 dB gain using 0.1-μm gate technology, which was the highest gain achieved from three-terminal devices at this frequency in 1997. Another result from this period [8.34] is a 90- to 140-GHz six-stage amplifier using similar transistors which achieved 15 ± 3 dB gain over the full waveguide band. The noise figure was 7 dB at 110 GHz.

From a transistor point of view, these amplifiers require the highest possible f_t and $f_{\max}$. Fujitsu has reported the highest f_t (at the time of writing) of 400 GHz and $f_{\max}$ of 469 GHz using InGaAs/InAlAs PHEMT technology from a transistor biased at $V_{ds} = 1.0$ V and $V_{gs} = 0.15$ V [8.35]. This was an enhancement-mode device, where the effective gate length is even smaller than 0.045 μm.

An interesting historical note is the progress which has been made since 1966 [8.5], when an $f_{\max}$ of 10 GHz was obtained from state-of-the-art Si BJTs. An improvement of 46.9 over 35 years has been achieved, something akin to Moore's law for ICs, but not nearly so dramatic.

8.3   FREQUENCY MULTIPLIERS

8.3.1   Introduction

Higher frequency electronic power sources are required in various modern communications, radar, and computer-based systems.

Traditionally, techniques for creating high-frequency oscillation can become expensive when required a number of times in a system. An alternative method, when
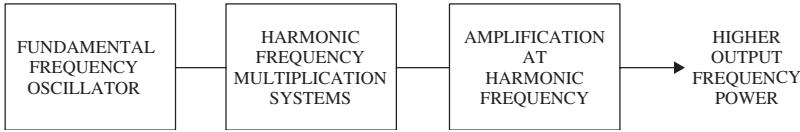
FIGURE 8.22   Frequency multiplier.

frequency planning permits, is to employ the technique of harmonic frequency multiplication. A basic approach to this procedure is illustrated in Figure 8.22. Here, the basic signal from a fundamental source is passed through a component known as a frequency multiplier, which is capable of creating output power at frequencies which are multiples of the input frequency.

When necessary, the power emerging from such frequency multiplier circuits may be significantly increased by employing stages of "relatively" inexpensive power amplification following the harmonic frequency multiplication stage.

The harmonic frequency multiplication system circuitry can be realized by fundamentally entirely passive components or by employing active elements such as bipolar, MESFET/HEMT, or HBT transistors.

8.3.2   Passive Frequency Multiplication

The principal mechanism involved with harmonic frequency generation utilizing passive elements requires that the passive component possess a fundamental nonlinearity. Such components can typically be nonlinear resistors, inductors, or capacitors [8.36, 8.37]. Utilizing any of these, harmonic frequencies are created whenever a sinusoidal signal is applied. Although numerous nonlinear element realizations have been employed, semiconductor diodes have been demonstrated to provide an efficient means of providing the nonlinear characteristics. Of these, varactor diodes have been most frequently employed.

Typical circuit realizations of passive multiplier circuits utilizing such diodes are illustrated in Figures 8.23 and 8.24 [8.38, 8.39]. In these figures, the diode (typically varactor) provides the circuit realization of a nonlinear capacitor.

In the circuit of Figure 8.23, the networks N_1 and N_R are realized such that they allow voltages to exist only at the fundamental frequency and the Rth harmonic, respectively, and voltages are short circuited at all other frequencies. In Figure 8.24, N_1 and N_R are filters which are realized such that they are essentially short circuited at the fundamental and Rth harmonic and open circuited at all other frequencies.

Based on physical considerations, it should be obvious that the output signal power at the Rth harmonic frequency cannot exceed that of the input.
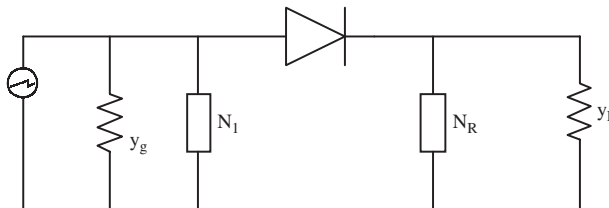
FIGURE 8.23   Series diode: classical passive multiplier realizations.
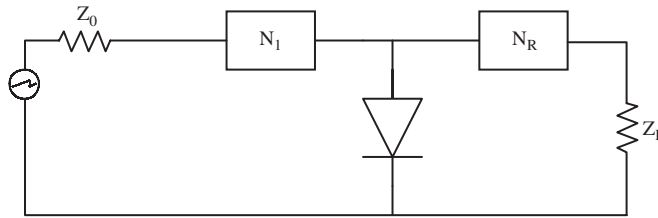
FIGURE 8.24   Shunt diode: classical passive multiplier realizations.

8.3.3   Active Frequency Multiplication

Harmonic frequency generation may also be achieved by employing active devices such as bipolar, MESFET, and HEMT transistors in a system such as that depicted in Figure 8.25 [8.40–8.42]. Figure 8.25 is a large-signal circuit model utilized for MESFET- and HEMT-type transistors in this connection. A perusal of this model admits the potential of employing numerous mechanisms for providing harmonic generation. A primary mechanism in this regard is resident in the output current source $I_{ds}(V_{gs}, V_{ds})$ and its derivatives, which are potentially nonlinear functions of both V_{gs} and V_{ds}. Among other elements which can provide contributions to harmonic generation are C_{gs} and C_{gd}.

A common circuit realization for frequency multiplication utilizing such active devices is shown in Figure 8.26. In this circuit, fundamental signal power is introduced through passive network N_1 and harmonic power is extracted through passive network N_2 at r_L.

The design of an efficient active frequency multiplier relies on selection and accurate modeling of the transistor, proper transistor bias for the specific harmonic required, input fundamental frequency power level, and proper synthesis of N_1 and N_2 subject to stability considerations. Currently, accurate design of *practical* frequency multiplier circuits also realizes application of nonlinear circuit analysis programs such as the Agilent ADS.
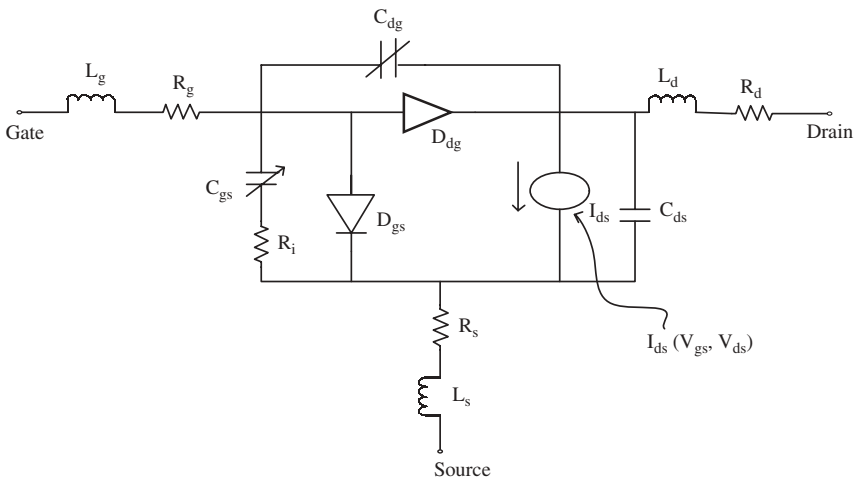
FIGURE 8.25   Active device model.
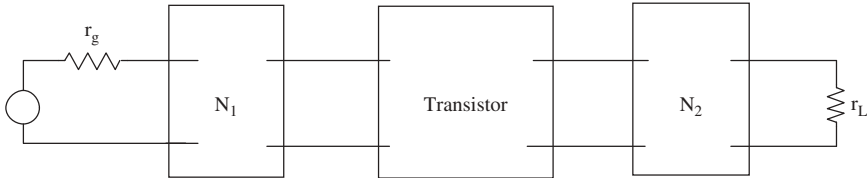
FIGURE 8.26   Active multiplier realization.
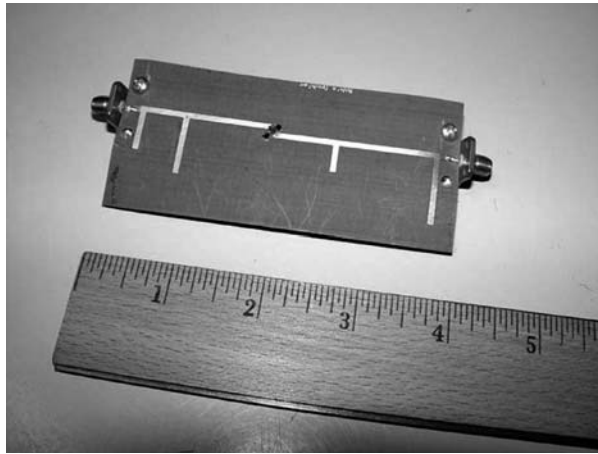
FIGURE 8.27   Photo of frequency doubler.
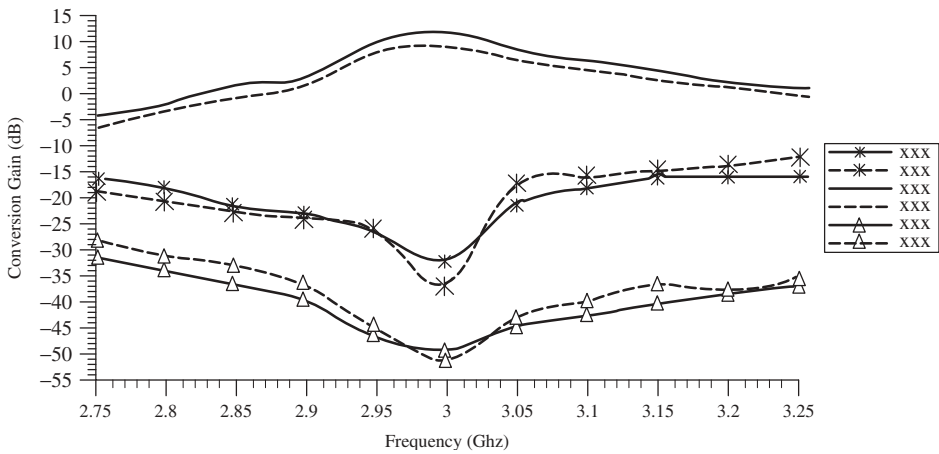
FIGURE 8.28   Doubler-conversion gain ($P_{in} = 0$ dBm, $V_{gs} = -0.7$ V, and $V_{ds} = 3$ V).

An example of the application of this approach is shown in Figure 8.27. This figure illustrates an example of a 3- to 6-GHz frequency doubler which was designed using an HP/Agilent 36163 PHEMT on 20-mil Duroid substrate. The gate of the HP/Agilent PHEMT was biased at *pinchoff*, while the drain had a V_{DD} of 3 V. The figure shows N_1 and N_2 realized with sections of transmission line and open-circuited stubs. Figure 8.28

shows the frequency response of the multiplier which is seen to have a conversion gain (P_{out} at $2f_0/P_{in}$ at f_0) of 12.5 dB at 6 GHz output frequency and suppression of fundamental and third harmonics of greater than -30 dB.

Another PHEMT tripler 2 to 6 GHz was recently reported to have 0 dB conversion gain at 0 dBm input power using similar design techniques [8.43].

8.4   DESIGN EXAMPLE OF 1.9-GHz PCS AND 2.1-GHz W-CDMA AMPLIFIERS

Agilent has found that enhancement-mode PHEMTs give outstanding performance in both 1.9-GHz PCS and 2.1-GHz W-CDMA applications for a relatively low cost [8.44, 8.45]. Other modeling papers are available describing the performance of these transistors [8.46]. The transistor used in these amplifiers is the 400-μm ATF-55143. These amplifiers operate with a 3-V supply and require about 0.45 V positive on the gate-to-source junction, similar to a Si BJT, which requires about 0.7 V for proper operation. The dc bias point is $V_{DS} = 2.7$ V and $I_{DS} = 10$ mA. Following the three steps outlined in the introduction of this chapter, the dc bias schematic, the RF matching circuits, and the total schematic are given in Figure 8.29. Even though $k < 1$ for this transistor, the LNA design is guaranteed to be stable. The source inductance is often used to bring the input noise match closer to achieve $S_{11\_AMP} = 0$; in this design it is used to lower the higher frequency out-of-band gain. The noise match is a high-pass structure, which helps to lower the gain below the band. The output match is a low-pass structure, so the gain above the band must be carefully controlled.

At P_1dBc the I_{ds} increases to 14.95 mA, dropping V_{ds} to 2.5 V. Therefore the dc power input is 36.54 mW. The P_1dBc is 11.5 dBm or 14.1 mW, giving an efficiency of $0.0141/0.03654 = 38.6\%$. In the schematic diagram, there are two values of output blocking capacitance: 2.2 pF is optimum for best S_{22} and 5.6 pF is best for output TOI.

The S parameters (with no source inductance) and noise parameters are given in Table 8.7. The Smith chart design of this amplifier is left as an exercise for the student. The component parts list for the total amplifier is given in Table 8.8. The resulting
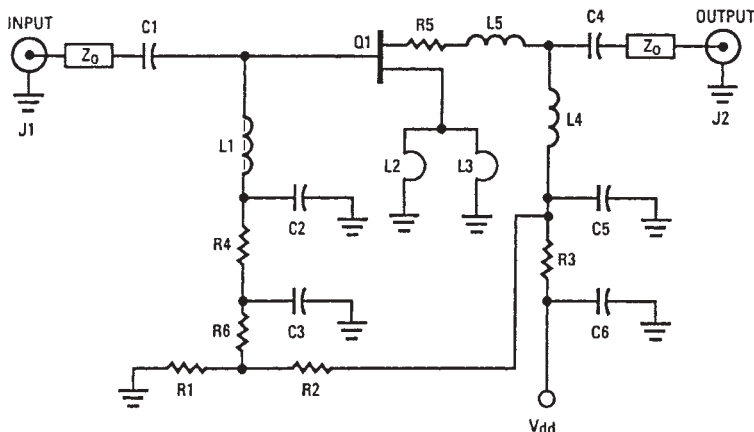
FIGURE 8.29   A 1.9-GHz PCS amplifier.

TABLE 8.7   ATF-55143 Typical Parameters at $V_{DS} = 2.7$ V, $I_{DS} = 10$ mA

S Parameters

	S_{11}			S_{21}		S_{12}		S_{22}		MSG/
Frequency (GHz)	Magnitude	Angle (deg)	dB	Magnitude	Angle (deg)	Magnitude	Angle (deg)	Magnitude	Angle (deg)	Magnitude (dB)
0.1	0.998	−6.4	20.86	11.044	174.9	0.006	86.2	0.819	−3.9	32.65
0.5	0.963	−31.2	20.46	10.549	155	0.026	70.4	0.786	−19.1	26.08
0.9	0.896	−53.8	19.68	9.641	137.5	0.043	57.3	0.737	−32	23.51
1.0	0.881	−59.2	19.44	9.376	133.4	0.047	54.4	0.72	−34.7	23.00
1.5	0.794	−83	18.21	8.133	115.6	0.06	42.2	0.651	−46	21.32
1.9	0.732	−99.5	17.25	7.284	103.3	0.068	34.4	0.602	−52.9	20.30
2.0	0.718	−103.4	17.01	7.087	100.6	0.07	32.6	0.592	−54.5	20.05
2.5	0.655	−122.3	15.94	6.267	87.1	0.076	24.8	0.538	−61.3	19.16
3.0	0.608	−140.2	14.96	5.599	74.8	0.082	17.9	0.485	−67.3	18.34
4.0	0.553	−175.9	13.28	4.615	51.7	0.089	5.6	0.39	−80.1	17.15
5.0	0.548	150.9	11.74	3.862	30.2	0.092	−5.4	0.321	−94.7	16.23
6.0	0.556	123.9	10.30	3.272	10.3	0.094	−14.6	0.280	−109	14.17
7.0	0.573	100.9	9.04	2.83	−8.3	0.096	−23.9	0.247	−124.1	12.29
8.0	0.590	78.6	7.89	2.481	−26.5	0.096	−32.8	0.204	−134.3	10.78
9.0	0.625	58.4	6.94	2.224	−44.3	0.102	−38	0.152	−146.7	9.94
10.0	0.699	39.2	6.03	2.002	−63.6	0.112	−49.7	0.098	166.8	9.89
11.0	0.752	22.7	4.89	1.755	−82.3	0.115	−61.1	0.112	100	9.34
12.0	0.789	8.4	3.78	1.546	−99.8	0.12	−72.4	0.167	62.3	8.81
13.0	0.815	−7	2.78	1.378	−117.8	0.122	−84.7	0.211	37	8.23
14.0	0.838	−22.8	1.81	1.231	−137	0.124	−98.3	0.274	12.6	7.69
15.0	0.862	−37.2	0.37	1.044	−155.9	0.119	−111.8	0.387	−7.6	6.82
16.0	0.856	−50.5	−1.27	0.864	−173.3	0.113	−124.4	0.491	−21.5	5.15
17.0	0.872	−59.7	−2.73	0.730	171.9	0.111	−135.6	0.568	−35.9	5.54
18.0	0.915	−70	−3.96	0.634	156	0.107	−149.4	0.628	−51.2	5.68

Noise Parameters

		Γ_{opt}			
Frequency (GHz)	F_{min} (dB)	Magnitude	Angle (deg)	$R_n/50$	G_a (dB)
0.5	0.2	0.64	19	0.12	25.29
0.9	0.26	0.59	22.7	0.12	23.24
1.0	0.27	0.54	26	0.12	22.76
1.9	0.39	0.54	48.3	0.11	19.01
2.0	0.4	0.54	49.9	0.11	18.66
2.4	0.48	0.45	59.8	0.1	17.35
3.0	0.57	0.39	75.6	0.09	15.69
3.9	0.72	0.26	108.7	0.07	13.79
5.0	0.88	0.2	167.5	0.06	12.26
5.8	1.02	0.22	−154.8	0.07	11.52
6.0	1.04	0.21	−147.8	0.08	11.37
7.0	1.19	0.26	−107.9	0.13	10.76
8.0	1.39	0.32	−75	0.23	10.2
9.0	1.54	0.41	−51.6	0.36	9.48
10.0	1.65	0.53	−33.6	0.54	8.38

TABLE 8.8   Amplifier Parts List

C1	5.6-pF chip capacitor
C2,C5	8.2-pF chip capacitor
C4	2.2-pF chip capacitor for best S_{22} and 5.6 pF for best OIP3 (see text)
C3, C6	10000-pF chip capacitor
J1, J2	SMA Connector, EFJohnson 142-0701-881
L1	2.7-nH inductor (Toko LL1608-FH2N7S)
L2, L3	Strap each source pad to the ground pad with 0.020-in. wide etch. The jumpered etch is placed a distance of 0.040 in. away from the point where each source lead contacts the source pad. Cut off unused source pad. See text
L4	10-nH inductor (Toko LL1608-FH10NK)
L5	5.6-nH inductor (Toko LL1608-FH5N6K)
Q1	Agilent Technologies ATF-55143 PHEMT
R1	910-Ω chip resistor
R2	5100-Ω chip resistor
R3	18-Ω chip resistor
R4	50-Ω chip resistor
R5	15-Ω chip resistor
R6	10-Ω chip resistor
Z0	50-Ω microstripline

gain and noise performance are in Figure 8.30, and other performance parameters are listed in Table 8.9. If higher gain is needed, one might consider a second stage using the 800-μm ATF-54143 discussed earlier in Chapter 4.

This example has demonstrated the design of a LNA using source inductance feedback and a two-element high-pass noise matching circuit while simultaneously achieving excellent TOI, gain, and efficiency with a low-pass two-element output matching circuit. In addition, the out-of-band performance was controlled for stability and lower gain. If Si BJTs had been used for this application, the noise figure would be higher (1.2 dB), the gain lower, and the cost lower by about one-fourth in high quantities. Another choice might be HBTs; at the time of this writing the market is still (and always will be) looking for the optimum lowest cost solution.

Another Agilent Application Note worth mentioning is Application Note 1076, using the ATF-10236 in LNA applications in UHF through 1.7 GHz frequency range. This uses a GaAs MESFET for the 800- to 900-MHz range for cellular and pager applications, the 1228- and 1575-MHz frequencies for global positioning systems, and many other applications. This also uses a 500-μm MESFET for low-noise applications, the ATF-10236. Noise figures of about 0.6 dB with a gain of 18 dB have been achieved at 1 GHz. Unfortunately, Agilent is planning to discontinue this line of MESFETs in favor of PHEMTs, despite the fact that MESFETs have the highest values of TOI.

8.5 STABILITY ANALYSIS AND LIMITATIONS

From a two-port viewpoint, unconditional stability is guaranteed if [8.1]

$$k = \frac{1 + |D|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} > 1 \tag{8.36}$$

ATF-55143 NOISE FIGURE vs. FREQUENCY

ATF-55143 GAIN vs. FREQUENCY

ATF-55143 INPUT AND OUTPUT RETURN LOSS vs. FREQUENCY
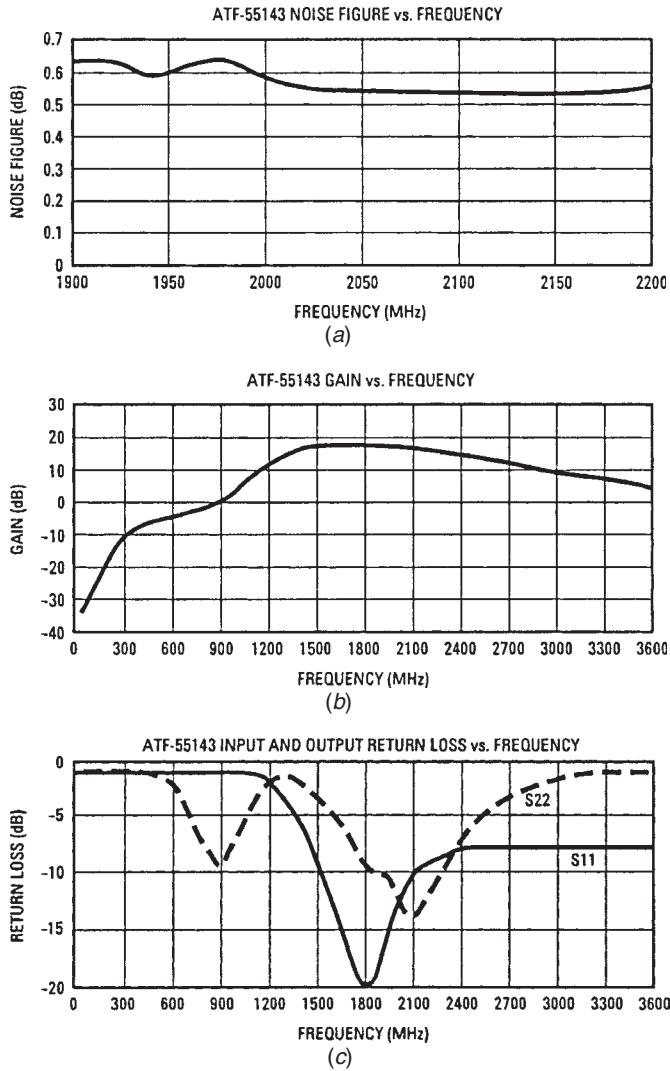
FIGURE 8.30   Performance of 1.9-GHz amplifier.

TABLE 8.9   Performance of 1.9-GHz Amplifier

Gain	17 dB
NF	0.6 dB
Input R_L	-15 dB
Output R_L	-10 dB
TOI	23.8 dBm
η (efficiency)	38.6%
P_1dBc	11.5 dBm ($C_{out} = 2.2$ pF)

and

$$|D| = |S_{11}S_{22} - S_{21}S_{12}| < 1 \qquad (8.37)$$

The generator stability circles are given by [8.6] the center and radius:

$$C_G = \frac{(S_{22} - DS_{11}^*)^*}{|S_{22}|^2 - |D|^2} \qquad (8.38)$$

$$R_G = \frac{|S_{12}S_{21}|}{||S_{22}|^2 - |D|^2|} \qquad (8.39)$$

where there is also a similar equation set for load stability. The inside of this circle is the unstable region if the 50-Ω point gives stability, that is, if $|S_{11}'| < 1$.

There are many ways of viewing the problem of stability, from both an amplifier and an oscillator perspective. Consider the negative-feedback system shown in Figure 8.31, which is a negative-feedback amplifier block diagram. Negative feedback reduces the system gain, but it also improves the stability by making the two-port more stable. We may define potential instability by the small-signal k factor defined previously in Chapter 4 (Eq. 4.7) which must be greater than unity for simultaneous match at both ports with a positive real part of the generator and load terminations. This simultaneous match at both ports is only possible at a single frequency.

Another more general definition [8.47] is BIBO (bounded input–bounded output), which states that a system is stable if every bounded input produces a bounded output. It may be shown that such a system $H(s)$ has all of its poles in the left-half plane. To investigate this, we need to find the roots of $P(s) = 1 + a(s)f(s)$, which is not an easy task. An alternative method is to focus on the behavior of the loop transmission $a(s)f(s)$, which vastly simplifies the problem.

While Eqs. (4.7) and (4.8) determine the stability for steady-state linear networks, a rigorous stability analysis of the characteristic system equation is required to detect natural frequencies or the lack thereof when nonlinear or non-steady-state behavior is present. This may be done with the Nyquist analysis [8.48].

An extended view of stability is to consider the gain and phase margin (which may be considered a subset of the Nyquist test), which is a good indication of how close you are to the Barkhausen oscillation condition, $a(s)f(s) = 1$. This requires a Bode plot of $a(j\omega)f(j\omega)$ versus ω, as shown in Figure 8.32:
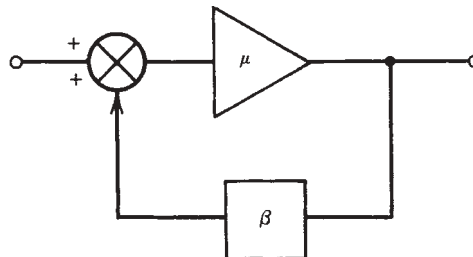
FIGURE 8.31   Negative-feedback amplifier.
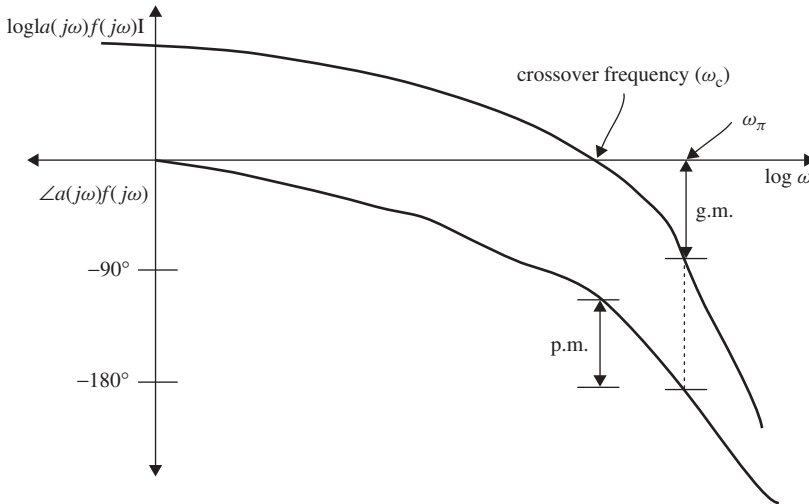
FIGURE 8.32 Gain and phase margins from Bode plot.

1. Gain Margin Find the frequency at which the phase shift of $a(j\omega)f(j\omega)$ is $-180°$. Call this frequency ω_π. Then

$$\text{Gain margin} = \frac{1}{|a(j\omega_\pi)f(j\omega_\pi)|}$$

2. Phase Margin Find the frequency at which the magnitude of $a(j\omega)f(j\omega) = 1$. Call this frequency ω_c, the crossover frequency. Then

$$\text{Phase margin} = 180° + \underline{/a(j\omega_c)f(j\omega_c)}$$

As we see from these definitions, gain and phase margins are measures of how closely $a(j\omega)f(j\omega)$ approaches a magnitude of unity and a phase shift of $180°$, the condition that could allow a persistent oscillation. The circuit must have the proper impedances to support this oscillation. The larger the gain margin and the phase margin can be, the greater the stability of the system will become.

Many amplifiers designed for $k > 1$ have oscillated. The reasons for this performance are unknown, possibly bad engineering, poor models, or other unexpected phenomena. Understanding the design of a multistage amplifier where $k < 1$ at low frequencies is a continual challenge. This was particularly true for the 1987 to 1992 MMIC program with monolithic multistage amplifiers [8.49]. Many papers have appeared to explain this disturbing result, but much controversy remains. An example is Ref. 8.50, which gives a novel method for finding RHP poles by calculating the normalized determinant function:

$$\text{NDF} = \frac{\Delta}{\Delta_{\text{on}}} \tag{8.40}$$

where Δ is the full network determinant, including all port terminations, and Δ_{on} is the resulting passive network determinant when all N dependent sources (i.e., voltage-controlled or current-controlled sources) are set to zero. This is similar to Bode's
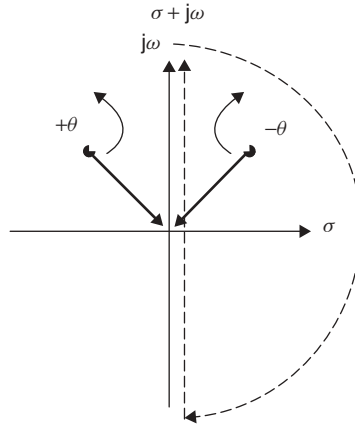
FIGURE 8.33 Nyquist plot.

[8.51] definition of the return difference Δ/Δ_0 for a single dependent source, where Δ_0 represents the network determinant when the dependent source is set to zero.

Computer programs will investigate the Nyquist plots for instability by finding if there are any RHP poles in the system (e.g., Serenade) [8.52]. Formal Nyquist analysis performs an integration of the characteristic system equation in the complex frequency plane. The path of integration begins at zero, proceeds to $+j$ infinity, follows a semicircle of infinite radius to $-j$ infinity, and continues along the imaginary axis to zero (see Fig. 8.33). Any natural frequencies in the RHP will be enclosed by the path of integration while those in the LHP will not. Rather than performing the integration explicitly, Serenade implements the Nyquist analysis by computing the determinant of the closed-loop system from dc to a high frequency and plotting the result in the complex plane. If the path crosses the negative real axis and encircles the origin, then a natural frequency exists in the RHP and the system is asynchronously unstable. The analysis is beneficial in examining broadband stability of the RF circuit, including the effects of the bias networks.

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PROBLEMS

8.1 Given the nonlinear model of the AT41400 (or packaged part) biased at $V_{CE} = 8$ V, $I_C = 40$ mA, design a class A amplifier with about 50% efficiency at $P_{1\,\text{dBc}}$ for a frequency of 8 GHz.

8.2 Using the nonlinear model of the MWT-7 MESFET biased at $V_{DS} = 5$ V, $I_D = 40$ mA, design an amplifier with about 50% efficiency at $P_{1\,\text{dBc}}$ at a frequency of 8 GHz.

8.3 Design a two-stage power amplifier with 1 W output at $P_{1\,\text{dBc}}$ at 10 GHz using the nonlinear models of the Filtronics LP750 driving the LP1500 biased at the recommended bias point for power.

8.4 Using the MWT-7 MESFET biased at $V_{DS} = 5$ V and $I_D = 40$ mA, design a unilateral amplifier at 4 GHz to give the gain of U. Find the $P_{1\,\text{dBc}}$.

8.5 Using the AT41400 (or packaged part), design a 5-GHz unilateral amplifier for U when biased at $V_{CE} = 8$ V, $I_C = 25$ mA. Change the design for $F = F_{\min}$ and $S'_{11} = 0$. Change the design for $P_{1\,\text{dBc}}$ at maximum value and $S'_{22} = 0$.

8.6 Using the LP3000 MESFET at 8 GHz, design a feedback amplifier at the recommended bias point for maximum $P_{1\,\mathrm{dBc}}$ with $S'_{22} = 0$.

8.7 Design a power amplifier for an output TOI > 45 dBm using the LP1500 PHEMT at the recommended bias point at 8 GHz.

8.8 Using the MWT-9 chip at a bias of $V_{DS} = 6$ V and $I_D = 60$ mA at 8 GHz, design a power amplifier for maximum $P_{1\,\mathrm{dBc}}$ and output TOI $> P_{1\,\mathrm{dBc}} + 10$ dB.

CHAPTER 9

POWER AMPLIFIER DESIGN

9.1 INTRODUCTION

During the last few years, state-of-the-art microwave transistor power amplifier design has shifted from the hybrid (i.e., discrete-component) realm to the monolithic circuit arena. This change has even occurred with portable handsets, where power amplifier costs are extremely sensitive. Here, too, the hybrid amplifier has virtually vanished and is only present in the infrastructure portions of modern networks. The change in design direction has occurred for two main reasons. First, the semiconductor processing skills of the industry as a whole have markedly improved to the point where cost, repeatability, and yield make it not only practical but also imperative to employ monolithic designs in deliverable hardware. This phenomenon is virtually independent of the circuit and device technology employed; hence, monolithic circuits employing GaAs, SiGe, or LDMOS substrates are selected by system requirements, not process difficulty, as was so often the case in the recent past. Second, considerable improvements in circuit-modeling techniques have occurred and CAD methods have become available to all RF and microwave designers. These new modeling and CAD methods will directly influence the final MMIC cost by reducing and eventually eliminating the key component cost driver, that is, "time to market."

In the following sections, accurate model development and nonlinear CAD simulation will be stressed, so that the designer will be assured of the best possible chance of "first-pass success" in developing some of the more demanding nonlinear two-port components. The determination of optimum load conditions, based on both modeling and measurements, will be discussed as it relates to the design of single- and multistage amplifiers. Finally, the chapter will conclude with the illustration of several monolithic design/synthesis examples focusing on bandwidth, efficiency, and power

output performance. Monolithic and power hybrid realizations and design constraints will be included in the examples as well as an analysis of the fundamental power output limitations in GaAs PHEMT, HBT, and LDMOS circuits.

9.2 DEVICE MODELING AND CHARACTERIZATION

The rapid growth in high-density RF circuits, such as GaAs and Si MMICs, and LTCC modules, has stressed the importance of accurate device and circuit modeling and characterization. The luxury of circuit tuning, which is common when microwave components are designed with discrete elements, is not viable when evaluating high-density microwave components. This is particularly true with ceramic modules or RF integrated circuits, which are in effect sealed and impossible to tune. The design is either correct and meets performance goals or is scrap. Unfortunately, the task of developing accurate device or circuit models is tedious and usually requires extensive S-parameter measurements, and such engineering assignments are not associated with the glamorous RF circuit design.

Although the development of an active device model is heavily based on S parameters, a discrete lumped-element model allows for circuit simulation flexibility. The elements of a good active device model are directly related to device physics and can be used to predict performance variations due to temperature effects and process variations [9.1]. Such variations are almost impossible to incorporate in design methodologies solely based on S parameters.

The engineer, whether designing a small-signal or nonlinear circuit, must first obtain a linear device model. As an example, a simple MESFET will be used as an illustration (Fig. 9.1). The element values in the model can be determined by various methods. The contact resistances R_d and R_g and the source resistance R_s are determined by dc measurement methods and are assumed to be frequency independent. The transconductance g_m and the drain-to-source resistance R_{ds} are easily determined from low-frequency
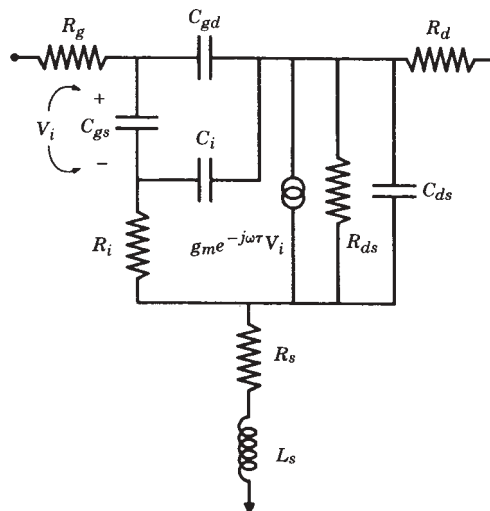
FIGURE 9.1   Lumped-element model for GaAs MESFET.

RF measurements usually performed at 100 MHz, which is much more accurate than determining these quantities at dc. The value of gate-to-source capacitance C_{gs}, an extremely important parameter, can be either measured or obtained from optimization methods, with the other elements fixed. It should be noted that C_{gs} and C_{gd} (gate-to-drain capacitance) and to a lesser extent R_{ds} are very bias dependent and thus must be evaluated throughout the operating range of the device. Other element values can also exhibit bias and temperature dependence.

As mentioned above, the three resistances R_g, R_d, and R_s can be measured with the aid of a curve tracer (essentially dc). The configuration for measuring R_g and R_s is shown in Figure 9.2. If a positive current step (ΔI_f) is applied to the gate, the FET drain can then be used as a probe to determine the voltage drop across the source resistance R_s. The value of R_s is then computed using the relation

$$R_s = \frac{\Delta V'_{ds}}{\Delta I_f} - R_{p2} = \frac{\Delta V_{ds}}{\Delta I_f} \tag{9.1}$$

where R_{p2} is the dc resistance of the probe. The resistance R_{p2} can be determined similarly by reversing the roles of the FET source and drain. The configuration for measuring R_g is shown in Figure 9.3. If the gate–source diode is forward biased, then R_g can be determined from the slope of the diode I–V characteristic. Thus,

$$R_g = \frac{\Delta V'_{gs}}{I_2 - I_1} - R_s - R_{p1} - R_{p2} \tag{9.2}$$

where R_{p1} and R_{p2} are the dc resistances of the probes.

At low RF frequencies, such as at 100 MHz, the capacitive reactances of the elements C_{gs}, C_i, C_{dg}, and C_{ds} in a typical GaAs FET are much larger than their related resistances and can be ignored when measuring R_{ds} and g_m. Hence, the values of g_m and R_{ds} can be accurately deduced from scalar S-parameter measurements. By assuming that the input impedance at these frequencies can be approximated by an open circuit, it is easy to show that

$$g_m = \left| \frac{R_s + R_{ds} + R_d + Z_0}{R_{ds}} \right| \frac{|S_{21}|}{2Z_0 - |S_{21}|R_{ds}} \tag{9.3}$$
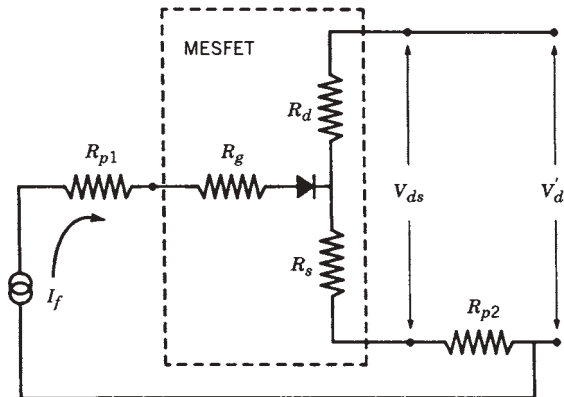
FIGURE 9.2   Configuration for measuring FET source resistance R_s.
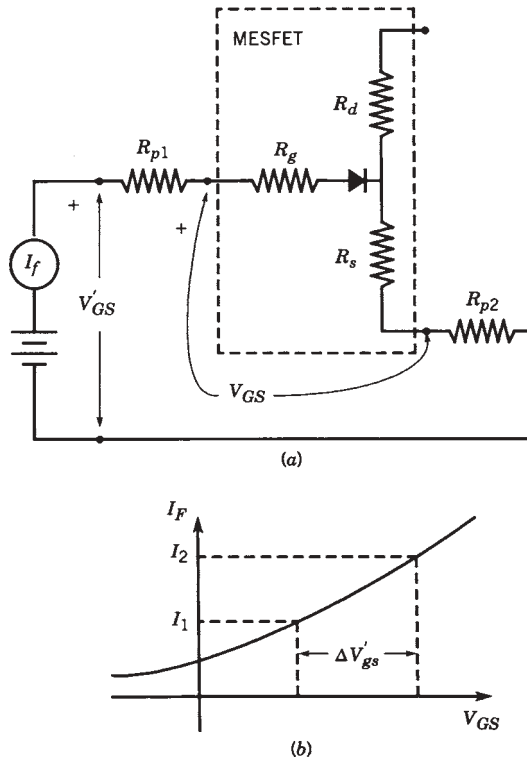
FIGURE 9.3 (*a*) Configuration for measuring FET gate resistance R_g. (*b*) Gate diode $I-V$ characteristic.

and

$$R_{ds} = \frac{1}{1 + g_m R_s} \left| Z_0 \frac{1 + |S_{22}|}{1 - |S_{22}|} - R_{ds} + R_d \right| \tag{9.4}$$

Obtaining the capacitive element values of the linear FET model is somewhat more difficult. The gate capacitance, which is the only capacitive element that can be measured indirectly, can be found using a method defined by DeLoach [9.2] to characterize microwave diodes. In this method, the FET gate, in conjunction with an external inductor (usually a bond wire), acts as a series resonant RLC network. The network is then placed across a through transmission line forming a single-pole band-reject filter. The DeLoach measurement circuit, with FET and gate inductor, is depicted in Figure 9.4. The FET drain is RF bypassed to aid stability during measurement.

If the transmission loss of the circuit shown in Figure 9.4 is measured as a function of frequency, the equivalent values of R, L, and C can be found. The analysis requires knowledge of the minimum transmission loss T_m, a second value of loss T, such that $T > T_m$, and the frequencies ω_1 and ω_2, where T occurs. A typical transmission loss characteristic is shown in Figure 9.5. Hence the values of R, L, and C can now be found from the following relations:

$$R = \frac{Z_0}{2[(T_m)^{1/2} - 1]} \tag{9.5}$$
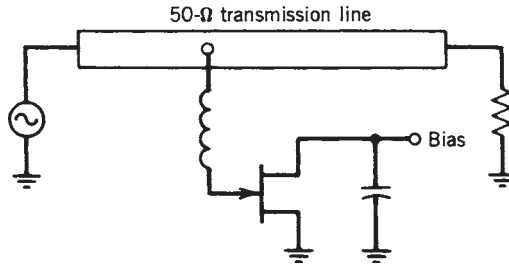
FIGURE 9.4   Measurement setup to determine C_{gs} by De Loach method.
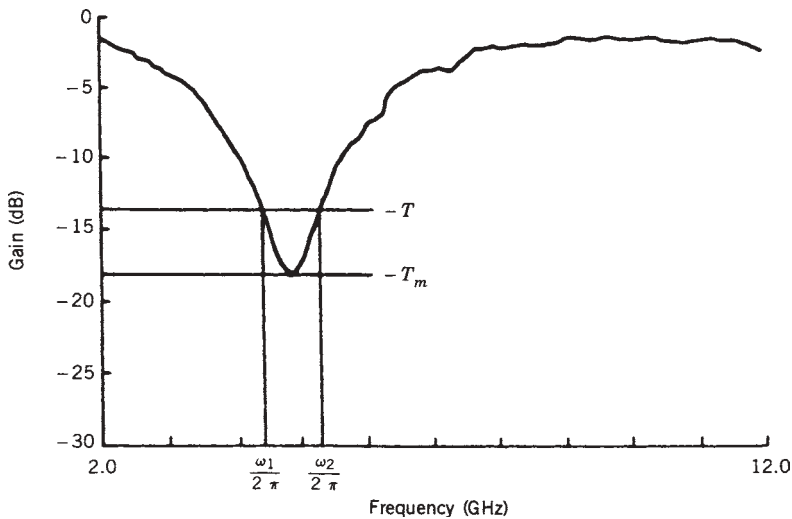
FIGURE 9.5   Band-stop filter response obtained from transmission loss measurement.

$$L = \frac{Z_0}{2[(T_m)^{1/2} - 1](\omega_2 - \omega_1)} \left| \frac{T_m - 1}{T - 1} \right|^{1/2} \qquad (9.6)$$

$$C = \frac{1}{\omega_2 \omega_1 L} \qquad (9.7)$$

The gate–source capacitance is then computed from the relation

$$C_{gs} Y (1 + g_m R_s)(C - C_d) \qquad (9.8)$$

where R_s and g_m have been determined from dc and RF measurements, respectively. Equation (9.8) is approximate and requires an estimated value for drain-to-source capacitance. This quantity is usually known and is typically 5% to 10% of the value of C. The dependence of C_{gs} on drain and gate bias can also be determined by observing the quantities ω_1 and ω_2 and by recomputing (9.6), (9.7), and (9.8).

The remaining model elements C_i, C_{dg}, C_{ds}, R_i, and t are found by setting the computed model S parameters equal to the measured device S parameters and then

adjusting the values with the aid of an optimizer such as the one available in Agilent Technologies' ADS. The dc measured element values should be fixed during optimization, while the elements C_{gs}, R_{ds}, and g_m should be tightly constrained. Excellent measured versus model performance can be obtained if the active device is carefully evaluated. A cascode dual-gate model (Fig. 9.6) and its computed versus actual performance (S parameters) are shown in Figure 9.7. As can be seen in the illustration, the model performance closely represents the measured S-parameter data. A dual-gate example was selected because it is more difficult to model than a single-gate device, thus illustrating the value of the approach.

The small-signal FET model formulation above is based very heavily on measured S-parameter data, which are difficult and tedious to obtain accurately. However, some measurement techniques yield good results provided a proper test fixture is employed during device evaluation.

The measurement technique employs microstrip calibration standards for the automatic network analyzer instead of coaxial shorts, opens, and sliding loads [9.3–9.5]. The microstrip standards help regain some of the accuracy typically lost if the system were calibrated in the coaxial line prior to the microstrip test fixture. The loss in accuracy would be due to the fact that the characteristics of the microstrip-to-coaxial transitions used on the fixture are imperfect. This calibration method, which is commonly called the TSD technique, requires the use of a microstrip through line (T), a microstrip short (S) (whose reflection coefficient does not have to be known), and a delay line (D). The delay line D should be approximately three-eighths wavelength longer than the through line at the highest frequency of use. The TSD technique can
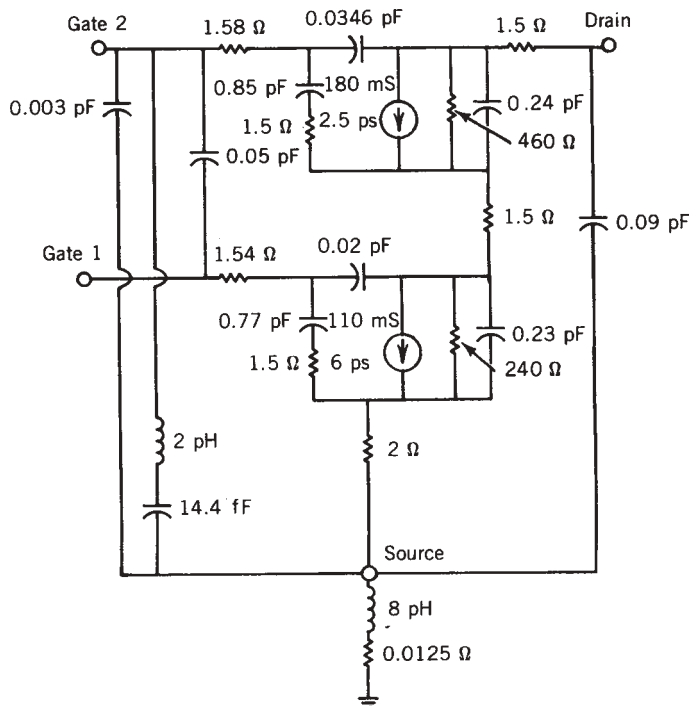
FIGURE 9.6   Cascode linear model of 450-μm dual-gate FET.
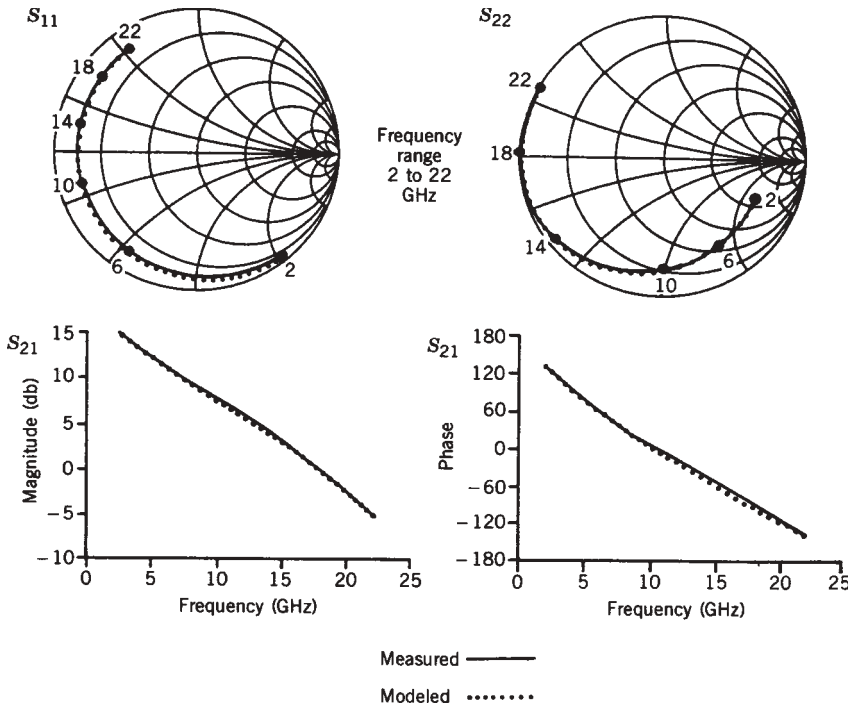
FIGURE 9.7   Measured versus computed response of dual-gate FET cascode model.

provide heightened levels of accuracy over the conventional "short-open-load-through" calibration method. Also, the TSD technique can be further improved by using a microstrip open, consisting of an empty test fixture, which will allow the open-circuit fringing capacitance and leakage (gap) capacitance to be included in the calibration procedure. Although the exact characteristics of the standard need not be known, it is assumed that the characteristic impedance Z_0 is constant with frequency. Hence care must be taken in selecting microstrip dimensions at frequencies above 18 GHz. A typical test fixture that is used to evaluate discrete active devices and monolithic circuits is shown in Figure 9.8.

Extending the foregoing small-signal model for nonlinear operation can be done in a variety of ways. The most obvious is to base a new circuit model on large-signal S parameters. This can easily be accomplished by measuring device S parameters at elevated power levels. The power level is usually chosen to correspond to the level encountered in the final circuit application. However, there are some negative aspects of using large-signal S parameters. First, as we have learned, S parameters are defined in a linear n-port system with a constant load impedance. Under large-signal conditions, the microwave n-port is not linear and large-signal S parameters cannot predict device performance for load impedances other than the one used during measurement (Z_0). Also, the value obtained for S_{22} is not the conjugate of the optimum load impedance.

To alleviate the limitations noted above, the active elements must be character- ized as a function of terminating impedance as well as a function of drive level. This technique, commonly called "load pull," has the advantage that the FET is operated
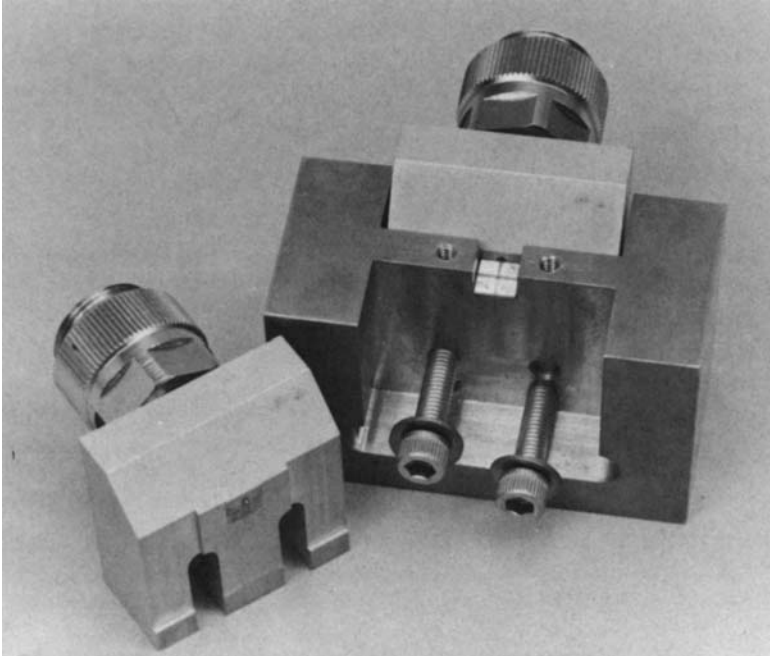
FIGURE 9.8   Typical *S*-parameter test fixture with APC-7 launchers. (Courtesy of Texas Instruments).

under conditions simulating actual circuit performance, but the method requires numerous measurements made at discrete frequencies and power levels [9.6, 9.7]. Although tedious, the concept is quite simple. The input impedance, power output, and gain of an active device are measured at a particular frequency and power level with a given load impedance. The load impedance can be supplied either passively with a preset tuner or actively by injecting a signal, which can vary in amplitude and phase, into the output of the device. The load-pull technique produces constant power contours, similar to constant-gain circles, on the Smith chart which are used in circuit synthesis. Load-pull techniques can also produce constant efficiency contours and large-signal gain contours. Typical constant power and efficiency contours for a power LDMOS transistor are shown in Figure 9.9.

The methods produce comparable results but are implemented quite differently. Elaborate mechanical tuners have been constructed that are controlled by the measurement system, which can step through a wide range of load impedances. These tuners are precalibrated at numerous frequencies, so that the data can be accumulated over a wide frequency range. The active load-pull method is typically implemented using a feed-forward technique so that the DUT is terminated with a virtual load [9.8]. The impedance of the load is determined by injecting a backward-traveling wave into the output of the DUT with the appropriate amplitude and phase. This signal must be coherent with the drive signal and is obtained by splitting the input signal and feeding it forward to the output port. A network analyzer is typically employed at the load to aid in system calibration. A typical measurement setup is shown in Figure 9.10. The active load-pull method is somewhat easier to use than the passive technique and
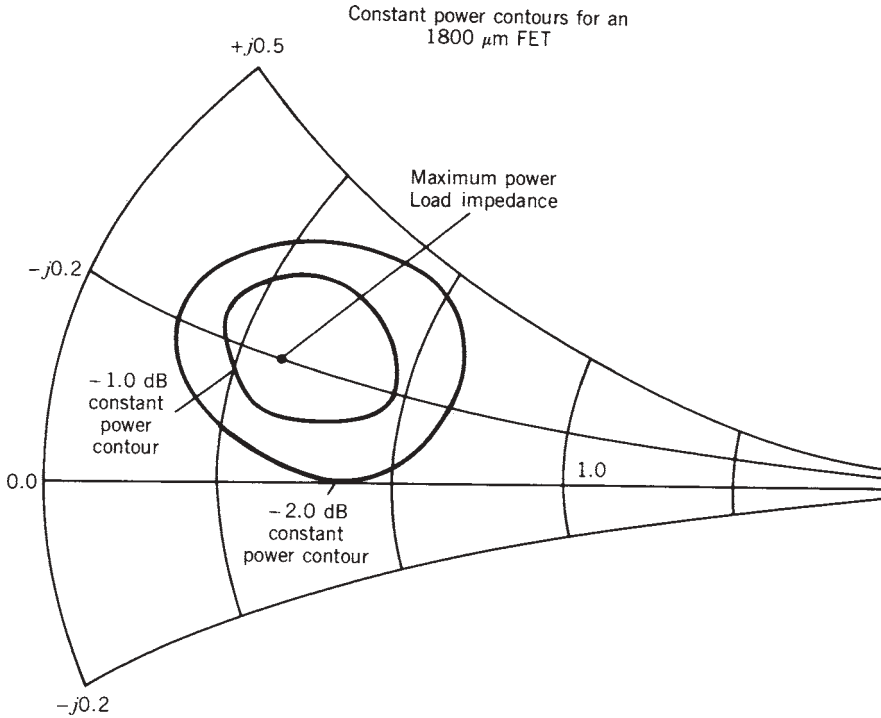
FIGURE 9.9   Constant-power contours for a typical power GaAs FET.

offers the advantage of being able to simulate any load impedance. Due to the loss inherent in mechanical tuners, very high or low impedances are difficult to simulate; hence the evaluation of very large power devices, which require low load impedances, is not practical unless broadband transformers are used to effectively change the measurement system impedance to a lower value. Solid-state tuners are also not an option with power devices, due to the obvious power-handling limitation of the actual tuner. As an example, the measurement of high-power LDMOS devices is accomplished by changing the measurement system impedance to either 12 or 5 Ω with the use of multisection transformers, as shown in Figure 9.11a. The performance of the six-section transformer is shown in Figure 9.11b. The transformers were designed to be able to accurately determine S parameters that represent each fixture half at the fundamental frequency of operation f_0 and its second and third harmonics, $2f_0$ and $3f_0$. A two-tier non-50-Ω Thru-Reflect-Line (TRL) calibration technique should be used to establish the measurement reference planes [9.42]. This fixture was successfully utilized to measure the load-pull performance of one of Motorola's LDMOS 90-W, 1.9-GHz high-power transistors [9.43].

There is only one key area in which load-pull data do not accurately predict nonlinear performance. In both the passive and active methods, the load impedance is usually synthesized at the fundamental frequency only. Harmonic terminations are typically ignored, although some effort has been made to synthesize fundamental and second-harmonic loads. The problem is somewhat worse with mechanical tuner approaches, in that the harmonic terminations vary widely for small changes of the tuner elements.
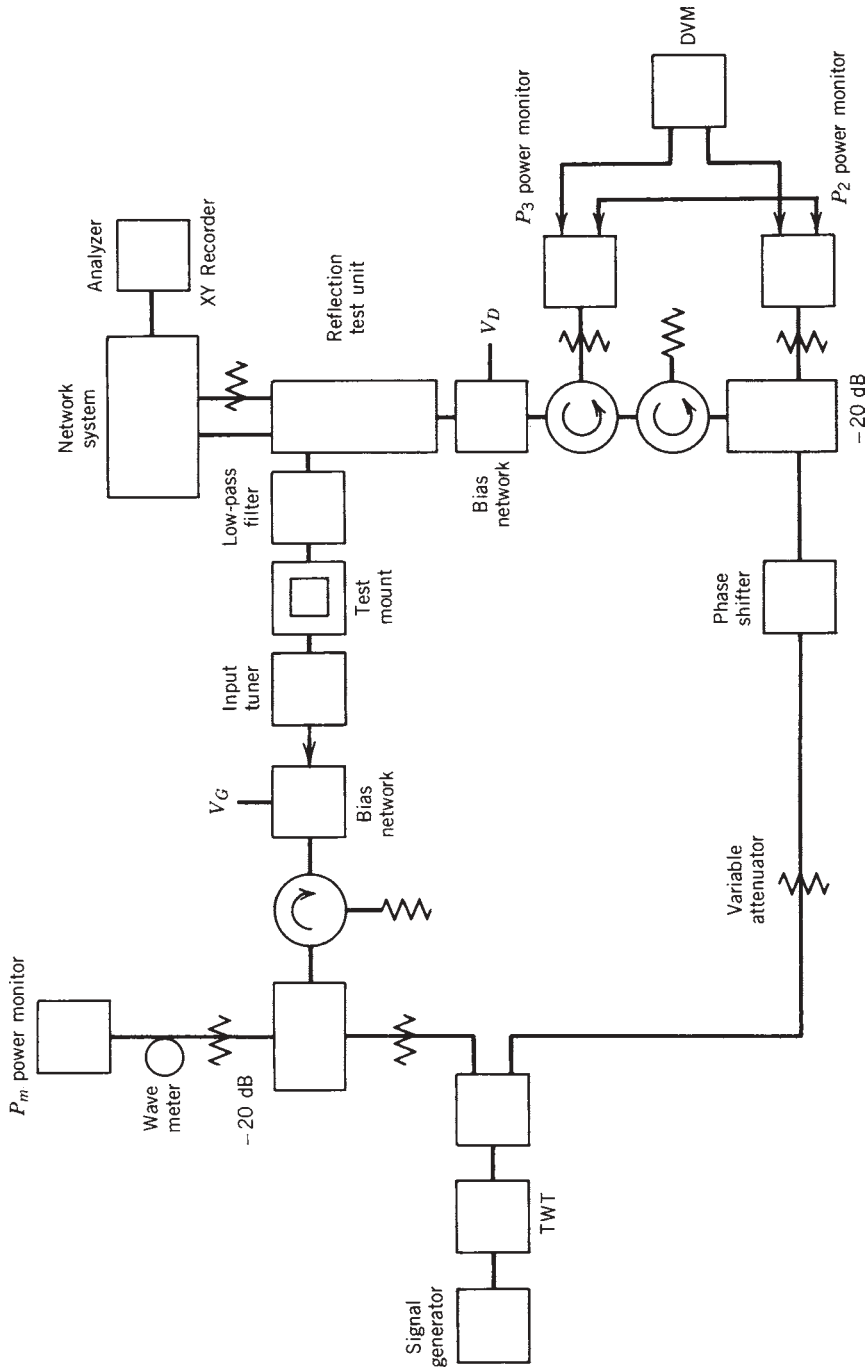
FIGURE 9.10 Active load-pull measurement setup.

Z_{in} (Transformer) Z_{in} (bias + Transformer)

(*a*)

(*b*)
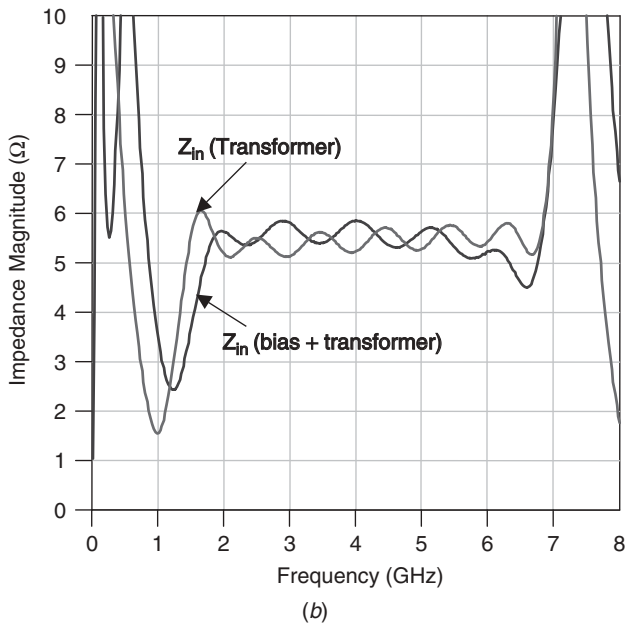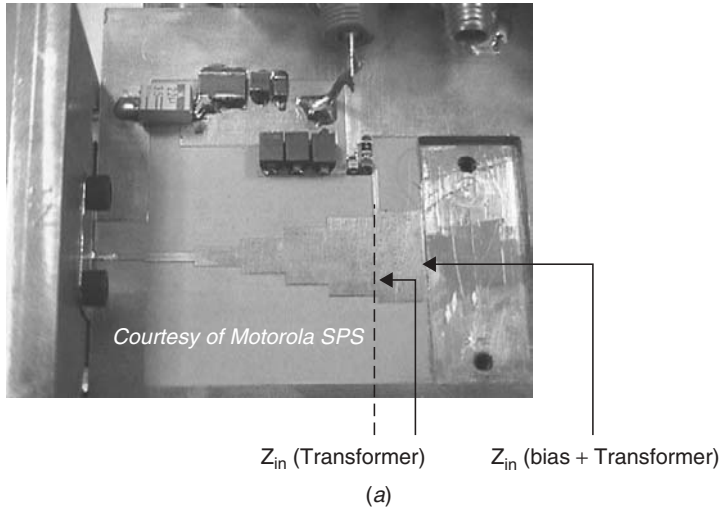
FIGURE 9.11   Six-section Chebyshev transformer: (*a*) 5 to 50 Ω; (*b*) performance.

However, second-harmonic load-pull setups can be constructed with diplexers and a second set of tuners and the appropriate software. Active load-pull techniques usually have nearly constant terminations, at least at low-order harmonics. Load-pull techniques have another drawback in that the data obtained cannot easily be integrated into a general nonlinear simulator.

A variety of numerical models which have the potential of simulating in-circuit FET performance have been proposed. These models range from the original low-frequency model presented by Shockley, which is valid for long-gate-length devices, to elaborate charge transport descriptions, which solve a set of partial differential equations in the

time domain. Time-domain solutions are inefficient and are not practical for interactive (real-time) computing. A significant amount of time can be saved by approximating the solutions to the semiconductor differential equations; but, adding the effects of the embedding circuit is difficult, since the FET input/output networks are usually characterized in the frequency domain. Another, more practical approach is to extend linear circuit theory to include nonlinear elements. The latter approach yields results similar to those obtained when designing with load-pull data [9.9].

It is evident from the discussion above that a numerical model with the efficiency of a frequency-domain linear solution is required for efficient interactive nonlinear design. Several such modeling approaches, commonly referred to as "harmonic balance" methods, are solved in the frequency domain but employ time-domain descriptions for the active-element nonlinearities. Thus nonlinear behavior of the total microwave circuit is obtained. Development of a CAD model of this type is relatively straightforward and begins with the linear FET model described previously (Fig. 9.1).

A nonlinear model may be formulated by taking the linear elements of the small-signal model and combining them with nonlinear descriptions of FET drain current, drain-to-source breakdown current, and gate–diode $I-V$ characteristics [9.10]. Simulation is not complete unless the effects of input and output terminations as well as feedback are included. The resulting model is shown in Figure 9.12. It should be noted that the element R_{ds} is included in the nonlinear description of the drain current I_d and
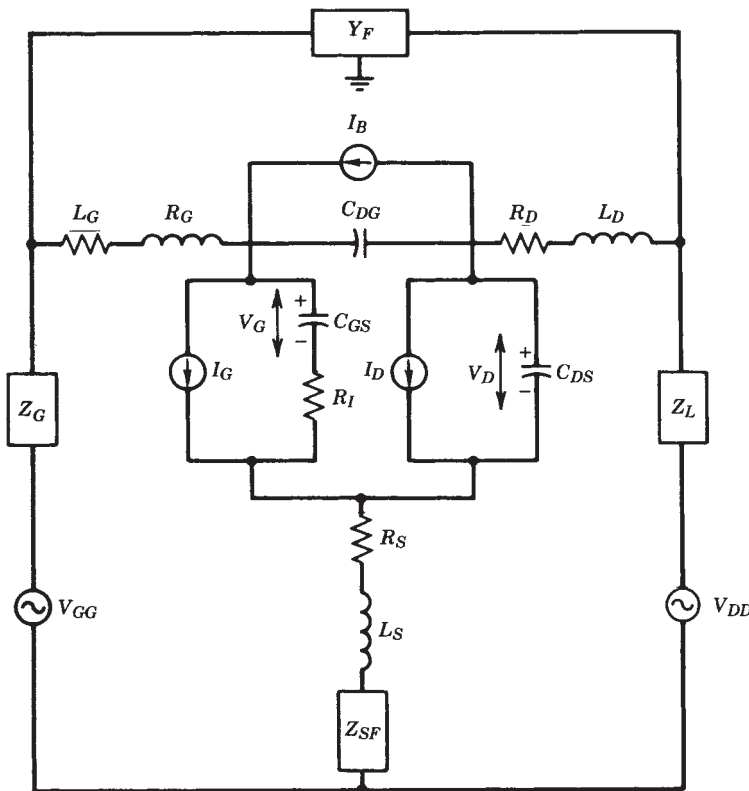
FIGURE 9.12 FET and circuit nonlinear model.

not as a separate model linear element; thus the effects on R_{ds} due to bias conditions are included.

The quantities Z_G and Z_L are the equivalent input and output impedances of the generator and load networks, which are usually determined from their two-port S-parameter descriptions, while the quantities Y_f and Z_{sf} are the two-port and one-port S-parameter descriptions of the shunt and series feedback networks, respectively. These S-parameter descriptions must include data at both fundamental and harmonic frequencies and can be obtained from either laboratory measurements or computer simulation. The sources V_{GG} and V_{DD} contain both dc and RF components and are selected to simulate actual circuit conditions. The nonlinear element values of the model are obtained solely from physical measurements.

The greatest contributor to the nonlinear characteristics of the FET is the drain current as a function of gate and drain voltage. The useful portion of the current at the FET drain terminal, which can be delivered to a load, is limited by the gate-to-drain breakdown current (I_b) and by the gate voltage swing, which is bounded by gate conduction and pinchoff. In this model the currents I_d, I_b, and I_g are assumed to be functions of the internal gate voltage V_g and the drain voltage V_d. Thus low-frequency measurements can be used to determine the time-dependent characteristics of these quantities. Typical characteristics for I_d, I_b, and I_g for a 300-μm FET are shown in Figure 9.13.

The drain current characteristics can be determined by measuring the current entering the FET as a function of gate and drain voltage. The burnout problem mentioned above, which can be encountered during static measurements of this type, can be eliminated by
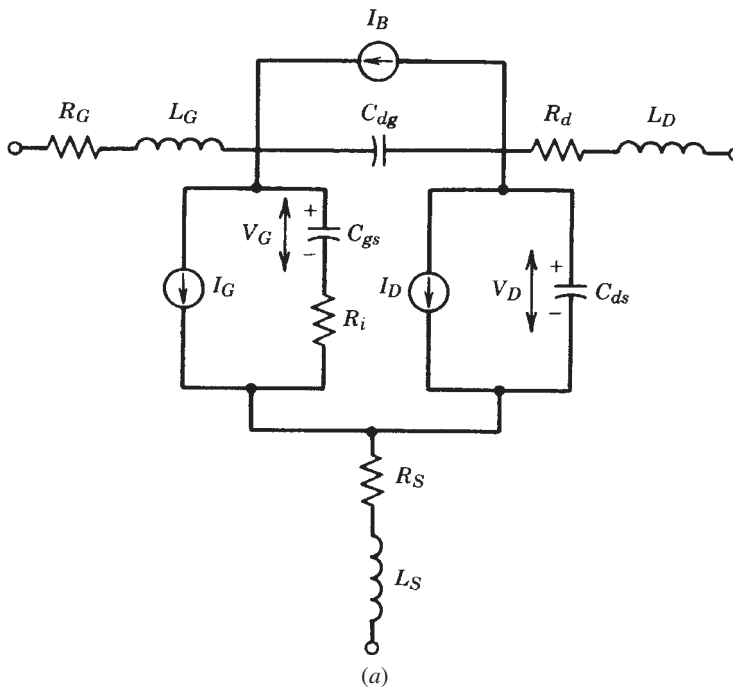
FIGURE 9.13 Typical characteristics for a 300-μm FET: (*a*) linear element values.
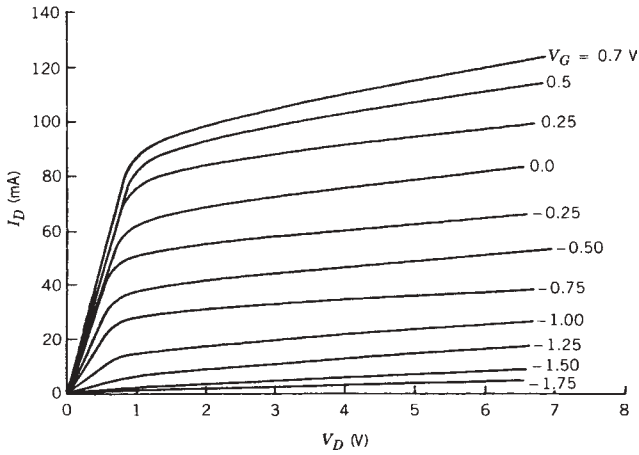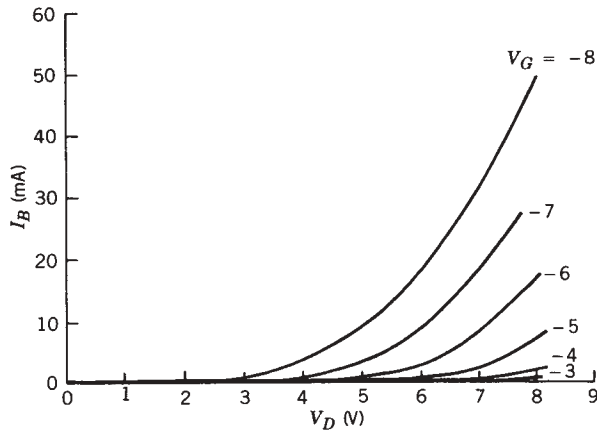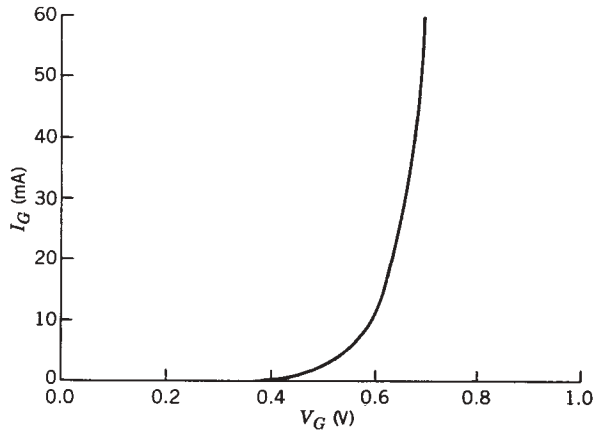
FIGURE 9.13   Typical characteristics for a 300-μm FET: (*b*) drain current characteristics; (*c*) drain-to-gate breakdown current as a function of terminal voltages; (*d*) forward gate diode *I* – *V* characteristic.

pulsing the drain voltage. Breakdown currents can also be obtained if the drain voltage is made sufficiently large so that the FET operating point is in the drain breakdown region. However, pulsed $I-V$ measurements of this type do not heat the FET to normal channel temperatures; hence, an abnormally high value of g_m is obtained, and the pulses used are usually too long to yield an accurate value of R_{ds} due to traps. Although the lack of heating can be overcome by statically heating the FET itself, trapped charge at the surface of the FET still causes erroneous values of R_{ds} to be obtained with this method. The change in R_{ds} as a function of frequency is illustrated in Figure 9.14.

To obtain a more accurate representation of R_{ds} and g_m of an operating FET, a measuring system employing low-frequency RF signals can be utilized [9.11]. The 1-MHz measurement test set depicted in Figure 9.15 applies large half-wave rectified RF voltages to both the gate and drain terminals. The 1 MHz frequency is about the lowest usable frequency, since one must be sure to be above the trap frequency of the devices being measured. During evaluation, the FET drain current is continuously monitored while the phase relationship between gate and drain signals is varied. Hence, for every phase difference, the operating point of the FET traverses a different continuous closed contour on the FET's drain current $I-V$ plane. A typical operating point path is shown in Figure 9.16. The exact shape of the contour depends on the phase relationship between the gate and drain voltages. By measuring a sufficient number of contours, the
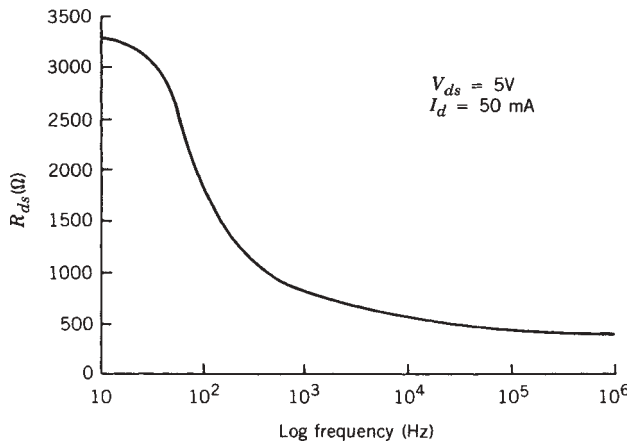
FIGURE 9.14   Drain-to-source resistance R_{ds} as a function of frequency.
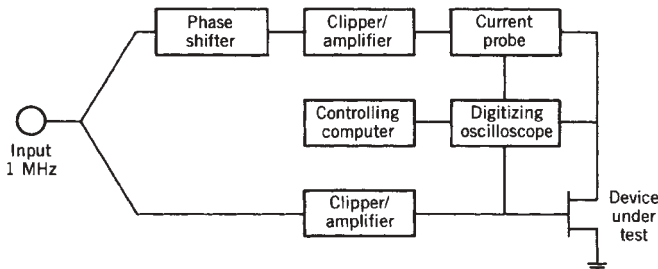
FIGURE 9.15   Measurement apparatus configuration for 1-MHz RF FET evaluation.
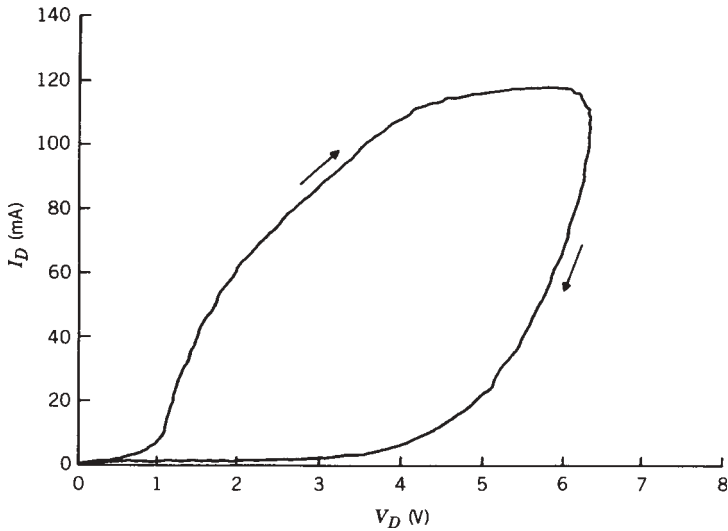
FIGURE 9.16   Typical FET operating path obtained during low-frequency RF evaluation.
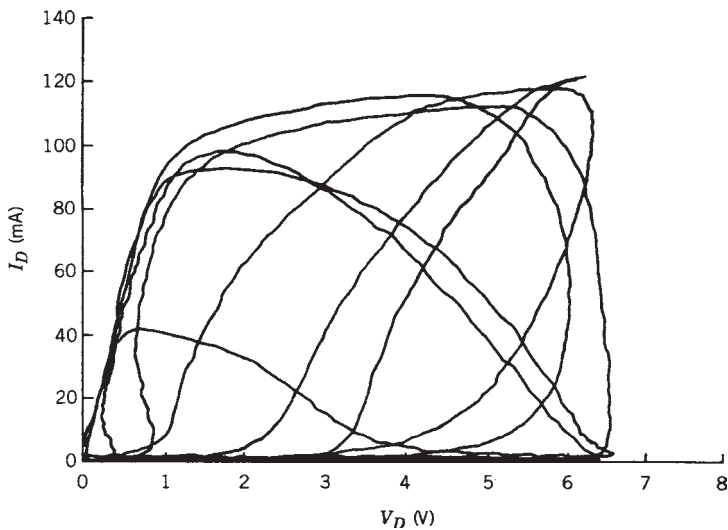
FIGURE 9.17   Entire FET operating region mapping obtained from low-frequency RF evaluation.

entire drain current characteristic can be mapped as shown in Figure 9.17. Computer algorithms are then used to generate FET drain current characteristic curves (Fig. 9.12) in which R_{ds} and g_m can be obtained from the digitized data. Gate-to-drain breakdown current characteristics can also be constructed by monitoring gate current and utilizing sufficiently large RF voltages. A comparison between the FET characteristics obtained from conventional pulsed $I-V$ measurements (long pulses; several microseconds; i.e. below trap frequency) and rectified sine wave measurements are shown in Figure 9.18.
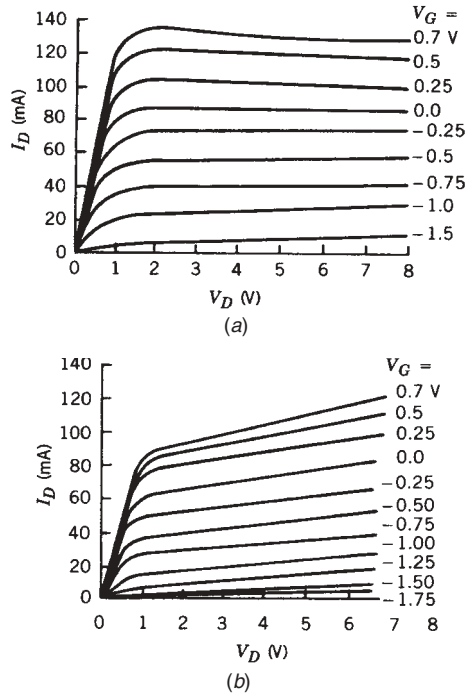
FIGURE 9.18   Comparison of FET drain current characteristics obtain from (*a*) pulsed $I-V$ and (*b*) rectified sine wave evaluation.

A CAD FET model can use the data directly in look-up table form or analytical functions describing FET characteristics can be formulated. It should be noted that pulsed $I-V$ measurements using short pulses (200 to 300 ps) to obtain the RF $I-V$ characteristics is preferable to the above method since the dc bias point can be set independently. This is important since a different $I-V$ plane will be obtained with different bias conditions. A typical short pulsed measurement system is shown in Figure 9.19. The advantage to the RF $I-V$ test method is that the measurement test set is simple and low cost.

Analysis of the nonlinear model of Figure 9.12 begins by applying Kirchhoff's laws in the frequency domain, resulting in a coupled, complex simultaneous algebraic equation set with V_g and V_d as the independent variables. For each Fourier component (dc, signal, and harmonics), there are two complex equations [9.10]

$$AV_g + BV_d = C \tag{9.9}$$

and

$$DV_g + EV_d = F \tag{9.10}$$

The quantities A, B, D, and E are linear combinations of model element values and frequency, while the quantities C and F are functions of circuit values, voltage generators, and the nonlinear currents I_g, I_b, and I_g. These nonlinearities are also a function of V_g and V_d; thus (9.9) and (9.10) are best solved with a nonlinear iterative numerical solver.
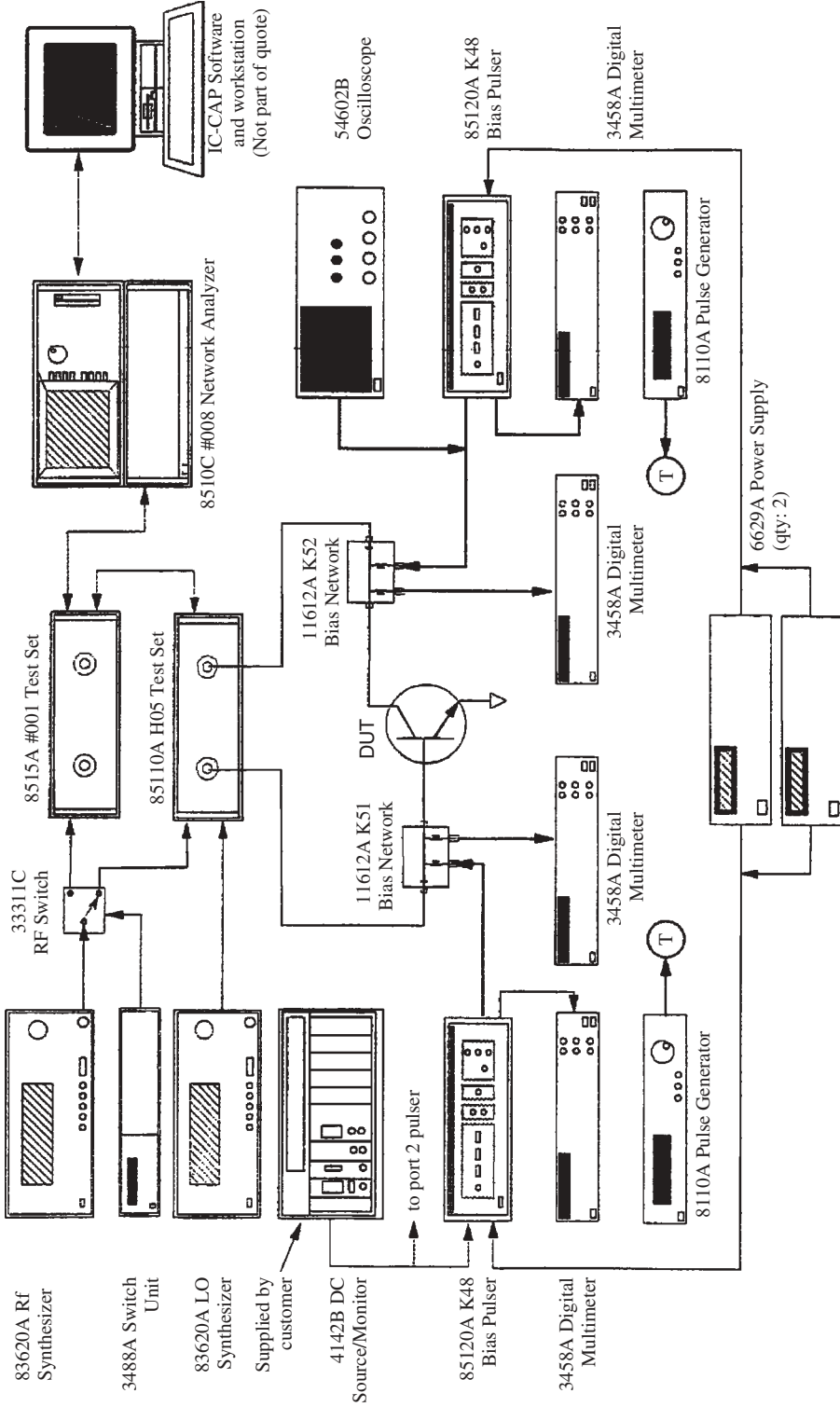
FIGURE 9.19 Pulsed I–V test setup for device characterization.

The solution of the harmonic balance problem above, illustrated in Figure 9.20, begins by solving a linearized version of (9.9) and (9.10). Initially, the forward gate and breakdown currents are set to zero and the drain current is calculated by assuming a linear value of conductance. As each iteration is done, Fourier transforms produce time-domain functions for V_g and V_d which are used to generate the nonlinear current functions I_d, I_b, and I_g. Frequency-domain solutions for the nonlinear elements are obtained by using an inverse transform and the total circuit problem is again solved. The iteration process continues until a self-consistent set of equations is obtained from the nonlinear solver. This self-consistent set of equations is checked by applying Kirchhoff's laws for each circuit loop (voltage) and at each circuit node (current). The consistency test must be applied at all frequencies—dc, signal, and harmonics—hence the name "harmonic balance."

With most practical circuit problems, sufficient accuracy is obtained when the dc component, signal, and five harmonics are used in the solution. Using fewer than three harmonics can lead to serious errors in the calculation of optimum load impedance, power output, and gain. Care must also be taken when describing the frequency-domain characteristics of the source and load impedances, since they are evaluated through the highest harmonic.

The following circuit data illustrate the accuracy obtainable when using the characterization technique and harmonic balance methods described above. In Figure 9.21
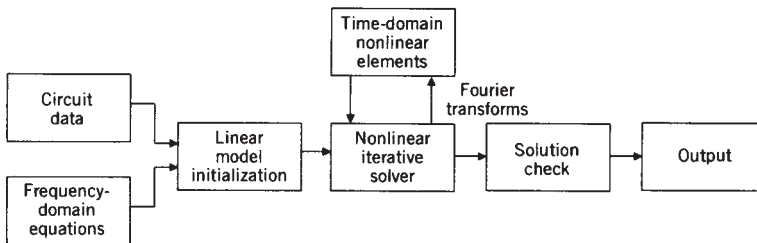
FIGURE 9.20   Large-signal model solution process.
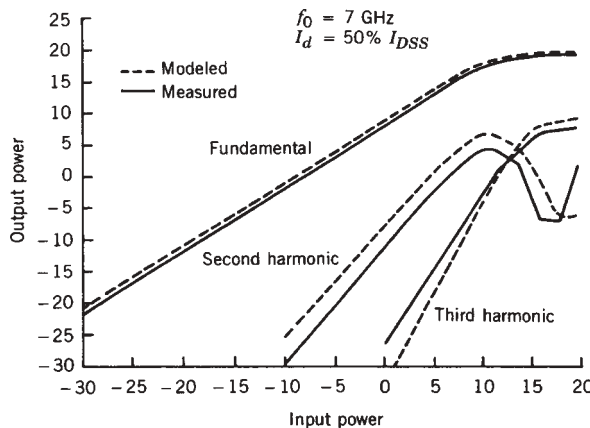
FIGURE 9.21   Modeled versus measured output harmonic content for a 300-μm FET in a 50-Ω system.

the performance of a 300-µm GaAs FET connected in a 50-Ω system is depicted. The saturation and harmonic characteristics of the amplifier are shown as the FET is driven at various power levels. A monolithic two-stage amplifier (Fig. 9.22a) was analyzed using a multi-FET model, and the measured-versus-modeled compression curve is shown in Figure 9.22b. The model can be extended to accommodate multiple-drive signals at various frequencies [9.12]. A model of this type was used to calculate the performance of a single-gate FET mixer with the gate and source terminals driven. The mixer's measured-versus-computed performance is shown in Figure 9.23.

Although the computer solution is done in both the time and frequency domains, all circuit quantities are available from the model. For example, because all the currents and voltages are known at each point in the circuit, voltage waveforms may be extracted or S parameters may be calculated. Also, since the load network can be numerically
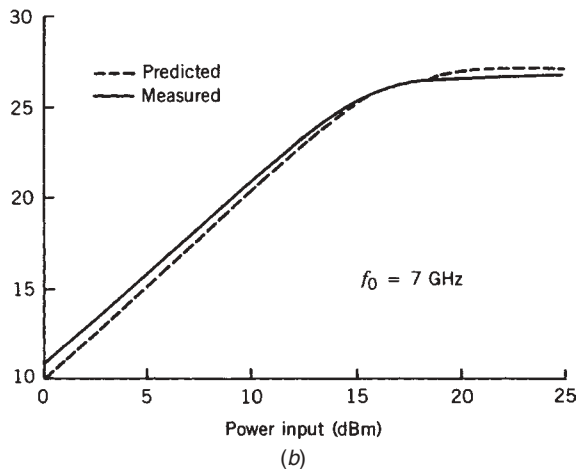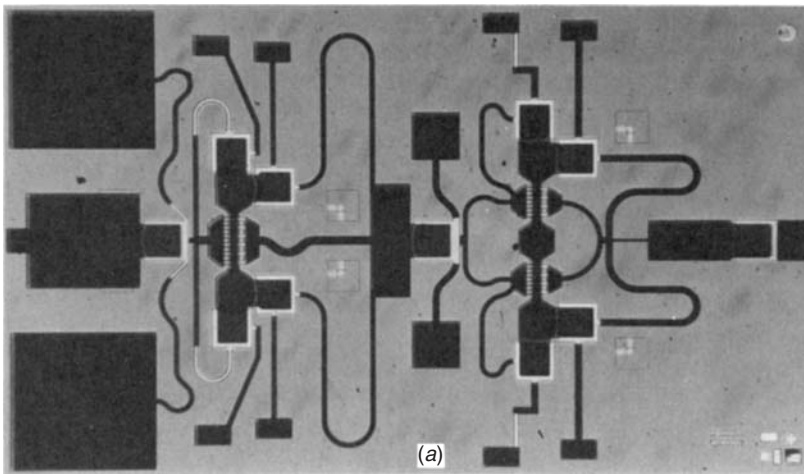
FIGURE 9.22 Monolithic two-stage power amplifier (400 mW) used in nonlinear analysis: (a) Chip photograph. (Courtesy of Texas Instruments.) (b) Comparison between measured and predicted output performance.
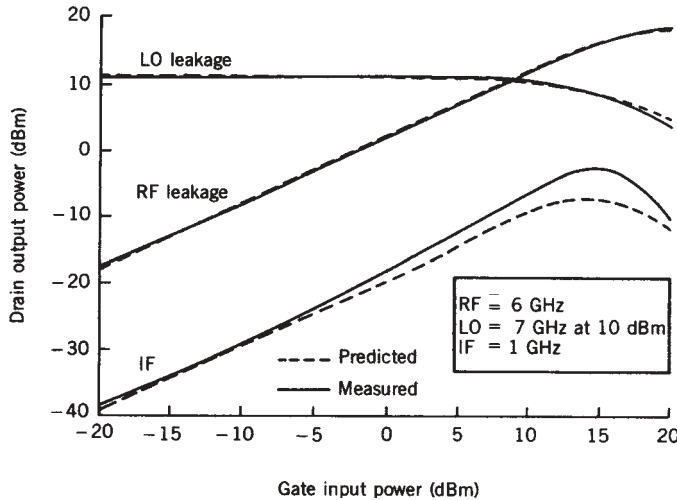
FIGURE 9.23 Measured versus predicted performance of 300-μm FET mixer in a 50-Ω system.

varied, the effects of harmonic terminations can be studied or optimum load contours, similar to the contours obtained from load-pull measurements, can easily be generated for any set of circuit conditions. The above method describes the general formulation for a table-based nonlinear device model. Since the region of operation between the points of the table are fit with cubic splines, higher order derivatives vanish; hence, these look-up table–based models do not predict higher order distortion very well.

The nonlinear behavior of other active devices, such as Si and GaAs bipolar transistors, can be modeled using the same techniques. A simplified nonlinear bipolar model that includes both the forward and reverse transistor current sources is shown in Figure 9.24a [9.13]. The diodes D_1 and D_2 are used to determine some of the device breakdown characteristics and forward base–emitter voltage. The charge storage effects are included in the elements C_{be} and C_{cb}.

The device model can be solved by using either time-domain or harmonic balance techniques provided that the characteristics of the current sources are known. All the current sources shown in the model are nonlinear and are functions of the internal circuit voltages as well as controlling currents, where applicable. The current sources representing D_1 and D_2 can be modeled in the forward direction by the diode equation controlled by the voltage across their associated capacitance and by polynomials or piecewise linear approximations in the reverse direction. They can also be modeled using look-up tables based on physical measurements. The remaining current source characteristics can also be determined from physical measurements or analytically.

The small-signal model applies to transistors operating at a fixed bias for a drive level remaining in the linear region; however, linear models can be expanded and modified for nonlinear operation (Fig. 9.24b). This can be accomplished by using the time-domain capabilities of SPICE, which calculates all voltages and currents in a model versus time.

The regions of nonlinearity are best described by Figure 9.25, which gives five limitations on linear operation for a common-emitter bipolar transistor. The turn-on

(a)

(b)
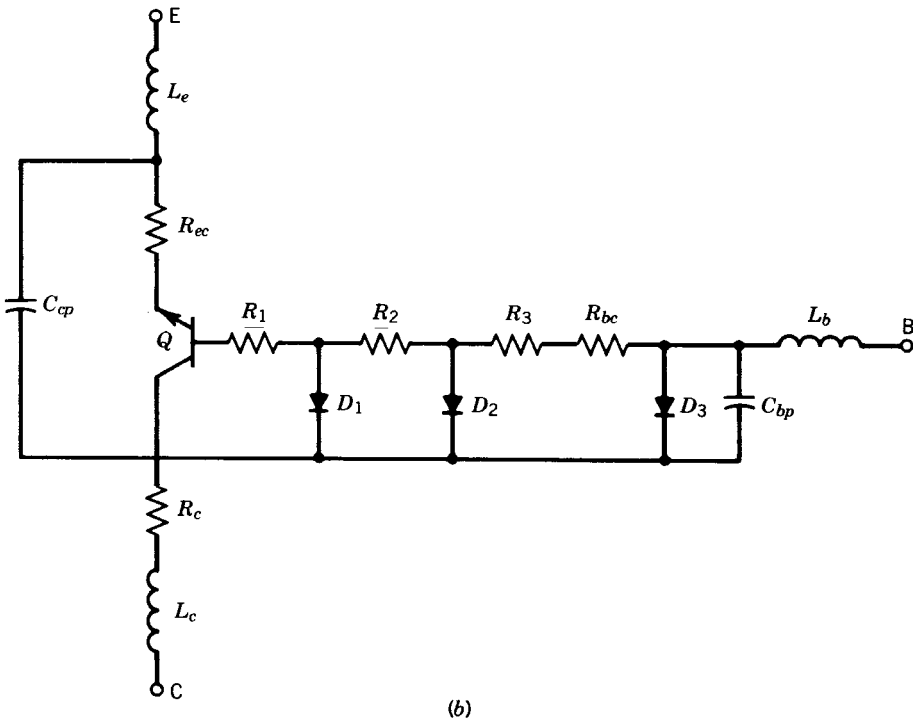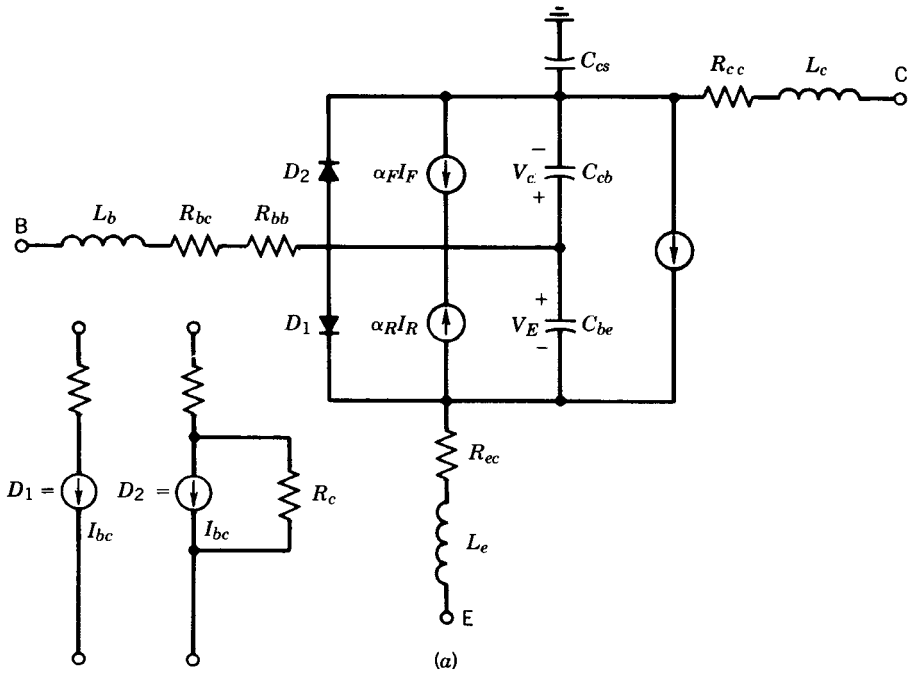
FIGURE 9.24 Nonlinear BJT models: (a) simple nonlinear model suitable for harmonic balance or SPICE analysis; (b) large-signal SPICE model.
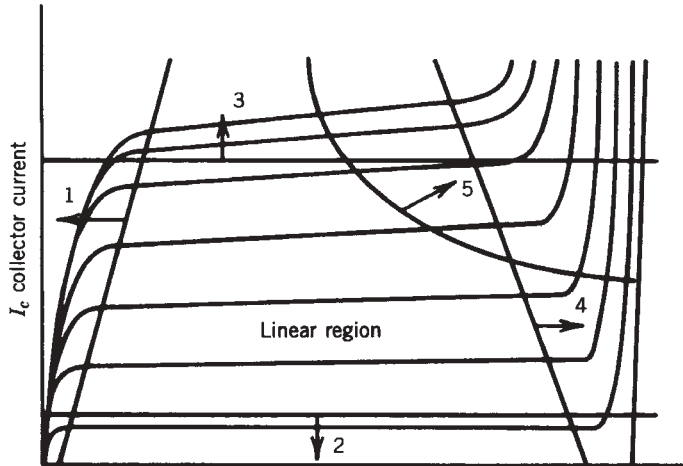
FIGURE 9.25   Bipolar transistor current–voltage characteristics showing linear and nonlinear regions.

nonlinearities occur at low voltages and low currents. The Kirk effect [9.14] limits high-current operations when the collector current density becomes comparable to the doping level in the collector region, which causes the electric field to change in a direction, thus widening the base region. Avalanche breakdown will limit the region of high collector–emitter voltage. The fifth limitation is nonlinear performance due to temperature effects such as thermal runaway and changes in $R_e = kT/QI_E$. Each of these five effects must be included in a large-signal SPICE model.

SPICE model parameters for typical silicon bipolar transistors are given in Table 9.1. Under small-signal conditions, the small- and large-signal models will give identical performance. However, when large-signal drive is applied, the SPICE model will yield nonlinear circuit performance characteristics such as compression, harmonic distortion, oscillator output waveforms and impedances, mixer conversion loss, and circuit transient response.

The nonlinear modeling method above, which is based on RF evaluation of the active device's $I–V$ and breakdown characteristics, allows the designer to evaluate fully the performance of any power field-effect or bipolar transistor. The nonlinear data obtained can be used, in conjunction with small-signal device evaluation, to formulate analytic models such as the one described by Curtice [9.15] for time-domain and harmonic balance simulation (ADS 2002 [9.46]) or nonlinear data can be encoded in a commercial simulator.

Modern analytic nonlinear models, such as the ones developed by Curtice for GaAs and LDMOS [9.47, 9.51], accurately predict circuit performance. These models are accurate for high-power, large-signal conditions and are self-consistent; that is, they are continuously accurate from small- to large-signal operation. A good example of an analytic nonlinear model for LDMOS is the MET model (Motorola electrothermal model). The MET LDMOS model [9.47] is an electrothermal model that can account for dynamic self-heating effects and was specifically tailored to model high-power RF LDMOS transistors used in base-station, digital broadcast, land mobile, and subscriber applications. It has been implemented in Agilent EEsof's ADS [9.46] harmonic balance

TABLE 9.1   Large-Signal SPICE Model Parameters for Microwave Bipolar Transistors

Symbol	Definition	Units	Value for AT-41400 and AT-60500
Transistors (Q)			
IS	Junction saturation current	A	1.65×10^{-18}
BF	Maximum forward beta		100
BR	Maximum reverse beta		5
NF	Current emission coefficient		1.03
VA	Early voltage	V	20
IK	Corner for high-current beta roll-off		0.10
ISE	Base–emitter leakage saturation current	A	5×10^{-15}
NE	Base–emitter leakage emission coefficient		2.5
CJE	Base–emitter zero-bias junction capacitance	F	1.8×10^{-15}
PE	Base–emitter built-in potential	V	1.01
ME	Base–emitter junction grading factor		0.60
FC	Forward-bias depletion capacitance coefficient		0.50
TF	Ideal forward transit time	ps	12
XTF	TF bias dependence coefficient		4
VTF	TF dependency on V_{bc}	V	6
ITF	TF dependency on I_c	A	0.3
PTF	Excess phase at $1/2\,\pi$ TF	deg	35
XTB	Beta temperature coefficient		1.818
Diodes (D_1, D_2, D_3)			
IS	Saturation current	A	1×10^{-25}
CJ0	Zero-bias junction capacitance	F	2.45×10^{-16}
VJ	Junction potential	V	0.76
M	Junction grading coefficient		0.53
FC	Forward-bias depletion capacitance coefficient		0.50
BV	Reverse breakdown voltage	V	45
IBV	Reverse breakdown current	A	1×10^{-9}

simulator, which is capable of performing small-signal, large-signal, harmonic balance, noise, and transient simulations.

The MET LDMOS is an empirical large-signal nonlinear model which is a single piece and continuously differentiable and includes static and dynamic thermal dependencies. This new model is capable of accurately representing the current–voltage characteristics and their derivatives at any bias point and operating temperature. A single continuously differentiable drain current equation models the subthreshold, triode, high current saturation, and drain-to-source breakdown regions of operation. Static thermal equations governing the electrothermal behavior of the drain-to-source nonlinear current model parameters were developed by measuring the nonlinear drain current under pulsed voltage conditions at different operating temperatures, ensuring an isothermal measurement environment. Figure 9.26 depicts the measured-versus-modeled performance of an LDMOS power device.

Pulsed *S* parameters (∼200 μs) were used to develop equations to model the capacitance functions of voltage and temperature which were described by functions that
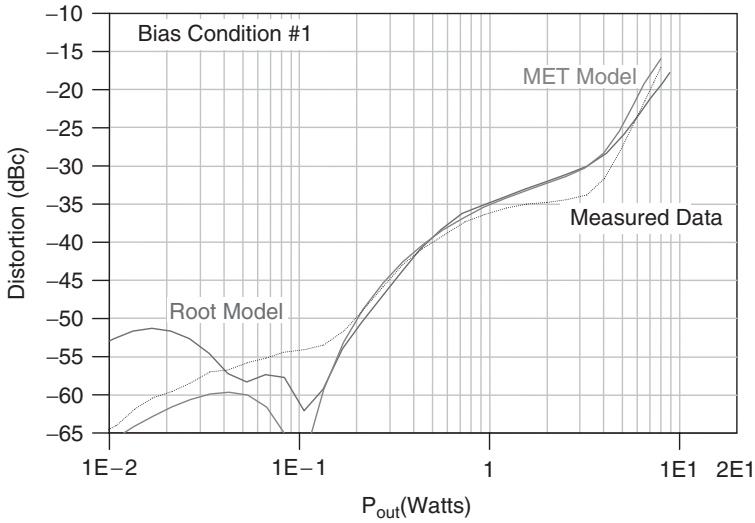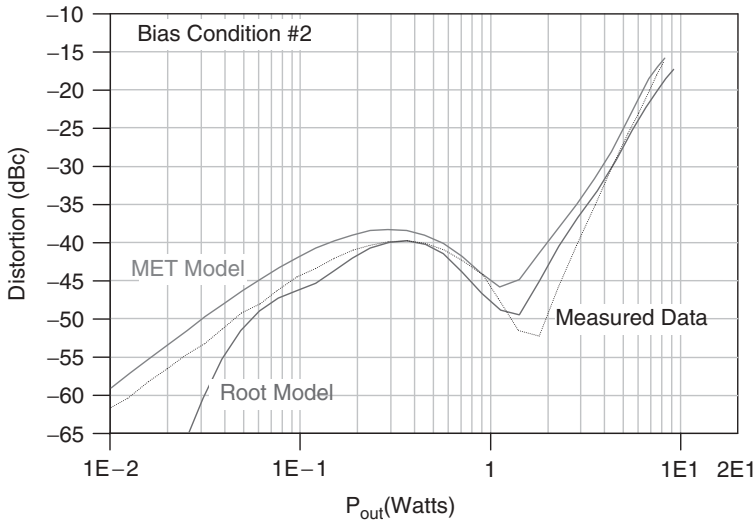
FIGURE 9.26   Third-order distortion performance for an LDMOS power device at several different bias conditions.

have no poles and facilitate robust numerical stability. The nonlinear capacitances were extracted with a small-signal model that represents the small-signal limit of the device nonlinear behavior at any given bias point. Using a thermal analog circuit, as in many previous circuit models, the MET LDMOS model accommodates thermal effects. The self-consistent temperature determined by these circuits sets the values of current control parameters, capacitance values, and source, drain, and gate resistances.

The large-signal equivalent circuit of the MET LDMOS model is shown in Figure 9.27. The model has one voltage- and temperature-dependent nonlinear current
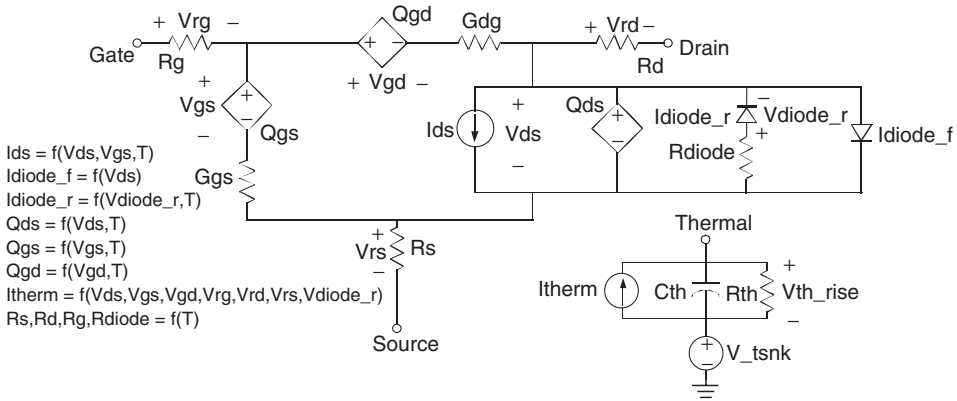
FIGURE 9.27   Large-signal equivalent circuit of MET LDMOS model.
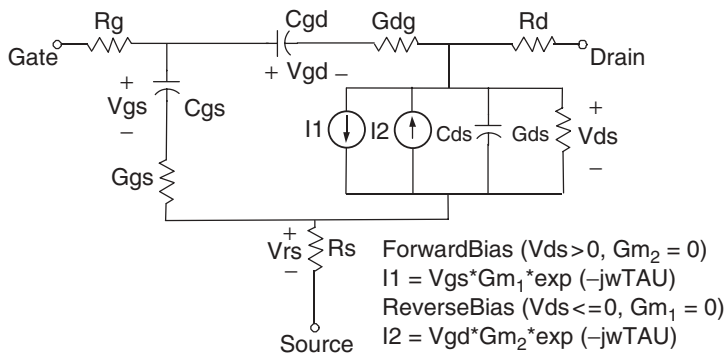
FIGURE 9.28   Isothermal small-signal equivalent circuit fo MET LDMOS model.

source, I_{ds}, as well as a forward diode and a reverse diode. The forward diode is a function of voltage while the reverse diode is temperature and voltage dependent. The reverse diode has a temperature-dependent series resistance associated with it. The model also has three voltage- and temperature-dependent nonlinear charges, Q_{gs}, Q_{gd}, and Q_{ds}. There are two internal gate conductances, G_{gs} and G_{dg}, as well as three temperature-dependent parasitic resistances, R_g, R_d, and R_s. The instantaneous temperature rise is calculated with the use of the thermal subcircuit, where I_{therm} is the total instantaneous power dissipated in the transistor, R_{th} is the thermal resistance, C_{th} is the thermal capacitance, and V_{tsnk} is a voltage source that represents the heat sink temperature of the system. The isothermal small-signal equivalent circuit model produced by linearizing the MET LDMOS model is shown in Figure 9.28. Table 9.2 contains all the MET LDMOS model parameter definitions and their units for a typical device with 5 mm of gate periphery. It should be noted that the model parameters are scalable for virtually any device size. The model parameters are scaled by two different parameters. The parameter AREA, which is the ratio of the desired gate periphery to

TABLE 9.2   LDMOS MET Model Parameters

Parameter Name	Parameter Definition	Default Value	Units
RG0	Gate resistance evaluated at T_{nom}	1	Ω
RG1	Gate resistance coefficient	0.001	Ω/K
RS0	Source resistance evaluated at T_{nom}	.1	Ω
RS1	Source resistance coefficient	0.0001	Ω/K
RD0	Drain resistance evaluated at T_{nom}	1.5	Ω
RD1	Drain resistance coefficient	0.0015	Ω/K
VTO0	Forward threshold voltage evaluated at T_{nom}	3.5	V
VTO1	Forward threshold voltage coefficient	−0.001	V/K
GAMMA	IDS equation coefficient	−0.02	—
VST	Subthreshold slope coefficient	0.15	V
BETA0	IDS equation coefficient; BETA Evaluated at T_{nom}	0.2	—
BETA1	IDS equation coefficient	−0.0002	1/K
LAMBDA	IDS equation coefficient	−0.0025	1/V
VGEXP	IDS equation coefficient	1.1	—
ALPHA	IDS equation coefficient	1.5	1/Ω
VK	IDS equation coefficient	7.0	V
DELTA	IDS equation coefficient	0.9	V
VBR0	Breakdown voltage evaluated at T_{nom}	75.0	V
VBR1	Breakdown coefficient at $V_{gs} = 0$ V	0.01	V/K
K1	Breakdown parameter	1.5	—
K2	Breakdown parameter	1.15	—
M1	Breakdown parameter	9.5	V
M2	Breakdown parameter	1.2	—
M3	Breakdown parameter	0.001	V
BR	Reverse IDS equation coefficient	0.5	1/(VΩ)
RDIODE0	Reverse diode series resistance evaluated at T_{nom}	0.5	Ω
RDIODE1	Reverse diode series resistance coefficient	0.001	Ω/K
ISR	Reverse diode leakage current	1×10^{-13}	A
NR	Reverse diode ideality factor	1.0	—
VTOR	Reverse threshold voltage coefficient	3.0	V
RTH	Thermal resistance coefficient	10	°C/W
GGS	Gate-to-source conductance	1×10^5	1/Ω
GGD	Gate-to-drain conductance	1×10^5	1/Ω
TAU	Transit time under gate	1×10^{-12}	s
TNOM	Temperature at which model parameters are extracted	298	K
TSNK	Heat-sink temperature	25.0	°C
CGST	CGS temperature coefficient	0.001	1/K
CDST	CDS temperature coefficient	0.001	1/K
CGDT	CGD temperature coefficient	0.0	1/K
CTH	Thermal capacitance	0.0	J/°C
KF	Flicker noise coefficient	0.0	—
AF	Flicker noise exponent	1.0	—
FFE	Flicker noise frequency exponent	1.0	—
N	Forward-diode ideality factor	1.0	—

<div align="right">(continued)</div>

TABLE 9.2 LDMOS MET Model Parameters (*continued*)

Parameter Name	Parameter Definition	Default Value	Units
ISS	Forward-diode leakage current	1×10^{-13}	A
CGS1	CGS equation coefficient	2×10^{-12}	F
CGS2	CGS equation coefficient	1×10^{-12}	F/V
CGS3	CGS equation coefficient	-4.0	V
CGS4	CGS equation coefficient	1×10^{-12}	F/V
CGS5	CGS equation coefficient	0.25	—
CGS6	CGS equation coefficient	3.5	1/V
CGD1	CGD equation coefficient	4×10^{-13}	F
CGD2	CGD equation coefficient	1×10^{-13}	F
CGD3	CGD equation coefficient	0.1	$1/V^2$
CGD4	CGD equation coefficient	4	V
CDS1	CDS equation coefficient	1×10^{-12}	F
CDS2	CDS equation coefficient	1.5×10^{-12}	F
CDS3	CDS equation coefficient	0.1	$1/V^2$
AREA	Gate periphery scaling parameter	1	—
NFING	Gate finger scaling parameter	1	—

the gate periphery of the transistor, used in the extraction of the model parameters, is used to set the total device area. The parameter NFING, which is the ratio of the desired number of fingers to the number of fingers of the transistor, is used in the extraction of the model parameters and to set the number of gate fingers [9.48].

The equations for the MET LDMOS model are as follows. The temperature dependency of parasitic resistances is given by

$$R_g = R_{G0} + R_{G1}(T - T_{NOM}) \tag{9.11}$$

$$R_d = R_{D0} + R_{D1}(T - T_{NOM}) \tag{9.12}$$

$$R_s = R_{S0} + R_{S1}(T - T_{NOM}) \tag{9.13}$$

$$T = V_{th\_rise} + V_{tsnk\_sint} + 273 = V_{th\_rise} + T_{SNK} + 273 \tag{9.14}$$

where T is the actual or total temperature (not the temperature rise) in kelvins and T_{NOM} is the temperature at which the parameters were extracted. The value of V_{tsnk} (°C) is numerically equal to the heat-sink temperature T_{SNK} (°C). Notice that although R_{G1}, R_{D1}, and R_{S1} have units of Ω/K, their numerical value will be the same if the units are $\Omega/°C$.

The forward-bias drain-to-source current equation is given by

$$V_{tof} = V_{To0} + V_{To1}(T - T_{NOM}) \tag{9.15}$$

$$\text{BETA} = \text{BETA}_0 + \text{BETA}_1(T - T_{NOM}) \tag{9.16}$$

$$V_{br} = V_{br0} + V_{br1}(T - T_{NOM}) \tag{9.17}$$

To maintain small- to large-signal model consistency, the gate-to-source voltage used in the calculation of the large-signal drain-to-source current is delayed τ seconds:

$$V_{gs\_delayed}(t) = V_{gs}(t - \tau) \tag{9.18}$$

$$V_{gst2} = V_{gs\_delayed} - (V_{tof} + (\gamma V_{ds}) \tag{9.19}$$

$$V_{gst1} = V_{gst2} - \frac{1}{2}\left(V_{gst2} + \sqrt{(V_{gst2} - V_K)^2 + \Delta^2} - \sqrt{V_K^2 + \Delta^2}\right) \tag{9.20}$$

$$V_{gst} = V_{ST} \ln\left(e^{V_{gst1}/V_{ST}} + 1\right) \tag{9.21}$$

$$V_{\text{br\_eff}} = \frac{V_{\text{br}}}{2}[1 + \tanh(M_1 - V_{gst}M_2)] \tag{9.22}$$

$$V_{\text{br\_eff1}} = \frac{1}{K_2}(V_{ds} - V_{\text{br\_eff}}) + M_3\left(\frac{V_{ds}}{V_{\text{br\_eff}}}\right) \tag{9.23}$$

$$I_{ds} = (\beta V_{gst}^{\text{VGEXP}})(1 + \lambda V_{ds})\tanh\left(\frac{V_{ds}\alpha}{V_{gst}}\right)(1 + K_1 e_{\text{br\_eff1}}^V) \tag{9.24}$$

The forward-bias drain-to-source diode is given by

$$V_t = \frac{kNT}{q} \tag{9.25}$$

where k is the Boltzmann's constant (8.62×10^{-5} eV/K), T is the temperature in kelvin, and q is the electron charge (1 eV),

$$I_{\text{diode\_}f} = I_{SS}\left(e^{(V_{ds}-V_{br})/Vt}\right) \tag{9.26}$$

The reverse-bias drain-to-source current equation is given by

$$V_{tor} = V_{ToR} + V_{To1}(T - T_{\text{NOM}}) \tag{9.27}$$

$$V_{gst2} = V_{gs\_delayed} - (V_{tor} - \gamma V_{ds}) \tag{9.28}$$

$$V_{gst1} = V_{gst2} - \frac{1}{2}\left(V_{gst2} + \sqrt{(V_{gst2} - V_K)^2 + \Delta^2)} - \sqrt{V_K^2 + \Delta^2}\right) \tag{9.29}$$

$$V_{gst} = V_{ST} \ln\left(e^{V_{gst1}/V_{ST}+1}\right) \tag{9.30}$$

$$I_{ds} = (\beta_R)(V_{ds})(V_{gst}) \tag{9.31}$$

The reverse-bias drain-to-source diode is given by

$$V_{t2} = \frac{kN_RT}{q} \tag{9.32}$$

$$I_{sm} = I_{SR}\left(\frac{T}{T_{\text{NOM}}}\right)^{3/N_R} \exp\left[\left(\frac{-E_g}{V_{t2}}\right)\left(1 - \frac{T}{T_{\text{NOM}}}\right)\right] \tag{9.33}$$

where E_g is the energy gap for silicon, which is equal to 1.11 [9.49], and T is temperature in kelvin,

$$I_{\text{diode\_}r} = I_{sm}\left(e^{V_{\text{diode\_}r}/V_{t2}} - 1\right) \tag{9.34}$$

The reverse-diode series resistance is given by

$$R_{\text{diode}} = R_{\text{DIODE0}} + R_{\text{DIODE1}}(T - T_{\text{NOM}}) \tag{9.35}$$

The gate-to-source capacitance equation is given by

$$C_{gs} = (C_{GS1} + C_{GS2}\{1 + \tanh[C_{GS6}(V_{gs} + C_{GS3})]\}$$
$$+ C_{GS4}[1 - \tanh(V_{gs}C_{GS5})])[1 + C_{GST}(T - T_{\text{NOM}})] \tag{9.36}$$

The gate-to-drain capacitance equation is given by

$$C_{gd} = \left(C_{GD1} + \frac{C_{GD2}}{1 + C_{GD3}(V_{gd} - C_{GD4})^2}\right)(1 + C_{GDT}(T - T_{\text{NOM}})) \tag{9.37}$$

The drain-to-source capacitance equation is given by

$$C_{ds} = \left(C_{DS1} + \frac{C_{DS2}}{1 + C_{DS3}V_{ds}^2}\right)[1 + C_{DST}(T - T_{\text{NOM}})] \tag{9.38}$$

The noise is calculated as in Ref. 9.49 as the sum of the thermal channel noise and the flicker noise, as shown by the following equation:

$$\overline{i_d^2} = \frac{8kTg_m}{3} + K_F\left(\frac{I_{ds^{A_F}}}{f^{F_{FE}}}\right) \tag{9.39}$$

where g_m is the transconductance of the device at the operating point, T is temperature in kelvin, and f is the frequency. In addition, all resistors are modeled as thermal noise sources:

$$\overline{i_{d_R^2}} = \frac{4kT}{R} \tag{9.40}$$

where R is the resistance value and T is the temperature in kelvin.

To avoid convergence problems, the maximum temperature rise, $V_{\text{th\_rise}}$ (°C) is limited to 300°C using the following equation:

$$V_{\text{th\_rise}} = \begin{cases} 0 & 0 \leq V_{\text{th\_rise}} \\ V_{\text{th\_rise}} & 0 < V_{\text{th\_rise}} < 250 \\ 250 + 50\tanh\left[\dfrac{V_{\text{th\_rise}} - 250}{50}\right] & 250 \leq V_{\text{th\_rise}} \end{cases} \tag{9.41}$$

The Curtice–Ettenberg FET model, often call the Curtice model, is the most widely used model by GaAs MMICs and analog circuit designers. More recently, the updated version of the model has proven useful in modeling today's GaN HEMT devices [9.50]. The original model [9.52], published in 1985, has some deficiencies that have been remedied by the new version [9.50]. Unfortunately, most of these improvements have not made it into the installed models in present-day circuit simulators.

It is a simple model for a complex device. It is a lumped, equivalent-circuit SPICE model, often called a compact model. Figure 9.29 shows the topology of the model. The model describes dc, small-signal, and large-signal behavior of the device. Because
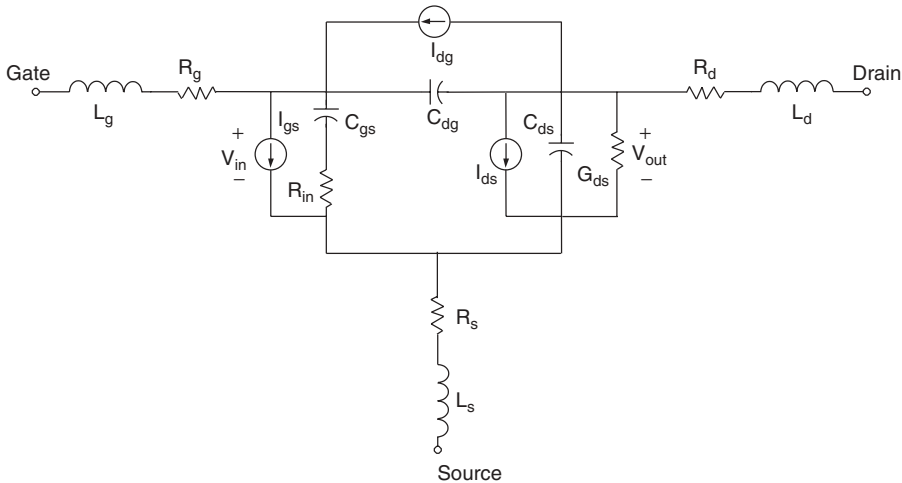
FIGURE 9.29   Typical large-signal model for GaAs MESFET.

of the relatively few device parameters and ease of extraction (polynomial fit), it is often the first model tried for initial circuit simulations. In the later stages of circuit development, the designer may use more sophisticated models that do better at such things as matching the transconductance nonlinearity and capacitance functions.

The gate control of drain current is specified by a cubic polynomial. That makes the transconductance a second-order polynomial. Extraction of polynomial coefficients is easily accomplished by many software packages. The pinchoff voltage is not a parameter of the model because it changes with drain–source voltage, as specified by the parameter β. This effect is common to all MESFETs and HEMTs, no matter what semiconductor material is used. It results because the larger energy of the electrons at larger drain–source voltage requires stronger transverse electric field to pinch off the drain current stream.

In many simulators convergence problems with this model usually are due to the gate–source voltage becoming outside of the range used for the polynomial fit. The cubic polynomial is not well behaved outside of the fitting range. Most of the time, the problem is in the pinchoff region. The implementation of the model in ADS 2002 seems to behave better than most in this regard. Steve Maas has described a method of fixing this problem by improving the extraction of the polynomial coefficients [9.53]. The updated version of the model fixes this by some additional code that properly handles operation near pinchoff and subthreshold conditions.

The 1985 model has nonlinear capacitance functions, drain–gate avalanche break-down currents, transconductance time delay, and forward gate–source conduction. Dispersion in drain–source conductance is provided but dispersion in transconduc-tance (GMO) is not. The drain–source voltage-controlled current source (or VCCS) does not have to match both GDS and GMO data because it has an additional resistor (RDS) in parallel with it. The RDS is not a function of voltage but should be chosen for the quiescent bias point.

While the original model was shown to agree well with data for GaAs MESFET power sweeps, load-pull measurements, and IMD data for class A and AB devices, many applications now involve multichannel operation and CDMA-type modulation

TABLE 9.3   Model Parameters for Curtice–Ettenberg Nonlinear Model

Parameters	Definition
A0, A1, A2, A3	Cubic polynomial coefficients for IDS–VGS relationship
VDSO	VDS for which *A*'s evaluated
BETA	Coefficient for pinchoff voltage change with VDS
GAMMA	Current saturation parameter
VBR	Gate–drain breakdown voltage
R1	Breakdown resistance
R2	Resistance relating breakdown voltage to channel currents
RD, RS, RG	Drain, source, and gate fixed resistances
RDSO	Drain–source RF resistance, in parallel with VCCS
VBI, RF	Built-in voltage, resistance for simple forward gate conduction model
IS,N	Parameters for alternate gate diode model
CDS	Constant drain–source resistance
CGS(V), CGD(V)	Gate–source and gate–drain capacitances, voltage functions available depend upon simulator
TAU	Transit time delay associated with transconductance
RIN	Resistance in series with CGS

schemes. This requires more careful extraction of model parameters and possibly some tailoring of the model to the application environment. For cell phone applications, the power chip must be operated over a wide temperature range and will have significant self-heating effects. The model for the design of such a circuit must include self-heating effects and have the transistor characterized over a wide temperature range. A simple approach is to incorporate a thermal analog circuit as part of the model. Such circuits have been used in SPICE and harmonic balance simulations for years [9.54, 9.55].

Table 9.3 shows the fundamental parameters of the simple form of the model. To use the simple model in power amplifier applications, one would evaluate all parameters at the expected operating temperature of the device. The capacitance and external parasitics should be evaluated in the region of the quiescent operating bias condition. If this is done properly, then the large-signal simulation results at low signal levels (from SPICE or a harmonic balance simulator) will be essentially the same as that obtained for small-signal (ac) simulations. Power simulations should produce good agreement with data for power output, gain, and power-added efficiency. If the characterization is carefully done, both the load-pull and IMD simulation should be in good agreement with data [9.56].

If an advanced version of the model is used, then the *A* coefficients need to be extracted at several different heat-sink temperatures and the thermal resistance and thermal time constant need to be measured. Using a thermal analog circuit, the model is then able to adapt its parameters to be self-consistent with the heating effects produced by the parameter values and the operating condition. For example, bias power converted to RF output power would not heat the device and is not included in such simulations.

9.3   OPTIMUM LOADING

The goal of designing with optimal load conditions is to achieve a specified performance parameter such as maximum gain, linearity, or power. This becomes more difficult as

circuit nonlinearities and the operating frequency increase. In the previous section, several modeling and simulation methods were described which varied from simple linear FET approximations to elaborate CAD simulations. The circuit performance obtained when using the previous modeling methods to determine proper device loading conditions, as they relate to maximizing power output performance, will now be described.

The simplest method commonly used to determine the optimum load impedance (Z_{opt}) for a GaAs FET or any other device is the load line approach. In this method, the operating point of the FET is approximated by a straight line extending from the maximum current point on the drain current axis to the maximum voltage (breakdown) point on the drain voltage axis on the FET characteristic curves. If dc measurements, such as a curve tracer, are used to obtain FET drain characteristics, the load resistance that is obtained will be quite different from the value determined from the RF drain characteristics. As an example, two such load lines are illustrated in Figure 9.30. The first line is drawn from I_{max}, obtained from (long-pulse) pulsed $I-V$ measurements (dc), to V_{br} and yields a load resistance value of 80 Ω. The second line is drawn form the true value of I_{max} (RF) to the same value of V_{br}. When the slope of the RF load line is calculated, the value obtained for R_{opt} is 120 Ω. A load error of this magnitude can seriously degrade the power output performance of any amplifier. The computation of R_{opt} using a RF load line approach can be further refined by absorbing the FET and mounting parasitics into the output circuit matching network. The parasitic absorption effectively places the value of R_{opt}, which was calculated from an RF load line, directly across the FET current source, thus simulating the results obtained for Z_{opt} from the load-pull method of Figure 9.10. This technique is Illustrated in Figure 9.31.
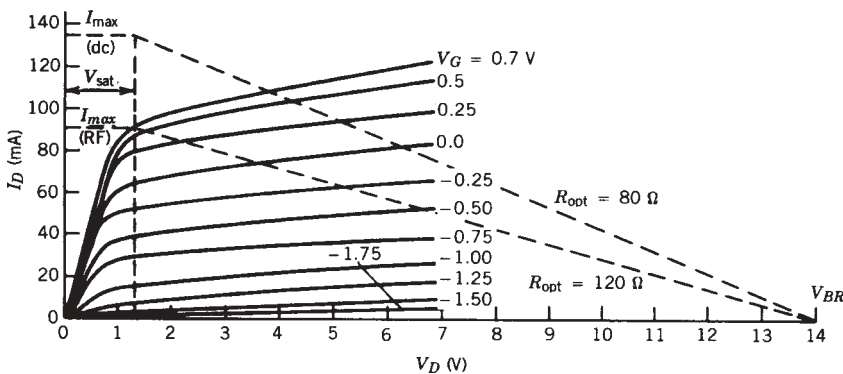
FIGURE 9.30   Calculation of R_{opt} using dc and RF load lines.
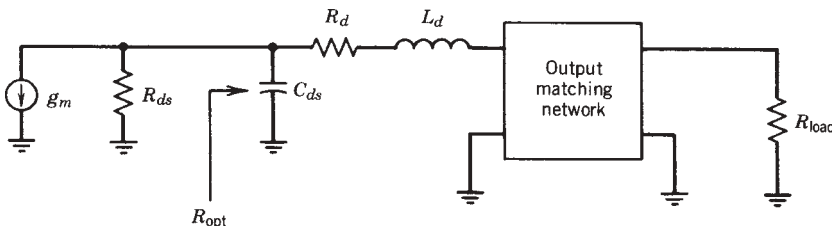
FIGURE 9.31   FET parasitic absorption into output matching network.

Absorbing the device parasitics in the above manner is a very effective method in designing broadband amplifiers when load-pull data or a nonlinear simulator is unavailable. In practice, about 1 dB of output power is sacrificed using this approach. Improvements in amplifier efficiency, accomplished by properly selecting harmonic terminations, also cannot be accomplished with the above simple technique. This is also a good check on the validity of either load-pull data or the performance of a nonlinear simulation.

The most accurate approach in determining optimum load impedance is with the use of a nonlinear simulator provided the active device is properly modeled. Constant-power contours can be generated by varying the output impedance terminating the FET (or active device) and observing the calculated circuit power output. The effect by other circuit parameters, such as dc bias, feedback, and input terminating impedance, on power output should be included in the search for Z_{opt}. The maximum power output (P_{max}) and several constant-power contours for a simple amplifier consisting of a FET with a 50-Ω input termination are shown in Figure 9.32a. The FET used in the analysis is the device described in Figure 9.13. It should be noted that 50-Ω harmonic terminations were used in the analysis, thus simulating an active load-pull measurement.

Optimizing the load termination at the signal harmonics can enhance amplifier efficiency and power output. In the case of broadband design, the designer usually does not have the flexibility in selecting the proper harmonic terminations since several harmonics can fall within the amplifier's operating bandwidth. However, harmonic termination optimization can be very effective for amplifiers designed to meet narrow-band phased-array radar applications or in the efficiency enhancement of class B power designs. To illustrate the importance in selecting the correct FET terminating impedance, an analysis of the same FET amplifier used in the above example was conducted using all of the above-described R_{opt} and Z_{opt} calculations including terminating the amplifier with a load equal to S_{22}^*. Harmonic terminations were also adjusted to maximize power output performance. The results are shown in Figure 9.32b. As can be seen in the above illustration, a good approximation to the true value of Z_{opt} can be had by using the RF load line method in conjunction with parasitic absorption techniques.

9.4 SINGLE-STAGE POWER AMPLIFIER DESIGN

The synthesis techniques for power GaAs FET single-stage amplifiers closely parallels the method employed in small-signal design with the exception of several major areas. The problem of gain shaping to achieve a specified frequency response, which typically means gain flattening, is even more constrained when designing power amplifiers because the output matching network must be designed for optimum power output performance. Terminating the FET with the optimum power load also implies that the small-signal output return loss of the finished amplifier will probably be poor. Since no gain shaping and impedance matching can be accomplished with the output matching network, the entire burden of gain flatness falls on the input network. Unless lossy matching or feedback techniques are employed in the design of the input network, the input reflection coefficient of the resulting amplifier will also be poor. If the operating bandwidth is sufficiently narrow, a stand-alone amplifier stage can exhibit low-input VSWR and flat gain performance. However, when broadband performance is desired,
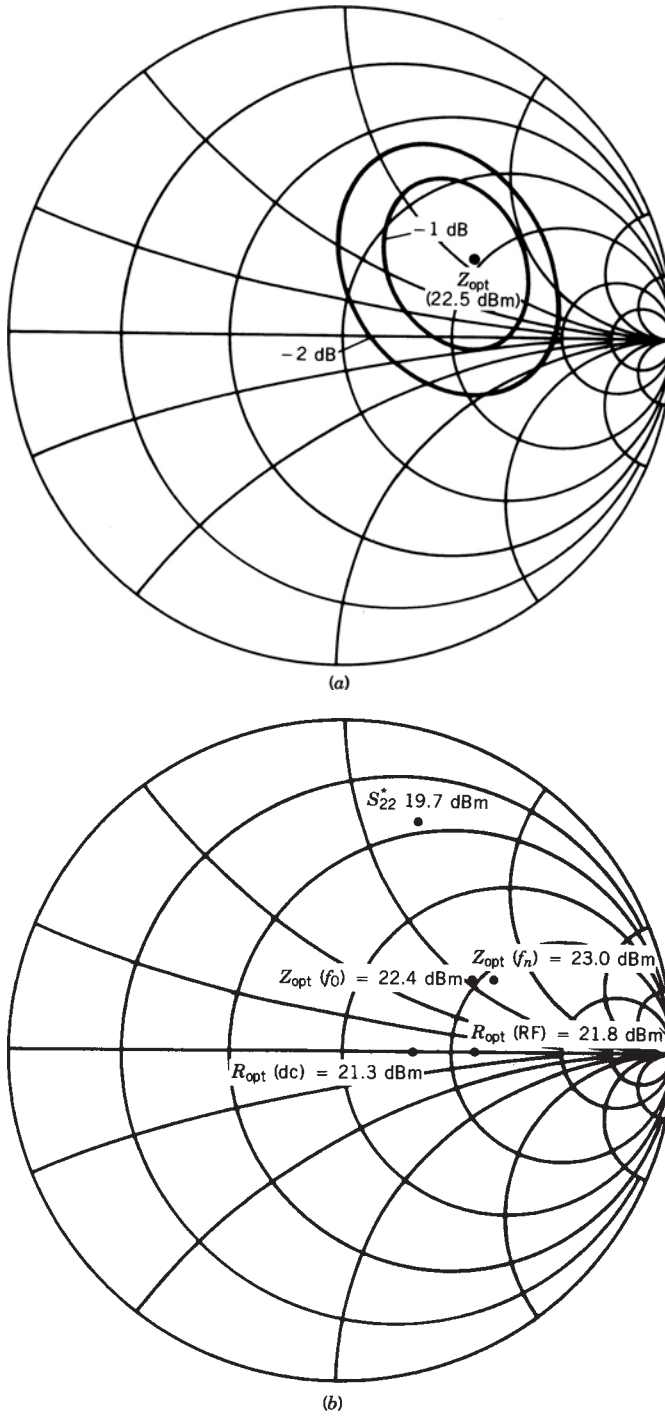
FIGURE 9.32 Nonlinear power output performance of typical FET: (*a*) constant-power contours obtained from harmonic balance simulator: (*b*) FET amplifier power output for various load terminations.

two identical amplifier stages can be combined with the use of 90° quadrature couplers (balancing) in order to achieve a low input and output VSWR. Drain and gate bias networks are usually ignored in small-signal design but can be very troublesome when realizing power gain stages. Special consideration must be given to the drain bias and decoupling networks, because drain currents of several amperes are not uncommon when using large-power GaAs FETs, particularly at low operating voltages. Amplifier stability requirements, especially at very low frequencies, further complicate bias circuit design. It should also be remembered that the fusing current of 0.001-in.-diameter gold wire is less than 1 A; hence, hybrid bias circuits can be comprised of several parallel bond wires. The fusing current problem becomes intensified in MMIC design since high-impedance microstrip decoupling lines are less than 10 μm wide. Similar to hybrid design, multiple drain bias networks are often employed to supply sufficient current to large-power devices.

The problems encountered in gate biasing are somewhat different. Although out-of-band stability requirements must be considered in gate bias network design, gate current requirements, which do not exist in small-signal designs, cannot be forgotten. At low drive levels and with reverse bias applied to the FET gate, no gate current is present. However, at high drive levels and with the same reverse bias applied, the RF signal can easily forward bias the FET for a short portion of the RF cycle. During these forward-bias excursions considerable gate currents can be developed even though the average current might only be several milliamperes. Large current spikes present on the gate bias line can drastically alter the operating point of the FET. These shifts in operating point will degrade the amplifier's power output performance. Most bias problems, however, can be eliminated with a "stiff" or very well regulated negative-voltage supply lines. Bias and matching network realization problems are easily illustrated with the following example.

A single-stage amplifier designed to operate within the 9- to 10-GHz frequency band can be synthesized using the 300-μm FET described in the previous section. This FET, when properly biased and terminated, can develop approximately 22.5 dBm of output power when driven into saturation. However, excellent power output and efficiency performance can only be obtained if the amplifier has optimum harmonic terminations. The importance of harmonic tuning varies depending on the device technology. GaAs or InGaP HBTs are the most sensitive to harmonic terminations, while power LDMOS devices are the least affected by harmonic loading.

The design begins by first synthesizing the output load network [9.16, 9.17, 9.18]. The network must transform the 50 Ω load impedance to the optimum load impedance (Z_{opt}) required by the FET. The optimum load impedance, which is shown in Table 9.4, was determined with the aid on a nonlinear solver for the fundamental frequency as well

TABLE 9.4 Optimum Load Impedance at Fundamental and Harmonic Frequencies

f_0 (GHz)	Z_{opt} (desired)		
	Fundamental	Second Harmonic	Third Harmonic
9.0	0.490$\underline{/23°}$	0.999$\underline{/80°}$	0.999$\underline{/180°}$
9.5	0.520$\underline{/28°}$	0.999$\underline{/82.5°}$	0.999$\underline{/180°}$
10.0	0.560$\underline{/31°}$	0.999$\underline{/85°}$	0.999$\underline{/180°}$
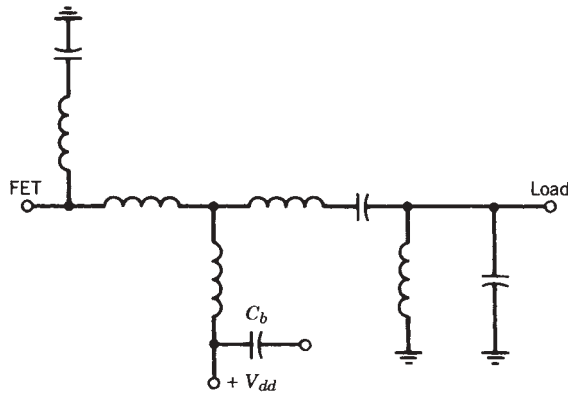
FIGURE 9.33   Lumped-element bandpass output network.
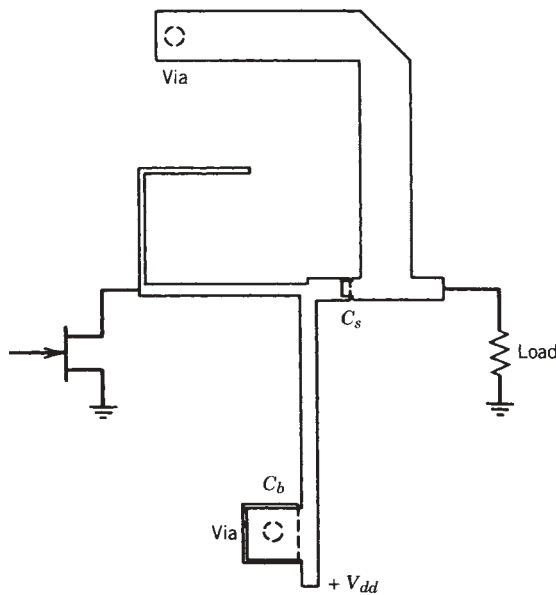
FIGURE 9.34   Distributed bandpass output network with harmonic terminations.

as for the second and third harmonics. Using these target values for the terminating impedance, a lumped-element matching network was synthesized using the method developed by Levy [9.25]. The bandpass network, which employs a shunt inductor and series capacitor to facilitate biasing and decoupling, is shown in Figure 9.33. The lumped-element realization was then converted to a distributed structure by employing high-impedance transmission lines for inductors, low-impedance transmission lines for the output parallel $L-C$ resonator, and a monolithic capacitor for the series match- ing capacitor [9.19]. A quarter-wavelength open-circuit resonator (third harmonic) was used to simulate the series $L-C$ network at the FET end of the network. Computer optimization was then used to trim the network performance. The resulting output

matching network is shown in Figure 9.34. The load impedances presented to the FET are summarized in Table 9.5. As can be seen in Table 9.5, the load obtained after optimization using nonideal elements is very close to the desired values presented in Table 9.4. A Smith chart plot of the target versus actual values is also shown in Figure 9.35.

The input matching network was synthesized in a similar manner in lumped-element form. The source and load impedances used were 50 Ω and S_{11}^* of the FET/load network combination, respectively. The network was then converted to microstrip monolithic topology. Amplifier gain flatness was achieved by optimizing only the input network of the complete circuit. The resulting small-signal gain is shown in Figure 9.36.

Although the above design employed harmonic terminations, a variety of output network topologies were analyzed to aid in illustrating the improvements in efficiency and power performance obtainable with this design approach. A summary of key performance variations as a function of output network design philosophy is presented in Table 9.6. It should be remembered that $Z_{\mathrm{opt}}(f_0)$ was synthesized to simulate the optimum load impedance obtained from a load-pull measurement test setup (harmonics terminated in 50 Ω).

The optimum network synthesized is substantially more complex than a simple two-element low-pass matching structure, but the added power and efficiency usually outweigh this drawback. It should also be noted that the networks presented, which were not designed to load the harmonics with optimum terminations, were also not allowed to degrade amplifier performance. Degradation in performance can occur when

TABLE 9.5   FET Load Impedance with Monolithic Distributed Bandpass Matching Network

f_0 (GHz)	Z_{load} (actual)		
	Fundamental	Second Harmonic	Third Harmonic
9.0	$0.510\underline{/25°}$	$0.749\underline{/134°}$	$0.961\underline{/-166°}$
9.5	$0.460\underline{/28°}$	$0.752\underline{/70°}$	$0.961\underline{/177°}$
10.0	$0.480\underline{/29°}$	$0.830\underline{/0°}$	$0.954\underline{/159°}$

TABLE 9.6   Key Performance Variations of a Single-Stage Amplifier as a Function of Output Matching Network Characteristics

f_0 (GHz)	Z_{load} (actual)	Z_{opt} (f_0)	R_{opt} (dc)	R_{opt} (RF)	Z_{opt} (ideal)	S_{22}^*
		Power Output (dBm)				
9.0	22.6	22.0	21.4	21.9	23.0	19.8
9.5	22.8	22.0	21.4	21.9	23.0	19.8
10.0	22.8	21.7	21.3	21.8	22.9	19.7
		Power-Added Efficiency (%)				
9.0	43.3	37.0	27.2	34.0	48.0	19.8
9.5	44.0	37.3	27.9	34.9	47.7	17.5
10.0	45.1	36.5	26.3	31.1	46.3	15.6
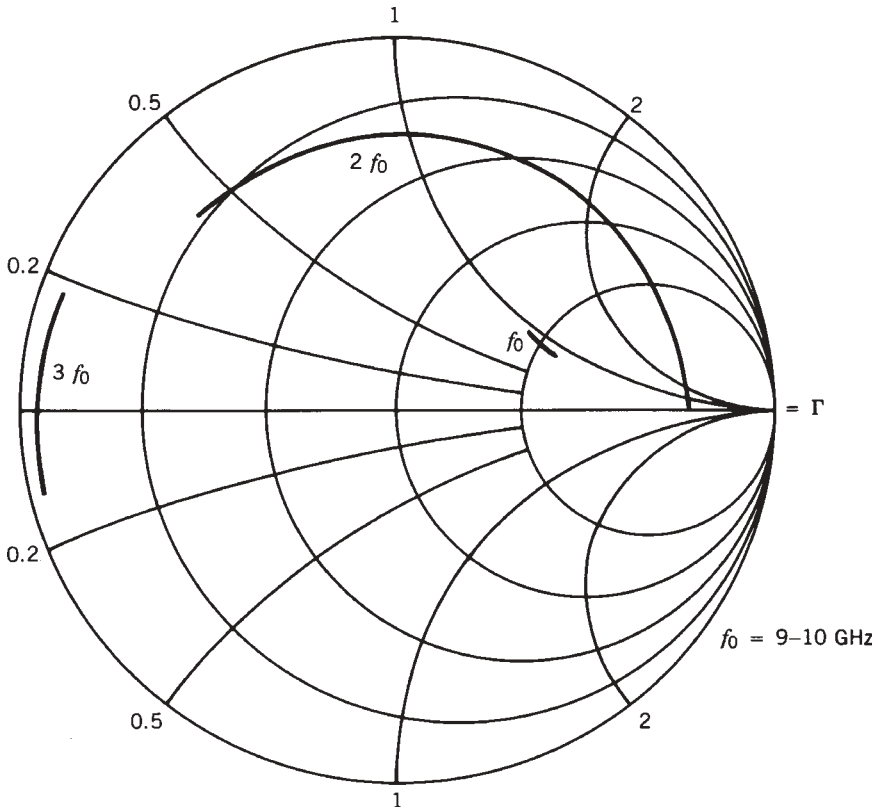
FIGURE 9.35   Desired load impedance as a function of frequency.
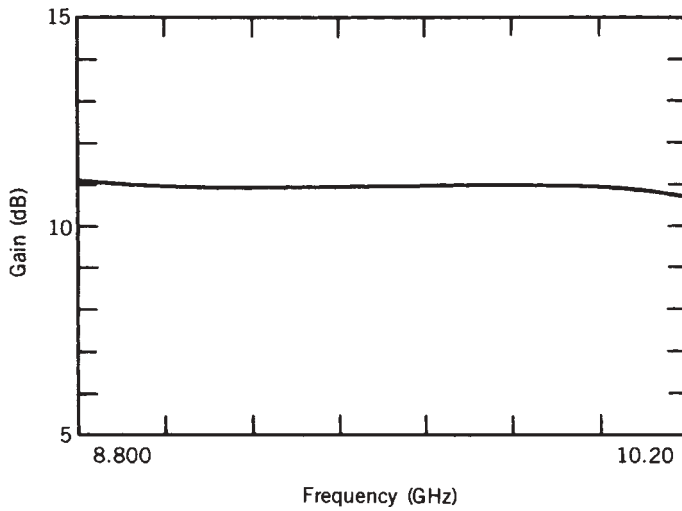
FIGURE 9.36   Calculated small-signal gain performance of single-stage amplifier.

the second, third, and fourth harmonics are terminated in such a manner as to reduce circuit power output and efficiency. This condition can easily occur with linear design methods or with design techniques, which only concentrate on fundamental frequency of operation, such as most load-pull techniques.

A nonlinear circuit simulator was also used to evaluate several popular forms of biasing, such as resistive dividers on the negative gate dc supply line and conventional self-biasing in the FET source path. In the self-biasing approach the source resistor was adjusted so that the small-signal drain current was exactly the same as with an ideal dual-power-supply scheme. However, as the input power to the amplifier was increased, the drain current decreased and the saturated output power achieved was approximately 0.5 dB less than that obtained in the above example. The source resistor was then adjusted so that the FET drain current under large-signal conditions was equivalent to the original small-signal case. Although the power output of the amplifier increased, it could never be completely restored. Amplifier efficiency was also markedly reduced.

The situation was similar when a high-dc-impedance (1-kΩ) gate bias supply was employed. The power output of the amplifier dropped several decibels when it was driven near saturation. However, no amount of bias voltage adjustment could restore amplifier performance. With the power supply impedance reduced to 50 Ω, amplifier performance was still poor.

The above example has shown that considerable improvement in power performance and efficiency can be obtained when the output load network is designed to optimally terminate the fundamental and harmonic frequencies. Matching techniques, which are commonly used in broadband design, can be successfully employed in designing practical narrow-band networks, particularly if monolithic realization is desired. However, careful bias design must be used in conjunction with the above RF techniques so that the final amplifier will perform to expectations.

9.5 MULTISTAGE DESIGN

Before the widespread availability of computer-aided analysis and synthesis, microwave multiple-stage power amplifiers were usually composed of cascaded balanced single-stage gain blocks. Although this approach allowed for ease of design, optimum performance and size could not be achieved. Presently, the design philosophy is shifting toward direct cascading of gain stages, which is due in part to the industry's demand for smaller, more efficient circuits, accurate modeling techniques, and the availability of numerous CAD amplifier synthesis packages. These commercially available computer programs are excellent in designing small-signal amplifiers but only provide starting values for multistage power amplifier design. The design problem is further compounded when broadband performance is required.

These complications are easily illustrated by examining the general design procedure of the small-signal two-stage amplifier depicted in Figure 9.37. The amplifier consists of three basic networks: (1) input network, (2) interstage network, and (3) output network. Typically the input and output networks are designed to provide an impedance transformation between the FET (or other active device) and measurement system, while the interstage network is used to provide the necessary gain shaping required to compensate for the 6 dB/octave rolloff of each FET. However, this technique cannot be directly applied to the design of power amplifiers.
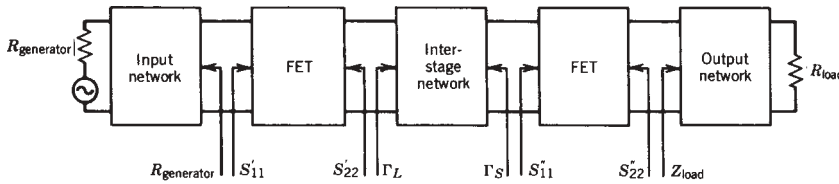
FIGURE 9.37   Representative two-stage amplifier. (Courtesy of Texas Instruments.)

As in the case of single-stage design, the output matching network for large-signal applications must be designed to terminate the FET with the optimum load impedance at both the fundamental and harmonic frequencies. Harmonic terminations unfortunately are not always possible in broadband designs because harmonics can easily fall within the operating bandwidth of the amplifier. Also, when the output network is designed for large-signal performance, the amplifier's output VSWR (small signal) will tend to be poor, although RF feedback may aid in improving the match but not in eliminating some of the mismatch problems. When designing multistage amplifiers for narrowband handset applications, where efficiency and power output performance are desired, optimum matching with no feedback is usually preferred. The design of these amplifiers should start with the design of the output network and output device since there is the least amount of design flexibility at this point in the circuit.

The design of the interstage network is similarly hampered because it must be designed for both gain shaping and maximum power transfer performance between amplifier stages, with the later condition taking precedence, especially at higher frequencies [9.20–9.22]. At the upper band edge, where the active device gains are at their lowest value, sufficient drive power must be available for the output device. Thus, the size of the driver device must be sufficiently large to supply this power. At the lower band edge the output device will exhibit more gain, hence requiring less drive power.

However, if the interstage network is designed to provide gain shaping by mismatching the output of the driver and the input of the output stage, the driver transistor may be loaded in such a manner as to prevent it from delivering sufficient drive power. Even if the mismatch loss from the interstage network is small (less than 1 dB), the power transfer loss can easily be several decibels, due to the fact that the driver device is not terminated with the network impedance, near Z_{opt}. Unfortunately, amplifiers designed using linear simulation methods usually exhibit excellent gain performance but can easily have severe power output performance shortfalls, especially if the operating bandwidth is large. The input network of the two-stage power amplifier, if it is of the lossless form, must then provide the remainder of the frequency response contouring required by the total amplifier at the expense of input VSWR. Thus, the completed amplifier can exhibit flat gain and power performance for broadband operation but may exhibit unmatched terminal impedances. The above description illustrates that the most difficult portion of designing multiple-stage amplifiers is the interstage network synthesis. A variety of network synthesis techniques have been described in the literature which were specifically developed to aid in the design of broadband amplifiers. These synthesis methods, which can either be low-pass or bandpass approaches, provide gain sloped responses and generate matching networks for complex-to-real or complex-to-complex load impedances. The synthesized networks are usually of lumped-element form which are later converted to distributed form. Excellent gain

flatness performance for small operation is obtained with these synthesis methods, such as the Real Frequency Technique proposed by Carlin [9.23] or the bandpass synthesis technique described by Mellor [9.24]. Although these methods produce networks with the required transfer function to achieve the amplifier's desired frequency response, the element values are often unrealizable. The terminal impedances are also unconstrained; thus, the resulting amplifier may exhibit poor power output performance. However, broadband synthesis techniques do provide excellent starting values for matching network elements. There is also the hidden problem of stability with multistage designs, particularly if the operating bandwidth is wide. The stability factor K is not a useful indication of stability with multistage designs. However, if the stability factor is less than unity, rest assured that there is a stability problem. Unfortunately, the converse is not true. The NDF method, which is tedious to implement and will be highlighted later, is an accurate way to determine stability [9.51].

The problems in designing multistage amplifiers with lossless networks can be eliminated or at least significantly reduced by employing either (1) RF feedback techniques or (2) some form of lossy matching networks. At frequencies where substantial device gain is available, RF feedback can provide excellent gain shaping, stability, and impedance control while significantly reducing distortion. Transformer, resistive series and shunt, as well as bootstrapping are just a few common feedback methods that can be successfully employed at lower microwave frequencies.

In the upper end of the microwave spectrum, the benefits of RF feedback become diminished since there is little available excess gain. It then becomes necessary to employ other techniques, such as loading, to control impedance variations. Resistive loading techniques are quite effective in achieving input and interstage networks with upward-sloped gain performance characteristics that still exhibit well-controlled terminal impedances.

The synthesis of loaded (lossy) matching networks is considerably more empirical than conventional network synthesis and is usually accomplished through optimization methods. Several basic element topologies [9.19], which are composed of R, L, and C, can be incorporated into input and interstage designs to dissipate power at the low-frequency end of the operating bandwidth while maintaining low loss at the higher frequencies. Typical topologies with their respective frequency response characteristics are shown in Figure 9.38. The simple networks shown in Figures 9.38a, b, and c can easily be combined in an interstage network in order to bound the impedance presented to the driver stage. For example, when the operating bandwidth is large, high-order networks are required to provide the impedance transformation and gain contouring. However, the input impedance (driver end) of the network can traverse a path near the rim of the Smith chart as the operating frequency approaches the low end of the operating band. Hence, these frequency-dependent series and shunt elements tend to confine the impedance seen by the driver transistor to a region closer to the impedance at the high end of the operating band while still providing the prescribed frequency response contour. The equalizer element in Figure 9.38d is very useful in eliminating gain peaks that may arise through narrow frequency bands. The network depicted in Figure 9.38e can be designed with a predescribed attenuation-versus-frequency performance for bandwidths exceeding several octaves and exhibits real terminal impedances at dc, thus aiding amplifier low-frequency stability. The above networks combined with bandpass matching techniques usually provide the best compromise between passband ripple performance, amplifier stability, and circuit complexity. Design trades of this
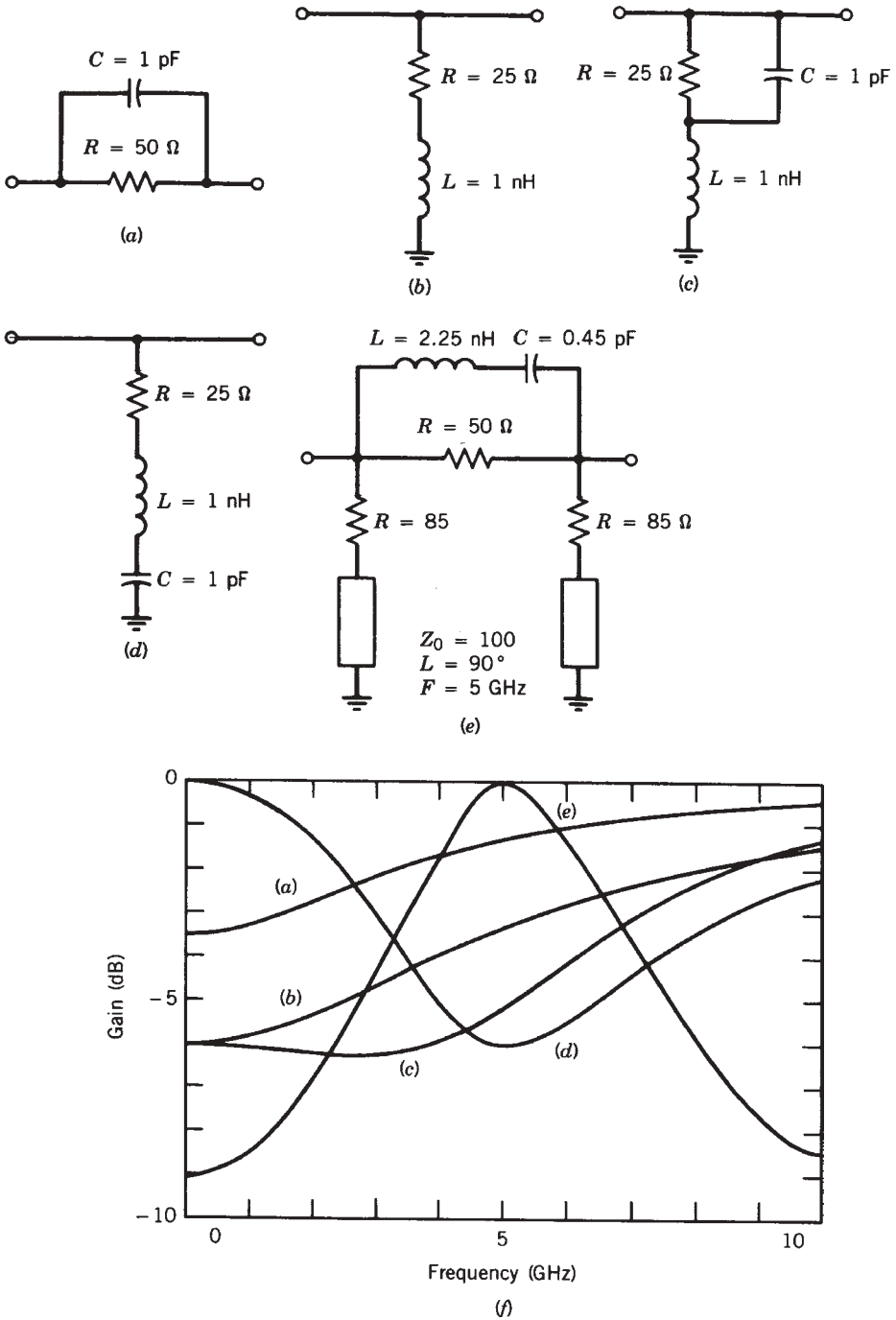
FIGURE 9.38 (*a–e*) Typical amplitude equalization networks. (*f*) Respective frequency characteristics.

type are illustrated in the following two-stage power amplifier design example. The design goals for a 6- to 18-GHz monolithic two-stage amplifier are shown in Table 9.6.

The first step in the design process is to determine the required output FET periphery from which the output power specification can be obtained. The FET can easily be sized by employing a RF load line analysis. If we assume a RF breakdown voltage of 18 V and a pinchoff voltage of -5 V dc, the maximum RF voltage swing is approximately 10.5 V. Hence, the peak-to-peak RF current required to develop 1 W at the load must be a minimum of 0.76 A. But, because of output circuit losses and the fact that the amplifier power output specification is at the 1-dB compression point and not at full saturation, considerably more RF current capacity in the output FET will be required. A current increase of approximately 50% should yield ample margin. With this in mind, an output FET size of 3000 μm was selected. The power output, neglecting circuit losses, with such a device should be approximately 32 dBm when fully saturated; thus, a 30-dBm power specification at the 1-dB compression point should be viable provided the FET is correctly terminated. As a comparison, with the design of handset power amplifiers, where the operating supply voltage is 3.2 V, the output device periphery can easily exceed 20,000 μm.

The next step in the design is the output network synthesis. Based on the RF load line and nonlinear analysis, the optimum load impedance (Z_{opt}) for the FET was determined as a function of frequency, and the output network was then designed using bandpass synthesis techniques. The lumped-element network model was then converted to a distributed-element form. The load impedance presented to the FET after circuit optimization is shown in Figure 9.39 and the lumped-element and distributed networks are shown in Figure 9.40.
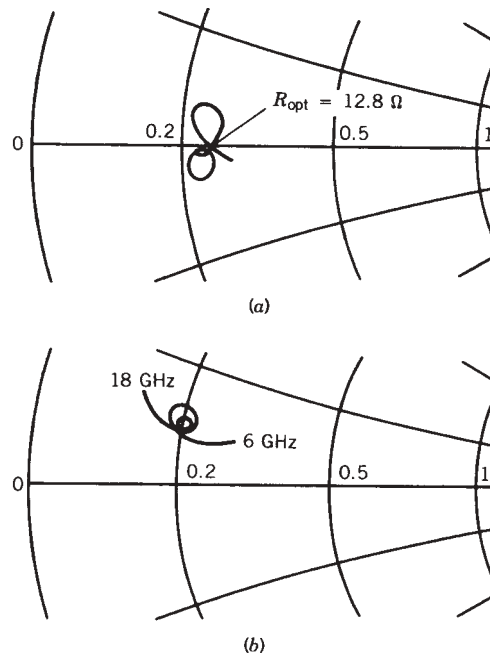
FIGURE 9.39 Optimum load impedance (actual and target) presented to output FET: (a) C_{ds} absorbed into output network ($\sim R_{\text{opt}}$); (b) actual load presented to FET (Z_{opt}).

(a)

(b)
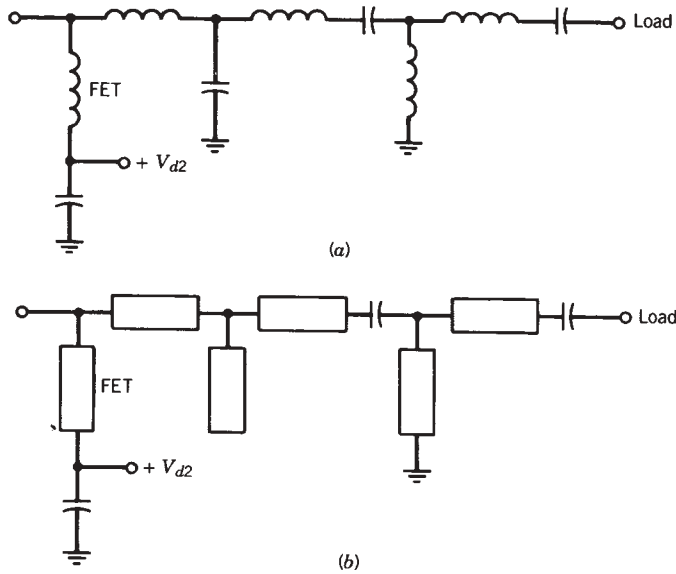
FIGURE 9.40   (*a*) Lumped-element and (*b*) distributed-element output network equivalent circuits.

The interstage design can then begin by synthesizing a matching network (complex source to complex load) using the S_{11} of the output FET and terminated output network as the load impedance and Z_{opt}^* of the driver FET as the source impedance [9.17, 9.19]. The resulting network provides maximum power transfer between driver and output stage with no gain shaping. Gain shaping can now be provided by adding lossy elements to the interstage network and adjusting the reactive elements so that the driver is still terminated for maximum power output performance. Final optimization can then occur after converting the network to distributed form and performing amplifier analysis at or near the saturated output power condition with proper dc bias. The lumped-element and distributed final interstage network models are shown in Figure 9.41.

The final step in the design process is to synthesize the input network. This can be accomplished by employing bandpass filter synthesis methods and then adding loss, thus improving stability and input VSWR. The final distributed-element amplifier model is shown in Figure 9.42 and the photograph of the completed MMIC is shown if Figure 9.43. As can be seen in the photograph, the networks were designed as symmetrical parallel pairs due to the extreme FET widths (in terms of wavelength) and low impedances. The measured gain and power output performance is shown in Figure 9.44. The sharp rolloff in power and gain beyond the band edges is due, as expected, to the high-order networks that were employed in the design. These high-order networks are also the reason why the in-band gain and power output performance is flat.

The design approach for two-stage amplifiers can be extended for multistage designs. A good example is the three-stage power LDMOS amplifier shown in Figure 9.45*a*. The MMIC amplifier consists of two 2.8-mm periphery input stage devices driving four 8.4-mm periphery driver FETs. The driver stage in turn is followed by four 19.8-mm output stages. The input of the amplifier is matched to a 50-Ω system with all active
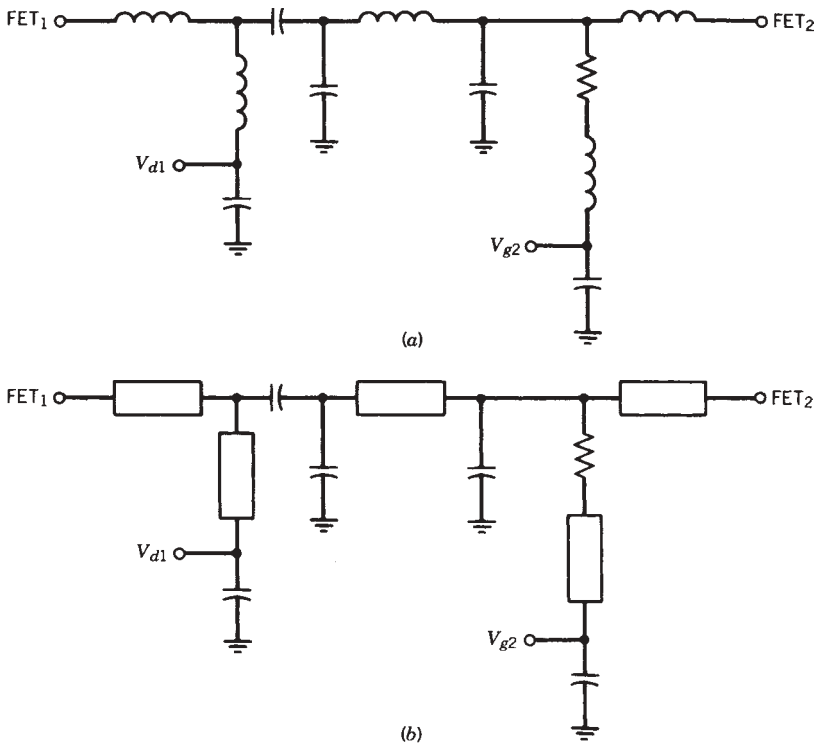
FIGURE 9.41   (*a*) Lumped-element and (*b*) distributed-element interstage network equivalent networks.

device combining being accomplished with reactive networks. To keep losses at a minimum and facilitate final circuit embedding, the output of the 40-W amplifier (1.8 and 2.2 GHz) is prematched to the 5- to 6-Ω level. The multimode 30-dB-gain amplifier (GSM/GSM EDGE/CDMA/TDMA/WCDMA) features a typical 0.2 dB gain flatness per band of interest and a quiescent current thermal tracking system and operates with a supply voltage of 26 to 28 V. Another interesting multistage amplifier is the MMIC amplifier shown in Figure 9.45*b*. This two-stage PHEMT amplifier was designed to operate between 57 and 65 GHz with a power output of 27 dBm.

The above design approach, although more empirical than small-signal design methods, does provide excellent results. However, it also requires some design experience and insight into network synthesis and topology limitations. Other nonlinear amplifier characteristics, such as third-order distortion, are best determined via nonlinear simulation. Common "rules of thumb" used to determine various distortion characteristics can easily give the design engineer erroneous results for broadband designs, especially when multiple stages are involved. As an example, the rule which states that the third-order intercept point is 10 dB greater than the amplifier's 1-dB compression point, could yield a $\pm$10-dB error for a single-stage single-gate power amplifier. The error could be 20 or 30 dB for a dual-gate variable-gain design when the amplifier is biased for reduced-gain operation. It should also be noted that the harmonic termination also influence amplifier distortion products, a problem that is common in multistage designs with nonresistive stage coupling.
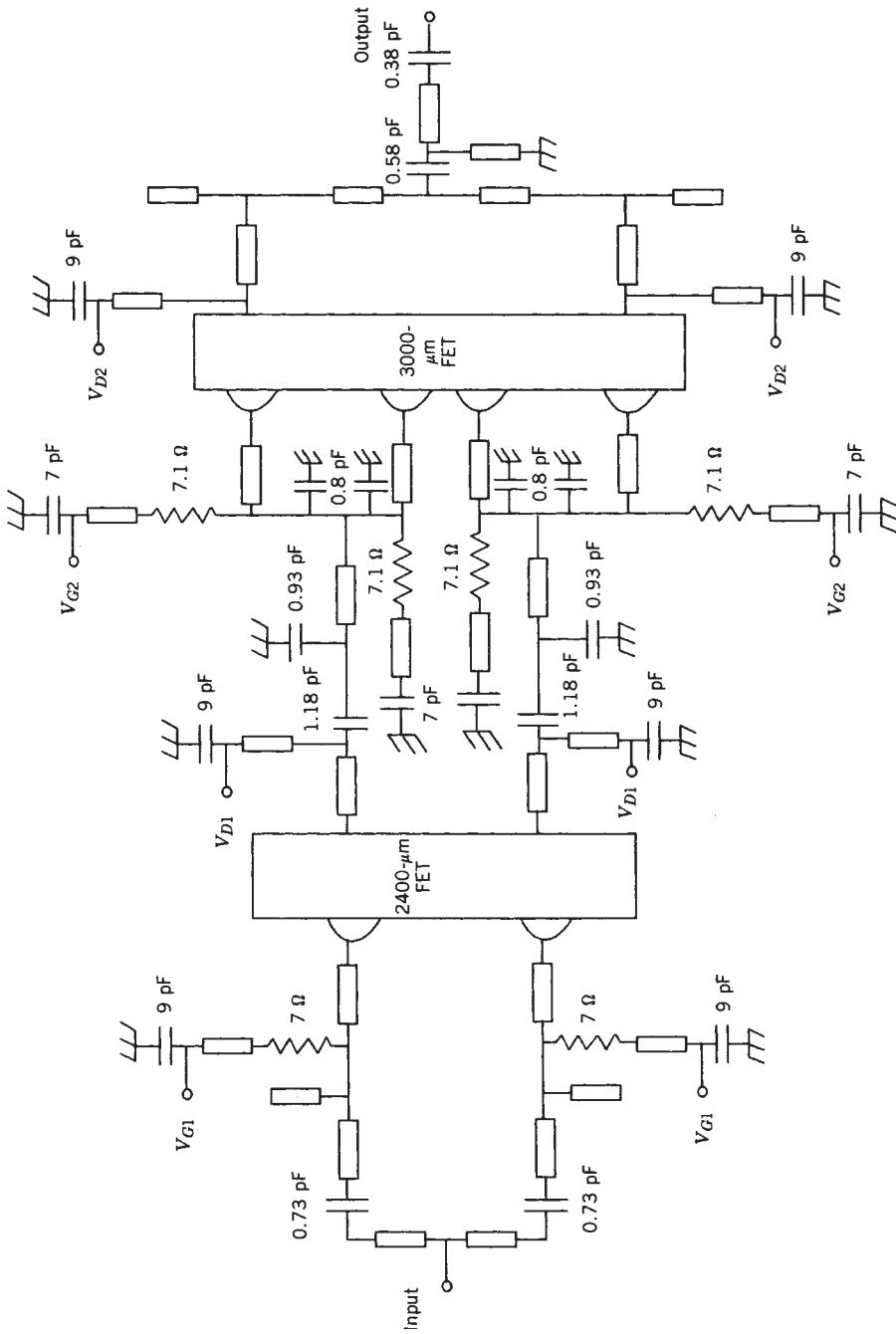
FIGURE 9.42 Final distributed-element amplifier circuit model.

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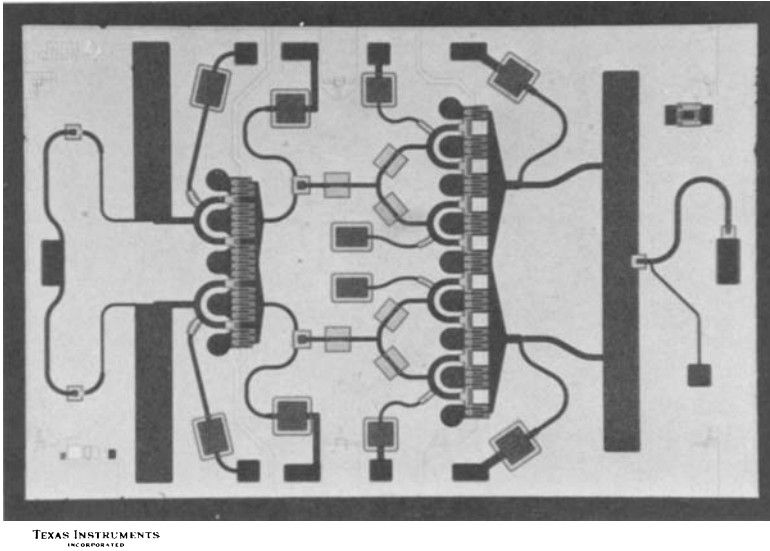
FIGURE 9.43 Monolithic two-stage 6- to 18-GHz amplifier.
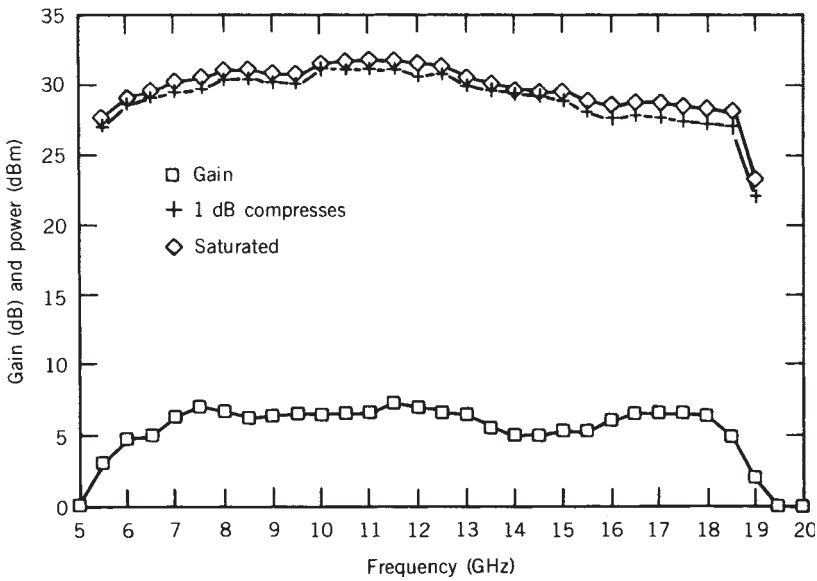
FIGURE 9.44 Measured gain and power output performance of monolithic two-stage amplifier.

9.6 POWER-DISTRIBUTED AMPLIFIERS

Since the 1940s, distributed techniques have been used to design very broadband electron tube amplifiers [9.26, 9.27]. The amplifiers then reappeared during the 1980s in solid-state form, typically employing GaAs FETs; the equivalent circuit of a FET
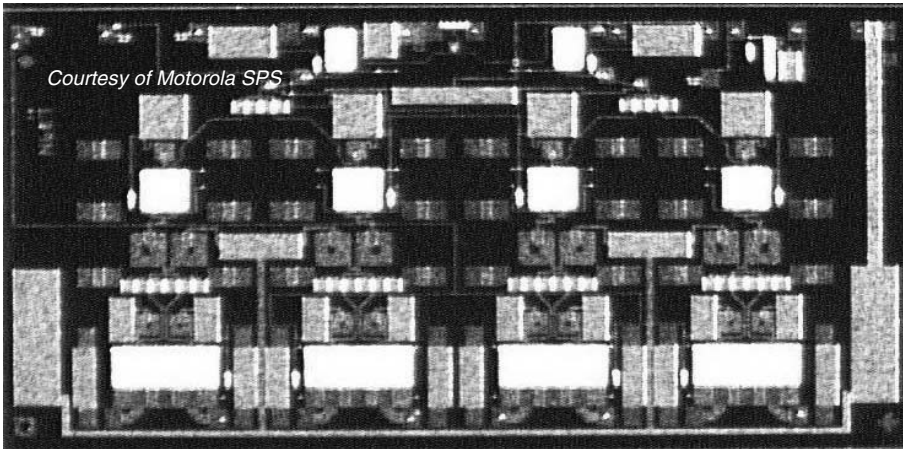
(*a*)
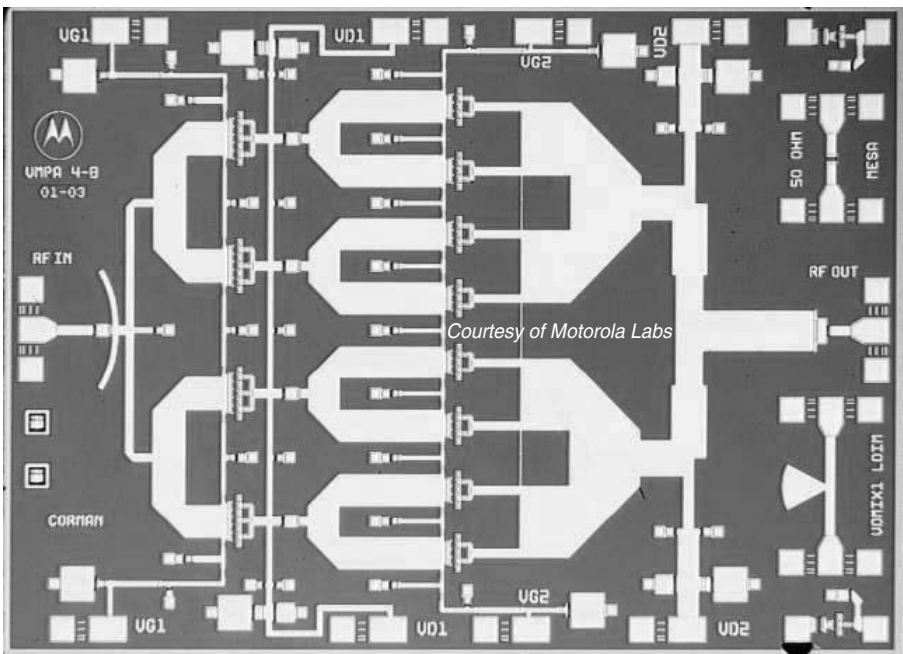
(*b*)

FIGURE 9.45   Multistage amplifier examples: (*a*) three-stage LDMOS MMIC 40-W amplifier; (*b*) 60-GHz 1/2-W amplifier.

is similar in nature to a vacuum tube [9.28–9.31]. Distributed amplifiers and mixers have now been used extensively in a variety of broadband system applications such as microwave electronic (ME) receivers, wide-band transmitter exciters, and low-noise oscilloscope preamplifiers. The rebirth of these techniques is due in part to the fact that exceptional bandwidth performance is obtainable because the input and output capacitances of the active devices are absorbed into the distributed structures. The

amplifiers also exhibit very low sensitivities to process variations and particularly in the small-signal case are very easy to design and simulate. In addition, a great deal of design flexibility is possible since the number of devices, device type (FET or HBT), device periphery, and transmission line characteristic impedance as well as the upper frequency cutoff of the amplifier can be varied. Hence, a wide range of application requirements can be addressed with this topology. The simplified amplifier structure is shown in Figure 9.46. However, these amplifiers have never demonstrated high-efficiency and high-power-output performance. Distributed amplifier theory does not inherently limit power and efficiency performance obtainable, but proper control of device size, internal impedance, and load impedance must be maintained [9.37, 9.57, 9.58, 9.62]. This new synthesis method still relies on the use of artificial transmission line structures to form the amplifier's input and output networks, which absorb the parasitic capacitances of each active device in the chain, but the new load targets vastly improve performance.

As can be seen, the small-signal amplifier is composed of two main artificial transmission line sections consisting of series inductances and capacitances which are usually supplied by the FET parasitics. If the FET model of Figure 9.47 is substituted into the above amplifier topology, two constant-k transmission lines which have different cutoff frequencies and attenuation characteristics result (Fig. 9.48). Since these lines are heavily loaded by the FET parasitic resistances R_i and R_{ds}, the number of active device sections cannot be added indefinitely because the attenuation along the transmission lines will eventually exceed the gain obtained by adding an additional active device. The phase shift from section to section for both the drain and gate transmission lines must also be made approximately equal so that the amplified signal currents from each active device add in phase along the output (drain) transmission line. Signals or waves which travel in the reverse direction on the output transmission line will be absorbed by the termination resistor, thus lowering the power output and gain performance of the resulting amplifier. However, without the termination resistor, stability and gain flatness problems usually result.
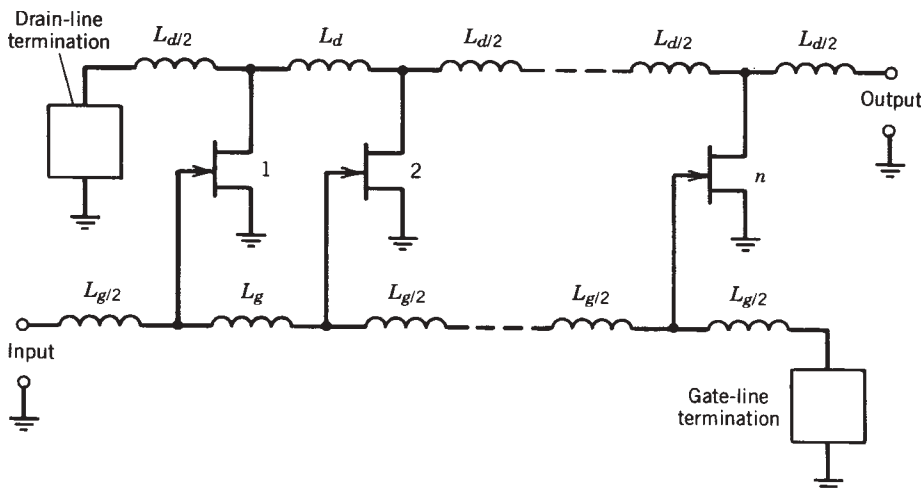
FIGURE 9.46   Schematic representation of a FET distributed amplifier. (From Ref. 9.33 © IEEE 1984.)
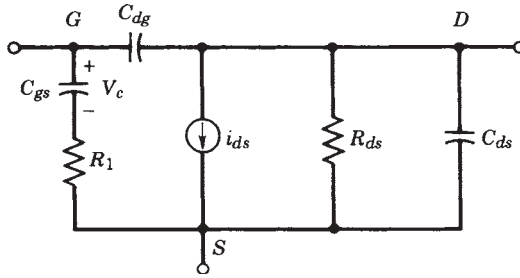
FIGURE 9.47   Simplified FET model.

One of the assumptions in the design of distributed amplifiers is that the artificial transmission lines of the gate and drain networks be terminated with a load equivalent to their characteristic impedance. This is somewhat difficult, in that the characteristic impedance of a constant-k transmission line network is a function of frequency and approaches infinity at cutoff. Hence, there is no physical combination of elements that can provide a proper termination at all frequencies, but there is a class of circuits known as constant-k m-derived networks which can be used in conjunction with the termination resistor to properly terminate the transmission lines. These terminations perform well through 80% of the usable bandwidth $(0.8 f_c)$. However, ideal operation of these networks can only occur when lumped elements are used to realize the amplifier circuit. Unfortunately, this is almost never the case, but very good approximations can be made using monolithic integrated circuits. A typical lumped-element distributed amplifier circuit which illustrates the use of optimized source and load terminations is shown in Fig. 9.48c.

With these general concepts in mind, a more in-depth analysis can be formulated. If we define the gate circuit radian cutoff frequency as $\omega_g = 1/R_i C_{gs}$ and the drain circuit radian cutoff frequency as $\omega_d = 1/R_{ds} C_{ds}$, then the propagation characteristics of the constant-k transmission line sections are known. By requiring the phase shift between each gate line section and drain line section to be equal, to assure proper amplifier performance, the cutoff radian frequency ω_c for both transmission lines must also be equal. With these constraints the gain of the amplifier can be defined as [9.32, 9.33]

$$G = \frac{g_m^2 R_{01} R_{02} \sinh^2 qn/2(A_d - A_g)r \; e^{-n(A_d+A_g)}}{4q_1 + (\omega/\omega_c)^2 r q_1 - (\omega/\omega_c)^2 r \sinh^2 q(A_d - A_g)/2r} \tag{9.42}$$

where $R_{01}[= (L_g/C_g)^{1/2}]$ and $R_{02}[= (L_d/C_d)^{1/2}]$ are the characteristic resistances of the gate and drain lines, respectively.

The magnitude of the amplifier's voltage gain for a single stage can be obtained from the power gain equation of (9.42) provided the assumption is made that ideal impedance transformers are placed between cascade connected amplifier stages, which transform the drain line impedance R_{02} to the succeeding gate line impedance R_{01}. Thus, the resulting voltage gain expression is

$$A = \frac{g_m (R_{01} R_{02})^{1/2} \sinh q_n/2(A_d - A_g)r \; e^{-n(A_d+A_g)/2}}{2q_1 + (\omega/\omega_c)^2 r^{1/2} q_1 - (\omega/\omega_c)^2 r^{1/2} \sinh^2 q(A_d - A_g)/2r} \tag{9.43}$$
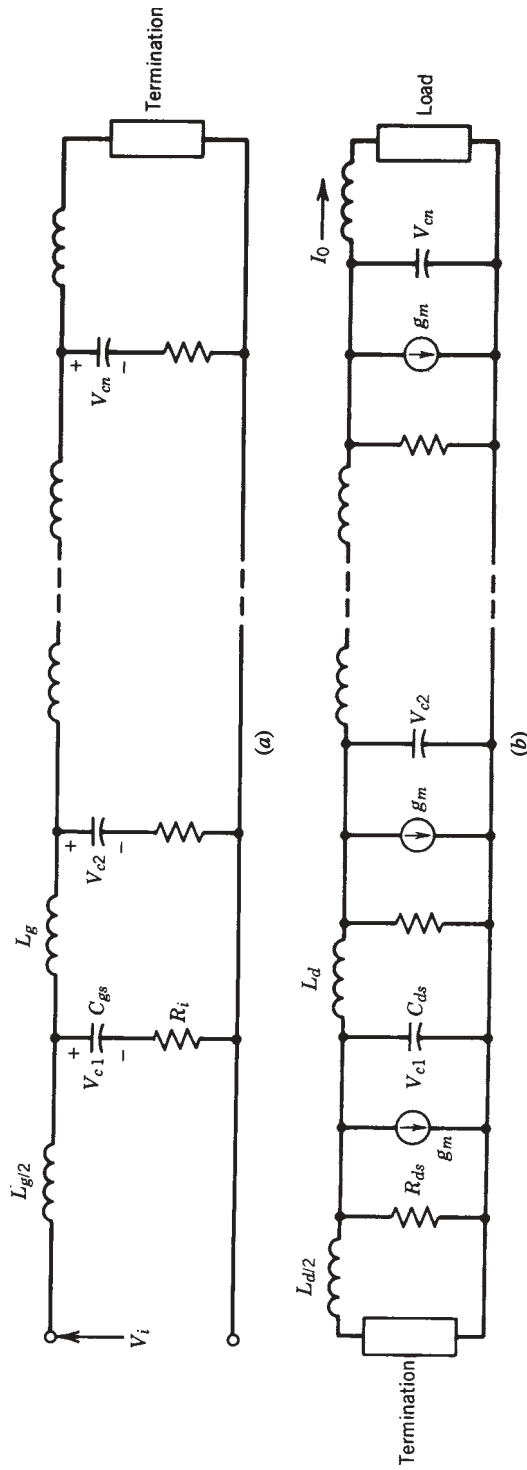
FIGURE 9.48 Constant-k lumped-element transmission lines: (a) input circuit or gate line; (b) output circuit or drain line; (c) simple lumped-element n-section amplifier showing m-derived terminations. (From Ref. 9.33 © IEEE 1984.)
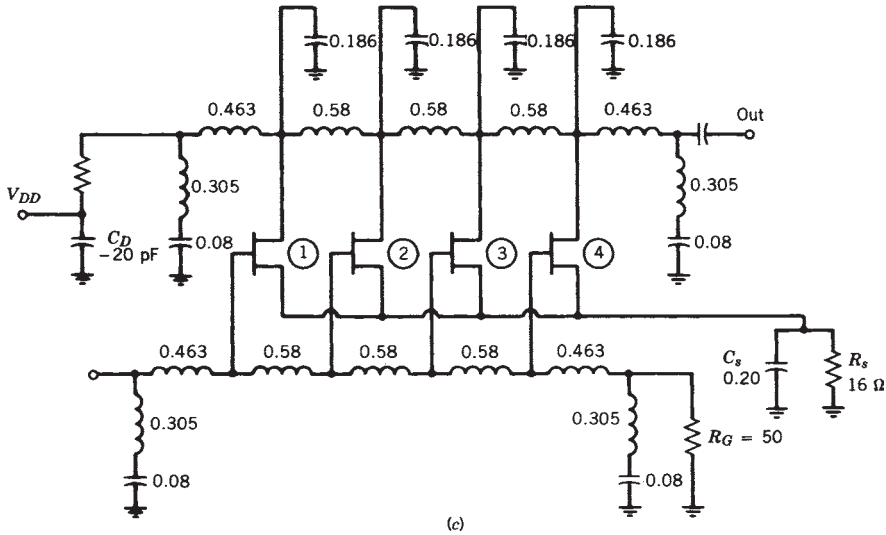
FIGURE 9.48   (*continued*)

By maximizing expression (9.43) for gain at a given frequency, the optimum number of devices N_{opt} can be shown to be

$$N_{\text{opt}} = \frac{\log_e(A_d/A_g)}{A_d - A_g} \tag{9.44}$$

It must be remembered that although N_{opt} can be large (>10), if gate and drain circuit losses are low, in practice very little gain improvement is obtained for $n > 10$. With all but the best state-of-the-art devices, typically little improvement is obtained beyond 6. The choice of n is further constricted in the design of power-distributed amplifiers, since the total gate periphery, device drive level, and saturation characteristics must be considered. The most critical factor in determining amplifier frequency response is transmission line attenuation, with the gate line typically being the dominant contributor. The expressions for attenuation and phase velocity are well known for constant-k transmission lines, and for the low-loss case, the attenuation factors for the gate and drain lines can be approximated as

$$A_g = \frac{(\omega_c/\omega_g)^{1/2} X_k^2}{q_1 - q_1 - (\omega_c/\omega_g)^2 r X_k^2 r^{1/2}} \tag{9.45}$$

$$A_d = \frac{(\omega_d/\omega_c)}{q_1 - X_k^2 r^{1/2}} \tag{9.46}$$

where $X_k = \omega/\omega_c$ is the normalized frequency, $\omega_g = 1/R_i C_{gs}$, $\omega_d = 1/R_{ds} C_{ds}$, and

$$\omega_c = \frac{2}{(L_g C_{gs})^{1/2}} = \frac{2}{(L_d C_{ds})^{1/2}} \tag{9.47}$$

The attenuation characteristics of these lines as a function of frequency with ω_d/ω_c and ω_c/ω_g as parameters are shown in Figure 9.49. It is evident from Figure 9.49a that the frequency response is primarily determined by the gate line while it is interesting to note that the attenuation on the drain line does not vanish at dc. Thus, the low-frequency gain of the amplifier is primarily determined by the g_m of the FET but is also a function of R_{ds}; hence, dual-gate FETs should exhibit superior gain performance because their equivalent g_m is greater and R_{ds} is larger than a similar-sized single-gate FET.

The design challenge now becomes the minimization of the quantities ω_d/ω_c and ω_c/ω_g. For a given cutoff frequency ω_c, active devices with the smallest R_iC_{gs} (similarly $R_{ds}C_{ds}$) product need to be selected or a capacitor can be added in series with each FET's gate terminal [9.34]. However, a series capacitor acts as a voltage divider on the input of the FET, lowering the effective RF drive voltage, which in turn lowers the amplifier's gain. This is not always a poor performance trade, since it may allow the use of larger FETs for a given frequency response, resulting in an amplifier with greater power output. Similarly, the drain line losses can be lowered by padding C_{ds} with an
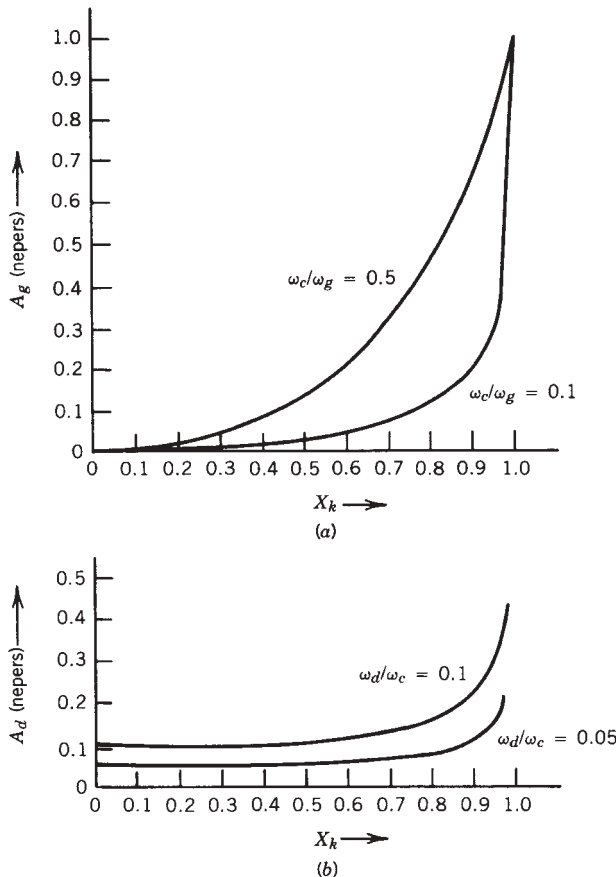
FIGURE 9.49 (a) Attenuation on gate line versus normalized frequency. (b) Attenuation on drain line versus normalized frequency. (c) Comparison between constant-k and constant-R filter sections. (From Ref. 9.33 © IEEE 1984.)

Constant K Constant R

Conditions

$$L = CR_L^2$$

$$L = \frac{3\, CR_L^2}{4} \qquad M = \frac{CR_L^2}{8}$$

$$C_B = C/8$$

Transfer Function

$$\frac{v_c}{i_{in}} = \frac{2R_L + R_L^2 C_s}{2 + 2R_L C_S + R_L^2 C^2 S^2}$$

$$\frac{v_c}{i_{in}} = \frac{8R_L}{8 + 4R_L C_S + R_L^2 C^2 S^2}$$

Cutoff Frequency

$$f_c = \frac{1}{\pi\sqrt{LC}} = \frac{1}{\pi R_L C}$$

$$f_c = \frac{\sqrt{2}}{\pi R_L C}$$

(c)
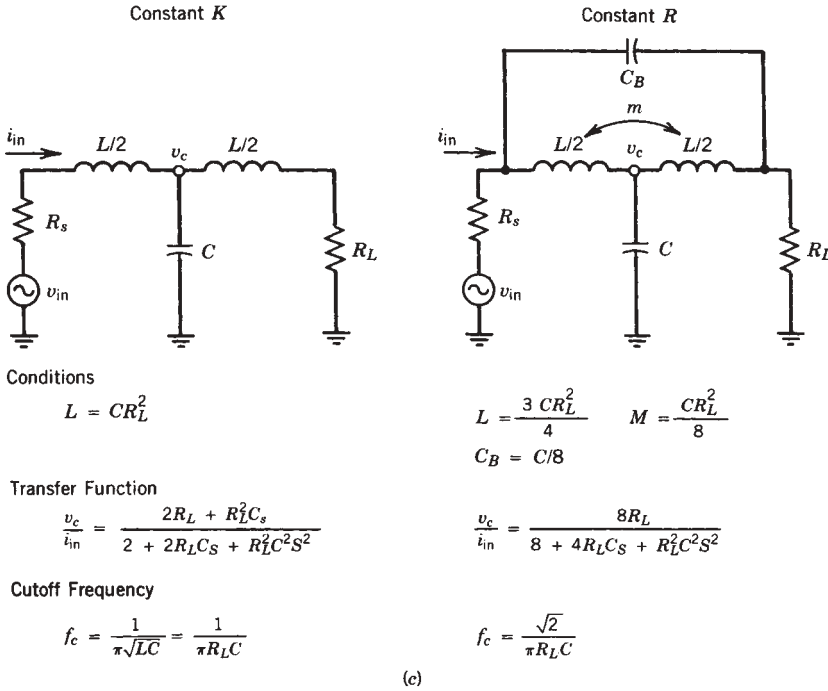
FIGURE 9.49   (*continued*)

external capacitor, but this will lower the drain line cutoff frequency. In practice, the only padding typically added to a microwave amplifier is a small series transmission line employed between the FET cells and the high-impedance transmission lines used to simulate the drain line inductances. This is used to help equalize the phase shift from section to section between the gate and drain circuits. When the operating frequency is low or the terminal impedance is substantially lower than 50 Ω, shunt capacitors at the drain (or collector) will be required.

A slightly different network, called the constant-R network [9.35, 9.36], can also be used to synthesize the amplifier's artificial transmission lines. This network, shown in Figure 9.49c, if correctly synthesized, exhibits a cutoff frequency $\sqrt{2}$ times greater than a conventional constant-k network for the same value of shunt capacitance. However, in practice, this performance improvement is rarely achieved due to the distributed nature of the network and the inability to achieve the proper coupling between input and output inductors. Bandwidth improvements for these structures are typically on the order of 20%.

The attenuation constants A_g and A_d can also be expressed in terms of fractional bandwidth, number of devices, and circuit parameters. Equations (9.45) and (9.46) can then be written as

$$A_g = \frac{2aX_k^2}{nq_1 + q(4a^2/n^2)rX_k^2 r^{1/2}} \tag{9.48a}$$

$$A_d = \frac{2b}{nq_1 - X_k^2 r^{1/2}} \tag{9.48b}$$

where

$$a = \frac{n\omega_c}{2\omega_g} \qquad b = \frac{n\omega_d}{2\omega_c} \tag{9.49}$$

By using (9.48b) and (9.49), an expression for normalized gain as a function of frequency can be derived from the voltage gain expression of (9.43). The expression

$$A_n = \frac{\sinh(b/n)e^b \sinh q(n/2)(A_d - A_g)re^{-q(n/2)(A_d+A_g)r}}{\sinh(b)q_1 + (4a^2/n^2)\ X_k^2 r^{1/2}q_1 - X_k^2 r^{1/2} \sinh q(A_d - A_g)/2r} \tag{9.50}$$

where the gain (A_0) of the amplifier at the low-frequency limit is given by

$$A_0 = \frac{g_m(R_{01}R_{02})^{1/2}\sinh(b)e^{-b}}{2\sinh(b/n)} \tag{9.51}$$

can be used to determine the 1 dB fractional bandwidth of any amplifier topology as a function of parameters a, b, and n. In Figure 9.50, several frequency response characteristics for an amplifier with four devices are shown for various values of a and b. By properly choosing a and b, the amplifier can be designed with a nearly flat frequency response throughout its operating bandwidth with an upper frequency limit close to the cutoff frequency of the transmission lines. Representative values for a and b which give the same fractional bandwidth are shown in Figure 9.51. These values can be found by iteratively solving expression (9.50).

We have now developed an analytical approach to design distributed small-signal amplifiers given the desired bandwidth, low-frequency gain, FET characteristics, and number of stages, but there are other factors that must be considered before a power-distributed amplifier can be designed. Also, the previous analysis assumes that ideal
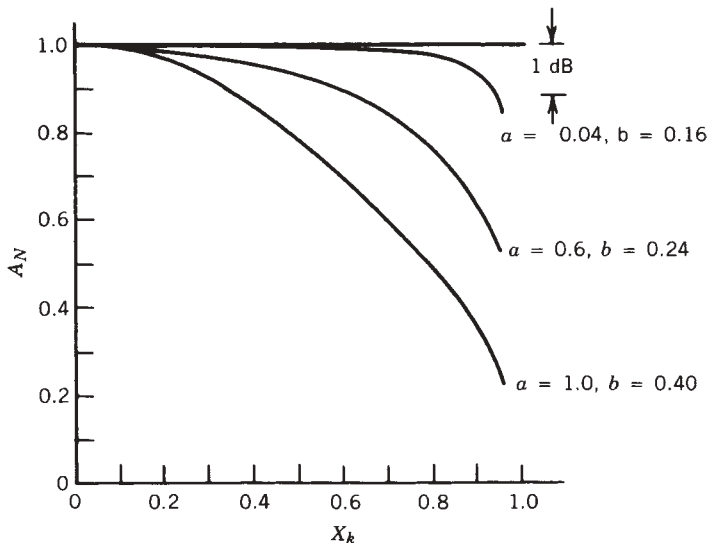
FIGURE 9.50 Normalized frequency response on $n = 4$ FET distributed amplifier for various values of a and b. (From Ref. 9.33 © IEEE 1984.)
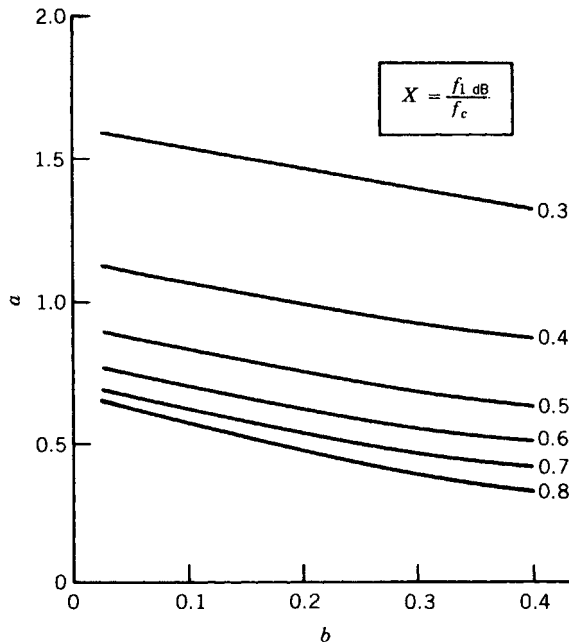
FIGURE 9.51 Representative values of *a* and *b* that yield the same fractional bandwidth. (From Ref. 9.33 © IEEE 1984.)

inductances and image terminations are employed in the design. However, in practice high-impedance lines are employed to simulate inductances and image terminations are rarely used because of stability and gain-peaking requirements. Regardless of the limitations with the previous analysis, it still yields the most straightforward approach to design a microwave power amplifier.

The power limitation problems of distributed amplifiers are similar to the problems encountered in the design of conventional topologies such as cascaded reactively matched gain stages, except distributed configurations are far less sensitive to device and circuit process variations. This process tolerance allows for a more efficient sizing of devices and sometimes leads, especially in broadband designs, to higher operating efficiency. As with any distributed amplifier, multiple devices add power (more output current) to the output network and some additional gain to the amplifier. In a conventional design, all of the distributed devices are imbedded within the same impedance conditions, and power limiting occurs on the final device where the power accumulates at the output load. What this means is that all of the distortion or power-limiting parameters are focused at only one of the devices in a conventional distributed-amplifier implementation. Distributing the power limiting across all of the devices while maintaining the benefit of broadband performance and conventional single-ended dc-to-RF power conversion efficiency would be the ideal goal for this new implementation of power amplifiers.

As with conventional approaches, the most basic dynamic range limitation mechanism is the maximum RF voltage swing that can be applied to the FET gate (Fig. 9.52). In a distributed amplifier, this usually translates to the largest signal that can be present on the gate line. Thus, the signal is limited in the positive direction by the forward
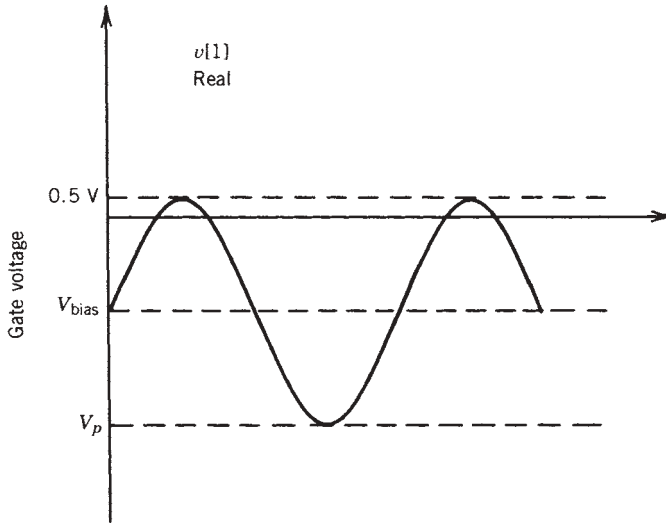
FIGURE 9.52   Maximum gate line RF voltage swing.

gate conduction voltage and in the negative direction by the magnitude of the FET's pinchoff voltage (V_p). If one assumes a typical high-voltage power FET pinchoff voltage of 5 V dc and 50 Ω gate line impedance, then the maximum input power to the amplifier is approximately 75 mW. Thus, the output power cannot exceed $P_{input} \times$ gain. The effective input power capabilities of the amplifier can be increased with the use of series gate capacitors, which unfortunately lowers the gain. There is probably no net benefit in using gate capacitors just for this purpose. If low pinchoff devices are used, the amplifier needs to be designed for sufficient gain so that the gate circuit does not clip.

The second power-limiting mechanism in distributed amplifiers which is not a hard limit in conventional designs is total gate periphery. For a given upper frequency of operation and a fixed constant transmission line impedance, there will exist a maximum total gate periphery. The periphery limit is easily understood if one considers that f_c is inversely related to C_{gs}, which forms a low-pass structure with L_g, and N_{opt} is proportional to the gate line attenuation, which also reduces the fractional bandwidth. This limitation, concerning maximum usable device size (gate periphery), can also be increased by adding a series gate capacitor. For practical power amplifier designs, this technique is a viable compromise because the loss in voltage drive level at the gate is almost exactly offset by the increase in device g_m. As an example, the maximum gate periphery for a typical 0.5-μm FET amplifier designed for 18-GHz operation is approximately 1500 μm, but if series capacitors are employed on the gates, the total gate periphery can be increased beyond 3000 μm. Hence, the power output capability can be raised but not necessarily doubled. The reason for this phenomenon will shortly become apparent.

Aside from the RF current limitation, which is proportional to gate periphery, the maximum RF voltage sustainable at the load is the other prime power-limiting mechanism. Typically, the limiting FET parameter is the drain-to-gate breakdown voltage. Unfortunately, addition elements cannot be employed to improve performance. In a

traveling-wave structure, the last FET (nearest the load) will have the largest applied RF voltage present across the drain–source terminals, provided there are no large standing waves on the drain line. The maximum approximate peak-to-peak voltage is defined as

$$V_{\max} = V_{\text{breakdown}} + V_{\text{pinchoff}} - V_{\text{knee}} \tag{9.52}$$

Using Eq. (9.52), a first-order approximation can be found for power output at a specified load impedance. Thus, in a 50-Ω system, a 1-W output power specification implies reverse breakdown voltages of 25 V, a parameter not readily obtained. These approximations are somewhat conservative because RF breakdown voltages are usually greater than dc values. It should also be noted that reducing the output load impedance may not be a viable option since the amplifier's gain will also be reduced.

A more subtle power-limiting phenomenon is the optimum load impedance seen by an individual FET in the structure. If the embedding transmission lines were ideal and there were no mismatched terminations, each FET would be terminated with an impedance equal to $Z_0/2$ (dc). This impedance can be quite far from the optimum load termination. To approximate the true optimum load for any FET, the ac load line can be drawn between $V_{\max}$ and $I_{\max}$ on the FET drain characteristic curves (Fig. 9.53). Unfortunately, the design engineer has very little control over the optimum terminating impedance in a conventional distributed amplifier since the load line is usually predetermined by other circuit parameters.

Due to the constraints mentioned above, maximum power output will be obtained from designs employing the largest possible FET cells. Nonoptimum loads also influence amplifier power-added efficiency in a detrimental manner. However, it is possible to improve the efficiency and power output of a distributed amplifier by tapering the drain line impedance from section to section, a process called tapering. Without tapering or employing frequency-dependent terminations, a large fraction of the developed power propagates toward the termination end of the drain line. The intent of impedance tapering is to force the backward-traveling current to zero at the termination, thus forcing all the developed current from each FET to travel in the forward
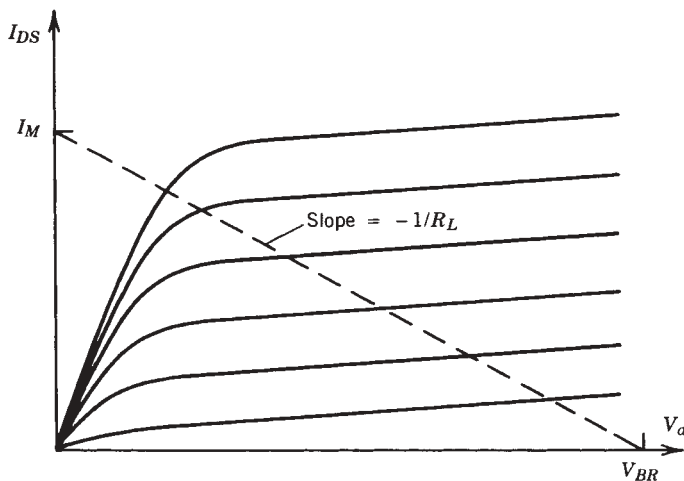
FIGURE 9.53 Optimum ac load impedance for class A operation.

direction only. It is also used to provide each FET with an optimal load impedance termination.

By operating the first FET into a section of line with impedance Z_0, all the current will flow into the next section. Then, if the next section has characteristic impedance of $Z_0/2$, one-third of the developed current from the second FET will cancel the reflected current from the first FET at the junction of the second FET. The remaining two-thirds of the current developed by the second FET and four-thirds of the current developed by the first FET now add and propagate toward the junction of the third FET, as shown in Figure 9.54. The transmission line impedance after the third FET must now be equal to $Z_0/3$. This process continues where each successive transmission line section has the impedance of Z_0/k, where k is the number of the stage of interest.

For the above example, each of the FETs (current sources) can be placed in a network, which presents an optimum load impedance of R_L (ohms). Thus, the output network of Figure 9.48b, neglecting the termination and adjusting for a four-cell amplifier, then becomes the circuit shown in Figure 9.55. Here, the objective is to operate
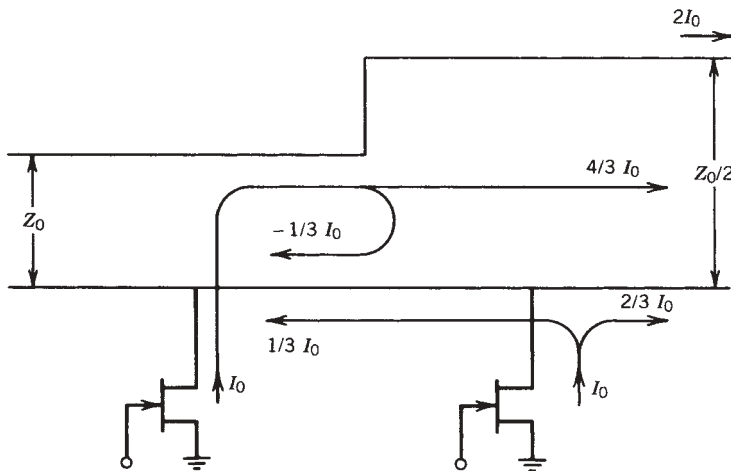
FIGURE 9.54   Current distribution in a correctly tapered drain circuit.
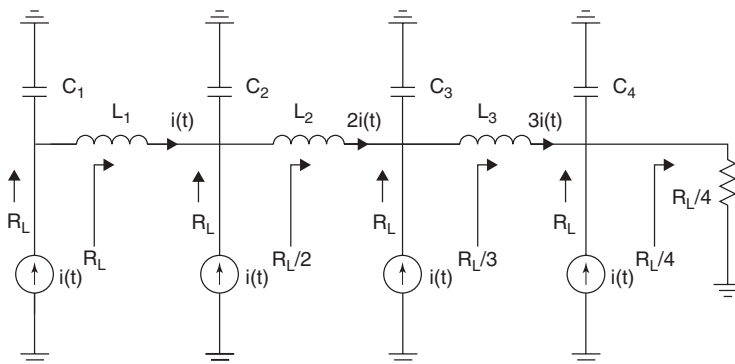
FIGURE 9.55   Current combining for a four-cell distributed amplifier.

each of the devices with identical conditions, including the load impedance (shown as R_L in Fig. 9.55); hence, this implies that the last section of transmission line must be designed with a characteristic impedance of $R_L/3$. Similarly, the adjacent node to the left has a virtual impedance of R_L with a branch impedance of $R_L/2$. By tapering the drain or output line characteristic impedance in this manner, the optimum load required to obtain power output, efficiency, or a combination of the two impedances can be synthesized. As before, this implies a load impedance of R_L/k, where $k = 4$.

Several assumptions were made in the above analysis which should not be forgotten. First, it was assumed that each device delivers equal current. Due to unequal drive voltages on the gate line and FET process variations, current equalization is in practice difficult to achieve. The gate and drain lines are also dispersive, which makes the tapering accurate only at a single frequency. The second area of concern is it is difficult to realize the L/C transmission line sections, with the impedances values, required for proper tapering. There are also other practical considerations. Proper tapering requires that the load impedance presented to the amplifier be R_L/k. Very low impedance loads are sometimes difficult to synthesize and then transform to a nominal system value of 50 Ω. However, tapering may help keep the load impedance presented to the last several FETs low, minimizing the power loss due to low breakdown voltage. Also, microstripline width tapering eases the fusing current problems encountered in biasing distributed-power amplifiers.

Now that the concepts and synthesis techniques have been developed, the design of a single- or dual-gate FET power amplifier can be illustrated. The design example chosen, which has been based on monolithic implementation, was specifically selected to highlight the problems of obtaining broadband frequency response and high power output. The performance goals for this design are summarized in Table 9.7.

The design engineer must begin by first selecting the general device type to be used. Typically, single-gate FET designs exhibit less gain than their dual-gate counterparts but suffer from lower power-added efficiency. Dual-gate designs, although difficult to stabilize, offer excellent gain performance and output voltage dynamic range improvements over a single-gate approach. They also have much higher values of R_{ds} for a given gate periphery, thus reducing drain line loss problems, particularly at higher microwave frequencies. Hence, a dual-gate design approach was selected.

Conventional power amplifiers designed for broadband performance usually require approximately 3 mm of gate periphery in the output stage to achieve 1-W performance. A similar amount of total gate periphery must then be employed in a distributed approach to achieve comparable performance. Since the number of stages in a typical amplifier must be at least 4 to achieve reasonable gain and for complexity reasons

TABLE 9.7   Performance Goals for Power Dual-Gate FET Distributed-Amplifier Design Example

Power output	1 W
Frequency response	2–18 GHz
Small-signal gain	8 dB
Input/output VSWR	<2 : 1
Amplitude flatness	$< \pm 0.5$ dB

should not exceed 10, it becomes evident that the device size must be between 300 and 750 μm.

Considering these constraints, a 450-μm intermediate doping profile dual-gate FET was selected. A simplified single-gate equivalent model for this device is shown in Figure 9.56. Using the FET element values given in Figure 9.55, basic amplifier design parameters can be calculated.

If we assume 50 Ω input and output amplifier impedances, the gate and drain line inductances can be calculated from the expression

$$Z_0 = \left(\frac{L_g}{C_g}\right)^{1/2} = \left(\frac{L_d}{C_d}\right)^{1/2} \tag{9.53}$$

The gate and drain line attenuation constants A_g and A_d can be found by solving Eqs. (9.45) and (9.46) using the expressions for the three cutoff frequencies ω_c, ω_g, and ω_d. By choosing an upper operating frequency limit such that $\omega < \omega_c$, the optimum number of stages (N_{opt}) can be determined from Eq. (9.44). Finally the dc gain and 1 dB corner frequency for any value of n can be calculated from Eqs. (9.50) and (9.51). The design parameters are shown in Table 9.8.

At first glance, it appears that the selected design approach cannot achieve the required bandwidth performance. However, the cutoff frequency of the gate line can be increased by adding capacitors in series with each FET gate. The addition of a series capacitor approximately equal to the original value of C_{gs} (0.42 pF) will lower the gain by ∼6 dB but will dramatically extend the amplifier's frequency response. The key amplifier parameters now become those given in Table 9.9.

Before proceeding, the lumped-element circuit model must be replaced with a transmission line equivalent. This is easily accomplished by substituting high-impedance, microstrip transmission lines with reactances equal to the reactance of L_g and L_d at the uppermost frequency of operation for the lumped inductors. Transmission line models for capacitors, junctions, and terminations should also be added at this time.

R_g = 1.5 Ω
R_s = 0.8 Ω
R_d = 1.0 Ω
R_i = 4.3 Ω
R_{ds} = 633 Ω
C_{gs} = 0.54 pF
C_{ds} = 0.18 pF
C_{dg} = 0.012 pF
g_m = 48 mS
L_s = 0.01 nH
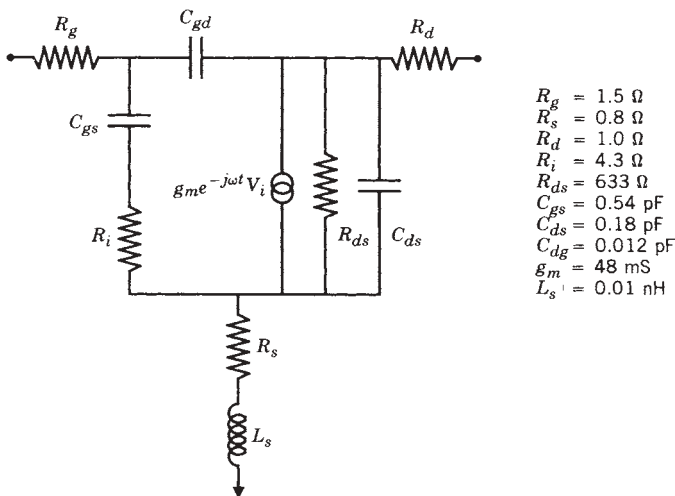
FIGURE 9.56 Simplified single-gate equivalent model of dual-gate FET.

**TABLE 9.8   Basic Amplifier Design Parameters
Obtained with FET Model of Figure 9.55
($C_{gs} = 0.54$ pF)**

$F_c = 11.78$ GHz
$N_{\text{opt}} = 7$
$L_g = 1.35$ nH
$L_d = 0.45$ nH

By Selecting n = 6 and f = 10 GHz

$A_0 = 16.0$ dB
$F_{1 \text{ db}} = 9.31$ GHz

**TABLE 9.9   Basic Amplifier Design Parameters
Obtained by Adding a Series Gate Capacitor to
Extend Useful Operating Bandwidth
($Cgs' = 0.24$ pF)**

$F_c = 26.58$ GHz
$N_{\text{opt}} = 8$
$L_g = 0.45$ nH
$L_d = 0.60$ nH

By Selecting n = 7 and f = 20 GHz

$A_0 = 10.3$ dB
$F_{1 \text{ db}} = 14.51$ GHz

Unfortunately, amplifier synthesis now becomes more empirical and will require the use of a nonlinear circuit simulator as well as an EM solver (such as ADS 2002 and Sonnet EM 8.0 [9.46, 9.61]). It should be noted that the substitution of distributed elements for lumped elements is only approximate and as such is only a starting point for the design.

The gate transmission line can easily be tapered by adjusting the values of each gate capacitor such that the drive voltages at each FET gate are equal. This condition is most important at the high-frequency end of the operating range assuring that each device contributes equal power to the drain line. Drive equalization offsets the normal losses encountered as the input signal propagates toward the termination end of the gate circuit. Hence, the series capacitors are largest at the termination end of the line where there is less available signal. With low-frequency amplifier designs, series gate resistors will also be required for stability reasons.

To maximize power output and accommodate the total drain current, some drain line tapering was employed. The impedance range of the tapering was less than ideal since the optimum impedance ratios for the lumped-element transmission line sections could not be realized with microstrip inductors and the capacitive parasitics of the active devices. The final circuit transmission line model is illustrated in Figure 9.57. A photograph of the monolithic amplifier, which is 3.48×1.27 mm in size, is shown in Figure 9.58 [9.37]. The complete dual-gate FET model (Fig. 9.59) was used in the final analysis to check key small-signal parameters such as stability, gain, and VSWR. The
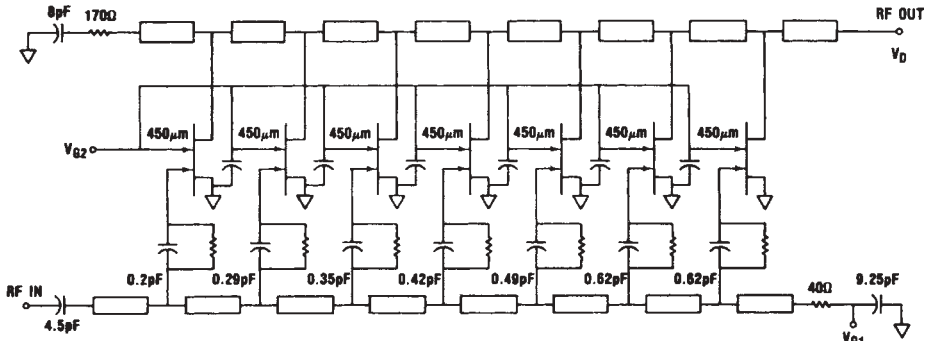
FIGURE 9.57   Transmission line model of dual-gate distributed power amplifier.
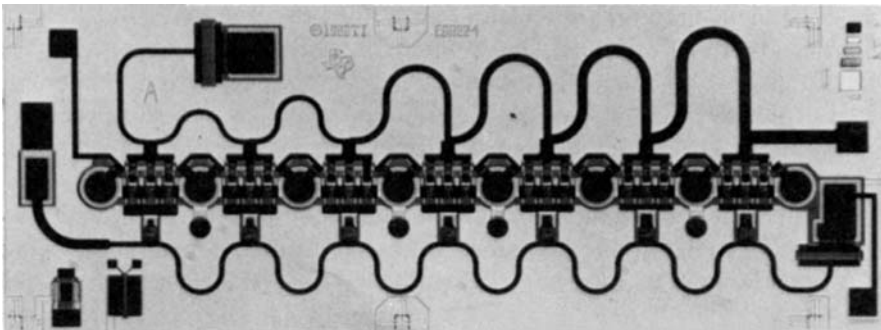
FIGURE 9.58   Monolithic dual-gate FET distributed power amplifier. (Courtesy of Texas Instruments.)
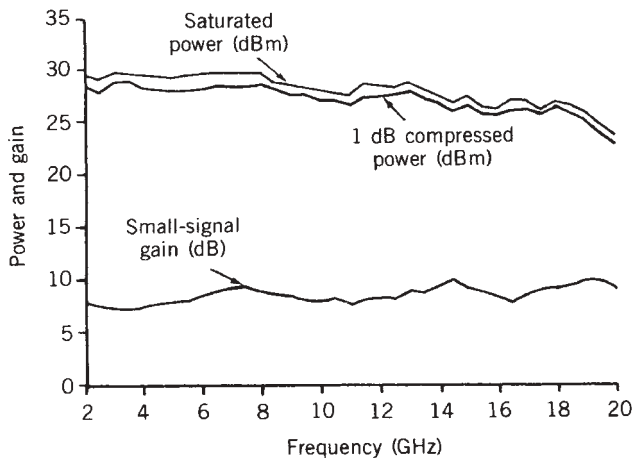
FIGURE 9.59   Measured gain and power output performance of monolithic distributed amplifier.
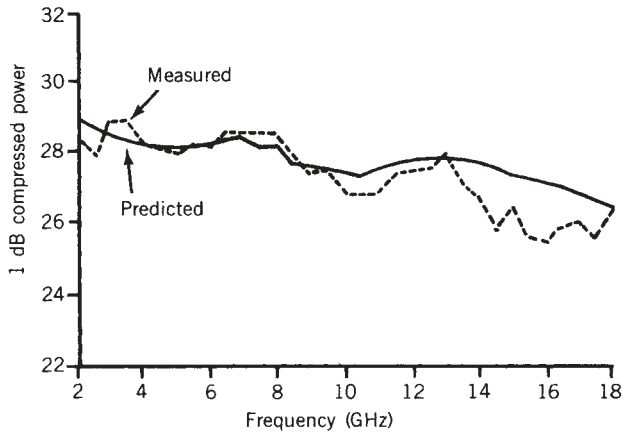
FIGURE 9.60 Measured versus predicted (Microwave SPICE) power output performance of monolithic distributed amplifier.

measured small-signal gain and power output performance are shown in Figure 9.60. The nominal gain was 8.6 ± 1.2 dB and the saturated power output averaged 28.5 dBm throughout the 2- to 18-GHz frequency range.

Although linear simulators give excellent design results for small-signal amplifiers, they do not give the designer insight into selecting optimum loading and bias conditions and understanding circuit power limitations. Fundamental design problems such as voltage clipping levels, current saturation characteristics, and breakdown conditions can only be analyzed with the aid of a nonlinear solver.

Based on these concepts, a high-efficiency, 31-dBm-output-power distributed amplifier for wireless applications with 3.2 V dc supply can be designed. The five-cell model was realized using an LTCC technology circuit substrate and discrete PHEMT (2.1-mm-gate-periphery) devices (Fig. 9.61). As with most power-distributed amplifiers, series
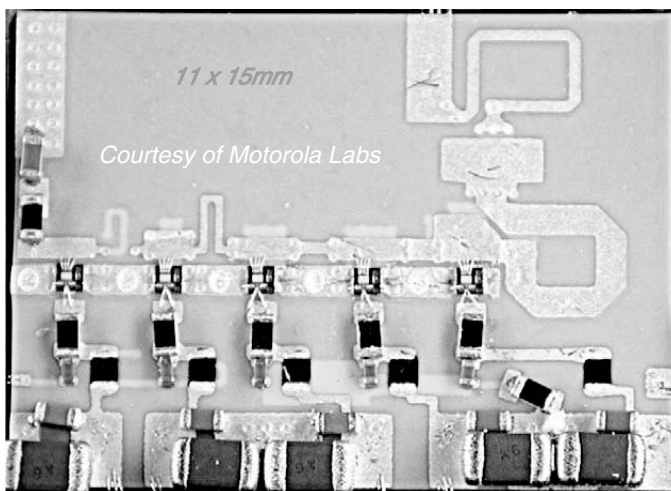
FIGURE 9.61 LTCC PHEMT low-voltage distributed power amplifier.

gate capacitors were employed to equalize the RF drive signal on each gate while series gate resistors were used to improve stability. The small-signal gain performance for the amplifier is shown in Figure 9.62a. LTCC technology is an excellent choice for fabricating high-power amplifiers because it provides high-circuit-density integration, low RF loss, and good thermal dissipation. Discrete semiconductor devices can also be placed directly on top of the 400-μm-diameter thermal vias, which are filled with silver.

The amplifier employs five 2.1-mm-gate-periphery devices operated in class B with a 3.2-V dc drain supply. The device size and supply voltage were chosen so that the amplifier output impedance would be about 3.3 Ω and the output power level would be greater than 1 W at saturation. The large-signal performance of the amplifier is shown in Figure 9.62b. As can be seen, the measured output power and efficiency performance are excellent. The dimensions of the power amplifier, which was constructed
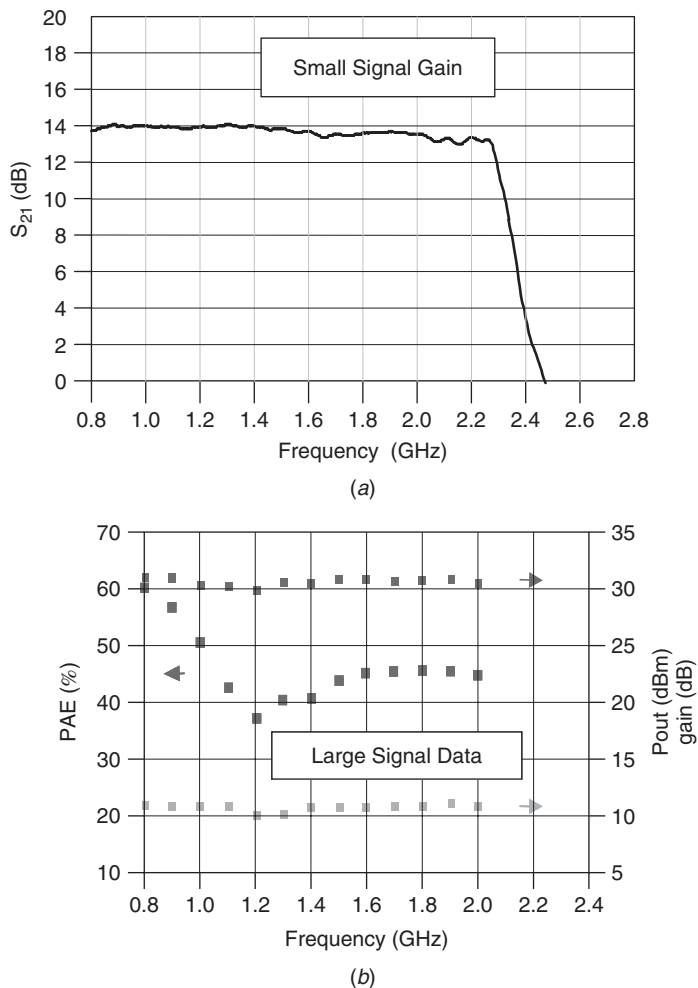
FIGURE 9.62 Low-voltage LTCC distributed amplifier performance: (*a*) amplifier small-signal gain (measured); (*b*) large-signal measured performance.

with Dupont 951 50- and 100-μm tapes, are 11 mm wide by 15 mm long. Unlike the amplifier described in the last section, which was designed for 50-Ω terminations, this low-voltage amplifier requires a broadband impedance transformer to transform the 3.3 Ω load impedance to 50 Ω throughout the band of interest from 800 MHz to 2.1 GHz. The transformer (Fig. 9.63) incorporates two 4:1 coupled-coil impedance transformers in series with additional matching elements. The transformer as well as total circuit optimization was accomplished using space-mapping techniques [9.59, 9.60] with the aid of ADS 2002 and Sonnet EM 8.0 [9.46, 9.61]. Without EM optimization adequate transformer performance would not be possible since no simple circuit model exists for the LTCC elements.

Constructing power amplifier modules using an LTCC implementation allows for the integration of most passive components, formation of thermal heat vias beneath the active devices, and the realization of very low loss transmission lines. The thermal vias exhibit a temperature rise of less than 5°C between the active device and the heat sink since they are solid silver and are larger than the active die area. It should also be noted that the loss in the drain line structure was measured to be less than 0.5 dB at 2 GHz.

As with any distributed power amplifier, series gate capacitors were employed to equalize the RF drive signal on each gate while series gate resistors were employed
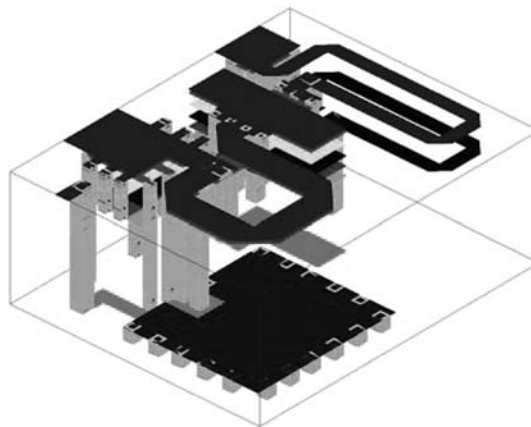
(a)
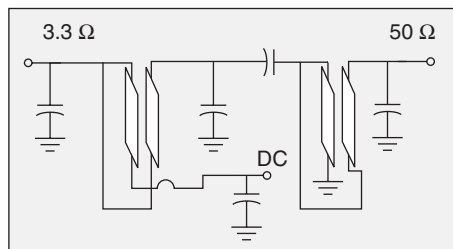
(b)

FIGURE 9.63 LTCC 3.3- to 50-Ω transformer: (a) layer configuration for multisection transformer; (b) multisection transformer schematic.

to improve stability. The dc supply to each device is supplied through the drain transmission line. The bias is applied at the hot plate of the bypass capacitor, which is at the base of the first transformer section. This 240-pF capacitor was fully integrated and was constructed using a dielectric $\varepsilon_r = 90$ paste with a paste thickness of approximately 25 μm.

The above designs illustrate the dramatic improvement that can be obtained in power-added efficiency when the drain transmission line is properly impedance tapered and the devices are selected for the correct load impedance. This was made possible because of the low-loss broadband performance of the 3.3- to 50-Ω output matching transformer which was realized using LTCC technology. The above design example also clearly illustrates the combination of analytical and empirical design techniques that must be employed in the synthesis of microwave power-distributed amplifiers, highlighting the importance of both nonlinear and EM simulators.

9.7 CLASS OF OPERATION

There are probably very few applications where amplifier efficiency is as important as it is in the design of large active element phased-array antennas. A variety of systems currently under development will require thousands of elements per array; thus, an improvement in power amplifier efficiency of as little as 5% can greatly impact prime power requirements and thermal design. In fact, some systems will not be feasible unless total power amplifier chain efficiencies exceed 25%. As the bandwidth requirements for new systems expand beyond the 10% range to greater than an octave, high-efficiency design becomes even more difficult. A more common application for high-efficiency RF amplifiers is in the transmitter output stage of hand-held communications equipment. In this application, higher efficiency translates into lower power consumption, that is, more "talk time" and of course smaller size and less heat.

Operating RF amplifiers in other than the class A mode is quite common in frequency ranges between HF and UHF but rarely at microwave frequencies except at low power levels. High-efficiency, class C amplifiers are quite common for applications not requiring linear performance. When linear performance is required, either class B or class AB designs are employed, although class D as well as class F switched amplifiers are starting to find applications. The theoretical efficiency for true class B operation with sinusoidal signals is 78.5%, which is far greater than the 50% theoretical maximum obtainable with class A operation. Although efficiencies near the theoretical limits are obtainable at low frequencies, it is difficult to achieve much better than 50% efficiency at the higher microwave frequencies. Efficiency limitations are not just a function of device and circuit losses but also are dependent on the device $I-V$ characteristics as well as the modulation format.

It should be noted that the operating conditions for various classes of operation are quite different. In class A operation, as previously mentioned, the active device is always operated in the active region. The device acts as a current source controlled by the input signal. The output voltage and current waveforms are undistorted but are exactly out of phase. For a sinusoidal input signal, the output waveforms are also sinusoids. If the device is ideal, the maximum output power is $(V_{dc})^2/2R_l$; however, the output power drops off rapidly as the drive power is reduced. For class B operation, the operation is somewhat different. Assuming that the device is ideal, it can now be

biased at threshold. Hence, the transistor only conducts during the positive half of the input signal, producing a half-wave-rectified signal. Obviously, some linearity is lost, but the output waveform is proportional to the input signal, with the theoretical peak efficiency reaching 78.5%. For class C the active device is biased further into the cutoff region so that the current conduction angle is less than $180°$. Practical class C amplifiers, such as the power tube amplifiers found in AM broadcast transmitters, can achieve 85% efficiency when operated with a conduction angle of about $150°$. Since the gain of these power tubes can be very high, this is also the power-added efficiency (PAE), defined as

$$\mathrm{PAE} = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{dc}}} \tag{9.54}$$

The voltage and current waveforms for almost ideal class A, B, and C amplifiers are shown in Figure 9.64. The output load is shunted with a resonant, parallel $L-C$ network which provides some harmonic filtering and energy storage. As expected, there
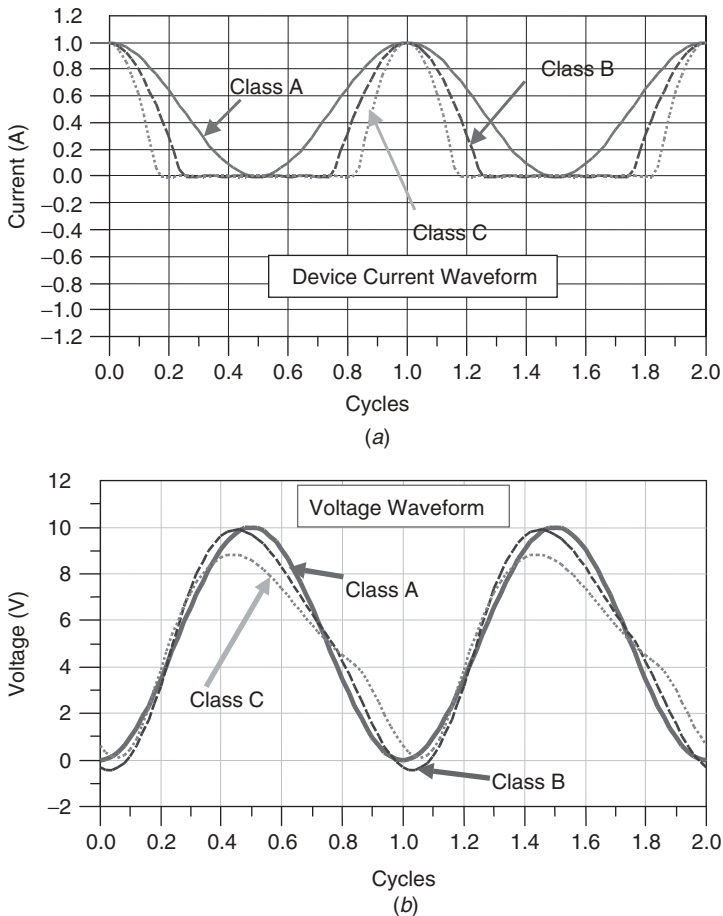
FIGURE 9.64 Comparison of class A, B, and C operation: (*a*) current waveform; (*b*) voltage waveform.
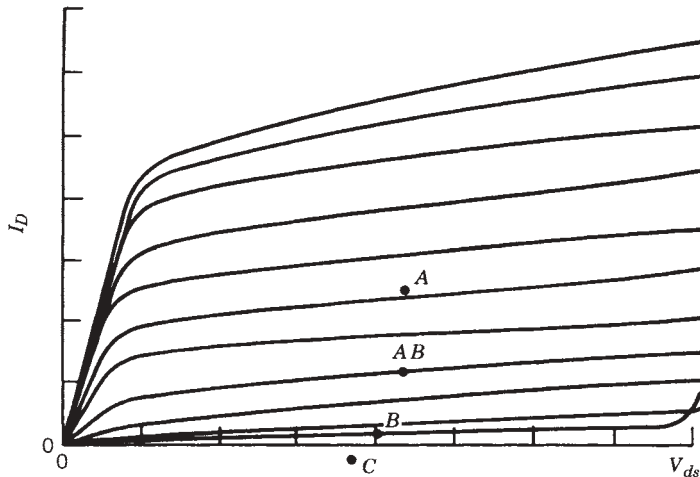
FIGURE 9.65   Typical operating point locations for various classes of amplifier operation.

is some harmonic distortion in the output waveform due to the truncated current during class A and B operation.

If we now consider the FET $I-V$ characteristics shown in Figure 9.65 for a typical GaAs FET, it becomes apparent that biasing the device for true class B operation is impractical since the g_m of the device at pinchoff is zero (small signal). Even biased at the zero-gain point, the finite value of leakage current reduces the efficiency obtainable. There are also other bias conditions that must be considered. With conventional class B design, the active device is biased to reproduce only one-half of the sinusoidal input signal. Hence, if the device is biased near cutoff and the drain (anode, collector, etc.) biased at breakdown, a positive input signal will cause the device to conduct. When the input signal reaches maximum and the load and gain are sufficient, the voltage across the drain can approach zero. Thus, a half-cycle sinusoid is reproduced at the device output. As the input signal swings negative, the device is in the cutoff region, thus clipping the other half cycle. If the device happens to be a GaAs FET with a finite gate-to-drain breakdown voltage, the drain should be biased back from the breakdown point by an amount equal to the magnitude of the input signal since the gate will become more negative than V_p during negative half cycles. The average current, neglecting leakage, under these conditions is $I_{\max} \times 2/\pi$ during the conduction half cycle. The reduced conduction angle in class B operation causes another problem. The half-wave-rectified sine wave at the output of single-ended designs is rich in harmonics or high in harmonic distortion. The harmonic problem can be solved in two ways. The most common way for a microwave amplifier is to use a narrow-band matching network at the output of the device. The Q of any real circuit element is more than sufficient to restore the missing half cycle by the current ringing or "flyback" of the network (Fig. 9.64b). This is exactly what occurs in the power amplifiers used in cellular telephone handsets. The other method employs amplifier circuits based on push–pull topologies. Regardless of the push–pull approach (transformer coupled, complimentary output, etc.), the output waveform is a composite of the waveforms generated by each half of the amplifier. Since each amplifier half is out of phase by 180°, the output waveform is a complete sine wave. A power push–pull amplifier used in base-station applications is shown in
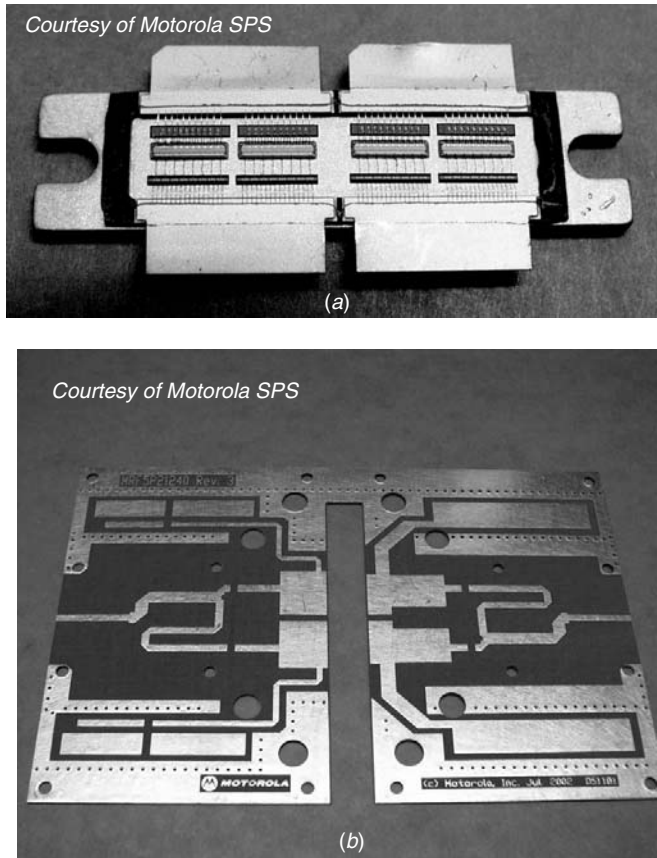
FIGURE 9.66   A 200-W push–pull amplifier device: (*a*) four 80-mm die and input/output matching; (*b*) external matching networks with differential combiner and divider.

Figure 9.66. The single-stage amplifier consists of four LDMOS 80-mm-gate-periphery die in conjunction with internal *L/C* matching elements. Each pair of die is connected in parallel at the package ports, thus comprising one-half of the push–pull amplifier. The matching elements transform the extremely low device impedances to practical levels where input/output baluns can easily be fabricated. After transformation, the input impedance and optimum load impedance of each side of the push–pull pair are shown in Table 9.10. The measured power output performance of the amplifier is shown in Figure 9.67. The efficiency and distortion characteristics are shown in Figure 9.68.

There are some practical issues with push–pull design at microwave frequencies that must be considered. First, complimentary structures (transformerless topologies) cannot be designed with GaAs FETs because *p*-channel FETs cannot be made to match the performance of *n*-channel devices due to the vast difference between hole and electron mobilities. Second, although transformers or baluns can be used, they are difficult to design and implement and can have bandwidth limitations. Also, when either single-ended or push–pull approaches are employed, there is almost always sufficient *Q* in the output circuit to cause voltage ringing (flyback) which attempts to reconstruct the missing half cycle from each device. This phenomenon can cause severe breakdown

TABLE 9.10   Input and Output Impedances as a Function of Frequency for WCDMA Push–Pull Amplifier

Frequency (MHz)	Z_{in} (Ω)	Z_{opt} (Ω)
2110	$5.39 - j13.89$	$3.69 - j10.51$
2140	$5.66 - j13.99$	$3.81 - j10.66$
2170	$5.53 - j14.51$	$3.79 - j11.05$
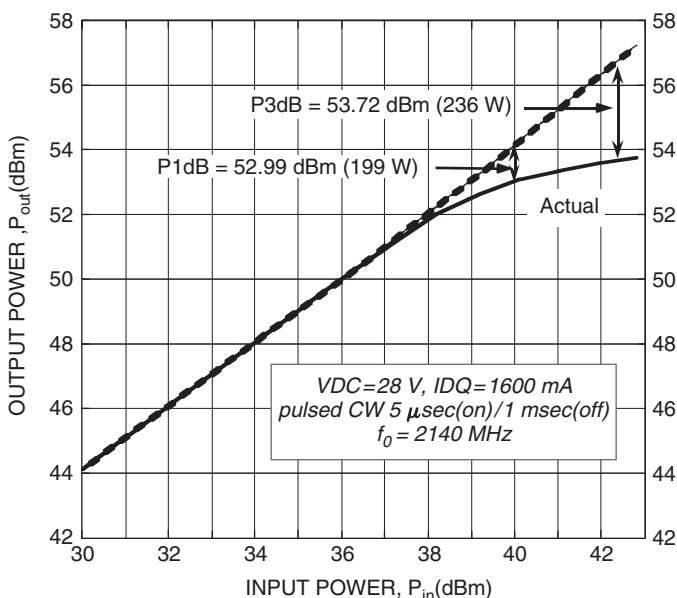
FIGURE 9.67   Pulsed CW output power versus input power for 200-W push–pull design.

problems if the devices are biased at a drain voltage much above $V_{br}/2$. For class A operation, the FET is biased at approximately the same drain voltage $V_{br}/2$. However, a considerably different load line results.

As shown previously, in the class A mode the operating point of the FET traverses a path from I_{max} ($V_{dd} = 0$) to V_{br} ($I_d = 0$), which is the typical dc load line. In the class B [9.38, 9.39] mode, the FET operating point traverses a path from I_{max} to approximately $V_{br}/2$. This difference in load line and bias point is illustrated in Figure 9.69. The final practical consideration is gain. Gain is also an efficiency driver, as can be seen in Eq. (9.54).

Most GaAs FETs fabricated today do not exhibit constant g_m as a function of drain current. Hence, when the FET is biased near pinchoff, the small-signal gain is essentially equal to zero. The gain problem can be partially overcome by operating the FET at reduced, rather than zero, current, or class AB. With currents on the order of 10% to 20% of I_{DSS}, there can be sufficient gain, depending on the frequency of operation, to be practical. Typically, about 6 dB of gain is lost by lowering the bias
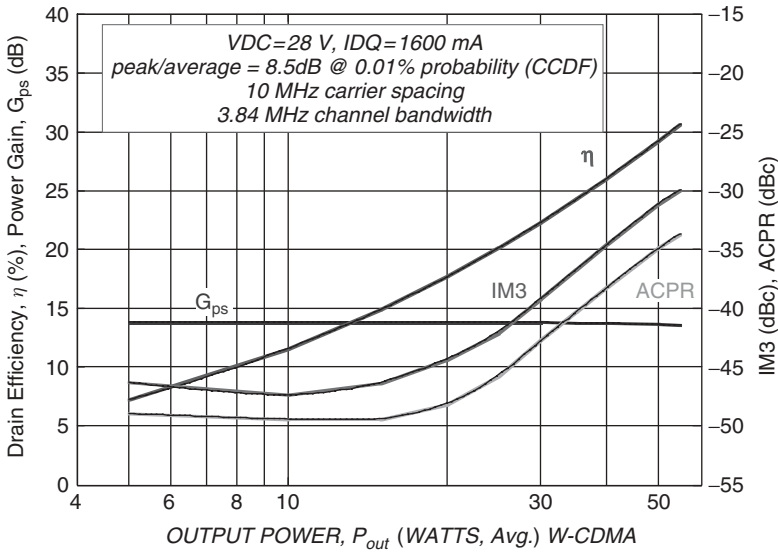
FIGURE 9.68 Two-carrier WCDMA ACPR, IM3, power gain, and drain efficiency versus output power for 200-W push–pull design.
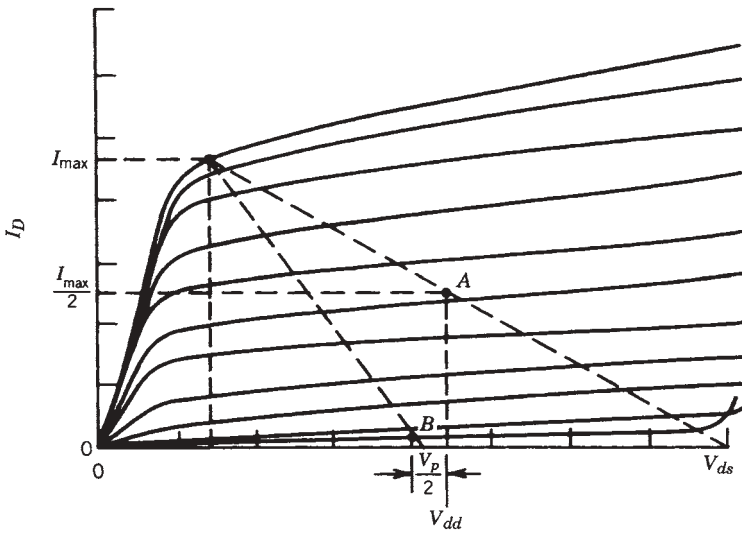
FIGURE 9.69 Class B versus class A load lines.

current from 50% to 60% of I_{DSS} to the 10% to 20% level required for class AB operation. This gain loss problem can also be reduced by adjusting the FET doping profile so that nearly linear g_m performance as a function of drain current is obtained. However, at lower microwave frequencies (<5 GHz), modern devices have plenty of gain. The amount of stable gain available will still dominate the design.

At lower frequencies, such as the HF and VHF regions, class B operation is well known. Class B or AB circuits can be implemented using either bipolar or field-effect transistors and the design of such amplifiers proceeds as with any *S*-parameter synthesis approach. There are, however, some biasing and thermal constraints that differ from the GaAs FET, especially with the bipolar transistor, that must be considered. As with all semiconductors, the maximum power dissipation is closely related to the amount of heat that can be removed from the semiconductor die provided the heat generated by the device is distributed relatively uniformly throughout the structure. When bipolar transistors are used at high current levels, the emitter current of the device is concentrated at the emitter–base edge. Current-crowding effects tend to forward bias the device at the edge of the emitter closest to the base contact. Hence, the center of the emitter injects very little current as compared to the area near the edges. Because of this effect, a high emitter periphery-to-area ratio is desired. In addition, most modern power BJTs employ emitter ballasting (or base) techniques, which help equalize bias within the active device and thus eliminate thermal "hot spotting." The ballasting is realized by controlling the resistance of the emitter contact area in such a way as to add a predetermined amount of series resistance in the emitter circuit, causing negative feedback and hence equalizing the device. This type of ballasting allows for a more efficient device and helps protect the final amplifier from high RF voltage breakdown problems caused by high VSWR. It also raises the saturation voltage and lowers the RF gain.

Another problem which is common with BJTs is thermal runaway. This condition is caused, particularly with class B or AB amplifiers, by the fact that the base-to-emitter voltage has a negative temperature coefficient. When the transistor is biased at low collector currents and no drive signal is present, the power dissipation and hence the device operating temperature are low. As drive is applied and the amplifier approaches large-signal performance, the power dissipation and thus the operating temperature rise. If the bias voltage is fixed and the base-to-emitter voltage has dropped due to a temperature rise, the quiescent operating current could be substantially greater than during the initial no-drive state. With a large quiescent current, the device will operate even hotter and hence the problem worsens. However, these problems are usually avoided by proper bias supply design. These bias supplies, which are temperature compensated, typically employ a sensing diode with similar characteristics to the base–emitter junction which is fabricated on the same transistor die or mounted adjacent to the power device. As the operating temperature of the device increases, the bias voltage also increases, thus maintaining a constant value of quiescent current and power dissipation.

Once the RF characteristics of the BJT are determined, the design of a push–pull amplifier proceeds in the same manner as the FET design previously described. The problem again becomes that of device matching and optimum load termination, with the additional task of balun synthesis. A typical HF class AB push–pull amplifier is illustrated in Figure 9.70 [9.40]. Transformer hybrids and matching transformers were employed in the input and output networks in order to provide proper phasing and impedance functions. A temperature-compensated bias network was also employed. The amplifier is capable of 120 W of output power throughout the 2- to 30-MHz frequency band, with an average power-added efficiency of 48%. Push–pull amplifiers of this type, employing BJTs or FETs, can be designed for a variety of frequency ranges extending to about 500 MHz [9.41]. As the operating frequency approaches

C_1, C_2 = 0.15 μF, electrolytic
C_3, C_9 = 0.04 μF, ceramic
C_4 = 0.0027, μF, ceramic
C_5 = 100 μF, electrolytic
C_6, C_7 = 0.1 μF, electrolytic
C_8 = 1000 pF, feedthrough, Allen-Gradley FA5C
   or equiv.
C_{10} = 5 μF, electrolytic
C_{11} = variable capacitor, ARCO 249 or equiv.
L_1, L_2 RF choke, 10 μH
L_3, L_4 = 15 turns of No. 20 wire on Q1 CF-108
   Indiana General ferrite core or equiv.

R_1 = 3.3 Ω, 0.5 W
R_2, R_3 = 30 Ω, 0.5 W in parallel with 30 Ω,
   0.5 W
R_4 = 5.6 Ω, 0.5 W in parallel with 5.6 Ω,
   0.5 W

T_1, T_6 = two twisted pairs (9 turns per inch) of
   No. 26 wire in parallel; five turns on Q1
   CF-108 Indiana General ferrite core or equiv.
T_2, T_3, T_4, T_5 = six twisted pairs (9 turns per
   inch) of No. 28 wire in parallel; five turns on
   Q1 CF-108 Indiana General ferrite core or
   equiv.

FIGURE 9.70   Typical class AB push–pull power amplifier employing BJTs. (Courtesy of RCA).

1 GHz, transformer hybrid techniques for power applications are replaced by classical microwave circuitry. Amplifiers with power levels exceeding 1 kW are common and are readily available on the commercial market.

   An interesting variation of the class B and C amplifier is the Doherty amplifier. Doherty tube amplifiers have been around since 1936, but in recent years, their solid-state equivalents have found some popularity. The basic circuit is comprised of two amplifiers embedded in a reactive combining network as shown in Figure 9.71. Key to
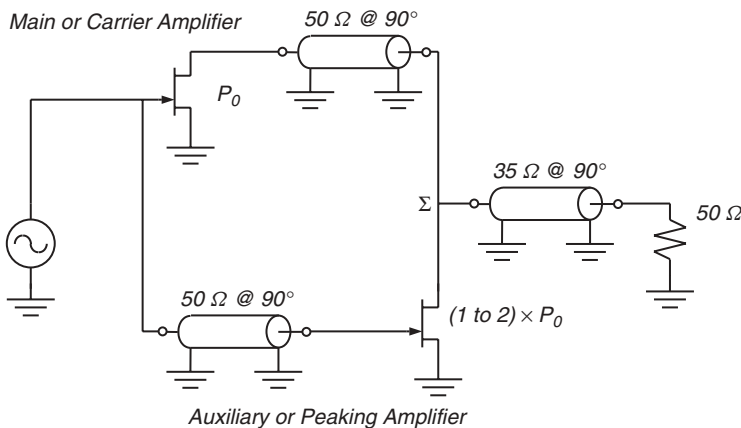
FIGURE 9.71   Doherty amplifier.

the circuit's operation is that the amplifiers are operated in different modes. The main amplifier is biased as a class B stage providing linear operation while the auxiliary amplifier typically is biased as a class C stage. The class C stage bias is set such that it begins to become active when the input signal is about 50% below peak drive level. When the peaking amplifier is off (i.e., low drive), its output appears as an open circuit (neglecting real circuit conditions); thus, the carrier amplifier ("main") is loaded with 100 Ω (Σ node at 25 Ω). If the class B stage is designed for a 50-Ω load, it will deliver about 50% of its maximum power output with a 100-Ω load, or about one-fourth (-6 dBc) of the maximum Doherty amplifier output. At this point, the class B stage is operating at the maximum theoretical efficiency of 78.5%. When full drive is applied to the Doherty amplifier, both stages are fully active, and because of the 35-Ω, quarter-wavelength long transmission line, both the class B and class C stages are terminated with their optimum load impedance of 50 Ω. Again, both stages are now operating at maximum efficiency. The resulting Doherty amplifier exhibits a broader range of high-efficiency operation, with peak efficiency occurring at P_0 and $\frac{1}{4}P_0$. Below $\frac{1}{4}P_0$, the efficiency falls in a similar manner to a conventional amplifier. Various combinations of load impedance with main and auxiliary amplifiers of different sizes can be configured to customize the efficiency-versus-power-output characteristics of the amplifier [9.63].

The push–pull class B amplifier concept can be extended to the realization of a class D amplifier. As in conventional push–pull operation, two active devices are required to reproduce the input signal, but in the class D realization the signal is reproduced as a square-voltage (or current) waveform at the device output nodes. The output node is connected through a series tuned circuit to restore only the fundamental frequency at the load (Fig. 9.72). At any point in time, one device is fully saturated while the other device is in the cutoff region. With ideal elements, the efficiency of this type of amplifier approaches 100% since neither device dissipates any power. Parasitic capacitances and finite switching speeds degrade the efficiency of real amplifiers since the active devices conduct current when they are in the active region of operation, which becomes a longer portion of a cycle as frequency increases. It is very common to find multikilowatt amplifiers in the HF region of the spectrum; class D amplifiers are rarely used at frequencies above several hundred megahertz.

Another high-efficiency topology is the class E amplifier circuit. As in the above high-efficiency topologies, the voltage across the active device is minimized when the transistor is conducting current or minimizing the conduction current when a voltage exits across the device. In addition, the relative time interval when current and voltage are simultaneously present at the output of the device compared to the cycle time must also be minimized. The class E amplifier is a single-ended switching amplifier. The basic circuit model is shown in Figure 9.73, where the active device is used as a switch. The voltage at the output of the device results from the charging and discharging of the shunt capacitance from the RF and dc voltages. The series tuned output $L–C$ network is set to exhibit a reactance of $+1.15\,R_{\text{load}}$, while the total shunt capacitance is set to have a reactance of $-0.1836/R_{\text{load}}$ for optimum efficiency [9.64, 9.65]. Amplifiers designed for class F operation employ harmonic tuning to force the waveform at the drain or collector of the active device to be a square wave. Odd-harmonic open circuits force the voltage to be a maximum while even-harmonic terminations are used to force the current waveform to be a half sinusoid. A simplified class F amplifier is shown in Figure 9.74.

(a)

(b)
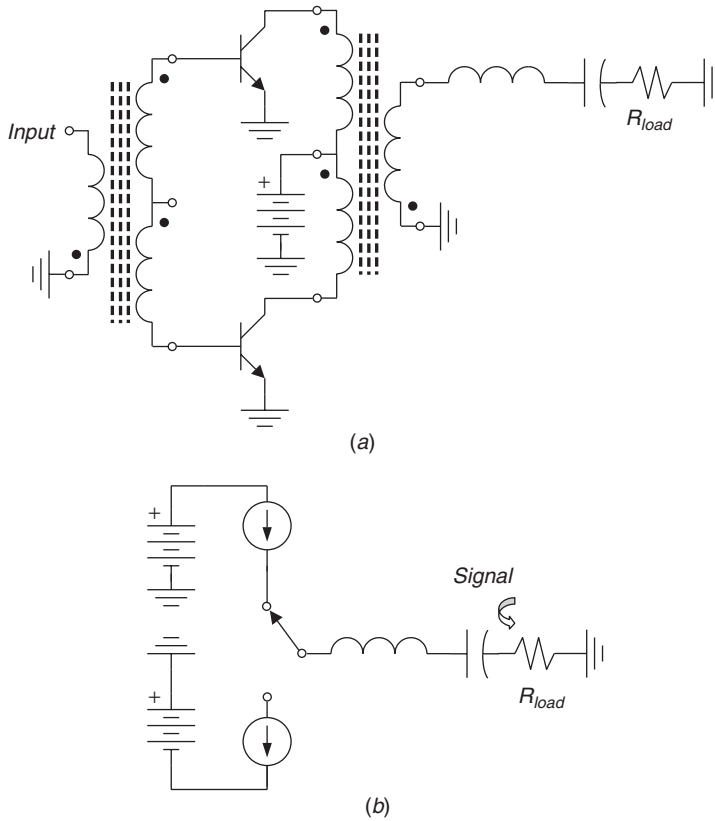
FIGURE 9.72   Class D amplifier: (*a*) ideal circuit; (*b*) ideal switching model.
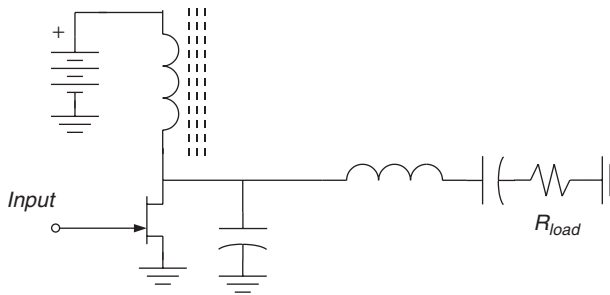
FIGURE 9.73   Class E amplifier ideal switching model.

9.8   POWER AMPLIFIER STABILITY

One of the key issues in the design of RF power amplifiers is circuit stability. As in any amplifier, small or large signal, oscillation can occur. However, it is also common that stability problems can manifest themselves as low-level spurious signal, not just full saturated oscillation. Stability problems are also very dependent on the device type; hence, certain devices are more prone to specific types of oscillation than others.
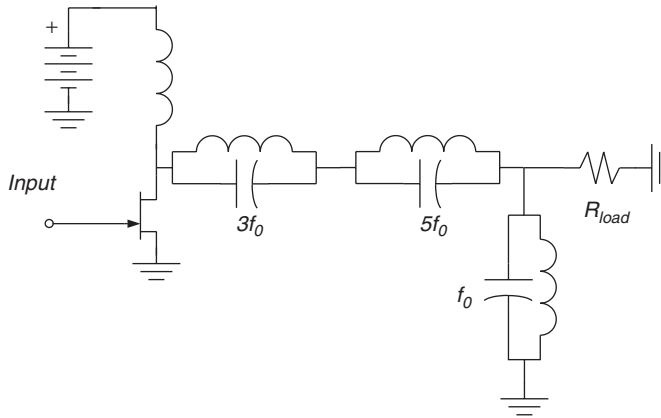
FIGURE 9.74   Simplified class F amplifier.

Modeling certain forms of oscillation can be very difficult, but stable power amplifier design can be accomplished using modern CAD tools, although it requires rigorous design skill. Unfortunately, designing stable amplifiers usually means compromising something. As in the design of the distributed-power amplifier, highlighted in the previous sections, gain is traded for stability. Sometimes, bandwidth, noise figure, efficiency, linearity, or power output must be compromised.

When designing oscillators, large amounts of positive feedback are employed to cause oscillation; hence, linear positive feedback must be minimized with amplifier design. Minimizing linear feedback is much harder than it appears since device parameters are a function of bias, frequency, and drive level. A common mistake when designing amplifiers is using ideal decoupling elements or none at all in the circuit simulation. Actual bias element values and all circuit parasitics must be included in any circuit simulation. A typical decoupling network requires several low-pass sections, sometimes realized with combinations of L and C, so that the decoupling is effective from near dc to well beyond the operating band of interest.

Parasitic oscillations are more difficult to analyze. Since all real active devices have nonlinear capacitive elements, parametric oscillations can occur. With devices such as PHEMTs, the gate-to-source capacitance is quite nonlinear with high Q. When large RF voltages are applied to the gate, parametric oscillations can occur because the "pumping" of this highly nonlinear capacitor produces a negative resistance. If the magnitude of the negative resistance is large enough, the amplifier can exhibit high- or low-level oscillations at the subharmonics (f_0/n) of the operating frequency. It should be noted that oscillations at other than the subharmonics of the operating frequency are also possible. These parasitic oscillations can be severe or can just become modulation on the RF carrier. Sometimes, the simple addition of "resistive damping" in the gate (or base) circuit can completely suppress the oscillations. The problem becomes more difficult as the number of amplifier stages increases.

In practice, RF and microwave designers rely heavily on the so-called Linville [9.67] or Rollett [9.69] stability criteria (K factor) in ascertaining the stability of their two-port circuit designs. Several variants of sets of conditions exist in the literature. All of these sets of conditions, which were derived by steady-state analyses, have been shown to be equivalent [9.51, 9.65–9.72]. Many other textbooks and leading CAD

software packages make the following or equivalent statement: A two-port network is unconditionally stable if and only if, for all frequencies ω, $K > 1$ and, alternatively, $|\Delta_s| < 1$ or $B_1 > 0$ or $1 - |S_{ii}|^2 > |S_{12}S_{21}|$ for $i = 1, 2$, where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta_s|^2}{2|S_{12}||S_{21}|} \tag{9.55}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta_s|^2 \tag{9.56}$$

and $\Delta_s = S_{11}S_{22} - S_{12}S_{21}$ is the determinant of the two-port S-parameter matrix.

The same conditions can be stated in terms of other circuit parameters such as Z, Y, H, $\ldots$, where K takes the invariant form

$$K = \frac{2\,\mathrm{Re}(\gamma_{11})\,\mathrm{Re}(\gamma_{22}) - \mathrm{Re}(\gamma_{12}\gamma_{21})}{|\gamma_{12}\gamma_{21}|} \tag{9.57}$$

and absolute stability is claimed if and only if $\mathrm{Re}(\gamma_{11}) > 0$, $\mathrm{Re}(\gamma_{22}) > 0$, and $K > 1$.

However, it has been shown [9.51] that these stability criteria are not rigorous and can fail if the unloaded N-node linear network (before being reduced to a two-port network) contains poles with positive real parts, that is, poles in the right-half plane (RHP). The failure of these traditional two-port stability criteria stems from the fact that no universal determination of the stability of any N-node linear network can be made from the locations of the zeroes of the determinant of the reduced two-port network. The network can be unstable even if all of the zeroes of the reduced two-port network determinant have negative real parts. This failure does not depend on the symmetry of the network and can occur in symmetric as well as nonsymmetric networks. Since the conditions for oscillations are the opposite of the conditions for stability, the notion that a circuit is always oscillatory at a frequency at which the imaginary part of its input or output admittance is zero, provided that the real part is negative, is also incorrect. *The process of reducing an N-node circuit network to a two-port can introduce pole-zero cancellation in the reduced two-port network determinant, making the traditional K-factor stability criteria invalid.*

A proper statement of the two-port stability criteria involving K should be: *An unloaded two-port which has no poles in the RHP will remain stable when loaded externally at its input and output ports if and only if $K > 1$ and $|\Delta_s| < 1$ for all ω.*

Therefore, the role of using K in determining the stability of an N-node linear network by means of its reduced two-port matrix is quite diminished. A separate test is required to determine if the unloaded N-node network contains any poles in the RHP before the traditional K-factor criteria can be applied to the reduced two-port matrix. Platzker et al. [9.51] describe a mathematically rigorous test referred to as the normalized determinant function (NDF) test based on contour plotting of a normalized determinant function to ascertain the stability of linear n-port networks.

The NDF function is defined as the ratio of the full N-node network determinant (including all port terminations) normalized to the full N-node passive network determinant where all dependent sources (i.e., voltage-controlled or current-controlled sources) contained within the network are set to zero:

$$\mathrm{NDF} = \frac{\Delta}{\Delta_{0M}} \tag{9.58}$$

where M is the number of dependent sources contained within the network. Note that any linear network parameters such as Y, Z, H can be used to calculate the determinants.

To determine stability, the complex quantity NDF is calculated for a given network along the frequency axis ω from $+\infty$ to $-\infty$ and its locus is plotted in the complex plane. If the locus of the NDF encircles the origin $(0, 0)$ in a counterclockwise direction, the determinant Δ contains zeroes in the RHP. From Routh [9.73] and Bode [9.74], if the determinant of a linear network contains any zeroes in the RHP, including the frequency axis ω, the network will be unstable; otherwise the network is stable.

Only after it is known that the full N-node network determinant contains no zeroes in the RHP can the K-factor stability criteria be applied to the reduced two-port network matrix to ascertain if it will remain stable under all passive load conditions. However, it should be noted that the inverse condition is very useful: If $K < 1$, the amplifier is unstable.

9.9   AMPLIFIER LINEARIZATION METHODS

The topic of amplifier linearity has become a very popular topic in the technical community due the widespread deployment of digital communication systems. There are a variety of methods in use today, ranging from simple RF feedback techniques to elaborate envelope elimination and restoration (ERR) techniques. In addition, analog and digital forms of predistortion can also be employed. Achieving high linearity is only part of the problem; modern systems also require high-efficiency operation [9.75–9.77].

The simplest form of linearization is to employ some form of negative feedback to the amplifier. At low frequencies, where device phase shifts and circuit elements are well behaved, multidecade feedback amplifiers have been implemented. As one approaches the microwave realm, keeping the feedback negative gets a bit harder. When operating at frequencies above several gigahertz, it is difficult to apply shunt feedback techniques with more than two stages due to the absolute phase shift of the loop itself resulting from its physical size. When using hybrid circuit techniques, shunt feedback at 2 GHz is a challenge. However, monolithic IC techniques can extend feedback amplifiers well into the microwave region [9.78]. CATV amplifiers employ both series and shunt feedback methods in order to achieve linear amplifier performance. These amplifiers have been realized in hybrid form for many years and typically operate from 50 to 1000 MHz. With modern devices and MMIC circuit methods, extremely linear performance can be obtained. A simplified schematic of a cascode feedback amplifier is shown in Figure 9.75. The transformers are typically wound (trifilar) on high μ ferrite beads while the amplifier can be realized with either hybrid or MMIC techniques. Since modern devices have so much gain at frequencies below 1 GHz, the difference between the open-loop gain and the closed-loop gain of the amplifier is very substantial; hence, a lot of linearity improvement is obtained in addition to temperature stability. The amplifier gain is essentially determined by the ratio R_e/R_f.

Linearizing RF power amplifiers tends to be a bit more difficult. One of the more popular methods to achieve linear amplifier performance is the use of feed-forward techniques. Feed-forward techniques have been used to linearize high-power amplifiers, such as the ones used in cellular base-station applications, and in ultralow-distortion amplifiers used in CATV trunk systems. The method is easy to understand but a little
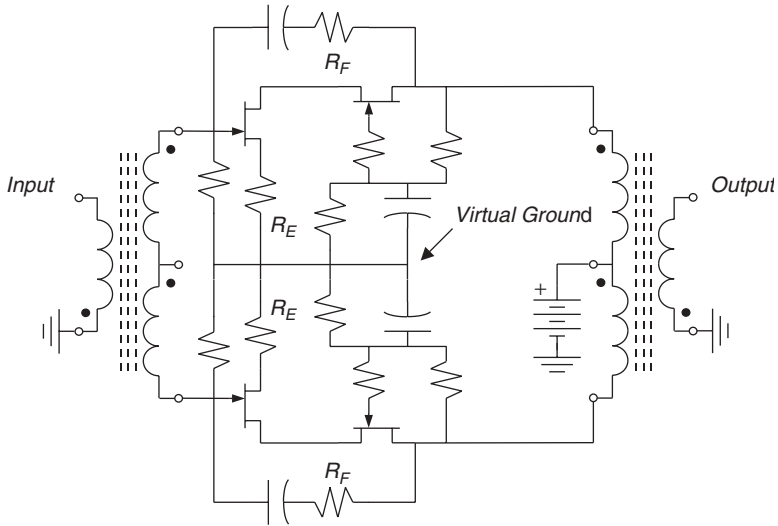
FIGURE 9.75   Cascode push–pull feedback amplifier model.
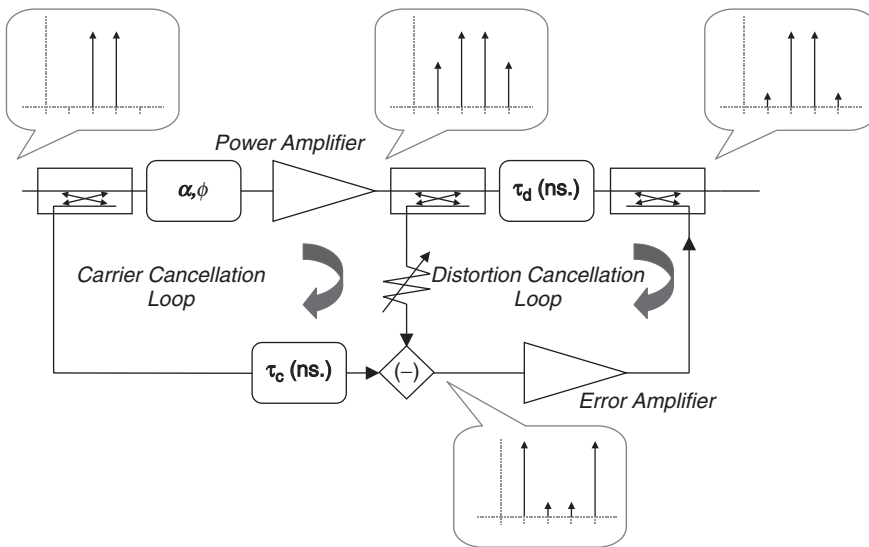
FIGURE 9.76   Feed-forward power amplifier.

difficult to implement. Feed-forward systems are composed of two amplifiers—the power amplifier you are trying to linearize and the error amplifier along with supporting hardware. A simplified system block diagram is shown in Figure 9.76. The technique begins by sampling some of the input signal, which is considered to be distortion free, and combining it with a sample of the power amplifier's output waveform. The sampled input signal is delayed by the group delay of the power amplifier and combined with the sampled output signal, which consists of desired carriers plus distortion. By adjusting the amplitude and phase of the sampled signals such that the carrier is canceled, just the

distortion components will remain at the input of the error amplifier. The remaining distortion waveform is then amplified by a very linear error amplifier and forward coupled into the output of the amplifier system. A delay line must be used at the output of the power amplifier before final combining to account for the delay in the error amplifier. If the delays and amplitudes are correctly matched, a substantial amount of distortion can be canceled. In practice, about 20 to 25 dB of distortion improvement can be obtained. As the operational bandwidth becomes wider, the problem becomes more difficult; however, broadband amplifiers can be realized. It should be noted that these schemes are open-loop systems and are prone to typical open-loop problems such as temperature drift, drive level, voltage pushing, and component matching. Typical delay line times are 5 to 20 ns, which can be realized with transmission lines or high-Q bandpass filters and equalizers.

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PROBLEMS

9.1 Derive (9.3) and (9.4) by assuming that the input is an open circuit at low frequencies. Show (9.3) can be simplified to (9.59): $|S_{21}| \simeq -2g_m Z_0$.

9.2 Derive the DeLoach relations given by (9.5) to (9.7).

9.3 Using the method outlined by DeLoach, determine the gate capacitance of a typical FET when $T = -10$ dB, $T_m = -15$ dB, $f_1 = 4.5$ GHz, and $f_2 = 5.5$ GHz. Assume typical values of g_m, R_s, and C_{gd} for a 300-μm FET.

9.4 For the FET I–V characteristics illustrated in Figure 9.24, calculate the RF and DC load lines when the breakdown voltage is 12 V.

9.5 Assuming that the output characteristics of an FET can be modeled using the following simple elements, design a four-element matching network for the 6- to 12-GHz frequency range that optimally terminates the FET for maximum power performance:

$$C_{ds} = 0.17 \quad \text{pF} \qquad R_d = 4 \ \Omega$$
$$R_{ds} = 270 \ \Omega \qquad R_{\text{opt}} = 77 \ \Omega$$
$$L_d = 0.22 \quad \text{nH}$$

9.6 Determine the largest gate periphery that can be used in the design of a six-cell distributed amplifier for the 2- to 8-GHz frequency range. Use the single-gate equivalent dual-gate FET model illustrated in Figure 9.48 and scale the element values accordingly.

9.7 Derive the power gain expression in (9.11) by first determining the current delivered to the output load on an FET-by-FET basis for the general amplifier case.

9.8 Determine the average value of drain current for a class B amplifier stage when driven for maximum output voltage swing and biased at a quiescent current of 15% I_{dss}.

9.9 Show that the ideal class A amplifier has an efficiency of 50% and the ideal class B amplifier has an efficiency of $\pi/4$ or 78.5%.

CHAPTER 10

OSCILLATOR DESIGN

10.1 INTRODUCTION

Oscillator design is very similar to amplifier design. The same transistors, the same dc bias levels, and the same set of S parameters can be used for the oscillator design. The load does not know whether it is connected to an oscillator or an amplifier (see Fig. 4.1).

For the amplifier design, M_1 and M_2 can be designed with a normal Smith chart, since S'_{11} and S'_{22} are normally less than unity. For oscillators, S'_{11} and S'_{22} are both greater than unity for oscillation. Thus a compressed Smith chart that includes reflection coefficients greater than unity is a useful tool for oscillator design.

Oscillators can be designed from several points of view:

1. *S*-parameter design [10.1, 10.2]
2. Small-signal negative resistance from a transistor model [10.3]
3. Series or parallel resonance
4. Low noise [10.4–10.6]
5. Large-signal analytic approach [10.7–10.9]
6. Nonlinear analysis [10.10, 10.11]

Each of these viewpoints will give additional insights into the many challenges facing oscillator designers. Referring to the oscillator of Figure 4.12, we can subdivide the problem into the low-loss resonator M_3, the active two-port with its S-parameter description, and the passive lossy load M_4.

In this chapter we emphasize the *S*-parameter design approach, which is the most useful to microwave designers. Before developing this concept, the compressed Smith chart or negative-resistance Smith chart will be developed as a design tool. Next, the oscillator design is viewed as either series or parallel resonance, a one-port design. Then the various resonators available to microwave designers are reviewed. Then two-port (or *n*-port) oscillator design is presented. At this point some design examples are given to demonstrate some useful designs. These include bipolar designs using lumped elements, distributed elements, and dielectric resonators.

Negative resistance of an oscillator can also be derived from the transistor equivalent circuit. An example of this design method is given, leading to a wide-band VCO design over 200 to 400 MHz. Some historically significant oscillator circuits are also given in this section.

The definition of oscillator Q is presented next. The two common techniques for measuring oscillator Q, load pulling and injection locking, are discussed.

The various descriptions of oscillator noise are developed leading to Leeson's noise model for the oscillator. Low-noise design examples are given, including varactor-tuned (VCO), YIG-tuned, and DRO fixed tuned. In addition, noise degeneration is shown to produce lower oscillator noise.

The large-signal analytic approach to oscillator design will be presented with a design example at 5.3 GHz using a power GaAs MESFET. Then a nonlinear oscillator model is used to design an 8.8-GHz GaAs MESFET oscillator. The present state of the art for oscillators is summarized at the conclusion of this chapter.

The conditions for oscillation can be expressed as

$$k < 1 \tag{10.1}$$

$$\Gamma_G S'_{11} = 1 \tag{10.2}$$

$$\Gamma_L S'_{22} = 1 \tag{10.3}$$

The stability factor should be less than unity for any possibility of oscillation. If this condition is not satisfied, either the common terminal should be changed or positive feedback should be added. Next, the passive terminations Γ_G and Γ_L must be added to resonate the input and output ports at the frequency of oscillation. This is satisfied by either (10.2) or (10.3). It will be shown in Section 10.5 that if (10.2) is satisfied, (10.3) must be satisfied, and vice versa. In other words, if the oscillator is oscillating at one port, it must be simultaneously oscillating at the other port. Normally a major fraction of the power is delivered only to one port, since only one load is connected. Since $|\Gamma_g|$ and $|\Gamma_L|$ are less than unity, (10.2) and (10.3) imply that $|S'_{11}| > 1$ and $|S'_{22}| > 1$.

The conditions for oscillation can be seen from Figure 10.1, where an input generator has been connected to a two-port. Using (4.73) for the representation of the generator, which is repeated here,

$$a_1 = b_G + \Gamma_1 \Gamma_G a_1 \tag{10.4}$$

and defining

$$\Gamma_1 = S'_{11} \tag{10.5}$$

$$S'_{11} = \frac{b_1}{a_1} \tag{10.6}$$
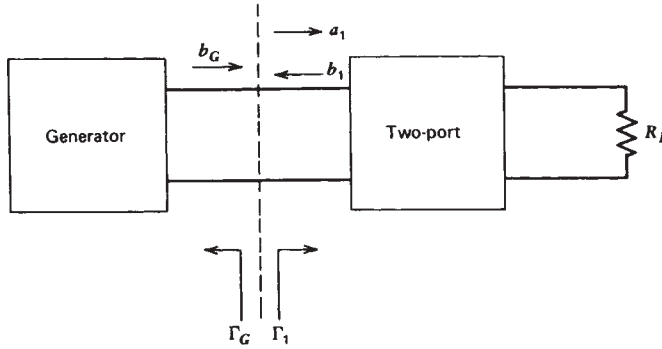
FIGURE 10.1 Two-port connected to a generator.

give

$$b_G = a_1(1 - \Gamma_1 \Gamma_G)$$

$$= \frac{b_1}{S'_{11}}(1 - S'_{11}\Gamma_G) \tag{10.7}$$

$$\frac{b_1}{b_G} = \frac{S'_{11}}{1 - S'_{11}\Gamma_G} \tag{10.8}$$

Thus the wave reflected from the two-port is dependent on b_G, S'_{11}, and Γ_G. If (10.2) is satisfied, b_G must be zero, which implies that the two-port is oscillating. Since $|\Gamma_G|$ is normally less than or equal to unity, this requires that $|S'_{11}|$ be greater than or equal to unity.

The oscillator designer must simply guarantee a stability factor less than unity and resonate the input port by satisfying (10.2), which implies that (10.3) has also been satisfied. Another way of expressing the resonance condition of (10.2) is the following:

$$R_{in} + R_G = 0 \tag{10.9}$$

$$X_{in} + X_G = 0 \tag{10.10}$$

This follows from substituting

$$S'_{11} = \frac{R_{in} + jX_{in} - Z_0}{R_{in} + jX_{in} + Z_0} \tag{10.11}$$

$$\Gamma_G = \frac{R_G + jX_G - Z_0}{R_G + jX_G + Z_0}$$

$$= \frac{-R_{in} - Z_0 - jX_{in}}{-R_{in} + Z_0 - jX_{in}} \tag{10.12}$$

into (10.2), giving

$$\Gamma_G S'_{11} = \frac{-R_{in} - Z_0 - jX_{in}}{-R_{in} + Z_0 - jX_{in}} \cdot \frac{R_{in} + jX_{in} - Z_0}{R_{in} + Z_0 + jX_{in}} = 1$$

which proves the equivalence of (10.2) to (10.9) and (10.10).

Before proceeding with the oscillator design procedures, some typical oscillator specifications are given in Table 10.1 for the major types of oscillators. The high-Q or cavity-type oscillators usually have better spectral purity (see Section 10.8) than do the low-Q VCOs, which have faster tuning speeds. The resonators are described in Section 10.4. The FM noise is usually measured at about 100 kHz from the carrier in units of dBc, which means decibels below the carrier level, in a specified bandwidth of 1 Hz. If the measurement bandwidth is 1 kHz, the specification changes by 10^3, as discussed in Section 10.8.

In selecting a transistor to meet the specifications, the amplifier transistors with the same frequency and power performance are usually suitable. Lower close-in noise can be achieved from silicon bipolar transistors compared to GaAs MESFETs because of the $1/f$ noise difference described in Figure 10.16.

TABLE 10.1   Specifications for Major Types of Oscillators

	Varactor-Tuned Oscillators				
Frequency Range, minimum	4900–5900 MHz	5200–6100 MHz	5400–5900 MHz	5800–6600 MHz	6500–8600 MHz
Power output into 50-Ω Load, minimum	10 mW/+10 dBm	10 mW/+10 dBm	10 mW/+10 dBm	5 mW/+7 dBm	10 mW/+10 dBm
Power output variation at 25°C, maximum	±1.5 dB	±1.5 dB	±1.5 dB	±1.5 dB	±1.5 dB
Operating case temperature range	0° to +65°C	0° to +65°C	0° to +65°C	0° to +65°C	0° to +65°C
Frequency drift over operating temperature, typical	60 MHz	70 MHz	60 MHz	70 MHz	100 MHz
Pulling figure (12 dB return Loss), typical	50 MHz	70 MHz	50 MHz	70 MHz	15 MHz
Pushing figure, +15 V dc supply, typical	6 MHz/V	8 MHz/V	8 MHz/V	8 MHz/V	10 MHz/V
Harmonics below carrier, typical	−25 dB	−25 dB	−15 dB	−25 dB	−20 dB
Spurious output below carrier, minimum	−60 dB	−60 dB	−60 dB	−60 dB	−60 dB
Tuning voltage, typical					
Low frequency	5.5 ± 2 V dc	5.5 ± 2 V dc	8 V dc minimum	5 ± 2.5 V dc	2 ± 1 V dc
High frequency	24+3/−4 V dc	24 ± 3 V dc	28 V dc maximum	24+3/−5 V dc	20 ± 5 V dc
Maximum tuning voltage	+30 V dc	+30 V dc	+30 V dc	+30 V dc	+30 V dc
Tuning port capacitance, nominal	45 pF	45 pF	45 pF	45 pF	26 pF
Phase noise, single sideband, 1 Hz bandwidth, typical					
50 kHz from carrier	−90 dBc	−85 dBc	−85 dBc	−85 dBc	−80 dBc
100 kHz from carrier	−97 dBc	−92 dBc	−92 dBc	−92 dBc	−88 dbc
Input power +1% regulation					
Voltage, nominal	+15 V dc	+15 V dc	+15 V dc	+15 V dc	+15 V dc
Current, maximum	50 mA	50 mA	50 mA	50 mA	100 mA
Case style	TO−8	TO−8	TO−8	TO−8	TO−8

(continued)

TABLE 10.1   (*continued*)

Fixed Tuned Dielectrically Stabilized Oscillators, 3–12 GHz

Frequency range[a]	3000–4499 MHz	4500–7999 MHz	8000–11999 MHz
Power output into 50-Ω Load, minimum	20 mW/+13 dBm	20 mW/+13 dBm	20 mW/+13 dBm
Power output variation over temperature, maximum	3 dB	3 dB	3 dB
Frequency accuracy (under all conditions) maximum[b]	0.1%	0.1%	0.1%
Temperature stability, maximum	±0.05%	±0.05%	±0.05%
Pulling figure (12 dB return loss), maximum	±0.02%	±0.02%	±0.02%
Pushing figure, +15 V dc Supply, maximum	±.001%	±0.001%	±0.001%
Harmonics below carrier, maximum	−20 dBc	−20 dBc	−20 dBc
Spurious output below carrier, maximum	−60 dBc	−60 dBc	−60 dBc
Phase noise, single sideband, 1 Hz bandwidth, typical			
10 kHz from carrier	−100 dBc	−100 dBc	−90 dBc
100 kHz from carrier	−125 dBc	−125 dBc	−115 dBc
Input power			
Voltage	+15 ± .5 V dc	+15 ± .5 V dc	+15 ± .5 V dc
Current, maximum	100 mA	75 mA	150 mA
Case style	OD-60	OD-70	OD-80
Weight, maximum	6.5 oz	4.5 oz	3.0 oz

YIG Oscillators

Frequency range, minimum	2–8 GHz	3–6 GHz	8–20 GHz
Power output, minimum	+14 dBm	+14 dBm	+13 dBm
Power output variation, maximum	±3 dB	±3 dB	±3 dB
Frequency drift over temperature, maximum	15 MHz	10 MHz	30 MHz
Pulling figure (12 dB return loss), typical	1 MHz	1 MHz	1 MHz
Pushing figure			
+15 V dc supply, typical	0.1 MHz/V	0.1 MHz/V	0.1 MHz/V
−5 V dc supply, typical	1 MHz	1 MHz/V	N/A
Magnetic susceptibility at 60 Hz, typical	50 kHz/G	50 kHz/G	50 kHz/G
Second harmonic, minimum at 25°C	−12 dBc	−12 dBc	−10 dBc
Third harmonic, minimum at 25°C	−12 dBc	−12 dBc	−12 dBc
Spurious output minimum	−60 dBc	−60 dBc	−60 dBc
Phase noise			
at 10 kHz offset	−105 dBc/Hz	−108 dBc/Hz	−90 dBc/Hz
at 100 kHz offset	−125 dBc/Hz	−130 dBc/Hz	−107 dBc/Hz
Main coil			
Sensitivity, typical	20 MHz/mA	20 MHz/mA	18 MHz/mA
3 dB bandwidth, typical	5 kHz	5 kHz	5 kHz
Linearity, typical	±0.1%	±0.1%	±0.2%
Hysteresis, typical	6 MHz	3 MHz	12 MHz
Input impedance at 1 kHz, typical	10 Ω/95 mH	10 Ω/95 mH	6 Ω/73 mH
FM coil			
Sensitivity, typical	310 kHz/mA	310 kHz/mA	410 kHz/mA
3 dB bandwidth, typical	400 kHz	400 kHz	400 kHz
Deviation			
at 400 kHz rate, minimum	40 MHz	40 MHz	40 MHz
at 1 MHz rate, minimum	20 MHz	20 MHz	20 MHz

TABLE 10.1   (*continued*)

	1.0 Ω/10 μH	1.0 Ω/10 μH	1.0 Ω/2 μH
Input Impedance at 1 MHz, typical	1.0 Ω/10 μH	1.0 Ω/10 μH	1.0 Ω/2 μH
dc Circuit power			
+15 V dc supply, maximum	100 mA	100 mA	175 mA
−5 V dc supply, maximum	50 mA	50 mA	N/A
YIG heater power			
Input voltage range	+24 ± 4 V dc	+24 ± 4 V dc	+24 ± 4 V dc
Current surge/steady state, maximum	250 mA/25 mA	250 mA/25 mA	250 mA/25 mA
Case style	11–019	11–019	11–002

[a]Center frequencies are customer selectable and may be specified to the MHz. Center frequencies are set at +25°C See page 11−3 for part number selection.
[b]The oscillator will stay within the frequency accuracy of the customer specified frequency under all conditions including the full temperature range, load pulling, frequency pushing, and aging.

10.2   COMPRESSED SMITH CHART

The normal Smith chart is a plot for the reflection coefficient of $|\Gamma| \leq 1$. The compressed Smith chart includes $|\Gamma| > 1$, and the chart is given in Figure 10.2 for $|\Gamma| \leq$ 3.16 (10 dB of return gain). This chart is useful for plotting the variation of S'_{11} and S'_{22} for oscillator design. The impedance and admittance properties of the Smith chart are
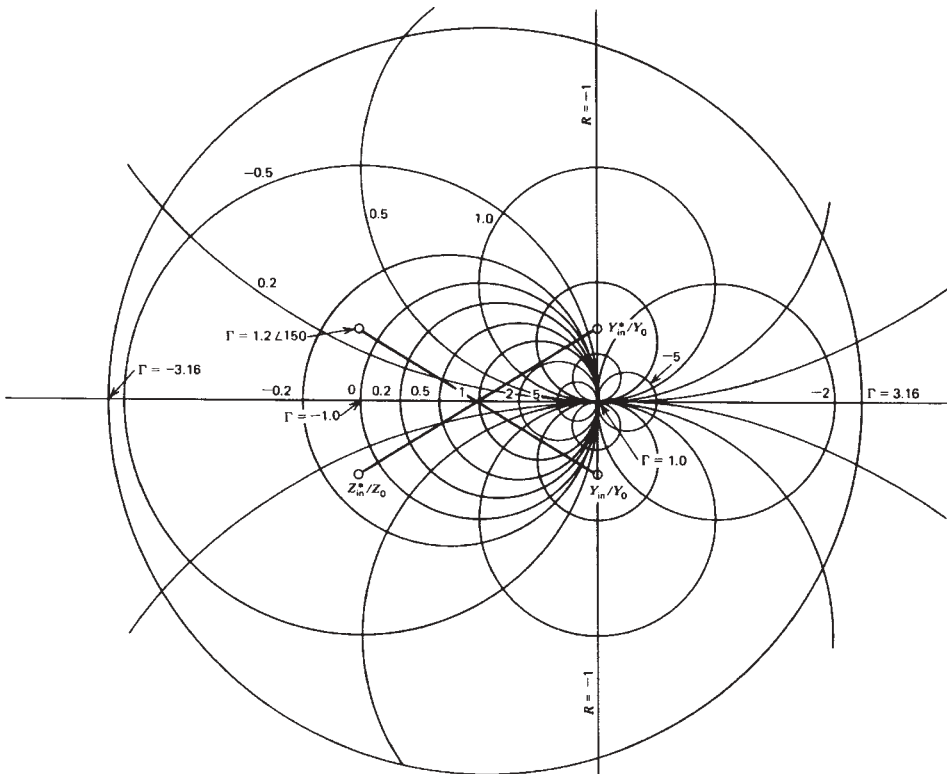
FIGURE 10.2   Compressed Smith chart.

retained for the compressed chart. For example, a Γ_{in} of $1.2\underline{/150°}$ gives the following values of Z and Y normalized to $Z_0 = 50\ \Omega$:

$$\frac{Z_{in}}{Z_0} = -0.10 + j0.25 \qquad \frac{Z_{in}^*}{Z_0} = -0.10 - j0.25$$

$$\frac{Y_{in}}{Y_0} = -1.0 - j3.0 \qquad \frac{Y_{in}^*}{Y_0} = -1.0 + j3.0$$

These values are plotted in Figure 10.2 for illustration.

A frequency resonance condition simply requires the circuit imaginary term be zero. If the impedance resonance is on the left-hand real axis, this is a series resonance; that is, at frequencies above resonance the impedance is inductive and below resonance the impedance is capacitive. If the impedance resonance is on the right-hand real axis, the resonance is a parallel resonance; that is, at frequencies above resonance the impedance is capacitive and below resonance the impedance is inductive.

An oscillator resonance condition implies that both the circuit imaginary term and the circuit real term are zero, as given by (10.9) and (10.10). Impedances and admittances can be transformed on the compressed Smith chart by the methods discussed in Chapter 5; however, when $|\Gamma|$ is greater than unity, the goal of impedance transformation is usually to achieve either a series or a parallel resonance condition. Another method for visualizing negative resistance is to plot $1/S_{11}$ and multiply the result by -1. This allows the designer to use readily available Smith charts, with $|\Gamma| \le 1$, to analyze circuits with $|\Gamma| \ge 1$. The proof of this concept can be shown by expressing the reflection coefficient of a one-port by

$$S_{11} = \frac{Z_s - Z_0}{Z_s + Z_0} \tag{10.13}$$

$$\frac{1}{S_{11}} = \frac{Z_s + Z_0}{Z_s - Z_0} = \frac{Z_1 - Z_0}{Z_1 + Z_0} \tag{10.14}$$

where $Z_1 = -Z_s$, which gives a negative resistance on Smith chart coordinates. For example, using the case in Figure 10.2,

$$S_{11} = 1.2\ \underline{/150°}$$

$$\frac{1}{S_{11}} = 0.833\ \underline{/-150°}$$

$$\frac{Z_1}{Z_0} = 0.10 - j0.25$$

$$\frac{Z_s}{Z_0} = -0.10 + j0.25$$

The impedance of the one-port is plotted at Z_1 but understood to be Z_s.

10.3   SERIES OR PARALLEL RESONANCE

Oscillators can be classified into two types, series resonant or parallel resonant, as shown in Figure 10.3. The equivalent circuit of the active device is chosen from the
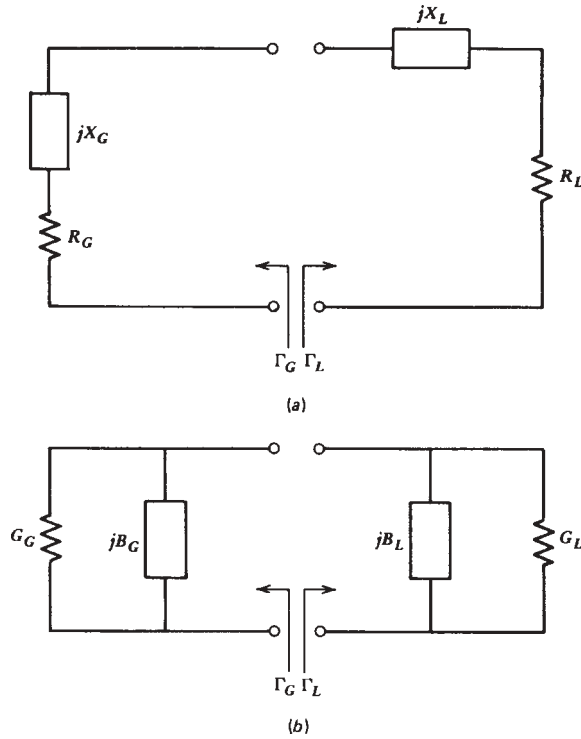
FIGURE 10.3 Oscillator equivalent circuits: (*a*) series resonant; (*b*) parallel resonant.

frequency response of the output port, that is, the frequency response of Γ_G. For the series resonant condition, the negative resistance of the active device must exceed the load resistance R_L at startup of oscillation by about 20%. As the oscillation builds up to a steady-state value, the resonance condition will be reached as a result of limiting effects, which cause a reduction of R_G under large-signal drive.

For startup of oscillation

$$|R_G| > 1.2R_L \tag{10.15}$$

for resonance

$$R_G + R_L = 0 \tag{10.16}$$

$$X_G + X_L = 0 \tag{10.17}$$

For the parallel resonant condition, the negative conductance of the active device must exceed the load conductance G_L at startup of oscillation by about 20%. The parallel resonant oscillator is simply the dual of the series resonant case. For startup of oscillation

$$|G_G| > 1.2G_L \tag{10.18}$$

For resonance

$$G_G + G_L = 0 \tag{10.19}$$

$$B_G + B_L = 0 \tag{10.20}$$

To design the oscillator for series resonance, the reflection coefficient of the active transistor is moved to an angle of $180°$ (i.e., the left-hand real axis of the compressed Smith chart). Keeping in mind (10.2) for the input resonating port, we see that a nearly lossless reactance will resonate the transistor. For the example in Figure 10.2,

$$\Gamma = 1.2 \ \underline{/150°} = S'_{11}$$

$$\Gamma_G = 0.83 \ \underline{/-150°} \simeq 1.0 \ \underline{/-150°}$$

The large-signal drive of the transistor will reduce S'_{11} to about $1.0 \underline{/150°}$. For parallel resonance oscillator design, the reflection coefficient of the active transistor is moved to an angle of $0°$ (i.e., the right-hand real axis of the compressed Smith chart). Alternatively, the reflection coefficient associated with impedance can be inverted to an admittance point, and the admittance can be moved to an angle of $180°$ (i.e., the left-hand real axis of the compressed Smith chart).

10.4   RESONATORS

Oscillators are often named by the type of resonator connected to the tuning port to give the desired Γ_G. The most common resonators are:

1. Lumped element
2. Distributed transmission line (microstripline or coaxial line)
3. Cavity
4. Dielectric resonator
5. Varactor
6. Ceramic resonators
7. Yttrium iron garnet (YIG)

All of these structures can be made to have low losses and high Q. The first four types give a fixed-tuned or mechanically tuned oscillator. The YIG or varactor resonator will give a wide-band tunable oscillator. For a high-Q resonator (>50), the reflection coefficient is simply the outer boundary of the Smith chart, with a phase depending on the transmission line length between the resonator and the active two-port device.

The lumped-element resonators are high-Q capacitors and inductors with associated parasitics. For example, a high-Q chip capacitor 0.050 in. in length has a typical parasitic inductance of 0.5 nH.

The distributed elements using microstripline are usually either open or shorted transmission lines of the correct length to give the proper angle to Γ_G. Other planar microstrip structures to consider are [10.12]:

1. Rectangular $\lambda/2$ microstripline
2. Circular disk
3. Circular microstrip ring

4. Triangular microstrip
5. Hexagonal microstrip
6. Elliptic microstrip
7. Coplanar waveguide resonators

All of these resonators can be made high Q on low-loss dielectric substrates.

Cavity resonators can be made from low-loss coaxial line or waveguide. The simplest coaxial cavity is a $\lambda/4$ shorted stub, where the output is coupled by a shorted loop (magnetic coupling) or an open probe (electric coupling). A mechanical tuning screw near the open-circuit end can be used to shorten the line and therefore raise the resonant frequency.

The lowest order rectangular waveguide cavity resonator is the TE_{101} mode, where the width and length of the cavity are $\lambda_g/2$ at the resonant frequency. Circular or elliptic waveguides can also be used as a cavity resonator.

10.4.1 Dielectric Resonators

A very popular low-cost resonator is the dielectric puck made from (Zr-Sn) Ti_2O_5 or $Ba_4 Ti_2O_5$ ($\varepsilon_r = 39.6$) coupled to a microstrip structure, as shown in Figure 10.4. The lowest order resonant mode is the $TE_{01\delta}$ mode, which easily couples to the microstrip TEM mode. To use dielectric resonators effectively in microwave circuits, it is necessary to have an accurate knowledge of the coupling between the resonator and various transmission lines. Figure 10.4 shows the magnetic coupling between a dielectric resonator and a microstrip. A dielectric spacer may be added under the puck to improve the loaded Q by optimizing the coupling. The resonator is placed on top of the microstrip substrate. The lateral distance between the resonator and the microstrip conductor primarily determines the amount of coupling between the resonator and the microstrip transmission line. Metallic shielding is required to minimize the radiation losses.

The $TE_{01\delta}$ mode in a dielectric resonator on top of a dielectric spacer can be approximated by a magnetic dipole of moment M. The coupling between the line and the resonator is accomplished by orienting the magnetic moment of the resonator perpendicular to the microstrip plane so that the magnetic lines of the resonator link with those of the microstripline, as shown in Figure 10.4. The dielectric resonator placed adjacent to the microstripline operates like a reaction cavity that reflects the RF energy
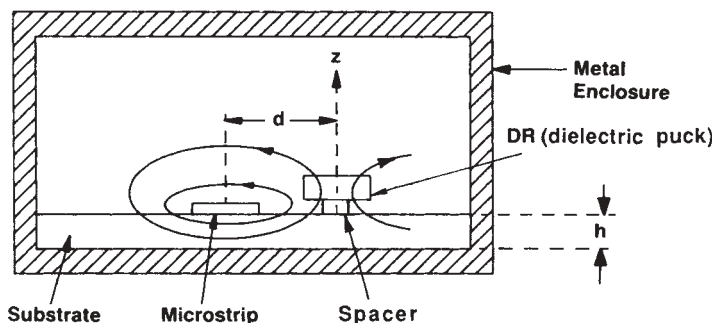
FIGURE 10.4   Coupling between a microstrip line and a dielectric resonator.
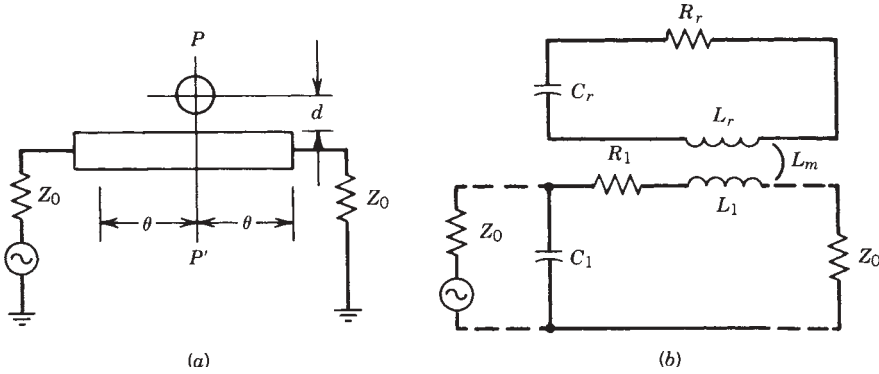
FIGURE 10.5   Equivalent circuit of the dielectric resonator coupled with a microstripline.

at the resonant frequency. It is similar to an open circuit with a voltage maximum at the reference plane at the resonant frequency. The equivalent circuit of the resonator coupled to a microstripline is shown in Figure 10.5, where L_r, C_r, and R_r are the equivalent parameters of the dielectric resonator; L_1, C_1, and R_1 are the equivalent parameters of the microstripline; and L_m characterizes the magnetic coupling. The transformed resonator impedance Z in series with the transmission line is given by

$$Z = j\omega L_1 + \frac{\omega^2 L_m^2}{R_r + j\omega(L_r - 1/\omega^2 C_r)} \tag{10.21}$$

Near resonance, ωL_1 can be neglected and Z becomes

$$Z = \omega Q_u \frac{L_m^2}{L_r} \frac{1}{1 + jX} \tag{10.22}$$

where $X = 2Q_u(\Delta\omega/\omega)$ and unloaded Q and the resonant frequency of the resonator are given by

$$Q_u = \frac{\omega_0 L_r}{R_r} \tag{10.23}$$

$$\omega_0 = \frac{1}{\sqrt{L_r \, C_r}} \tag{10.24}$$

At resonance, $X = 0$ and

$$Z = R = \omega_0 Q_u \frac{L_m^2}{L_r} \tag{10.25}$$

Equation (10.25) indicates that the circuit shown in Figure 10.5 can be represented by the parallel tuned circuit shown in Figure 10.6, where L, R, and C are given by

$$L = \frac{L_m^2}{L_r} \tag{10.26}$$
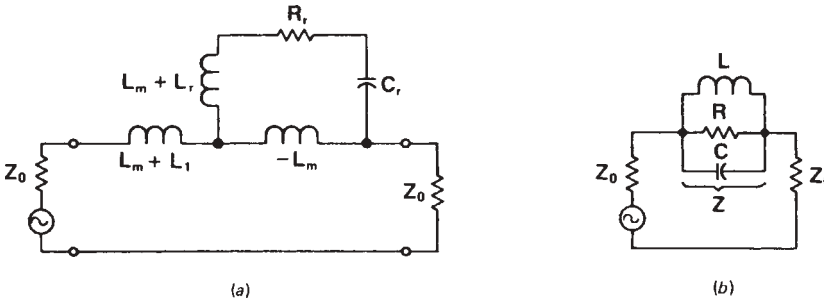
FIGURE 10.6 (*a*) Simplified equivalent circuit; (*b*) final equivalent circuit of a dielectric resonator coupled with a microstrip line.

Khanna (1982)
97 dBc/Hz (10 kHz),
8.5

Abe et al.(1979)
86 dBc/Hz (10 kHz), 6 GHz

Saito et al.(1979)
94 dBc/Hz (10 kHz), 6 GHz

Sone (1978) NEC
91 dBc/Hz (10 kHz), 6 GHz

Khanna (1984)
97 dBc/Hz (10 kHz),7.2 GHz

O.Ishihara et al.
(1980), Mitsubishi
94 dBc/Hz (10 kHz), 12 GHz

S.Fiedziuszko (1985)
100 dBc/Hz (10 kHz), 7.2 GHz
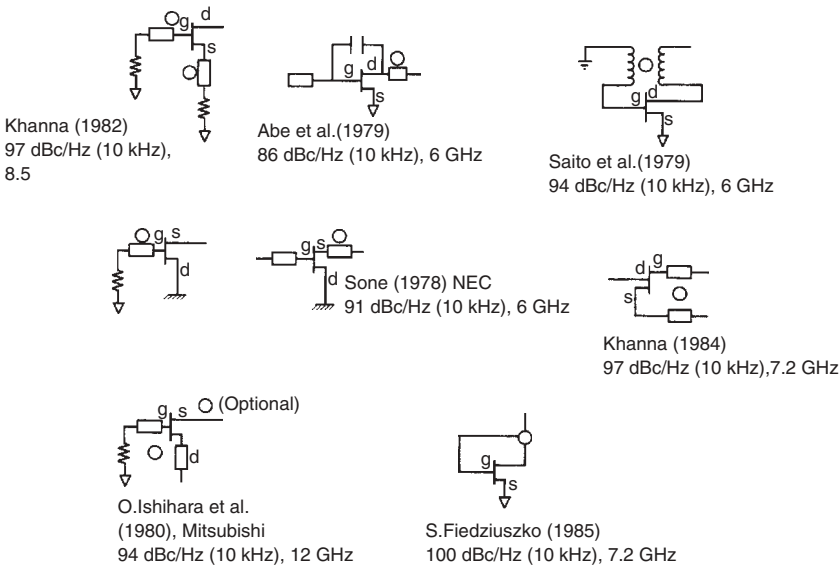
FIGURE 10.7 Recommended methods of frequency stabilization for dielectric resonator oscillators (DROs).

$$C = \frac{L_r}{\omega_0^2 L_m^2} \tag{10.27}$$

$$R = \omega_0 Q_u \frac{L_m^2}{L_r} \tag{10.28}$$

The coupling coefficient β at the resonant frequency ω_0 is defined by

$$\beta = \frac{R}{R_{\text{ext}}} = \frac{R}{2Z_0} = \frac{\omega_0 Q_u}{2Z_0} \frac{L_m^2}{L_r} \tag{10.29}$$

If S_{110} and S_{210} are defined as the reflection and transmission coefficients at the resonant frequency of the resonator coupled to the microstrip, β can be shown to be given

by [10.13]

$$\beta = \frac{S_{110}}{1 - S_{110}} = \frac{1 - S_{210}}{S_{210}} = \frac{S_{110}}{S_{210}} \tag{10.30}$$

This relation can be used to determine the coupling coefficient from the directly measurable reflection and transmission coefficients. The value of β can also be accurately calculated from a knowledge of the circuit configuration. The quantity L_m^2/L_r in (10.26) is a strong function of the distance between the resonator and the microstripline for given shielding conditions and substrate thickness and dielectric constant. The relation between different quality factors is well known and is given by

$$Q_u = Q_L(1 + \beta) = Q_e\beta \tag{10.31}$$

The external quality factor Q_e is used to characterize the load coupling.

The S parameters of the dielectric resonator coupled to a microstrip with the lengths of transmission lines on input and output, as shown in Figure 10.5, can be determined from the previous relations and are given by [10.14]

$$S = \begin{bmatrix} \dfrac{\beta}{\beta + 1 + jQ_u\Delta\omega/\omega_0}e^{-2j\theta} & \dfrac{1 + jQ_u\Delta\omega/\omega_0}{\beta + 1 + jQ_u\Delta\omega/\omega_0}e^{-2j\theta} \\ \dfrac{1 + jQ_u\Delta\omega/\omega_0}{\beta + 1 + jQ_u\Delta\omega/\omega_0}e^{-2j\theta} & \dfrac{\beta}{\beta + 1 + jQ_u\Delta\omega/\omega_0}e^{-2j\theta} \end{bmatrix} \tag{10.32}$$

where 2θ is the electrical line length between the input and output planes.

Figure 10.6 shows a simplified equivalent circuit arrangement for a dielectric resonator. Figure 10.7 shows recommended methods of how to use dielectric resonators in oscillators. Figure 10.8 shows the physical dimensions of a dielectric resonator (DR) used in a simulator. The relationship between these various and physical locations is shown in Figures 10.8a and 10.8b. An actual circuit using a DR is shown in Figure 10.9 and its selected phase noise is shown in Figure 10.10.

10.4.2 YIG Resonators

For wide-band electrically tunable oscillators, we use either a YIG or a varactor resonator. The YIG resonator is a high-Q, ferrite sphere of yttrium iron garnet, $Y_2Fe_2(FeO_4)_3$, that can be tuned over a wide band by varying the biasing dc magnetic field. Its high performance and convenient size for applications in microwave integrated circuits make it an excellent choice in a large number of applications, such as filters, multipliers, discriminators, limiters, and oscillators. A YIG resonator makes use of the ferrimagnetic resonance, which, depending on the material composition, size, and applied field, can be achieved from 500 MHz to 50 GHz [10.15]. An unloaded Q greater than 1000 is usually achieved with typical YIG material.

Figure 10.11 shows the mechanical drawing of a YIG oscillator assembly. The drawing is somewhat simplified and the actual construction is actually more difficult to do. Its circuit diagram is shown in Figure 10.12. A schematic for a YIG oscillator is shown in Figure 10.13 and its selected phase noise using a bipolar transistor is shown in Figure 10.14. Figure 10.15 shows a phase noise comparison of different types of oscillators, and Figure 10.16 shows the normalized phase noise as a function of frequencies and semiconductor type.
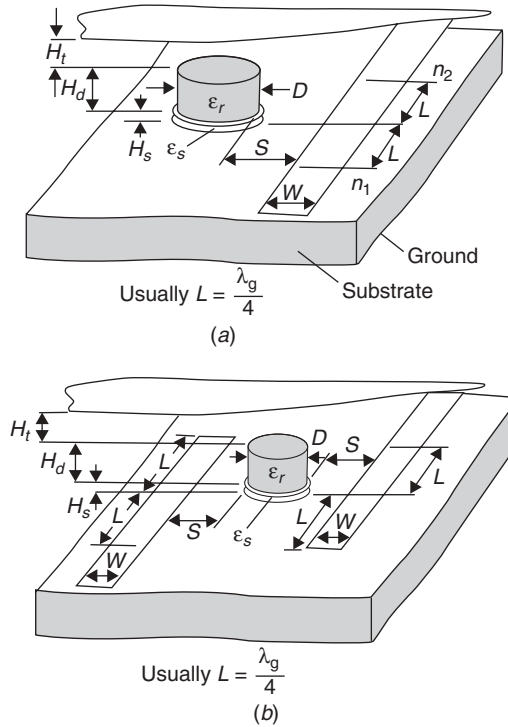
FIGURE 10.8 DRO on microstrip as (*a*) band-stop filter and (*b*) bandpass filter.
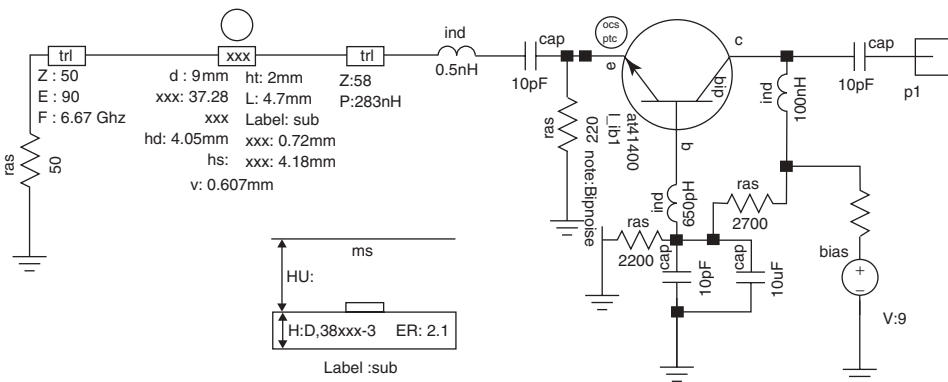
FIGURE 10.9 Typical circuit for a dielectric resonator–based oscillator at about 6.6 MHz as well as mechanical dimensions of resonator assembly.

10.4.3 Varactor Resonators

The dual of the current-tuned YIG resonator is the voltage-tuned varactor, which is a variable reactance achieved from a low-loss, reverse-biased semiconductor *pn* junction. These diodes are designed to have very low loss and therefore high *Q*. The silicon varactors have the fastest settling time in fast-tuning applications, but the gallium
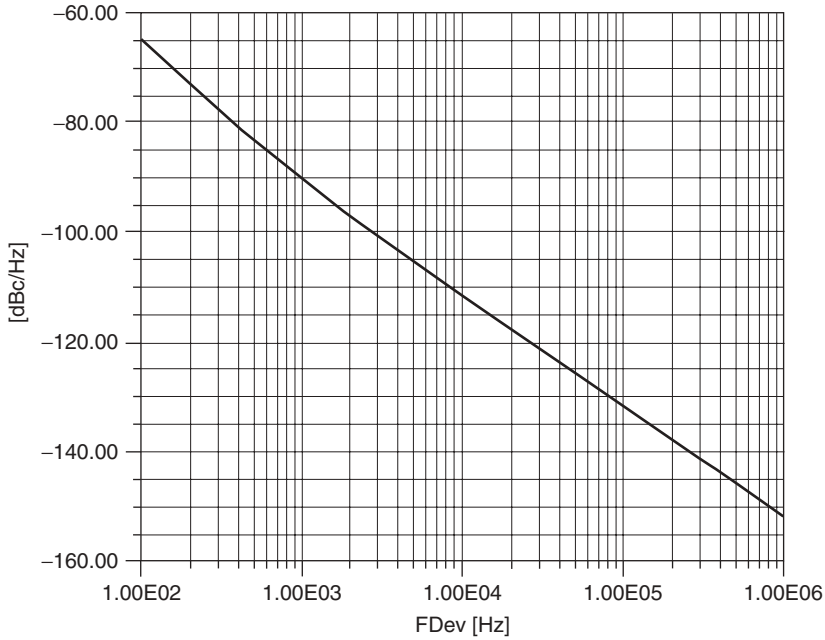
FIGURE 10.10   Predicted phase noise of DRO shown Figure 10.9. Note the bend in the curve due to the flicker noise component.
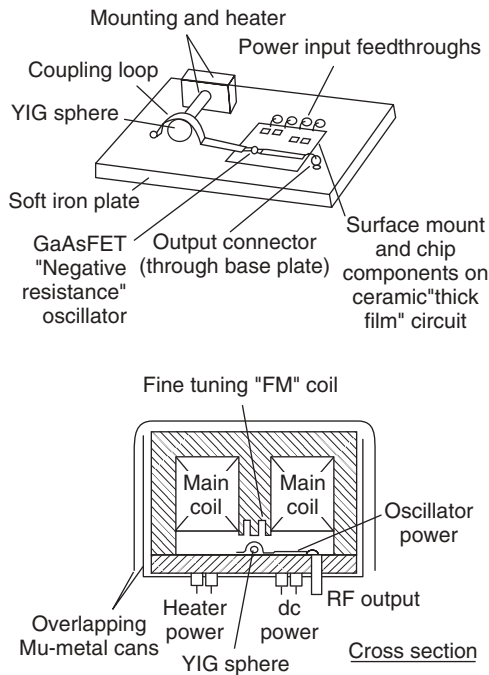
FIGURE 10.11   YIG sphere serves as the resonator in the sweep oscillators used in many spectrum analyzers.
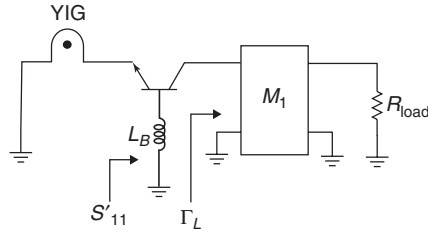
FIGURE 10.12   Circuit diagram for YIG-tuned oscillator depicted in Figure 10.11.
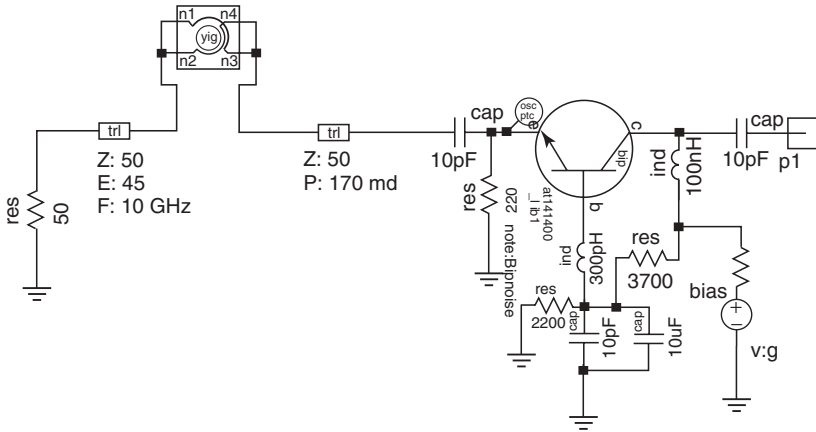
FIGURE 10.13   Schematic for a 10-GHz YIG oscillator using the YIG model in Serenade. The equivalent parameters for this parallel resonant circuit are 422 pH and 0.6 pF. The transformer ratio is 0.1.
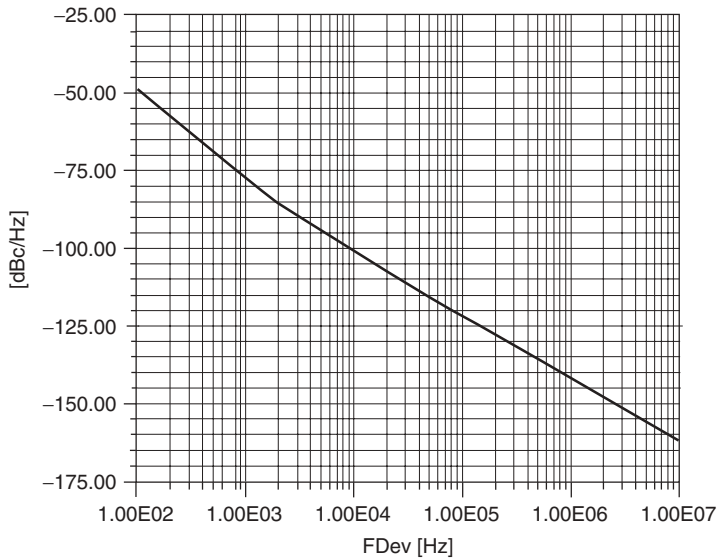
FIGURE 10.14   Predicted phase noise at 10 GHz for oscillator shown in Figure 10.13. Again, note the influence of the flicker corner frequency.
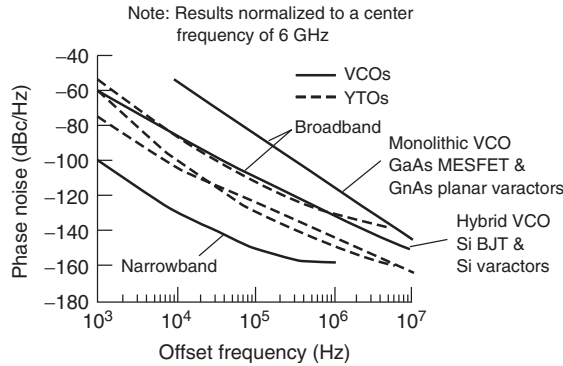
FIGURE 10.15 Phase noise comparison of different YIG and varactor-tuned oscillators.
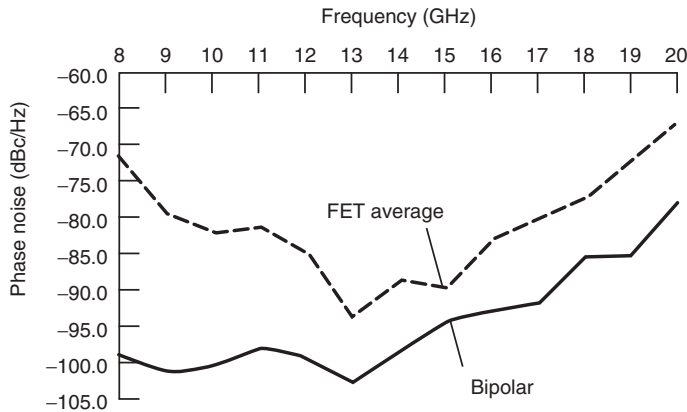
FIGURE 10.16 Phase noise at 10 kHz off the carrier of silicon bipolar transistors versus FETs.

arsenide varactors have higher Q values. The cutoff frequency of the varactor is defined as the frequency where $Q_v = 1$. For a simple series RC equivalent circuit, we have

$$Q_v = \frac{1}{\omega R C_v} \tag{10.33}$$

$$f_{c0} = \frac{1}{2\pi R C_v} \tag{10.34}$$

The tuning range of the varactor will be determined by the capacitance ratio C_{max}/C_{min}, which can be 12 or higher for hyperabrupt varactors. Since R is a function of bias, the maximum cutoff frequency occurs at a bias near breakdown, where both R and C_v have minimum values. Tuning diodes or GaAs varactors for microwave and millimeter-wave applications are frequently obtained by using a GaAs FET and connecting source and drain together. Figure 10.17 shows the dynamic capacitance and dynamic resistors as a function of tuning voltage. In using a transistor instead of a diode, the parameters become more complicated. Figure 10.18 shows the capacitance,
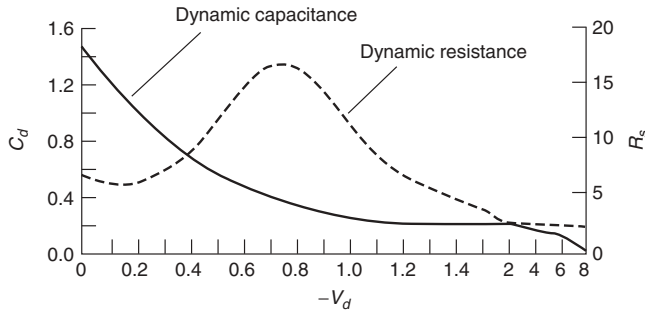
FIGURE 10.17 Dynamic capacitance and dynamic resistance as a function of tuning voltage for a GaAs varactor.
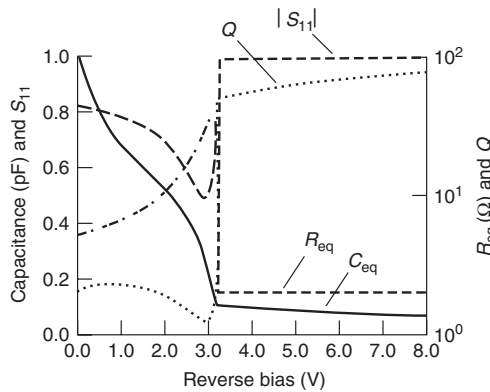
FIGURE 10.18 Varactor parameters: capacitance, equivalent resistance, and Q, as well as the magnitude of S_{11} as a function of reverse voltage.

equivalent resistor, and Q as well as the magnitude of S_{11} as a function of reverse voltage. This is due to the breakdown effects of the GaAs FET.

10.4.4 Ceramic Resonators

An important application for a new class of resonators called ceramic resonators (CRs) has emerged for wireless applications. The CRs are similar to ridged coaxial cable, where the center controller is connected at the end to the outside of the cable. These resonators are generally operating in quarter-wavelength mode and their characteristic impedance is approximately 10 Ω. Because their coaxial assemblies are made for a high-ε, low-loss material with good silver plating throughout, the electromagnetic field is internally contained and therefore provides very little radiation. These resonators are therefore ideally suited for high-Q, high-density oscillators. The typical application for this resonator is VCOs ranging from not much more than 200 MHz up to about 3 or 4 GHz. At these high frequencies, the mechanical dimensions of the resonator become too tiny to offer any advantage. One of the principal requirements is that the physical length is considerably larger than the diameter. If the frequency increases, this can no longer be maintained.

Calculation of Equivalent Circuit   The equivalent parallel resonant circuit has a resistance at resonant frequency of

$$R_p = \frac{2(Z_0)^2}{R^* l}$$

where Z_0 = characteristic impedance of the resonator
l = mechanical length of the resonator
R^* = equivalent resistor due to metalization and other losses

As an example, one can calculate

$$C^* = \frac{2\pi \varepsilon_0 \varepsilon_r}{\log_e (D/d)} = 55.61 \times 10^{-12} \frac{\varepsilon_r}{\log_e (D/d)} \tag{10.35}$$

and

$$L^* = \frac{\mu_r \mu_0}{2\pi} = \log_e \left(\frac{D}{d}\right) = 2 \times 10^{-7} \log_e \left(\frac{D}{d}\right) \tag{10.36}$$

$$Z_0 = 60\ \Omega \frac{1}{\sqrt{\varepsilon_r}} \log_e \left(\frac{D}{d}\right) \tag{10.37}$$

A practical example for $\varepsilon_r = 88$ and 450 MHz is

$$C_p = \frac{C^* l}{2} = 49.7\ \text{pF} \tag{10.38}$$

$$L_p = 8L^* l = 2.52\ \text{nH} \tag{10.39}$$

$$R_p = 2.5\ \text{k}\Omega \tag{10.40}$$

Manufacturers supply these resonators on a prefabricated basis. Figure 10.19 shows the standard round/square packaging available and the typical dimensions for a ceramic resonator.

The available material has a dielectric constant of 88 and is recommended for use in the 400- to 1500-MHz range. The next higher frequency range (800 MHz to 2.5 GHz) uses an ε of 38, while the top range (1 to 4.5 GHz) uses an ε of 21. Given the fact that ceramic resonators are prefabricated and have standard outside dimensions, the following quick calculation applies:

	$\varepsilon_r = 21$	$\varepsilon_r = 38$	$\varepsilon_r = 88$
Relative dielectric constant of resonator material			
Resonator length, mm	$l = \dfrac{16.6}{f}$	$l = \dfrac{12.6}{f}$	$l = \dfrac{8.2}{f}$
Temperature coefficient, ppm/°C	10	6.5	8.5
Available temperature coefficients	−3 to +12	−3 to +12	−3 to +12
Typical resonator Q	800	500	400
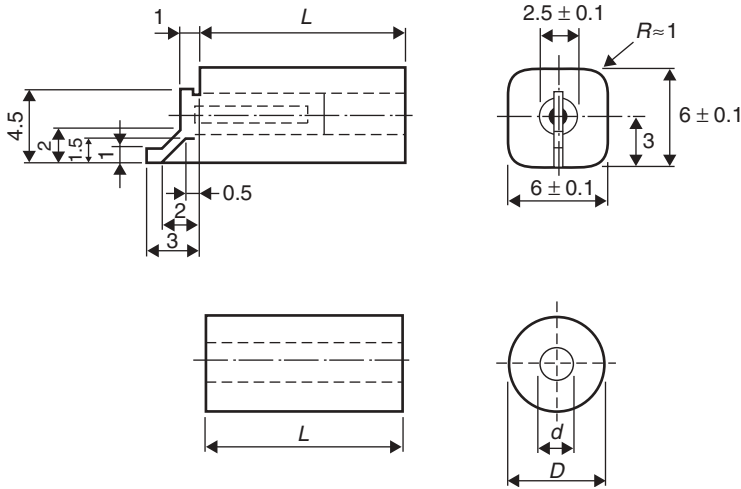
FIGURE 10.19   Standard round/square packaging.
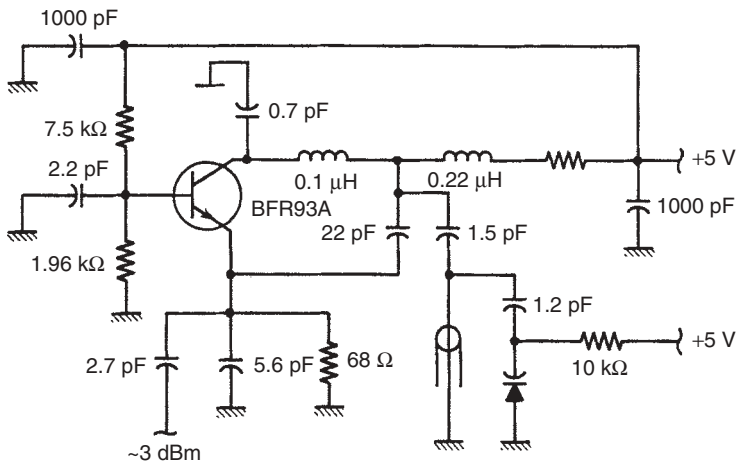
FIGURE 10.20   Schematic of ceramic resonator-based oscillator.

Figure 10.20 shows the schematic of such an oscillator. Figures 10.21 and 10.22 show the simulated and measured phase noise of the ceramic resonator-based oscillator.

By using ceramic resonator-based oscillators in conjunction with miniature synthesizer chips, it is possible to build extremely small phase-locked loop (PLL) systems for cellular telephone operation. Figure 10.23 shows one of the smallest currently available PLL-based synthesizers manufactured by Synergy Microwave Corporation. Because of the high-Q resonator, these types of oscillators exhibit extremely low phase noise. Values of better than 150 dB/Hz, 1 MHz off the carrier, are achievable. The ceramic resonator reduces the sensitivity toward microphonic effects and proximity effects caused by other components.
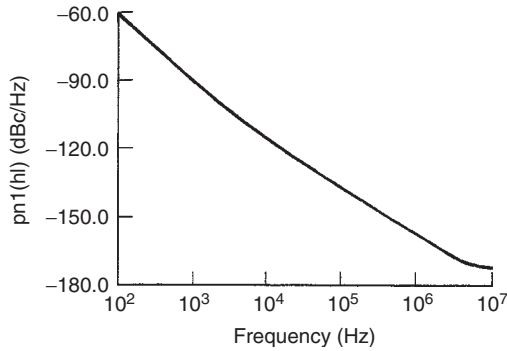
FIGURE 10.21   Simulated phase noise of an *npn* bipolar 1-GHz ceramic resonator–based oscillator.
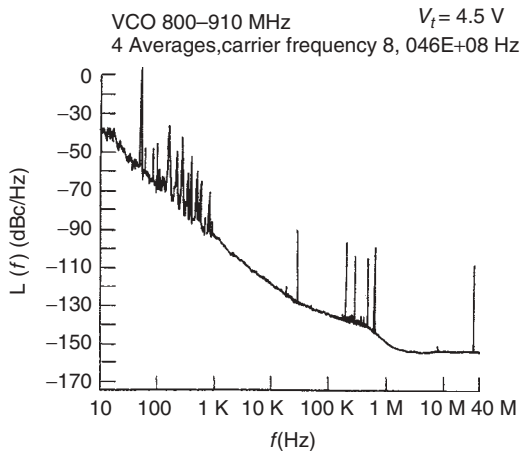
FIGURE 10.22   Measured phase noise of a ceramic resonator-based oscillator.

10.4.5   Resonator Measurements

Accurate characterization of microwave resonators is essential for their effective use. The important parameters that are required to fully describe a resonator for a given mode are the resonant frequency f_0, the coupling coefficient, and the quality factors Q_u (unloaded Q), Q_L (loaded Q), and Q_e (external Q due to resistive loading). The network analyzer displays the magnitude and phase of the reflection and transmission coefficients for the single-port resonator. Many methods for Q measurement are possible, but we will describe here only one simple technique using Q loci on the Smith chart.

The single-ended resonator is the most commonly used configuration for microwave resonant circuits. The parallel-tuned circuit is known as the detuned short configuration, and the series-tuned circuit is known as the detuned open configuration. Either configuration can be converted to the other by displacing the reference plane by a quarter wavelength. The important parameters of these resonant circuits are defined in Table 10.2.
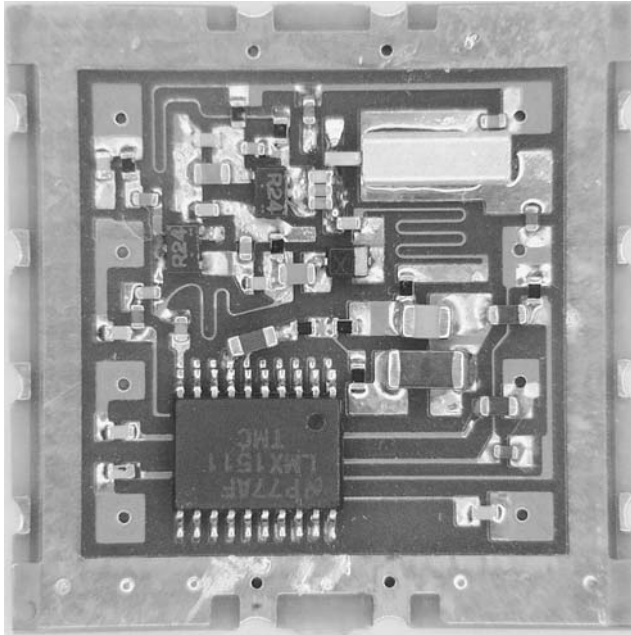
FIGURE 10.23 Miniature PLL-based synthesizer manufactured by Synergy Microwave Corporation.

TABLE 10.2   Physical Dimensions of DR

```
BLK

DRMS 1 2 D=6.12e-3 HD-2.45e-3 ER=38 HT=1.5e-3 S=.5e-3;
        + W=1.1e-3 L=4e-3 SRD=1e-4 BPF SUB;
        trf 2 0 0 3 N=1
        pug: 2POR 1 3
END
DATA
        SUB: MS er=2.4 h=0.380e-3 met1=cu 3.175e-6
        and=0.0001
END
```

Since analysis of the resonant circuits is similar for the two configurations, we restrict our discussion to the parallel-tuned circuit. The input impedance of the parallel resonant structure can be written

$$\frac{1}{Z_{\text{in}}} = \frac{1}{R} + \frac{1}{j\omega L} + j\omega C \tag{10.41}$$

or

$$Z_{\text{in}} = \frac{R}{1 + 2jQ_u\delta} \tag{10.42}$$

where $\delta = (\omega - \omega_0)/\omega_0$ represents the frequency-detuning parameter.

TABLE 10.3   Resonator Parameters

Parameter	Series Tuned	Parallel Tuned
f_0	$\dfrac{1}{\sqrt{LC}}$	$\dfrac{1}{\sqrt{LC}}$
Q_u	$\dfrac{\omega L}{R}$	$\dfrac{R}{\omega L}$
$\beta = \dfrac{Q_u}{Q_e}$	$\dfrac{Z_0}{R}$	$\dfrac{R}{Z_0}$
Q_L	$\dfrac{Q_u}{1+\beta}$	$\dfrac{Q_u}{1+\beta}$

The locus of the impedance, using (10.42), can be drawn by varying frequency. As impedance is a linear function of frequency, a circular locus will be produced when plotted on the Smith chart, as illustrated by circles A, B, and C in Figure 10.24. Circle A, for which $R \simeq Z_0$ passes near the origin, is called the condition of critical coupling ($\beta = 1$ from Table 10.3) since it provides a perfect match to the transmission line at resonance. Circle C, with $R > Z_0$, is said to be overcoupled ($\beta > 1$), and circle B, with $R < Z_0$, is undercoupled. The coupled coefficient for any given impedance locus can be easily determined by measuring the reflection coefficient S_{110} at resonance.

For the undercoupled case,

$$\beta = \frac{1 - S_{110}}{1 + S_{110}} \tag{10.43}$$

and for the overcoupled case,

$$\beta = \frac{1 + S_{110}}{1 - S_{110}} \tag{10.44}$$

The evaluation of β locates the intersection of the impedance circle with the real axis, as shown in Figure 10.25. To measure various quality factors, (10.42) can be written
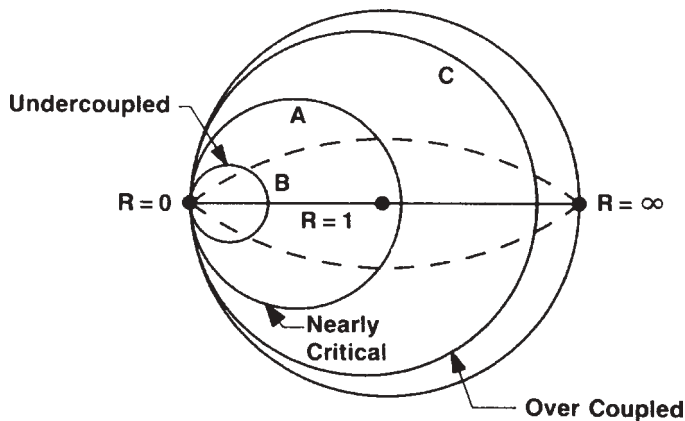
FIGURE 10.24   Input impedance of a resonant cavity referred to the detuned-short position plotted on the Smith chart for three degrees of coupling.
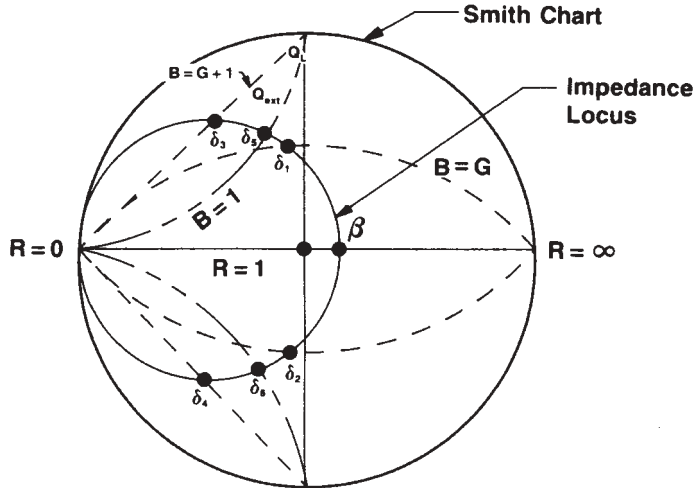
FIGURE 10.25 Identification of the half-power points from the Smith chart: Q_u locus given by $B = G$ $(X = R)$; Q_L by $B = G + 1$; Q_e by $B = 1$.

as

$$\overline{Z}_{\text{in}} = \frac{Z_{\text{in}}}{Z_0} = \frac{\beta}{1 + 2jQ_u\delta} = \frac{\beta}{1 + 2jQ_L(1 + \beta)\delta} = \frac{\beta}{1 + 2jQ_e\beta\delta} \qquad (10.45)$$

where Q_u, Q_L, and Q_e are interrelated by the well-known relation

$$Q_u = Q_L(1 + \beta) = Q_e\beta \qquad (10.46)$$

The normalized frequency deviations corresponding to various quality factors are given by

$$\delta_u = \pm\frac{1}{2Q_u} \qquad \delta_L = \pm\frac{1}{2Q_L} \qquad \delta_e = \pm\frac{1}{2Q_e} \qquad (10.47)$$

The impedance locus of Q_u, for example, can be determined by using (10.47) in (10.45) and is given by

$$(Z_{\text{in}})_u = \frac{\beta}{1 \pm j} \qquad (10.48)$$

Equation (10.48) represents the points on the impedance locus where the real and imaginary parts of the impedance are the same. Figure 10.25 represents the locus of these points (corresponding to $B = G$) for all possible values of B. This locus is an arc whose center is at $Z = 0 \pm j$, and the radius is the distance to the point $0 \pm j0$. The intersection of this arc with the impedance locus determines the Q_u measurement points,

$$Q_u = \frac{f_0}{f_1 - f_2} \qquad (10.49)$$

The frequencies f_1 and f_2 are called half-power points because these points correspond to $R = X$ on the impedance locus or $B = G$ on the admittance locus.

The loaded and external Q values can be determined in a similar way. The impedances corresponding to Q_e and Q_L are

$$(Z_{\text{in}})_e = \frac{\beta}{1 \pm j\beta} \tag{10.50}$$

and

$$(Z_{\text{in}})_L = \frac{\beta}{1 \pm j(1 + \beta)} \tag{10.51}$$

Using (10.50) and (10.51), the Q_e and Q_L loci can be easily determined. These loci are shown in Figure 10.25.

10.5 TWO-PORT OSCILLATOR DESIGN

A common method for designing oscillators is to resonate the input port with a passive high-Q circuit at the desired frequency of resonance. It will be shown that if this is achieved with a load connected on the output port, the transistor is oscillating at both ports and is thus delivering power to the load port. The oscillator may be considered a two-port structure as shown in Figure 1.1, where M_3 is the lossless resonating port and M_4 provides lossless matching such that all of the external RF power is delivered to the load. The resonating network has been described in Section 10.4. Normally, only parasitic resistance is present at the resonating port, since a high-Q resonance is desirable for minimizing oscillator noise. It is possible to have loads at both the input and the output ports if such an application occurs, since the oscillator is oscillating at both ports simultaneously.

The simultaneous oscillation condition is proved as follows. Assume that the oscillation condition is satisfied at port 1:

$$\frac{1}{S'_{11}} = \Gamma_G \tag{10.52}$$

From (1.125),

$$S'_{11} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{S_{11} - D\Gamma_L}{1 - S_{22}\Gamma_L} \tag{10.53}$$

$$\frac{1}{S'_{11}} = \frac{1 - S_{22}\Gamma_L}{S_{11} - D\Gamma_L} = \Gamma_G \tag{10.54}$$

By expanding (10.48), we get

$$\Gamma_G S_{11} - D\Gamma_L \Gamma_G = 1 - S_{22}\Gamma_L$$

$$\Gamma_L(S_{22} - D\Gamma_G) = 1 - S_{11}\Gamma_G$$

$$\Gamma_L = \frac{1 - S_{11}\Gamma_G}{S_{22} - D\Gamma_G} \tag{10.55}$$

From (1.126),

$$S'_{22} = S_{22} + \frac{S_{12}S_{21}\Gamma_G}{1 - S_{11}\Gamma_G} = \frac{S_{22} - D\Gamma_G}{1 - S_{11}\Gamma_G} \tag{10.56}$$

$$\frac{1}{S'_{22}} = \frac{1 - S_{11}\Gamma_G}{S_{22} - D\Gamma_G} \tag{10.57}$$

Comparing (10.55) and (10.57) gives

$$\frac{1}{S'_{22}} = \Gamma_L \tag{10.58}$$

which means that the oscillation condition is also satisfied at port 2; this completes the proof. Thus, if either port is oscillating, the other port must be oscillating as well. A load may appear at either or both ports, but normally the load is in Γ_L, the output termination. This result can be generalized to an n-port oscillator by showing that the oscillator is simultaneously oscillating at each port [10.2, 10.12]:

$$\Gamma_1 S'_{11} = \Gamma_2 S'_{22} = \Gamma_3 S'_{33} = \cdots = \Gamma_n S'_{nn} \tag{10.59}$$

Before concluding this section on two-port oscillator design, the buffered oscillator shown in Figure 10.26 must be considered. This design approach is used to provide the following:

1. A reduction in loading–pulling, which is the change in oscillator frequency when the load reflection coefficient changes
2. A load impedance that is more suitable to wide-band applications [10.1]
3. A higher output power from a working design, although the higher output power can also be achieved by using a larger oscillator transistor

Buffered oscillator designs are quite common in wide-band YIG applications, where changes in the load impedance must not change the generator frequency.
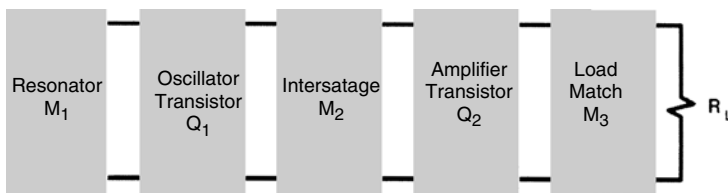
Decouples Resonator from Load Variations

Similar Devices for Q_1 and Q_2

$P_{OUT}\ Q_2 > P_{OUT}\ Q_1$

FIGURE 10.26   Buffered oscillator design.

Two-port oscillator design may be summarized as follows:

1. Select a transistor with sufficient gain and output power capability for the frequency of operation. This may be based on oscillator data sheets, amplifier performance, or *S*-parameter calculation.
2. Select a topology that gives $k < 1$ at the operating frequency. Add feedback if $k < 1$ has not been achieved.
3. Select an output load matching circuit that gives $|S'_{11}| > 1$ over the desired frequency range. In the simplest case this could be a 50-Ω load.
4. Resonate the input port with a lossless termination so that $\Gamma_G S'_{11} = 1$. The value of S'_{22} will be greater than unity with the input properly resonated.

In all cases the transistor delivers power to a load and the input of the transistor. Practical considerations of realizability and dc biasing will determine the best design.

For both bipolar and FET oscillators, a common topology is common base or common gate, since a common-lead inductance can be used to raise S_{22} to a large value, usually greater than unity even with a 50-Ω generator resistor. However, it is not necessary for the transistor S_{22} to be greater than unity, since the 50-Ω generator is not present in the oscillator design. The requirement for oscillation is $k < 1$; then resonating the input with a lossless termination will provide that $|S'_{22}| > 1$.

A simple example will clarify the design procedure. A common-base bipolar transistor (HP2001) was selected to design a fixed-tuned oscillator at 2 GHz. The common-base *S* parameters and stability factor are given in Table 10.4. Using the load circuit in Figure 10.27, we see that the reflection coefficients are

$$\Gamma_L = 0.62 \underline{/30°}$$
$$S'_{11} = 1.18 \underline{/173°}$$

Thus a resonating capacitance $C = 20$ pF resonates the input port. In a YIG-tuned oscillator, this reactive element could be provided by the high-*Q* YIG element. For a DRO, the puck would be placed to give $\Gamma_G \simeq 1.0 \underline{/-173°}$.

Another two-port design procedure is to resonate the Γ_G port and calculate S'_{22} until $|S'_{22}| > 1$, then design the load port to satisfy (10.3). This design procedure is summarized in Figure 10.28.

An example using this procedure at 4 GHz is given in Figure 10.29 using an AT-41400 silicon bipolar chip in the common-base configuration with a convenient value

TABLE 10.4   HP2001 Bipolar Chip Common Base
($V_{CE} = 15$ V, $I_C = 25$ mA)

$L_B = 0$	$L_B = 0.5$ nH
$S_{11} = 0.94 \underline{/174°}$	$1.04 \underline{/173°}$
$S_{21} = 1.90 \underline{/-28°}$	$2.00 \underline{/-30°}$
$S_{12} = 0.013 \underline{/98°}$	$0.043 \underline{/153°}$
$S_{22} = 1.01 \underline{/-17°}$	$1.05 \underline{/-18°}$
$k = -0.09$	-0.83
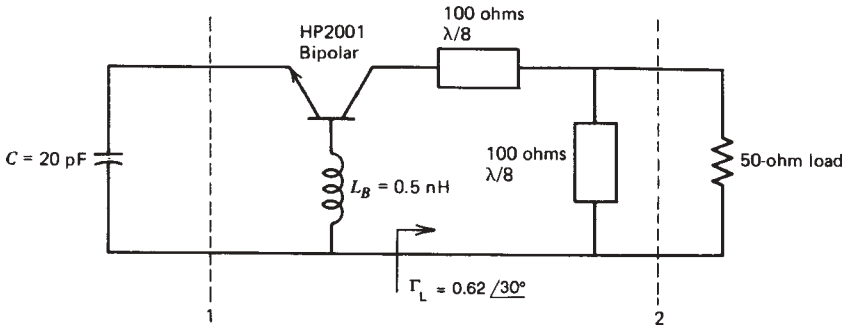
FIGURE 10.27   Oscillator example at 2 GHz.
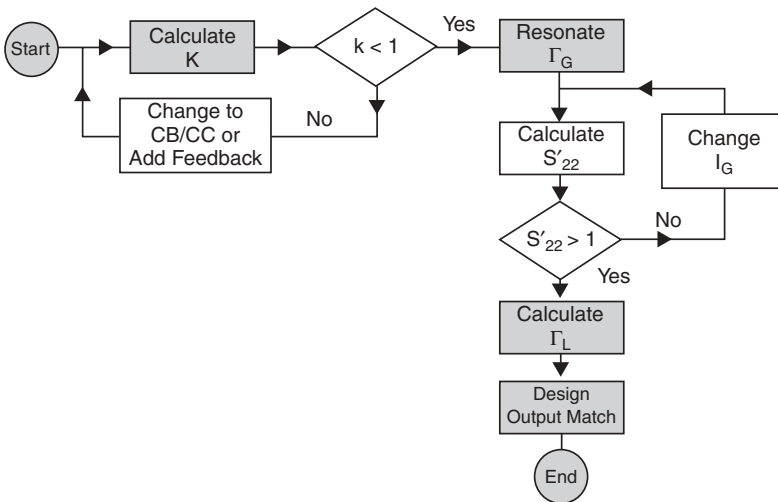
FIGURE 10.28   Oscillator design flowchart.

of base and emitter inductance 0.5 nH. The feedback parameter is the base inductance, which can be varied if needed. The two-port common-base S parameters were used to give

$$k = -0.805$$

$$S'_{11} = 1.212\underline{/137.7^\circ}$$

Since a lossless capacitor at 4 GHz of 2.06 pF gives $\Gamma_G = 1.0\underline{/-137.7^\circ}$, this input termination is used to calculate S'_{22} from (1.126) giving $S'_{22} = 0.637\underline{/44.5^\circ}$. This circuit will not oscillate into any passive load. Varying the emitter capacitor about 20° on the Smith chart to 1.28 pF gives $S'_{22} = 1.16\underline{/-5.5^\circ}$, which will oscillate into a load of $\Gamma_L = 0.861\underline{/5.5^\circ}$. The completed lumped-element design is given in Figure 10.30.

Figure 10.31a shows a 10-GHz oscillator using a feedback inductance in the base and a series resonant circuit consisting of a 200-pH inductor and 0.7-pF capacitor. The combination of those two reactances allows for a wide range of realizable inductance
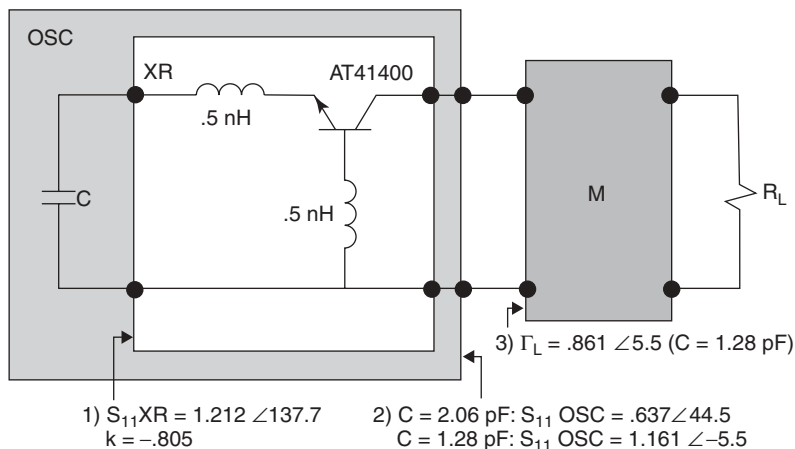
FIGURE 10.29   A 4-GHz LRO using AT41400.
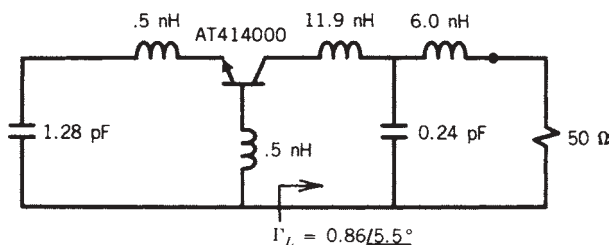
FIGURE 10.30   Completed LRO.

values. The collector also includes an output matching network. Figure 10.31*b* shows the influence of the base inductance which affects both the negative resistance at the input and the resonance frequency. By replacing the 0.7-pF capacitor with a tuning diode ranging from 0.5 to 5 pF, the frequency can also be varied. The largest amount of positive feedback for oscillation occurs between 0.5 and 1 pF is given in Figure 10.32, where the DR will serve the function of the emitter capacitor. This element is usually coupled to the 50-Ω microstripline to present about 1000 Ω of loading ($\beta \simeq 20$) at f_0, the lowest resonant frequency of the dielectric puck, at the correct position on the line. The load circuit will be simplified to 50 Ω ($\Gamma_L = 0$), so the oscillator must have an output reflection coefficient of greater than 100, thus presenting a negative resistance between -49 and -51 Ω. The computer file for analyzing this design is given in Table 10.5, where the variables are the puck resistance, the 50-Ω microstripline length, and the base feedback inductance. The final design is given in Figure 10.33, where the 10-μH coils are present for the dc bias connections that need to be added to the design. It is important to check the stability of this circuit with the DR removed. The input 50-Ω termination will usually guarantee unconditional stability at all frequencies. The phase noise of this oscillator is very low at -117 dBc/Hz at 10 kHz frequency offset [10.16], which is discussed in Sections 10.8 and 10.11.

(a)

(b)
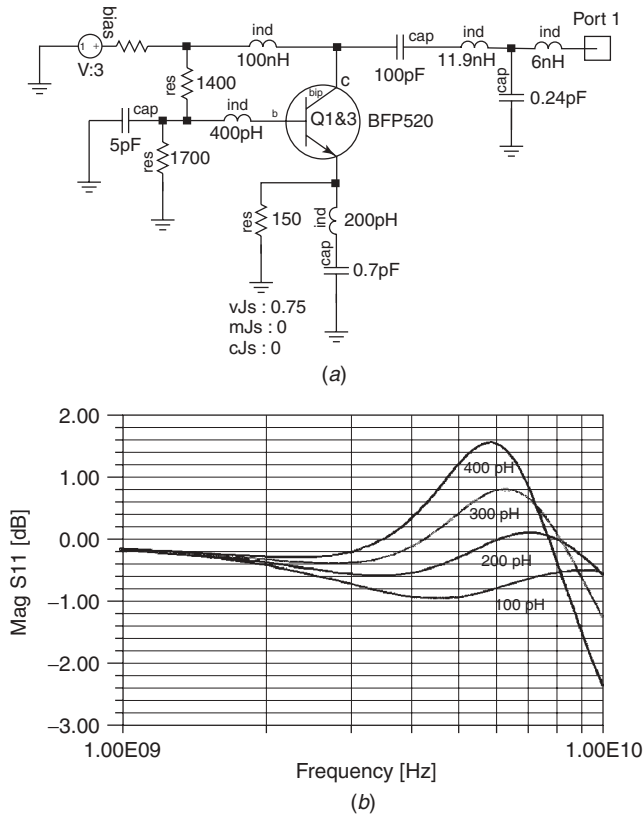
FIGURE 10.31 (*a*) Schematic of a Clapp–Gouriet-based lumped-resonator oscillator (LRO), including a collector matching network. This is a very popular circuit when used with dielectric resonators, which are placed in the emitter circuit, coupled to a transmission line. Changes at the collector, base, and emitter of the circuit have a strong effect on the resonant frequency for the LRO type. Even the DRO will show a soft response as to frequency changes as a function of load shifts (capacitive and resistive). (*b*) Effect of varying the LRO base inductance as indicated by the magnitude of S_{11}, in dB, looking into the oscillator output port (collector). An initial value of 400 pH was necessary to generate the sufficiently high negative resistance that is a prerequisite for oscillation startup. To complicate life, we will find that because the base and emitter circuits are highly interactive, there is no single, unique set of base and emitter component values that will support oscillation at a given frequency. (*c*) Effect of varying the emitter capacitance of the LRO as indicated by the magnitude of S_{11}, in dB, looking into the oscillator output port (collector). A value of about 20 dB is needed to guarantee oscillation startup at the desired frequency of about 10 GHz.

Another DRO example using the parallel feedback and the MSA-0835, a silicon MMIC described in Chapter 3, is shown in Figure 10.34. In this oscillator the dielectric puck will load the input and output transmission lines with about 1000 Ω at the correct microstripline position to give an output reflection coefficient greater than 100. The completed circuit design is given in Figure 10.35 for 4-GHz oscillation. This type of circuit can also be used as a self-oscillating mixer (SOM), where the signal is coupled to the input port and the IF is filtered from the output port with gain [10.17].

(c)
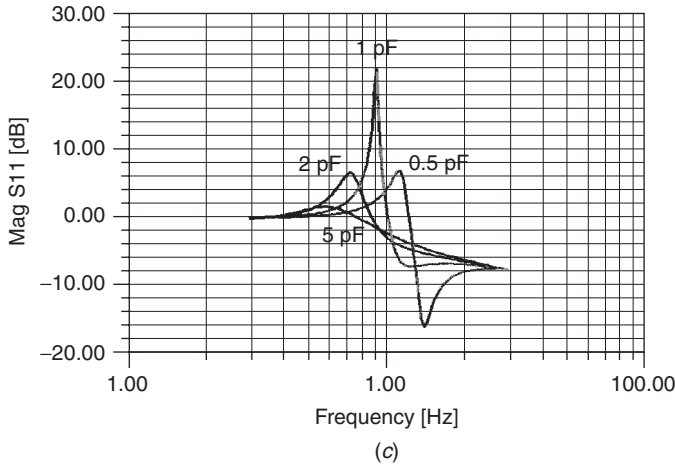
FIGURE 10.31   (*continued*)
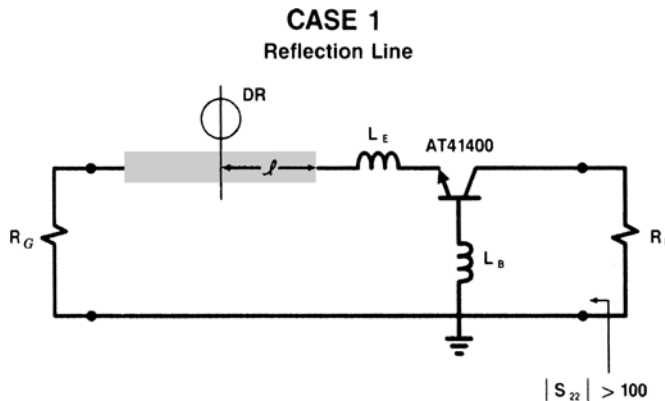
FIGURE 10.32   Transmission line oscillator with dielectric resonator.

10.6   NEGATIVE RESISTANCE FROM TRANSISTOR MODEL

Two-port oscillator design requires a complete set of four complex parameters (e.g., *S* parameters) to complete the design. An alternative approach is to use the transistor model for producing the negative resistance. An oscillator can be considered an amplifier with positive feedback, as shown in Figure 10.36, where the gain is

$$A = \frac{\mu}{1 - \mu\beta} \tag{10.60}$$

and is infinite when the loop gain $\mu\beta$ is unity and the phase shift is $360°$. This is the Barkhausen criterion for oscillation; a small portion of the output signal is fed back to the input in phase with the input signal. The initial input signal is generated by noise and the energy source is the dc bias supply.

TABLE 10.5   Supercompact File for DRO Design in Figure 10.33

```
*
-
* AT41400 AT 7.5V, 30 mA IN DRO
* OSCILLATOR By Vendelin et al. Microwave Journal June
1986 pp. 151−152
BLK
      TRL       1 2            Z=50 P=250 MIL K=6.6
      RES       2 3            R=?955.06?
      TRL       3 4            Z=50 P=?224.16 MIL?
                                K=6.6
      IND       4 0            L=1 E4NH
      IND       4 5            L=.5 NH
      TWO       6 7    5        Q1
      IND       6 0            L=?.33843 NH?
      IND       7 0            L=1 E4NH
      OSC:2POR 1 7
END
*
FREQ
      4 GHZ
END
OUT
      PRI OSC S
END
OPT
      OSC
      MS22 = 100 GT
END
DATA
  Q1:S
  4    .8057 -176.14 2.5990 74.77 .0316 56.54 .4306
        -22.94
END
```
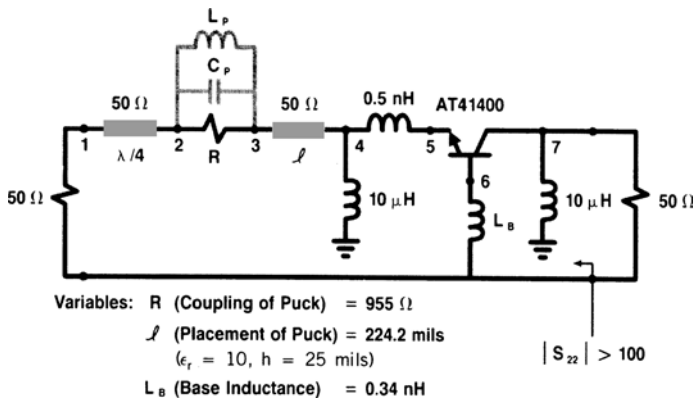

FIGURE 10.33   Equivalent circuit for dielectric resonator oscillator (DRO).
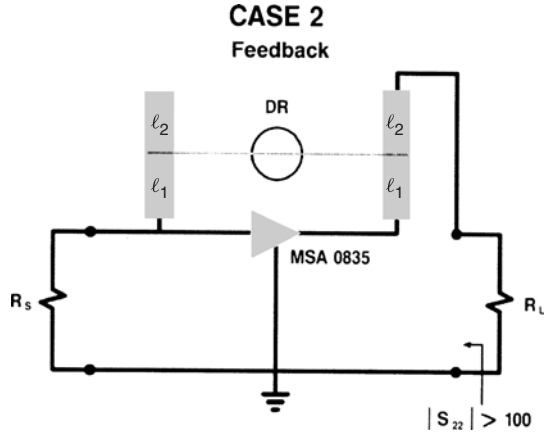
FIGURE 10.34   Feedback oscillator using MSA 0835.
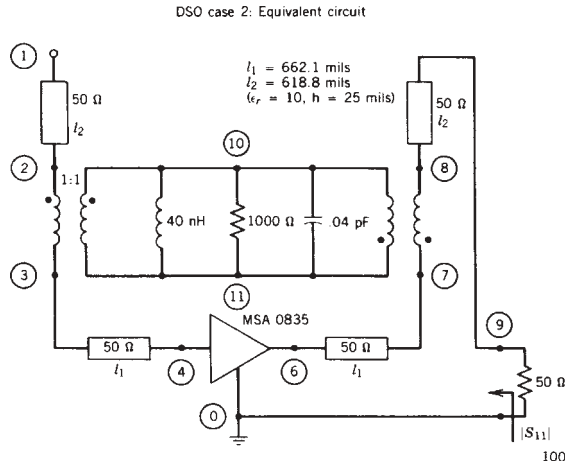
FIGURE 10.35   Equivalent circuit for DRO using MSA 0835.
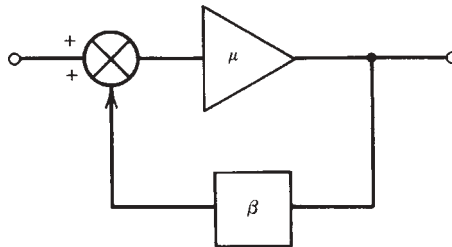
FIGURE 10.36   Feedback amplifier.
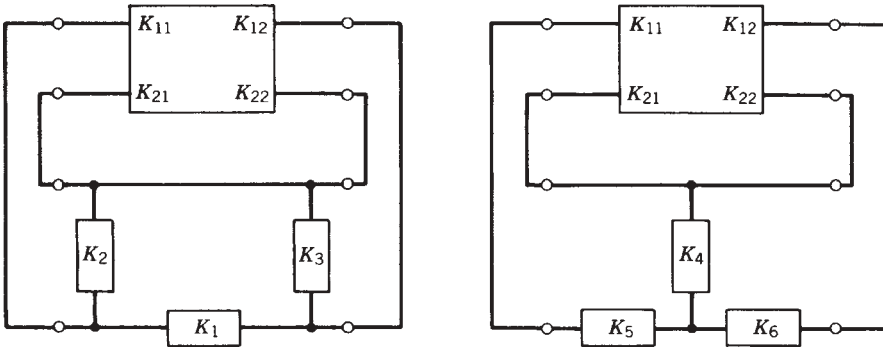
FIGURE 10.37   Two oscillator circuits.
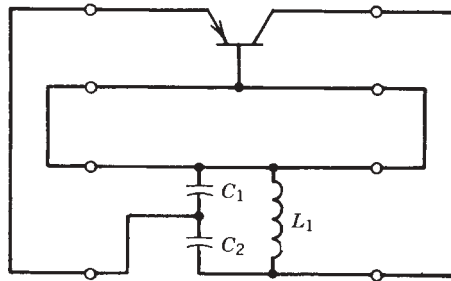
FIGURE 10.38   Feedback oscillator using capacitive voltage divider; Colpitts oscillator.
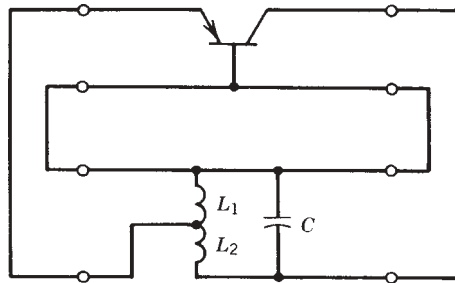
FIGURE 10.39   Feedback oscillator using inductive voltage divider; Hartley oscillator.

Two networks that may be used to provide the feedback are given in Figure 10.37, the Π and T networks. There are four degrees of freedom in the design, three reactances and one resistive load. For the two-port design method, the four degrees of freedom are the magnitude and angle of Γ_G and Γ_L.

Several examples of amplifiers with feedback are given in Figures 10.38 to 10.41, where the names are given to the original vacuum tube prototypes. There is a large amount of energy stored in the resonant tank. Some of this energy is coupled to the load (not shown) and a small amount is coupled to the input in phase with the original input signal. A resonant circuit is required if the output is to be a single-frequency signal.
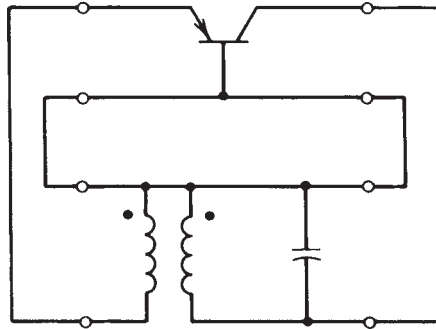
FIGURE 10.40   Feedback oscillator using mutual coupling; Armstrong oscillator.
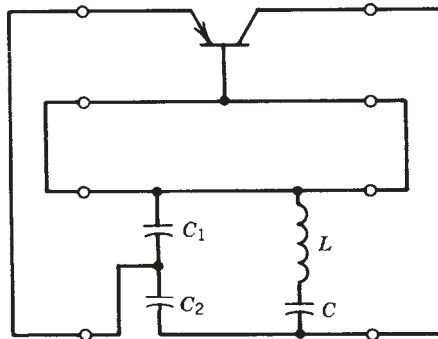
FIGURE 10.41   Feedback oscillator using series resonant circuit; Clapp–Gouriet oscillator.

Feedback from the output to the input is responsible for generating a negative resistance between terminals, and if a resonant circuit can be formed by the parasitics or other elements, the amplifier becomes an oscillator. A circuit that often becomes an unintentional high-frequency oscillator is the emitter follower of Figure 10.42, specifically when the base is driven from a capacitor with sufficient lead inductance. When analyzing this with a linear CAD tool, a negative resistance is evidenced from base to ground and a negative resistance from emitter to ground.

Following is a derivation of the negative resistance responsible for the oscillation. As shown in Figure 10.42, the bipolar transistor and the two capacitors will generate a negative resistance. The negative resistance is responsible for the cancellation of the resonator and load losses, and oscillation can be obtained. To see how a negative resistance is realized, the input impedance of the circuit will be derived.

If h_{oe} is sufficiently small ($h_{oe} \ll 1/R_L$), the equivalent circuit is as shown in Figure 10.42. The steady-state loop equations are

$$
\begin{aligned}
V_{\text{in}} &= I_{\text{in}}(X_{C1} + X_{C2}) - I_b(X_{C1} - \beta X_{C2}) \\
0 &= -I_{\text{in}}(X_{C1}) + I_b(X_{C1} + h_{ie})
\end{aligned}
\tag{10.61}
$$
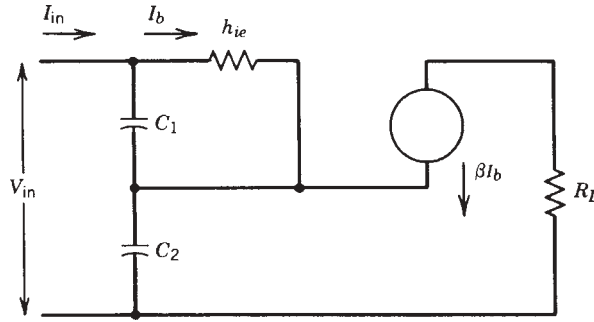
FIGURE 10.42   Negative input impedance generated by capacitive feedback.

After I_b is eliminated from these two equations, Z_{in} is obtained as

$$Z_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{(1 + \beta)X_{C1}X_{C2} + h_{ie}(X_{C1} + X_{C2})}{X_{C1} + h_{ie}} \tag{10.62}$$

If $X_{C1} \ll h_{ie}$, the input impedance is approximately equal to

$$Z_{\text{in}} \approx \frac{1 + \beta}{h_{ie}}X_{C1}X_{C2} + (X_{C1} + X_{C2})$$

$$\approx \frac{-g_m}{\omega^2 C_1 C_2} + \frac{1}{j\omega[C_1 C_2/(C_1 + C_2)]} \tag{10.63}$$

That is, the input impedance of the circuit shown in Figure 10.42 is a negative resistor

$$R = \frac{-g_m}{\omega^2 C_1 C_2} \tag{10.64}$$

in series with a capacitor

$$C_{\text{in}} = \frac{C_1 C_2}{C_1 + C_2} \tag{10.65}$$

which is the series combination of the two capacitors. With an inductor L (with the series resistance R_s) connected across the input, it is clear that the condition for sustained oscillation is

$$R_s = \frac{g_m}{\omega^2 C_1 C_2} \tag{10.66}$$

and the frequency of oscillation

$$F_0 = \frac{1}{2\pi\sqrt{L(C_1 C_2/(C_1 + C_2))}} \tag{10.67}$$

This interpretation of the oscillator readily provides several guidelines that can be used in the design. First, C_1 should be as large as possible, so that

$$X_{C1} \ll h_{ie} \tag{10.68}$$

and C_2 is to be large, so that

$$X_{C2} \ll \frac{1}{h_{oe}} \tag{10.69}$$

When these two capacitors are large, the transistor base-to-emitter and collector-to-emitter capacitances will have a negligible effect on the circuit's performance. However, (10.58) limits the maximum value of the capacitances since

$$R_s \leq \frac{g_m}{\omega^2 C_1 C_2} \leq \frac{G}{\omega^2 C_1 C_2} \tag{10.70}$$

where G is the maximum value of g_m. For a given product of C_1 and C_2, the series capacitance is a maximum when $C_1 = C_2 = C_m$. Thus (10.70) can be written

$$\frac{1}{\omega C_m} > \sqrt{\frac{R_s}{g_m}} \tag{10.71}$$

This equation is important because it shows that for oscillations to be maintained the minimum permissible reactance $1/\omega C_m$ is a function of the resistance of the inductor and the transistor's transconductance g_m.

An oscillator circuit known as the Clapp circuit or Clapp–Gouriet circuit is shown in Figure 10.43. This oscillator is equivalent to the one just discussed, but it has the practical advantage of being able to provide another degree of design freedom by making C_v much smaller than C_1 and C_2. It is possible to use C_1 and C_2 to satisfy the condition of (10.70) and then adjust C_v for the desired frequency of oscillation ω_0, which is determined from

$$\omega_0 L - \frac{1}{\omega_0 C_v} - \frac{1}{\omega_0 C_1} - \frac{1}{\omega_0 C_2} = 0 \tag{10.72}$$

Consider a Clapp–Gouriet VCO example, as shown in Figure 10.44. The transistor operated at 1 mA has a G_{max} of 40 mS and the dynamic g_m is found to be 20 mS.
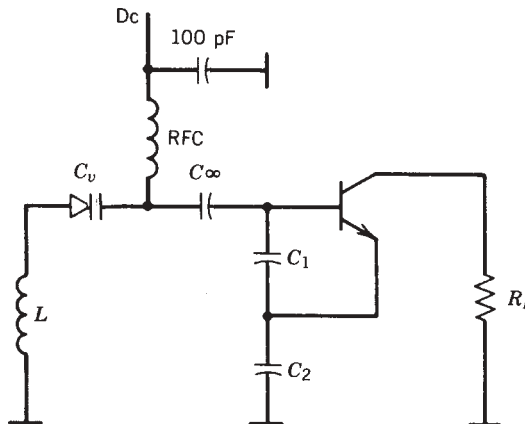
FIGURE 10.43   Figure 10.43 VCO using capacitive feedback.
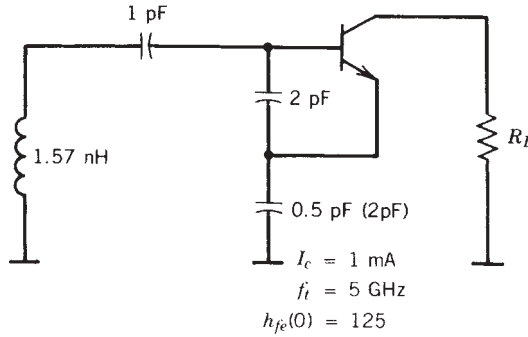
FIGURE 10.44   Practical valued for VCO at 7.5 GHz.

The reduction of G_{max} is explained in Section 10.3. The inductor, a quarter-wavelength transmission line, has a Q_0 of 200. The oscillator is to be designed for 7.5 GHz.

The feedback is provided by the voltage divider C_1 and C_2, where C_1 is C_{te} and about 2 pF and C_2 is C_{ce} and about 0.5 pF. The transistor is operated at 1 mA and has an F_t of 5 GHz and an ac gain h_{fe} of 125.

First we use (10.70) to determine the negative resistance under feedback conditions. From

$$r = \frac{-gm}{\omega^2 C_1 C_2} \tag{10.73}$$

we obtain $r = -9\ \Omega$. This means that the loss resistance r' of the combination of L and C_0 must be less then 9 Ω. With an unloaded Q_0 of 200 and a series capacitor of 1 pF as a typical value for the tuning diode, we need an inductance of 1.57 nH. This value can be computed from

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_v} = \frac{1}{0.2857}\ \text{pF} \tag{10.74}$$

and

$$L = \frac{1}{\omega^2 C} = 1.57\ \text{nH} \tag{10.75}$$

Finally, we compute $R_s = \omega L_s / Q_0 = 0.26\ \Omega$ with

$$L_s = \frac{X_1 - X_v}{\omega} = 1.12\ \text{nH} \qquad L_v = 0.45\ \text{nH} \tag{10.76}$$

where X_v accounts for 0.45 nH of package inductance in the varactor. The use of C_{ce} as feedback capacitor is somewhat dangerous because its value is small compared to C_{te} or C_1 and may vary greatly. A better solution is to add an external capacitor which also makes it possible to control the temperature response. By adding 1.5 pF to C_{ce}, the new value of C_2 becomes 2 pF, or C_1 and C_2 are equal. We have to make sure that the relationship of (10.71) is valid.

Finally, we must see over what tuning range the oscillator can be used. By rearranging (10.71) and calculating the effect of C_v, we can determine

$$f_{\min} = 6.5 \text{ GHz(2 pF)} \qquad R_s = 0.183 \ \Omega < |-3| \ \Omega \qquad (10.77)$$

$$f_{\max} = 9.2 \text{ GHz(0.5 pF)} \qquad R_s = 0.260 \ \Omega < |-1.5| \ \Omega \qquad (10.78)$$

where $L = 0.902$ nH. A practical tuning diode, however, can have a much lower Q than assumed for the inductor. Some diodes exhibit values such as 5, in which case the system has to be reevaluated.

For $F_0 = 7.5$ GHz and the same working condition we calculate

$$R_v = \frac{1/\omega C}{Q} = \frac{21.2}{5} = 4.24 \ \Omega \neq |-2.25|$$

The oscillator will not work. There is no change of C_1 and/or C_2 possible for which oscillation can be resumed since

$$\frac{1}{\omega C} < \sqrt{2.25/0.02} = 10.61 \qquad \text{or} \qquad C > 2.00 \text{ pF}$$

However, by increasing the dc bias of the transistor to about 2 to 3 mA and adjusting for $g_m = 0.042$, we find that

$$R_s = 4.24 < |-4.728|$$

For higher frequencies or at about 9 GHz, the oscillator requires more gain and the dc bias point must be moved to 7 mA in order to obtain constant working conditions over temperature and semiconductor tolerances. The power dissipation must not be higher than the manufacturer's specifications.

We have briefly mentioned that the oscillator amplitude stabilizes due to the nonlinear performance of the transistor. There are various mechanisms involved, and depending on the circuit, several of them simultaneously may be responsible for the performance of an oscillator. Under most circumstances, the transistor is operated in an area where the dc bias voltages are substantially larger than the ac voltages. Therefore, the theory describing the transistor performance under these conditions is called "small-signal theory." In a microwave transistor oscillator, however, we are dealing with a feedback circuit that applies positive feedback. The energy that is generated by the initial switch-on of the circuit is fed back to the input of the circuit, amplified, and returned to the input again until oscillation starts. The oscillation would theoretically increase in value unless some limiting or stabilization occurs. In transistor circuits, we have two basic phenomena responsible for limiting the amplitude of oscillation:

1. Limiting because of gain saturation and reduction of open-loop gain
2. Automatic bias generated by the rectifying mechanism of either the *pn* junction in the bipolar transistor or the junction FET
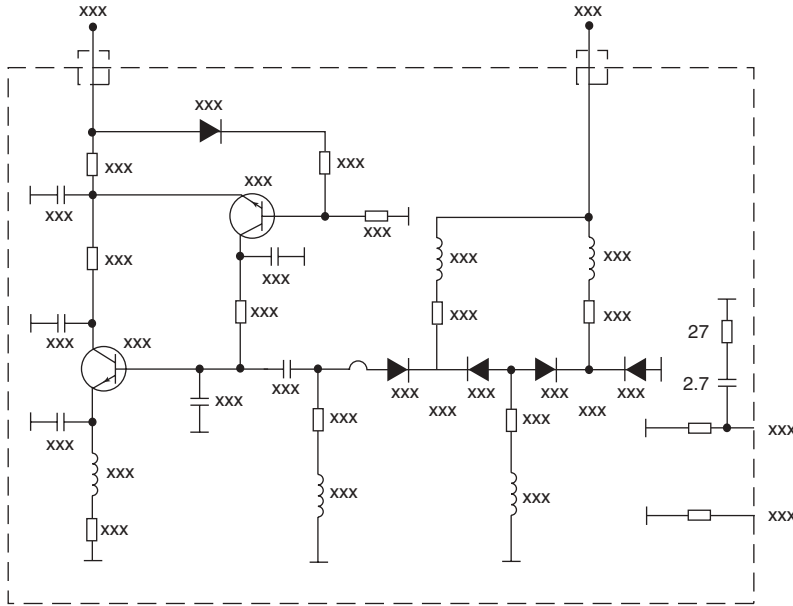
FIGURE 10.45 BJT-based oscillator with noise feedback. The noise sampling is done in the collector. The biasing with *pnp* transistor has always been used for grounded-emitter microwave circuits, but the feedback loop was so narrow that no noise or feedback/cancellation was possible.

A third factor, external automatic gain control (AGC), will not be considered here.

Figure 10.45 shows a wide-band BJT-based oscillator covering 612 to 1124 MHz. This circuit requires a total of four tuning diodes. It would be possible to improve the phase noise further if each tuning diode is replaced by two parallel tuning diodes, whereby each parallel combination would have half the resistance. In addition, this circuit has a noise feedback canceling circuit. The dc control *pnp* transistor acts both as a dc stabilization transistor and a noise feedback. This type of feedback circuit can provide a drastic noise improvement within the loop bandwidth of the circuit used. Figure 10.46 shows the measured phase noise improvement for such a feedback circuit using a novel design where the oscillator and the feedback are combined in a custom RFIC. For these arrangements there are either already existing patents or patents pending. This feedback shows an improvement of about 15 dB phase noise. The noise improvement can be expanded to 1 MHz off the carrier if the feedback circuit has the appropriate gain and exactly 180° phase shift within the required bandwidth.

10.7 OSCILLATOR *Q* AND OUTPUT POWER

The oscillator will deliver power at frequencies near f_0 as the load is changed from the ideal condition of a 50-Ω termination. This effect can easily be measured by finding the maximum frequency shift for a load mismatch of all phases.

For example, consider a 6-dB attenuator terminated in a sliding short circuit which can give a complete phase rotation around the Smith chart. Since the load VSWR is
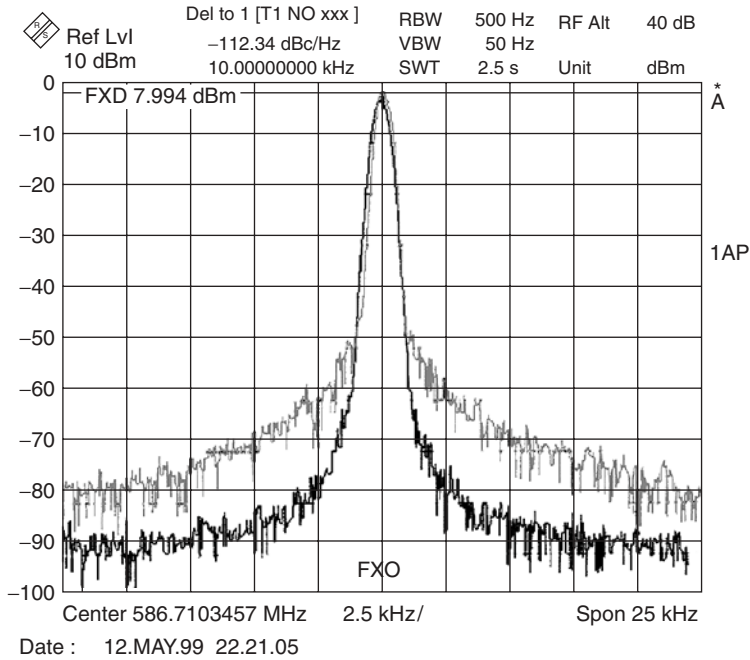
FIGURE 10.46 Phase noise improvement caused by the feedback circuit, including a tuning diode. However, the tuning diode coupling is only about 10 MHz/V and therefore does not add much to the modulation noise.

1.67 : 1, the change in frequency will give the oscillator Q or Q_{ext} by [10.18]

$$Q_{ext} = \frac{f_0}{2\Delta f} \left(S - \frac{1}{S} \right) \tag{10.79}$$

For a 10-GHz oscillator with a 10-MHz frequency deviation, we have

$$Q_{ext} = \frac{10}{2(0.01)} \left(1.67 - \frac{1}{1.67} \right) = 536$$

The load VSWR must not be too large for this measurement since this could cause the oscillation to stop.

Another method for measuring the oscillator Q is by injection locking the free-running oscillator with a known signal level. If a low-level signal P_i is injected into the oscillator at a distance Δf from the carrier, then [10.19]

$$Q_{ext} = \frac{2f_0}{\Delta f} \sqrt{\frac{P_{in}}{P_{out}}} = \frac{2f_0}{\Delta f} \frac{1}{\sqrt{G_i}} \tag{10.80}$$

where G_i is the injection gain. Both of these measurement techniques are used to measure the oscillator external Q, which is a measure of the average stored energy in

the oscillator circuit. This figure of merit is the energy ratio delivered externally to all dissipative loads. The Q_{ext} of the oscillator is

$$Q_{ext} = 2\pi \frac{\text{time-averaged stored energy}}{\text{energy delivered to load per cycle}} \tag{10.81}$$

The load that accepts this power is calculated from the loaded Q of the oscillator at the load port and is given by

$$\frac{1}{Q_L} = \frac{1}{Q_u} + \frac{1}{Q_e} \tag{10.82}$$

For a parallel resonant load this is given by

$$\frac{\omega L}{R_T} = \frac{\omega L}{R_u} + \frac{\omega L}{R_e} \tag{10.83}$$

where the useful power is delivered to R_e, the external load. Notice that Q_e is different from Q_{ext}, although these parameters often have the same name. The loaded Q is also given by

$$\frac{1}{Q_L} = \frac{1+\beta}{Q_u} \tag{10.84}$$

where

$$\beta = Q_u/Q_e \tag{10.85}$$

The oscillator output power is difficult to predict, but we can expect it to be less than the saturated power of the same transistor in large-signal amplifier applications. The available power from the transistor must be absorbed in (1) losses in the tuning elements and resonator (Q_u) and (2) power to the load. An estimate for the output power for GaAs MESFETS has been derived by Johnson [10.8].

It is helpful to use the common-source amplifier to compute the oscillator output power. For oscillators, the objective is to maximize $P_{out} - P_{in}$ of the amplifier, which is the useful power to the load. An empirical expression for the common-source amplifier output power is

$$P_{out} = P_{sat} \left(1 - \exp \frac{-GP_{in}}{P_{sat}} \right) \tag{10.86}$$

where P_{sat} is the saturated output power of the amplifier and G is the tuned small-signal common-source transducer gain of the amplifier, which is identical to $|S_{21}|^2$. Since the objective is to maximize $P_{out} - P_{in}$,

$$d(P_{out} - P_{in}) = 0 \tag{10.87}$$

$$\frac{\partial P_{out}}{\partial P_{in}} = 1 \tag{10.88}$$

$$\frac{\partial P_{out}}{\partial P_{in}} = G \exp \left(-\frac{GP_{in}}{P_{sat}} \right) = 1 \tag{10.89}$$

$$\exp \left(\frac{GP_{in}}{P_{sat}} \right) = G \tag{10.90}$$

$$\frac{P_{in}}{P_{sat}} = \ln \frac{G}{G} \tag{10.91}$$

At the maximum value of $P_{out} - P_{in}$, the amplifier output is

$$P_{out} = P_{sat} \left(1 - \frac{1}{G} \right) \tag{10.92}$$

and the maximum oscillator output power is

$$P_{osc} = P_{out} - P_{in}$$
$$= P_{sat} \left(1 - \frac{1}{G} - \ln \frac{G}{G} \right) \tag{10.93}$$

Thus the maximum oscillator output power can be predicted from the common-source amplifier saturated output power and the small-signal common-source transducer gain G. A plot of (10.93) is given in Figure 10.47, which shows the importance of high gain for a high oscillator output power. Another gain that is useful for large-signal
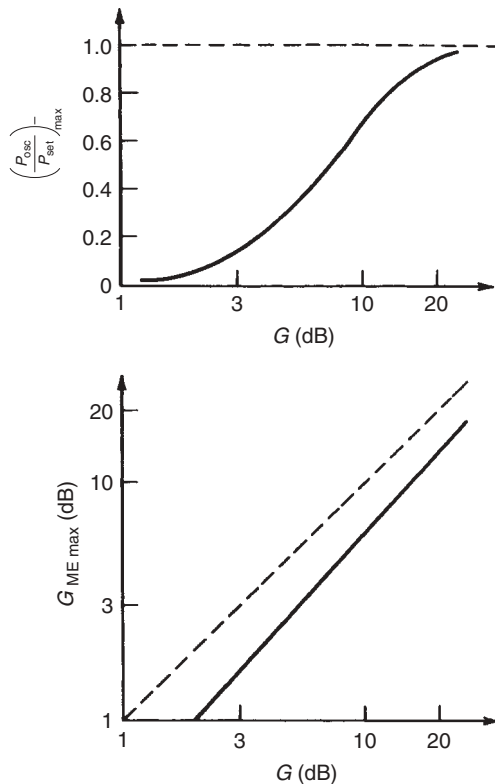
FIGURE 10.47   Maximum oscillator power and maximum efficient gain versus small-signal transducer power gain.

amplifier or oscillator design is the maximum efficient gain, defined by

$$G_{\text{ME}} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{in}}}$$
(10.94)

For maximum oscillator power the maximum efficient gain is, from (10.91) and (10.92)

$$G_{\text{ME,max}} = \frac{G - 1}{\ln G}$$
(10.95)

This gain is also plotted in Figure 10.47, showing a considerably smaller value of $G_{\text{ME,max}}$ compared to G, the small-signal gain. From these results, the oscillator output power will approach P_{sat} at low frequencies, where the gain is large. As the gain approaches unity, the oscillator power approaches zero.

10.8   NOISE IN OSCILLATORS: LINEAR APPROACH

Noise generated by the transistor and passive devices shows up at the output signal of amplifiers. In the case of an oscillator, which is a nonlinear device, these noise voltages and currents are modulating the signal produced by the oscillator. While introducing the concept of noise in oscillators, we first discuss noise measurement techniques and then calculate some of the noise voltages and currents that are modulated onto the carrier. This allows us finally to use Leeson's model [10.4] to obtain an expression of the normalized (in 1 Hz bandwidth) single-sideband noise ($\mathscr{L}$ in dBc/Hz) power. Finally, we analyze the various contribution to the noise and calculate the noise of VCOs.

We start by looking at different noise test techniques [10.20–10.26] that give rise to noise descriptions that are related to one another. The following equations are common definitions of oscillator spectral purity:

$S_\theta(f_m) = $ spectral density of phase fluctuation

$$S_\theta(f_m) = \Delta\theta_{\text{rms}}^2$$
(10.96)

$S_{\dot\theta}(f_m) = $ spectral density of frequency fluctuations

$$S_{\dot\theta}(f_m) = \Delta f_{\text{rms}}^2$$
(10.97)

$\mathscr{L}(f_m) = $ ratio of noise power in 1 Hz bandwidth (BW)
        at f_m offset from carrier to carrier signal power

$$\mathscr{L}(f_m) = \frac{N(1 \text{ Hz BW})}{C}$$
(10.98)

10.8.1   Using a Spectrum Analyzer

The easiest technique for measuring oscillator noise is to view the oscillator spectrum directly on a spectrum analyzer, giving a display as in Figure 10.48. This method allows direct measurement of $\mathscr{L}(f_m)$. The oscillator output power is read off the screen in dBm. The noise at a frequency offset f_m away from the carrier may also be read directly. Noise measured in this way will usually require correction factors, since the
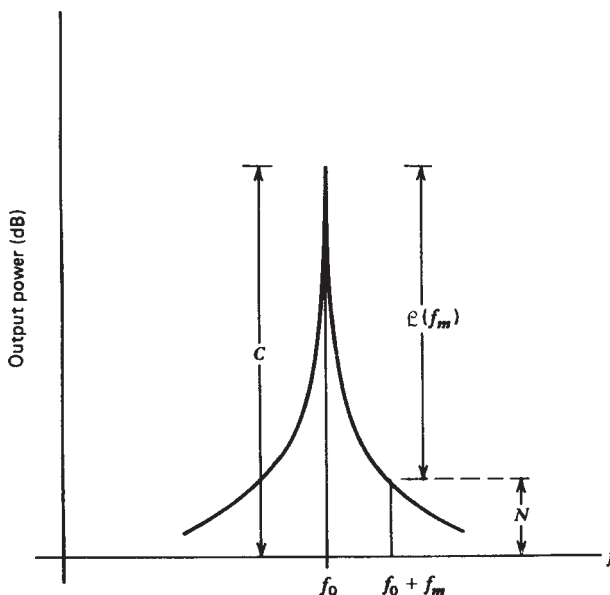
FIGURE 10.48   Oscillator output power spectrum.

detector of the analyzer is ordinarily an envelope rather than a true rms detector, the log amplifiers amplify noise peaks less, and the bandpass filters may be Gaussian or trapezoidal in shape, which requires correction to a square bandpass. Additionally, since 1-Hz bandpass filters are uncommon, this results in measurement of the noise in a wider bandwidth which must be corrected to 1 Hz by reducing the noise measured by 10 dB for every decade by which the filter is wider than 1 Hz.

After applying these corrections,

$$\mathcal{L}(f_m) = \frac{\text{noise power with corrections at } f_m}{\text{carrier power}} = \frac{N(1 \text{ Hz Bw})}{C} \qquad (10.99)$$

Certain precautions must be taken when measuring $\mathcal{L}(f_m)$ in this fashion. The technique is most useful when it can be determined that the noise of the oscillator being measured is worse than that of the local oscillator of the spectrum analyzer. The reason for this is apparent from Figure 10.49a, which shows a spectrum analyzer from the front end. The noiseless local oscillator translates the oscillator under test to an IF where the amplitude and noise can be analyzed with narrow fixed filters. The spectrum analyzer cannot distinguish between noise from its own local oscillator and that from an oscillator under test (which may be better), as in Figure 10.49b. This situation frequently occurs at microwave frequencies where multiplied, low-noise oscillators often outperform the commonly used YIG-tuned oscillator in spectrum analyzers.

An important point that should be made is that the bulk of oscillator noise particularly close to the carrier is phase or FM noise. Oscillator limiting mechanisms, whether self-limiting or AGC type, tend to eliminate AM noise. Under these conditions $\mathcal{L}(f_m)$ can be related to phase modulation in the following way. A table of Bessel functions will reveal that if a carrier is phase modulated (for a small modulation index
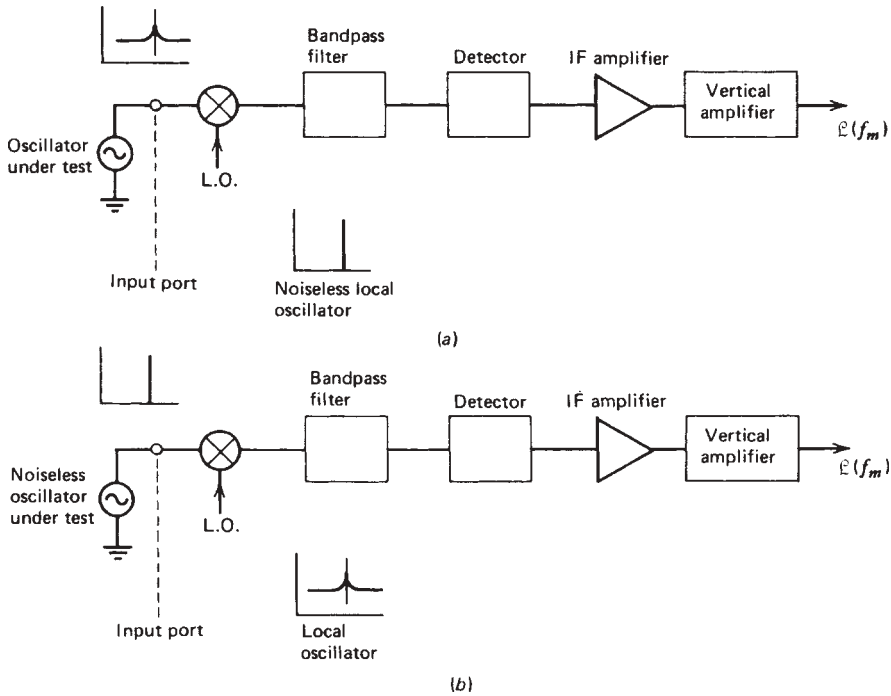
FIGURE 10.49 Measurement of noise-to-carrier ratio with spectrum analyzer: (*a*) noiseless local oscillator; (*b*) noiseless oscillator under test.

$\Delta\theta_{\text{peak}} \ll \pi/2$), the ratio of the first-order sideband to the carrier J_0 is

$$\frac{J_1}{J_0} \simeq \frac{1}{2}\Delta\theta_{\text{peak}} \simeq \frac{1}{2}\sqrt{2}\,\theta_{\text{rms}} \qquad (10.100)$$

Since $\mathcal{L}(f_m)$ is the ratio of noise power (J_1^2) to carrier power (J_0^2),

$$\mathcal{L}(f_m) = \frac{N}{C} = \left(\frac{J_1}{J_0}\right)^2 = \frac{1}{2}\,\theta_{\text{rms}}^2 \qquad (10.101)$$

This description of $\mathcal{L}(f_m)$ holds only where it can be assumed that the $f_0 \pm \Delta f$ noise sidebands are correlated (i.e., caused by the same modulation source). This is not true in the additive noise region, where the noise at $f_0 \pm \Delta f$ is not correlated (i.e., independent thermal noise generation at $\pm\Delta f$).

10.8.2 Two-Oscillator Method

Frequency Discriminator A more sensitive technique is to measure $S_{\dot\theta}(f_m)$. Figure 10.50 shows a common oscillator noise measuring approach that gives $S_{\dot\theta}(f_m)$.

Describe oscillator 1 as

$$v_1 = V_1 \cos[\omega_1 t + \theta_1(t)] \qquad (10.102)$$
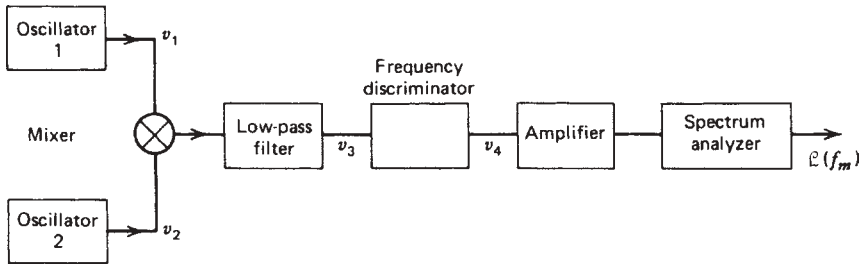
FIGURE 10.50 Measurement of spectral density of frequency fluctuations with frequency discriminator.

and oscillator 2 as

$$v_2 = V_2 \cos[\omega_2 t + \theta_2(t)] \tag{10.103}$$

Then mixing these oscillators together gives an IF low enough to apply to the frequency discriminator:

$$
\begin{aligned}
v_3 &= V_1 V_2 \cos[\omega_1 t + d\theta_1(t)] \cos[\omega_2 t + d\theta_2(t)] \\
&= \frac{V_1 V_2}{2} \cos\{(\omega_1 - \omega_2)t + [d\theta_1(t) - d\theta_2(t)]\}
\end{aligned}
\tag{10.104}
$$

The sum frequency term is eliminated by a low-pass filter. The output from the discriminator is

$$v_4 = K\omega_{\text{in}} \tag{10.105}$$

The frequency of the foregoing signal is

$$\omega_4 = (\omega_1 - \omega_2) + \frac{d\theta_1(t) - d\theta_2(t)}{dt} \tag{10.106}$$

where $\omega_1 - \omega_2$ is a constant and $[d\theta_1(t) - d\theta_2(t)]/dt$ represents the sum of the frequency fluctuations in ω_1 and ω_2.

The output of the discriminator will be

$$v_4(t) = K\left[(\omega_1 - \omega_2) + \frac{d\theta_1 - d\theta_2}{dt}\right] = K_2 + K\frac{d\theta_1 - d\theta_2}{dt} \tag{10.107}$$

A high-pass filter will remove the constant term, leaving

$$
\begin{aligned}
v_4(t) &= K\frac{d\theta_1 - d\theta_2}{dt} = K\frac{d\theta_1}{dt} - K\frac{d\theta_2}{dt} = K d\omega_1 - K d\omega_2 \\
&= 2\pi K(df_1 - df_2)
\end{aligned}
\tag{10.108}
$$

This time function is then applied to a low-frequency spectrum analyzer. In the transform domain or frequency domain

$$v_4(f_m) = 2\pi K[dF_1(f_m) - dF_2(f_m)] \tag{10.109}$$

Since $dF_1(f_m)$ and $dF_2(f_m)$ are uncorrelated, they combine as follows:

$$\Delta f_{\text{rms}} = dF_1(f_m) + dF_2(f_m) = \sqrt{\overline{(dF_1)^2} + \overline{(dF_2)^2}} \qquad (10.110)$$

$$v_4(f_m) = 2\pi K \sqrt{\overline{(dF_1)^2} + \overline{(dF_2)^2}} \qquad (10.111)$$

Since spectrum analyzers normally display power rather than voltage, the display represents

$$[v_4(f_m)]^2 = (2\pi K)^2 \, [\overline{(dF_1)^2} + \overline{(dF_2)^2}] \qquad (10.112)$$

It will be recognized that $\overline{dF_1^2} = S_{\dot\theta}(f_m)$ for oscillator 1 and $\overline{dF_2^2} = S_{\dot\theta 2}(f_m)$ for oscillator 2.

The spectrum analyzer display is proportional to the sum of the spectral densities $S_{\dot\theta}(f_m)$ for oscillator 1 and oscillator 2:

$$[v_4(f_m)]^2 = (2\pi K)^2 \, [S_{\dot\theta 1}(f_m) + S_{\dot\theta 2}(f_m)] \qquad (10.113)$$

Now $\mathscr{L}(f_m)$ represents noise sideband power to carrier power caused by phase fluctuations as a function of frequency from the carrier. The term $S_{\dot\theta}(f_m)$ represents FM deviation squared as a function of frequency offset from the carrier.

The two parameters may be related as follows:

$$S_{\dot\theta}(f_m) = \overline{\Delta f(f_m)^2} \qquad (10.114)$$

$$df(t) = \frac{1}{2\pi} d\omega(t) = \frac{1}{2\pi} \frac{d\theta(t)}{dt} \qquad (10.115)$$

Then in the transform domain

$$df(f_m) = \frac{1}{2\pi}(s) \, d\theta(f_m) \qquad (10.116)$$

$$S_{\dot\theta}(f_m) = \overline{df(f_m)^2} = \left(\frac{s}{2\pi}\right)^2 \overline{d\theta(f_m)^2} \qquad (10.117)$$

$$\overline{d\theta(f_m)^2} = \left(\frac{2\pi}{s}\right)^2 S_{\dot\theta}(f_m) = \frac{1}{f_m^2} S_{\dot\theta}(f_m) \qquad (10.118)$$

$$\mathscr{L}(f_m) = \frac{1}{2}\overline{\theta(f_m)^2} = \frac{1}{2 f_m^2} S_{\dot\theta}(f_m) \qquad (10.119)$$

This technique affords better sensitivity than direct measurement of $\mathscr{L}(f_m)$ at microwave frequencies, since the translation down to low RF permits the use of spectrum analyzers with lower noise local oscillators or fast Fourier transform analyzers. In general, the sensitivity of this system is limited by the internal noise of the frequency discriminator.

Double-Balanced Mixer   A more sensitive scheme removes the frequency discriminator as shown in Figure 10.51. We assume that the oscillators are or can be adapted so that one can be phase locked to the other. In Figure 10.51 the oscillators are set so that they are at approximately the same frequency. Oscillators 1 and 2 then mix
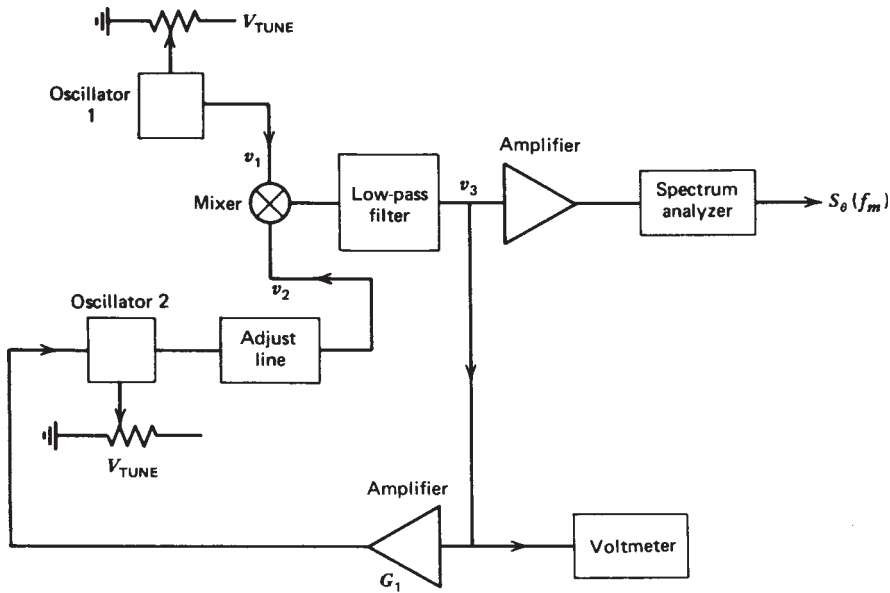
FIGURE 10.51   Measurement of spectral density of phase fluctuations with a mixer.

to produce sum and difference frequencies. The sum frequencies are removed by the low-pass filter. The difference frequency error signal is sent back to lock oscillator 2 to oscillator 1. Inside the loop bandwidth, which can be adjusted by varying the gain of G_1, the noise of oscillator 2 tracks that of oscillator 1. Outside the loop bandwidth, the noise of the two oscillators shows no correlation.

The mixer is usually a double-balanced mixer consisting of four diodes. The IF port is dc coupled to provide the phase-locked dc signal. This phase-locked dc signal is adjusted to be 0 V on the voltmeter, since the sensitivity $dv/d\theta$ is maximum for this condition. This is done by adjusting a line length such that the phases of the two oscillators are 90° apart.

Figure 10.52 shows the typical sensitivity of the mixer. Beyond the loop bandwidth, the output of the mixer may be described as follows:

$$v_1 = V_1 \cos(\omega t + \theta_{n1}) \tag{10.120}$$

$$v_2 = V_2 \cos\left(\omega t + \theta_{n2} - \frac{\pi}{2}\right) \tag{10.121}$$

$$v_3 = V_1 V_2 \cos(\omega t + \theta_{n1}) \cos\left(\omega t + \theta_{n2} - \frac{\pi}{2}\right)$$

$$= \frac{V_1 V_2}{2} \cos\left(\theta_{n1} - \theta_{n2} + \frac{\pi}{2}\right) \tag{10.122}$$

The θ_{n1} and θ_{n2} terms are rms phase noise, which can be combined as

$$\theta_{nT} = \sqrt{\overline{\theta_{n1}^2} + \overline{\theta_{n2}^2}} \tag{10.123}$$
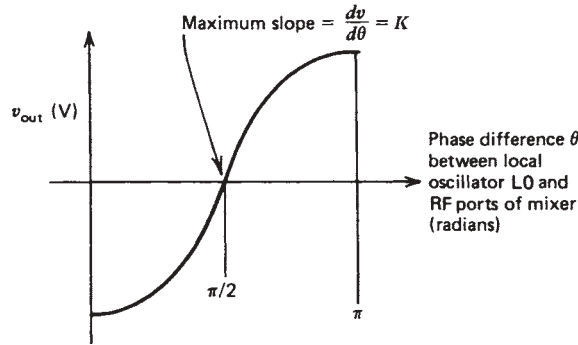
FIGURE 10.52   Output voltage of doubly balanced mixer versus phase difference between local oscillator and RF signal ports.

$$v_3 = \frac{V_1 V_2}{2} \cos\left(\theta_{n1} - \theta_{n2} + \frac{\pi}{2}\right) = \frac{V_1 V_2}{2} \cos\left(\theta_{nT} + \frac{\pi}{2}\right)$$

$$= -\frac{V_1 V_2}{2} \sin \theta_{nT} \qquad\qquad (10.124)$$

For θ_{nT} very small,

$$\sin \theta_{nT} \simeq \theta_{nT} = \sqrt{\overline{\theta_{n1}^2} + \overline{\theta_{n2}^2}} \qquad\qquad (10.125)$$

Since the spectrum analyzer displays power, it will show the square of the term

$$-\frac{V_1 V_2}{2} \sqrt{\overline{\theta_{n1}^2} + \overline{\theta_{n2}^2}} \qquad \text{or} \qquad \left(\frac{V_1 V_2}{2}\right)^2 (\overline{\theta_{n1}^2} + \overline{\theta_{n2}^2})$$

$$\overline{\theta_{n1}^2} = S_\theta(f_m) \text{ of oscillator1} \qquad\qquad (10.126)$$

$$\overline{\theta_{n2}^2} = S_\theta(f_m) \text{ of oscillator2} \qquad\qquad (10.127)$$

If the spectral densities have equal power distribution but are not correlated, the mixer output is 3 dB greater than either one alone. This technique yields the sum of the $S_\theta(f_m)$ for oscillators 1 and 2.

Now $S_\theta(f_m)$ can be related to $\mathscr{L}(f_m)$. The term $S_\theta(f_m)$ is equal to $\mathscr{L}(f_m)$ folded about itself. Therefore, $S_\theta(f_m) = 2\mathscr{L}(f_m)$ if the noise sidebands about f_1 are correlated and $S_\theta(f_m) = \sqrt{2}\mathscr{L}(f_m)$ if they are not correlated.

In Figure 10.53 the noise below $f_0 - \Delta f$ is assumed to be uncorrelated to the noise above $f_0 + \Delta f$ in oscillators 1 and 2. Closer than $f_0 \pm \Delta f$ the assumption is that there is correlation of the noise above and below the carrier in both oscillators. Beyond $\pm\Delta f$ we assume that this is the noise floor of the device. Closer than $\pm\Delta f$ we assume that the noise is caused by phase modulation mechanisms in the device or other components that generate related sidebands above and below the carrier. When these two spectrums are mixed together, the following occurs: If $f_1 = f_2$, then (if we ignore the sum frequency components, which are eliminated by the low-pass filter) $f_1 - f_2 = 0$; f_1 then mixes against the noise spectrum of f_2. This causes the noise spectrum of f_2 to fold upon itself. For instance, f_1 mixing against $f_2 \pm \Delta f_x$ will
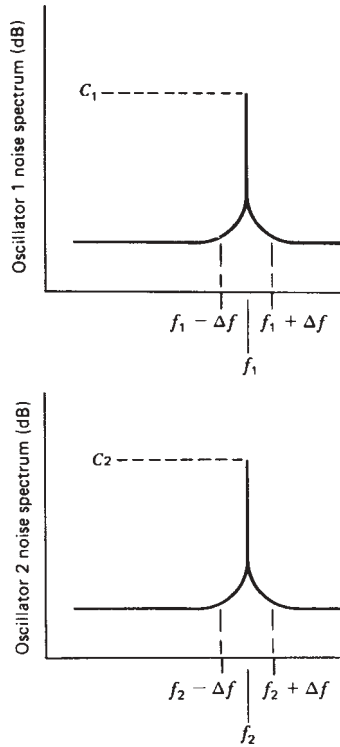
FIGURE 10.53   Noise spectrum of two oscillators at f_1 and f_2 carrier frequency.

yield two correlated noise components at Δf_x which add in power to cause a 6-dB increase as in Figure 10.54. However, if f_1 mixes against $f_2 \pm \Delta f_y$, there is only a 3-dB increase, since the noise at $f_2 - \Delta f_y$ is not correlated to that at $f_2 + \Delta f_y$.

The reverse also occurs: f_2 can mix with the noise of f_1 at $f_1 \pm \Delta f_x$ and $f_1 \pm \Delta f_y$ to cause an additional 3-dB increase in noise measured at the mixer's output. This increase occurs because this reverse process generates another spectrum identical in amplitude to that in Figure 10.54; however, the noise of the two oscillators is not correlated except within the phase-locked-loop bandwidth. The mixer takes these two uncorrelated spectrums and adds them at its output, causing an additional 3-dB increase in noise, as shown in Figure 10.55. Then $\mathcal{L}(f_m)$ can be obtained from this spectrum by subtracting 9 dB from the part where the upper and lower noise sidebands are correlated and by subtracting 6 dB from the area where no correlation exists.

It is possible to go back to Figure 10.54 before the addition of 3 dB (due to two uncorrelated oscillators) to see how $S_\theta(f_m) = \Delta\theta_{\mathrm{rms}}^2$ is related to $\mathcal{L}(f_m)$. Since

$$\mathcal{L}(f) = \tfrac{1}{2}\Delta\theta_{\mathrm{rms}}^2 \tag{10.128}$$

and

$$S_\theta(f_m) = \Delta\theta_{\mathrm{rms}}^2 \tag{10.129}$$

we see that the folded-over spectrum of a single oscillator at Δf_x or where the upper and lower sidebands of f_1 are correlated is equal to $S_\theta(f_m)$.
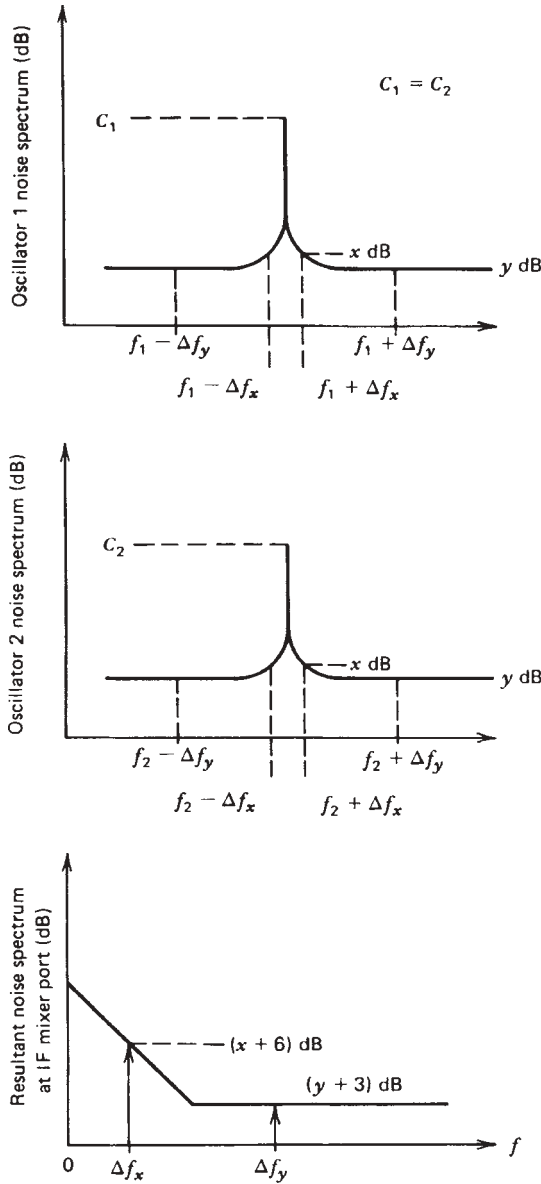
FIGURE 10.54 Resultant noise spectrum due to foldover of spectrum about the carrier for one oscillator.

The noise spectrum of an amplifier would appear as in Figure 10.56. For a moment, it is of interest to discuss the $1/f$ noise spectrum near dc. Noise in amplifiers is often modeled as in Figure 10.57, which was also discussed in Chapter 7. In bipolar amplifiers, e_n is related to the thermal noise of the base spreading resistance:

$$e_n = \sqrt{4kTr_bB} \qquad (10.130)$$
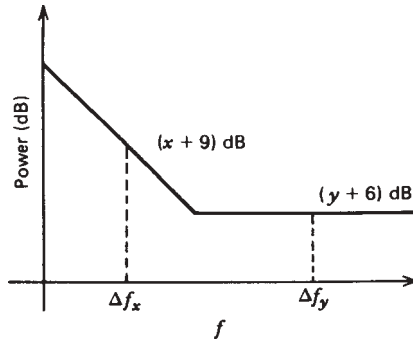
FIGURE 10.55   Power spectrum of mixer IF port as displayed on a spectrum analyzer due to the combined effects of foldover and addition of 3 dB for noise spectrum of two uncorrelated oscillators.
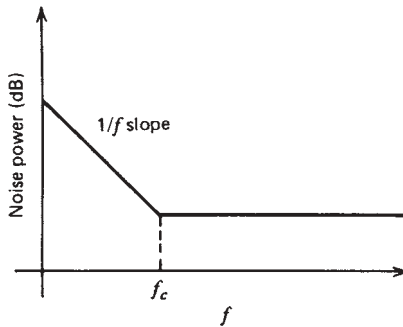
FIGURE 10.56   Noise power versus frequency of a transistor amplifier.
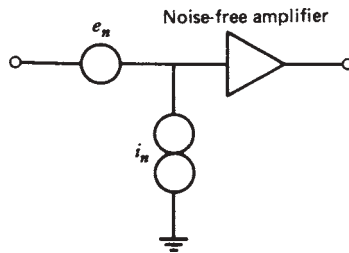
FIGURE 10.57   Equivalent noise sources at the input of an amplifier.

This noise source has a relatively flat frequency response. The i_n noise source is associated with the shot noise in the base current:

$$i_n = \sqrt{2q I_b B} \tag{10.131}$$

This i_n noise generator has associated with it a $1/f$ noise mechanism.

In FET devices, the situation is reversed. The e_n noise generator has a $1/f$ noise component where i_n shows none. It is interesting to note that, in general, the $1/f$ noise corner of bipolar silicon devices is lower than that of silicon JFETs. Silicon JFETs are less noisy than silicon MOSFETS. GaAs MESFETs usually have the highest $1/f$ corner frequencies, which can extend to several hundred megahertz. Carefully selected bipolar devices can have $1/f$ noise corners below 100 Hz.

There are various instruments that can measure e_n and i_n directly with no carrier signal present. These measurement methods would provide a noise plot as in Figure 10.56. However, if a carrier signal is applied to the amplifier, the noise plot would be modified as in Figure 10.58. The low-frequency noise sources can effect the phase shift through the amplifier, causing the $1/f$ phase noise spectrum about the carrier.

10.8.3   Leeson's Oscillator Model

Since an oscillator can be viewed as an amplifier with feedback [10.4], it is helpful to examine the phase noise added to an amplifier that has a noise figure F. Let F be defined by [see (2.1)]

$$F = \frac{(S/N)_{\text{in}}}{(S/N)_{\text{out}}} = \frac{N_{\text{out}}}{N_{\text{in}}G} = \frac{N_{\text{out}}}{it\,GkT\,B} \tag{10.132}$$

Then

$$N_{\text{out}} = FGkTB \tag{10.133}$$

$$N_{\text{in}} = kTB \tag{10.134}$$

where N_{in} is the total input noise power to a noise-free amplifier. The input phase noise in 1 Hz bandwidth at any frequency $f_0 + f_m$ from the carrier produces a phase deviation given by (Fig. 10.59)

$$\Delta\theta_{\text{peak}} = \frac{V_{\text{nRMS1}}}{V_{\text{avsRMS}}} = \sqrt{\frac{FkT}{P_{\text{avs}}}} \tag{10.135}$$
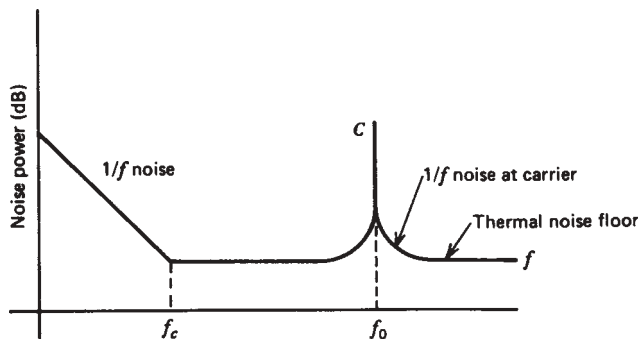
FIGURE 10.58   Noise power versus frequency of a transistor amplifier with an input signal applied.
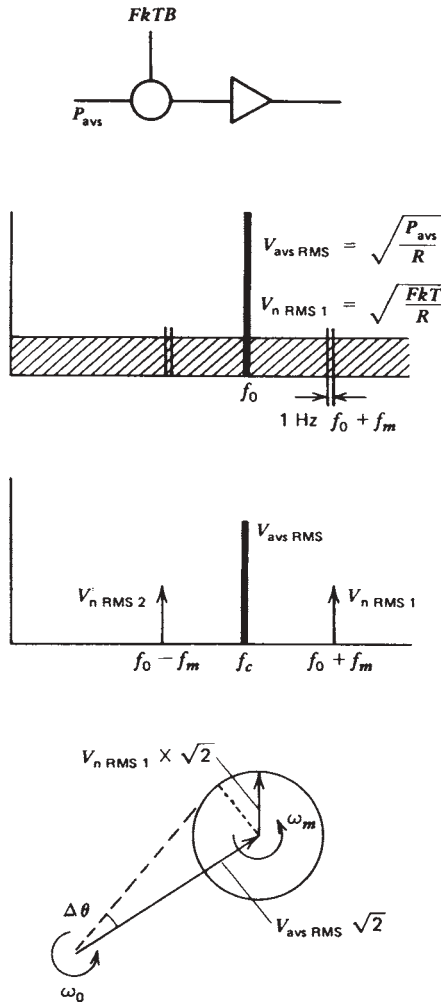
FIGURE 10.59 Phase noise added to carrier.

$$\Delta\theta_{1\text{RMS}} = \frac{1}{\sqrt{2}}\sqrt{\frac{FkT}{P_{\text{avs}}}} \tag{10.136}$$

Since a correlated random phase relation exists at $f_0 - f_m$, the total phase deviation becomes

$$\Delta\theta_{\text{RMS total}} = \sqrt{\frac{FkT}{P_{\text{avs}}}} \tag{10.137}$$

The spectral density of phase noise becomes

$$S_\theta(f_m) = \Delta\theta_{\text{RMS}}^2 = \frac{FkTB}{P_{\text{avs}}} \tag{10.138}$$

where $B = 1$ for 1 Hz bandwidth. Using

$$kTB = -174 \quad \text{dBm/Hz} \qquad (B = 1) \tag{10.139}$$

allows a calculation of the spectral density of phase noise that is far removed from the carrier (i.e., at large values of f_m). This noise is the theoretical noise floor of the amplifier. For example, an amplifier with $+ 10$ dBm power at the input and a noise figure of 6 dB gives

$$S_\theta(f_m > f_c) = -174 \quad \text{dBm} + 6 \quad \text{dB} - 10 \quad \text{dBm} = -178 \quad \text{dB}$$

For a modulation frequency close to the carrier, $S_\theta(f_m)$ shows a flicker or $1/f$ component which is empirically described by the corner frequency f_c. The phase noise can be modeled by a noise-free amplifier and a phase modulator at the input as shown in Figure 10.60. The purity of the signal is degraded by the flicker noise at frequencies close to the carrier. The spectral phase noise can be described by

$$S_\theta(f_m) = \frac{FkTB}{P_{\text{avs}}} \left(1 + \frac{f_c}{f_m} \right) \qquad (B = 1) \tag{10.140}$$

The oscillator may be modeled as an amplifier with feedback as shown in Figure 10.61. The phase noise at the input of the amplifier is affected by the bandwidth of the resonator in the oscillator circuit in the following way. The tank circuit or bandpass resonator has a low-pass transfer function

$$L(\omega_m) = \frac{1}{1 + j(2Q_L\omega_m/\omega_0)} \tag{10.141}$$

where

$$\frac{\omega_0}{2Q_L} = \frac{B}{2} \tag{10.142}$$

is the half bandwidth of the resonator. These equations describe the amplitude response of the bandpass resonator; the phase noise is transferred unattenuated through the
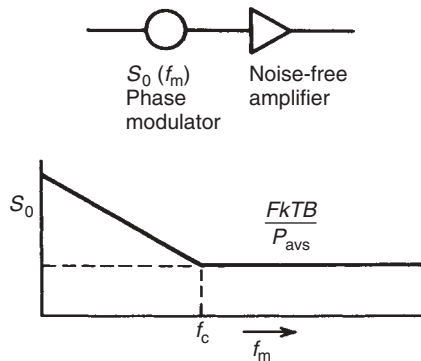
FIGURE 10.60   Phase noise modeled by a noise-free amplifier and a phase modulator.
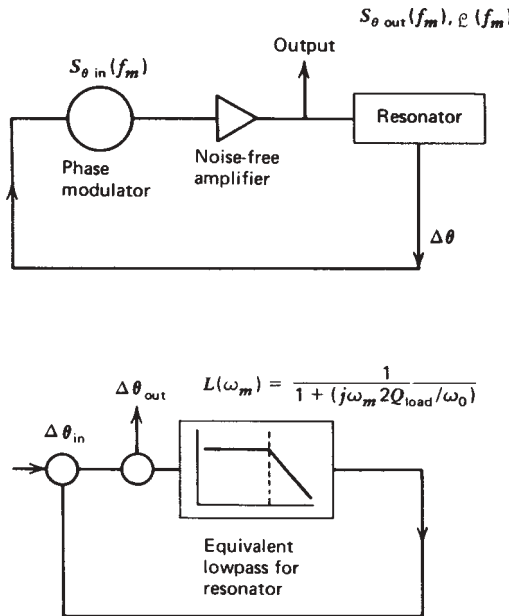
FIGURE 10.61   Equivalent feedback models of oscillator phase noise.

resonator up to the half bandwidth. The closed-loop response of the phase feedback loop is given by

$$\Delta\theta_{\text{out}}(f_m) = \left(1 + \frac{\omega_0}{j2Q_L\omega_m}\right)\Delta\theta_{\text{in}}(f_m) \tag{10.143}$$

The power transfer becomes the phase spectral density

$$S_{\theta\text{out}}(f_m) = \left[1 + \frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2\right]S_{\theta\text{in}}(f_m) \tag{10.144}$$

where $S_{\theta\text{in}}$ was given by (10.140). Finally,

$$\mathcal{L}(f_m) = \frac{1}{2}\left[1 + \frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2\right]S_{\theta\text{in}}(f_m) \tag{10.145}$$

This equation describes the phase noise at the output of the amplifier. The phase perturbation $S_{\theta\text{in}}$ at the input of the amplifier is enhanced by the positive phase feedback within the half bandwidth of the resonator, $f_0/2Q_L$.

Depending on the relation between f_c and $f_0/2Q_L$, there are two cases of interest, as shown in Figure 10.62. For the low-Q case, the spectral phase noise is unaffected by the Q of the resonator, but the $\mathcal{L}(f_m)$ spectral density will show a $1/f^3$ and $1/f^2$ dependence close to the carrier. For the high-Q case, a region of $1/f^3$ and $1/f$ should
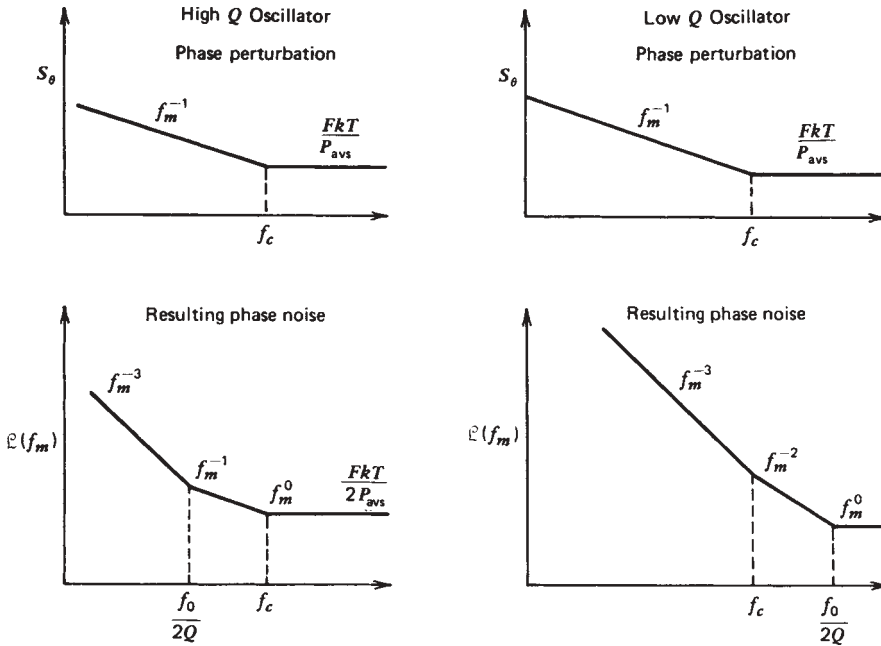
FIGURE 10.62 Oscillator phase noise for high-Q and low-Q resonator viewed as spectral phase noise and as noise-to-carrier ratio versus frequency from the carrier.

be observed near the carrier. Substituting (10.140) in (10.145) gives an overall noise of

$$\mathcal{L}(f_m) = \frac{1}{2} \left[1 + \frac{1}{f_m^2} \left(\frac{f}{2Q_L} \right)^2 \right] \frac{FkT}{P_{\text{avs}}} \left(1 + \frac{f_c}{f_m} \right)$$

$$= \frac{FkTB}{2P_{\text{avs}}} \left[\frac{1}{f_m^3} \frac{f^2 f_c}{4Q_L^2} + \frac{1}{f_m^2} \left(\frac{f}{2QL} \right)^2 + \frac{f_c}{f_m} + 1 \right] \quad \text{(dBc/Hz)} \quad (10.146)$$

Leeson (in 1966) introduced a linear approach for the calculation of oscillator phase noise. His formula [10.1] was extended by Scherer of Hewlett-Packard (HP Application Note), adding the flicker corner frequency calculation to it, and Rohde added the VCO term [10.2]. The phase noise of a VCO is now determined by

$$\mathcal{L}(f_m) = 10 \log \left\{ \left[1 + \frac{f_0^2}{(2 f_m Q_{\text{load}})^2} \right] \left(1 + \frac{f_c}{f_m} \right) \frac{FkT}{2P_{\text{sav}}(1 - Q_{\text{load}}/Q_0)} + \frac{2kTRK_0^2}{f_m^2} \right\}$$

where $\mathcal{L}(f_m)$ = ratio of sideband power in 1 Hz bandwidth at f_m to total power in dB (spectral density)

f_m = frequency offset

f_0 = center frequency

f_c = flicker frequency

Q_{load} = loaded Q of tuned circuit

Q_0 = unloaded Q of tuned circuit; $Q_0 > Q_{\text{load}}$

$$F = \text{noise factor}$$
$$kT = 4.1 \times 10^{-21} \text{ at 300 K (room temperature)}$$
$$P_{\text{sav}} = \text{average power at oscillator output}$$
$$R = \text{equivalent noise resistance of tuning diode (typically 200 } \Omega \text{ to 10 k}\Omega)$$
$$K_0 = \text{oscillator voltage gain}$$

When adding an isolating amplifier, the noise of an *LC* oscillator is determined by

$$S_\phi(f_m) = \frac{a_R F_0^4 + a_E[F_0/(2Q_L)]^2}{f_m^3}$$
$$+ \frac{(2GFkT/P_0)[F_0/(2Q_L)]^2}{f_m^2}$$
$$+ \frac{2a_R Q_L F_0^3}{f_m^2}$$
$$+ \frac{a_E}{f_m} + \frac{2GFkT}{P_0}$$

where G = compressed power gain of loop amplifier
$\quad\quad F$ = noise factor of loop amplifier
$\quad\quad k$ = Boltzmann's constant
$\quad\quad T$ = temperature, K
$\quad\quad P_0$ = carrier power level (W) at output of loop amplifier
$\quad\quad F_0$ = carrier frequency, Hz
$\quad\quad f_m$ = carrier offset frequency, Hz
$\quad\quad Q_L$ = loaded Q of resonator in feedback loop, $= \pi F_0 \tau_g$
$\quad a_R, a_E$ = flicker noise constants for resonator and loop amplifier, respectively

More detailed information about this is given in the original paper by Leeson and in [10.3]. The following table shows the large signal flicker corner frequency f_c as a function of I_c for a typical small-signal microwave BJT (data from Motorola):

I_c (mA)	f_c (kHz)
0.25	1
0.5	2.74
1	4.3
2	6.27
5	9.3

Examining (10.146) gives the four major causes of oscillator noise: the up-converted $1/f$ noise or flicker FM noise, the thermal FM noise, the flicker phase noise, and the thermal noise floor, respectively [10.27, 10.28].

10.8.4 Low-Noise Design

By rearranging the equation and evaluating each term, we obtain, for 1 Hz bandwidth,

$$\mathcal{L}(f_m) = \frac{1}{2}\left[1 + \frac{w_0^2}{4\,\omega_m^2}\left(\frac{P_{\text{in}}}{\omega_0\,W_e} + \frac{1}{Q_u} + \frac{P_{\text{sig}}}{\omega_0\,W_e}\right)^2\right]\left(1 + \frac{\omega_c}{\omega_m}\right)\frac{FkT_0}{P_{\text{avs}}}$$

Input power over reactive power

Phase perturbation

Resonator Q

Flicker effect

Signal power over reactive power

(10.147)

This equation is extremely significant because it contains most of the causes of the phase noise in bipolar and FET-based oscillators.

To minimize the phase noise, the following design rules apply:

1. Maximize the unloaded Q.

Different Types of Sources

Free-running sources:

The classification of free-running microwave oscillators is generally done versus the resonator used in the oscillator and its Q factor

High Phase Noise				Ultralow Phase Noise		
Wide-Band Circuits: $\Delta f/f$ from 5% to 100% (and more)				Fixed Frequency: $\Delta f/f < 1\%$		
Oscillator:	MMIC VCO	Hybrid VCO	YIG oscillator	Hybrid DRO and VC-DRO	Surface acoustic wave oscillator (up to 3 GHz)	Sapphire DRO
•Resonator:	L and C passive elements	Microstrip or coplanar lines	Yttrium iron garnet crystal	Dielectric resonator	Surface acoustic wave resonator	WGM sapphie resonator

| 1 | 10 | 10^2 | 10^3 | 10^4 | $2\,10^4$ | 10^5 |

Low Q factor   Very high Q factor

•:The data given on the axis are strongly approximate; the Q factor highly depends on the technology, the materials, and the packaging.

We present an overview of different free-running sources as a function of technology. The approximate data depend on the Q factor, which again highly

(a)
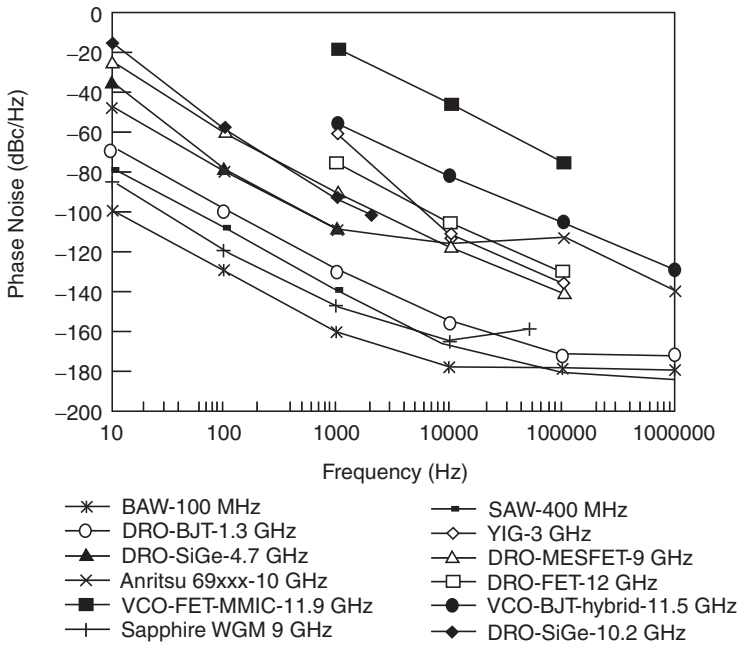
$$L_{equ10GHz}(f) = L_{osc}(f) + 20 \log (10 \text{ GHz}/f_{osc})$$

(b)
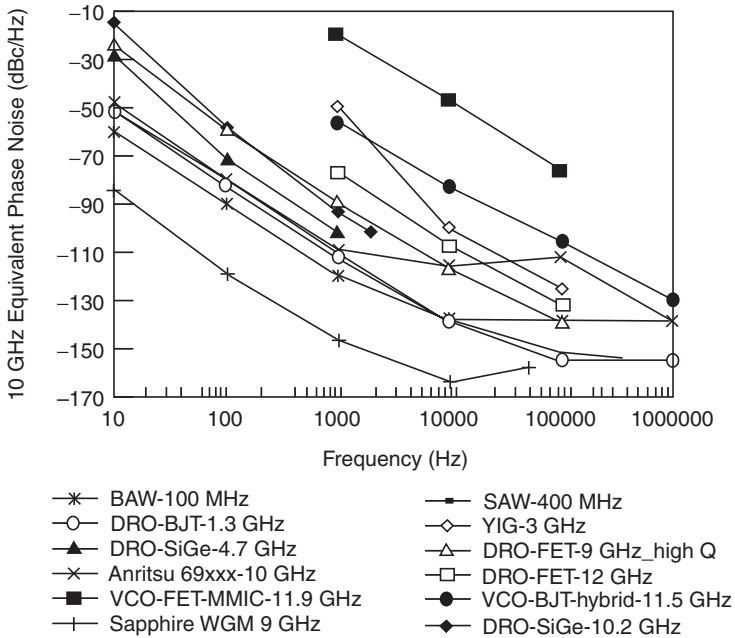
FIGURE 10.63   Survey of published high-frequency oscillator using different topology, show the phase noise as a function of the offset from the carrier.

depends on the technology, the material, and the packaging. The plots in Figures 10.63*a* and *b* are a survey of published high-performance oscillators using different technology and show the phase noise as a function of the offset from the carrier, or its normalized phase noise relative to 10 GHz.

2. Maximize the reactive energy by means of a high RF voltage across the resonator and obtain a low *LC* ratio. The limits are set by breakdown voltages of the active devices and the tuning diodes and the forward-bias condition of the tuning diodes.

    A way to obtain a low *LC* ratio is to use ceramic resonator–based designs; the typical characteristic impedance for those is somewhere around 8 to 15 Ω. An equivalent circuit can be obtained by using microstrip or stripline resonators with low impedances. These are also insensitive to radiation and adjacent components and are much less influenced by design tolerances. The only drawback is that the tuning sensitivity in a VCO is reduced. See Figure 10.64.

3. Avoid saturation at all cost and try to either have limiting or AGC without degradation of *Q*. Isolate the tuned circuit from the limiter or AGC circuit. Use antiparallel tuning diode connections to avoid forward bias.

    Typical cases are either differential circuits or circuits in which the amplifier limiting occurs by dc bias shift. There have been recent discussions to minimize the flicker corner phase noise contribution by using a small conducting angle. Several papers by Lee promote this concept. Its major application should be for MOSFETs and MESFETs. The use of antiparallel diodes is explained in the following references: U. L. Rohde and D. P. Newkirk, *RF/Microwave Circuit Design for Wireless Applications*, Wiley, 2000, T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, Cambridge University Press, 1998, A. Hajimiri and T. H. Lee, *The Design of Low-Noise Oscillators*, Kluwer Academic, 1999.

4. Choose an active device with the lowest noise figure under high-current operation. An example would be a bipolar transistor like the BFP-620, a silicon–germanium HBT which would be biased around 15 to 20% of IC maximum. By doing so, the
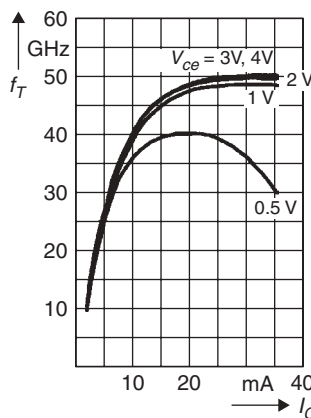
FIGURE 10.64   Bias-dependent transition frequency f_T measured at 2 GHz by monitoring the frequency-dependent current gain. For low-noise operation, one typically sets a bias point in the middle of the curve (e.g., 5 mA). An active dc-stabilizing circuit is recommended.

flicker corner frequency impact is reduced. On the other hand, the device should really produce 10 to 15 dBm output so that the signal-to-noise radio is high. Recent developments of HBTs invite their use in microwave and millimeter-wave applications. On the other hand, semiconductor manufacturers have introduced techniques to make these "hot" devices stabile from dc to light. Unfortunately, this is done at the expense of the noise figure. Therefore, if possible, a medium-power transistor should be used with an f_T not much more than five times the operating frequency. If more aggressive devices are used, typically the phase noise suffers.

While CMOS devices in the past have not been considered for high-performance oscillators, recent trends indicate that they will start to play a role in differential or ring-type oscillators. Various publications give guidelines on how to reduce their noisy performance. Since these devices are not available in discrete form, but rather are part of an IC, one needs to consult a foundry manual. Bell Labs has reported oscillators ranging from 75 to 100 GHz and GaAs FETs at one or more levels of complexity. They have a Shottkey barrier diode from gate to source, similar to silicon NFETs. This diode becomes conductive at about 0.7 V; therefore, the RF voltage swing should not be made too high so the transistor diode becomes conductive. In selecting the GaAs FET, one should contact the manufacturer or factory to obtain a bias-dependent set of flicker corner frequencies. Unfortunately, the designer will find that this is a well-kept secret in most cases because the manufacturer has not measured it.

5. Phase perturbation can be minimized by using high-impedance devices such as FETs, where the signal-to-noise ratio or the signal voltage relative to the equivalent noise voltage can be made very high. This also indicates that in the case of a limiter the limited voltage should be as high as possible.

6. Choose an active device with low flicker noise. The effect of flicker noise can be reduced by RF feedback. An unbypassed emitter resistor of 10 to 30 Ω in a bipolar circuit can improve the flicker noise by as much as 40 dB [10.21]. The proper bias point of the active device is important, and precautions should be taken to prevent modulation of the input and output dynamic capacitance of the active device, which will cause amplitude-to-phase conversion and therefore introduce noise.

   The plot in Figure 10.65 shows the phase noise of a MESFET, both as an amplifier and as an oscillator. Under large-signal conditions, the device gets much noisier. Currently there is no established relationship that allows for conversion of one into the other reliably.

7. The energy should be coupled from the resonator rather than another portion of the active device so that the resonator limits the bandwidth because the resonator is also used as a filter. A dielectric-resonator oscillator using this principle is described later.

8. Finally, a combination of proper resonator and dc biasing is important. Figure 10.66 shows a simulation of phase noise as a function of consistent current and consistent voltage and two different resistors. The consistent voltage at the base implies not that there is no source or emitter resistor but that the base is low resistance. This can be substituted by a regular bias at the base with an RF choke from the base to the biasing circuit and a big capacitor (1 to 100 pF) to ground at the RF cold side. The base to gate is a high-resistance point and
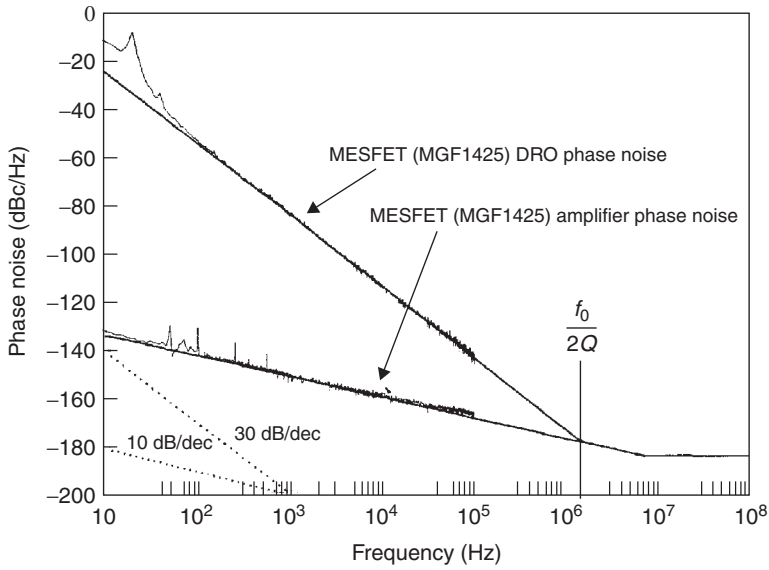
FIGURE 10.65 PM to FM noise conversion in a 4-GHz oscillator.
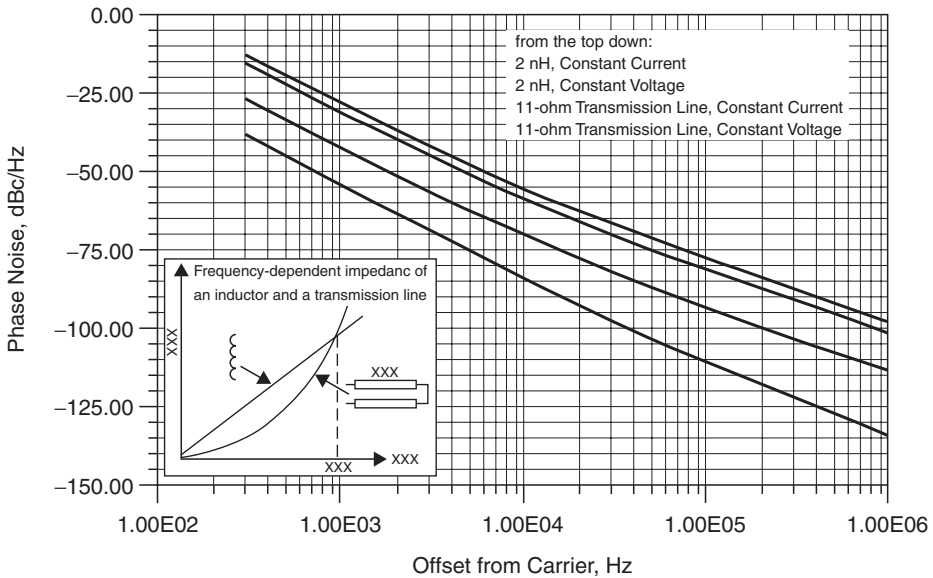
FIGURE 10.66 Transistor oscillators are sensitive to the bias network and to the resonator circuit. As a test we have differentiated constant-current and constant-voltage biasing as well as interchanging inductors with transmission lines. The phase noise improves with the use of a transmission line and a constant-voltage bias source. (A constant-voltage source prevents a dc bias shift. The dual of a constant voltage at the base is a constant-current source at the emitter.)

tends to collect humming and noises, and by short circuiting each dc voltage at the base, the phase noise improves. Likewise, if an inductor is substituted by a low-resistance transmission line, phase noise improves further.

The loading effect of a tuning diode is due to losses, and these losses can be described by a resistor parallel to the tuned circuit.

Tuning diode noise contribution alone!:

It is possible to define an equivalent noise $R_{a,\text{eq}}$ that, inserted in Nyquist's equation

$$V_n = \sqrt{4kT_0R \ \Delta f} \tag{10.148}$$

where $kT_0 = 4.2 \times 10^{-21}$ J at about 300 K, R is the equivalent noise resistor, and Δf is the bandwidth, determines an open noise voltage across the tuning diode. Practical values of $R_{a,\text{eq}}$ for carefully selected tuning diodes are in the vicinity of 100 Ω to 15 kΩ. If we now determine the noise voltage $V_n = \sqrt{4 \times 4.2 \times 10^{-21} \times 200}$, the resulting voltage value is 1.83×10^{-9} V $\sqrt{\text{Hz}}$.

This noise voltage generated from the tuning diode is now multiplied with the modulation sensitivity, resulting in the rms frequency deviation

$$(\Delta f_{\text{rms}}) = K_0 \times (1.83 \times 10^{-9} \text{ V}) \quad \text{in 1 Hz bandwidth} \tag{10.149}$$

To translate this into the equivalent peak-phase deviation,

$$\theta_d = \frac{K_0\sqrt{2}}{f_m}(1.83 \times 10^{-9} \text{ rad}) \quad \text{in 1 Hz bandwidth}$$

or for a typical modulation sensitivity of 2 MHz/V,

$$\theta_d = \frac{5.176 \times 10^{-3}}{f_m} \text{ rad} \quad \text{in 1 Hz bandwidth}$$

For $f_m = 25$ kHz (typical spacing for adjacent channel measurements for FM mobile radios), $\theta_d = 2.07 \times 10^{-7}$. Now this can be converted into the SSB signal-to-noise ratio

$$\mathcal{L}(f_m) = 20 \log_{10} \frac{\theta_d}{2}$$
$$= -133.68 \ \text{ dBc/Hz} \tag{10.150}$$

This is the value typically achieved in the Rohde–Schwarz SMIQ signal generator VCO part and considered state of the art for a free-running oscillator. This evaluation is based only on the last part of the "modernized" Leeson equation.

Let us now examine some test results. If we go back to (10.147), Figure 10.67 shows the noise sideband performance as a function of Q, whereby the top curve with $Q_L = 100$ represents a somewhat poor oscillator and the lowest curve with $Q_L = 100,000$
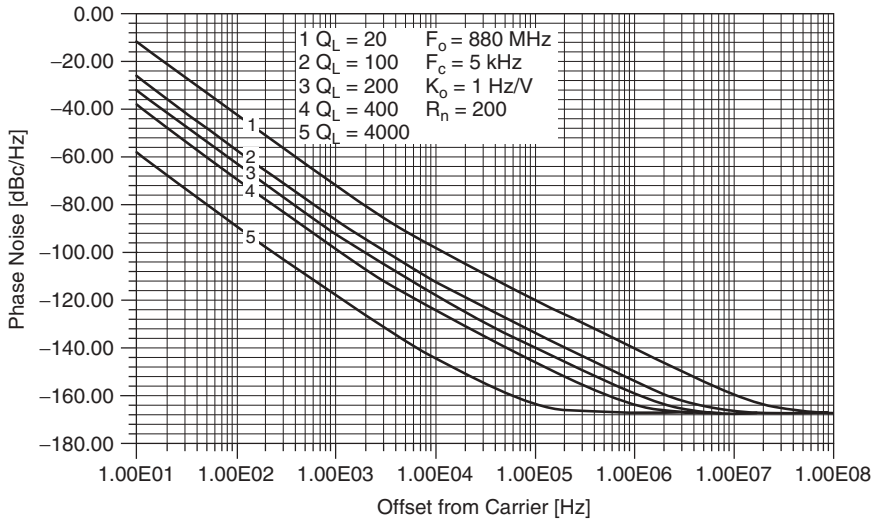
FIGURE 10.67 Predicted phase noise of an 880-MHz oscillator (*not* a VCO) as a function of Q. The final Q (4000) can only be obtained with a large helical resonator and is only a value given for comparison purposes; it is not practically achievable.
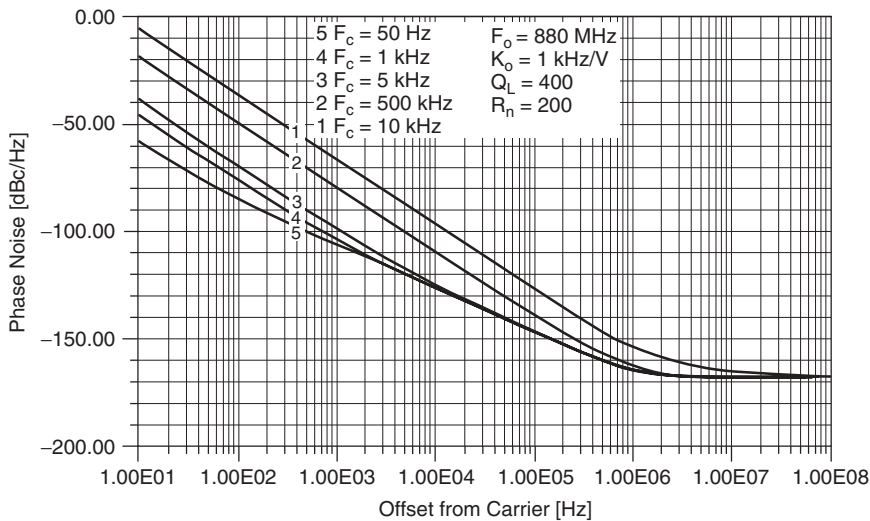
FIGURE 10.68 Predicted phase noise of an 880-MHz oscillator (*not* a VCO) with a resonator Q of 400, varying the flicker corner frequency from 50 Hz (silicon FET) to 10 MHz (GaAsFET).

probably represents a crystal oscillator where the unloaded Q of the crystal was in the vicinity of 3×10^6. Figure 10.68 shows the influence of flicker noise.

Corner frequencies of 1 Hz to 10 kHz have been selected, and it becomes apparent that at around 1 kHz the influence is fairly dramatic, whereas the influence at 20 kHz off the carrier is not significant. Finally, Figure 10.69 shows the influence of the tuning diodes on a high-Q oscillator.
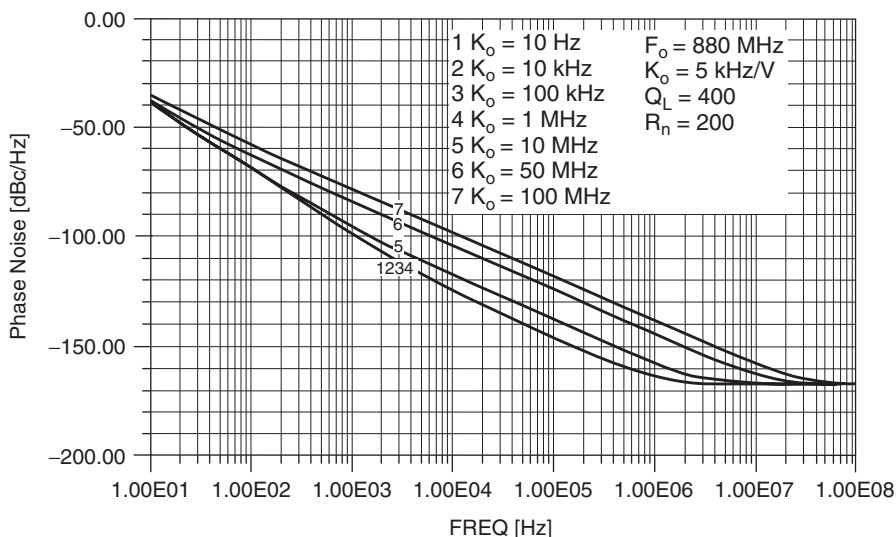
FIGURE 10.69   Predicted phase noise of an 880-MHz VCO with tuning sensitivity ranging from 10 Hz to 100 MHz/V. It *must* be noted that above a certain sensitivity—in this case 10 MHz/V—the phase noise is determined only by the circuit's tuning diode(s) and is no longer a function of the resonator and diode Q.

Curve A uses a lightly coupled tuning diode with a K_0 of 10 kHz/V; the lower curve is the noise performance without any diode. As a result, the two curves are almost identical, which can be seen from the somewhat smeared form of the graph. Curve B shows the influence of a tuning diode at 100 kHz/V and represents a value of -143 dBc/Hz from -155 dBc/Hz, already some deterioration. Curve C shows the noise if the tuning diode results at a 1-MHz/V modulation sensitivity, and the noise sideband at 25 kHz has now deteriorated to -123 dBc/Hz. These curves speak for themselves.

It is of interest to compare various oscillators. Figure 10.70 shows the performance of a 10-MHz crystal oscillator, a 40-MHz LC oscillator, the 8640 cavity tuned oscillator at 500 MHz, the 310- to 640-MHz switched reactance oscillator of the 8662 oscillator, and a 2- to 6-GHz YIG oscillator at 6 GHz.

Neither linear nor nonlinear CAD programs can handle the SSB phase noise prediction. The PLL Design Kit [10.29] has been specifically written to handle low-noise VCO design.

The following is a short synthesis of a VCO using the PLL design kit. The starting parameters are as follows:

Tuning range	3.8–4.2 GHz
Tuning diode hyperabrupt	0.5–2.5 pF
Bipolar transistor	$f_T = 6$ GHz, $I_c = 15$ mA, $h_{fe} = 150$
K_{VCO}	40 MHz/V

Based on these parameters, the data in Table 10.6 were calculated. Table 10.6 shows a calculation of the elements used to cover the specified range. Based on the dc input power, we have calculated the output power. The SSB phase noise was calculated
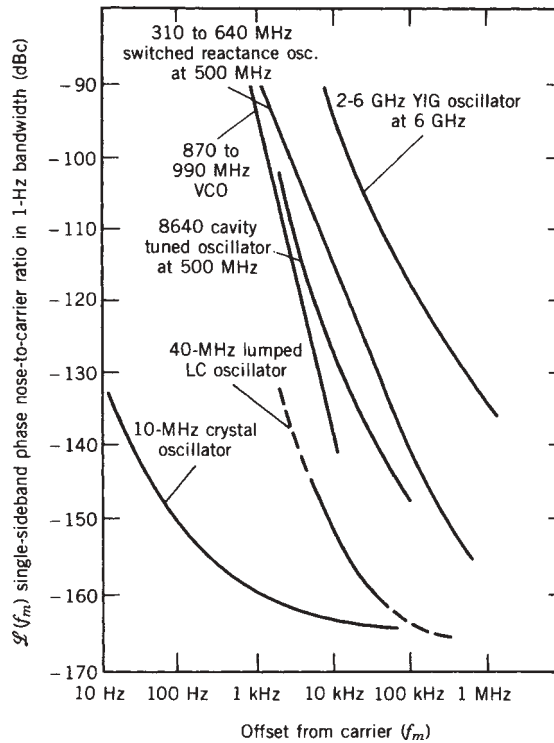
FIGURE 10.70   Comparison of noise sideband performance of a crystal oscillator, LC oscillator, cavity-tuned oscillator, switched reactance oscillator, and YIG oscillator.

TABLE 10.6   Calculation of VCO Tuning Range

$F_{min} = 3800$ MHz
$F_{max} = 4200$ MHz
Center range $= 4000$ MHz
Tuning ratio $= 1.105$
$C_{min}(\text{at} V_{max})$ of tuning diode $= 0.5$ pF
$C_{max}(\text{at} V_{min})$ of tuning diode $= 2$ pF
Bipolar transistor chosen:
   Transistor is operated at $I_c = 6$ mA, $V_c = 8$ V
   Cutoff frequency of transistor $= 12$ GHz at 7 mA
Theoretical output power based on Fourier analysis $= 21$ mW or 13 dBm
Board stray capacitance $= 1$ pF
Stripline oscillator used
Transmission line $Z = 50$ Ω
Half-wave circuit:
   $C_{in} = 2$ pF, $C_{out}(\text{min}) = 0.5$ pF
   Center conductor $= 15.3$ mm
   $C_{out}(\text{max}) = 0.774$ pF
Frequency-compensated microstrip calculation:
   Substrate $\varepsilon = 2.3$
   Substrate thickness $= 1.6$ mm
   Width $= 4.76$ mm
   Mechanical length $= 10.1$ mm

first for a MESFET with a flicker frequency of 10 MHz and a noise figure of 10 dB, plotted in Figure 10.71. The first portion of the phase plot is horizontal and indicates the incidental noise of the oscillator, which is 40 Hz. On a spectrum analyzer this would look similar in linear form. There is no modulation effect of pickup shown. Figure 10.72 shows the phase noise for the same oscillator using a Texas Instruments bipolar HBT, described in Figure 3.9 ($f_c = 5$ kHz, $F = 10$ dB).

Using capacitive feedback and loose coupling, Figure 10.73 shows the oscillator in a grounded-base configuration and inductive output coupling.
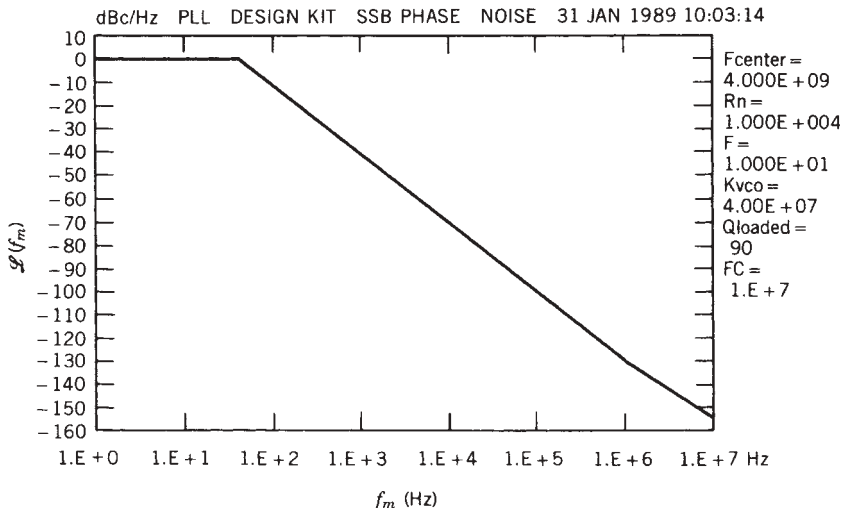
FIGURE 10.71   Single-sideband phase noise for a 4-GHz oscillator using element values as shown in Table 10.6 using a MESFET.
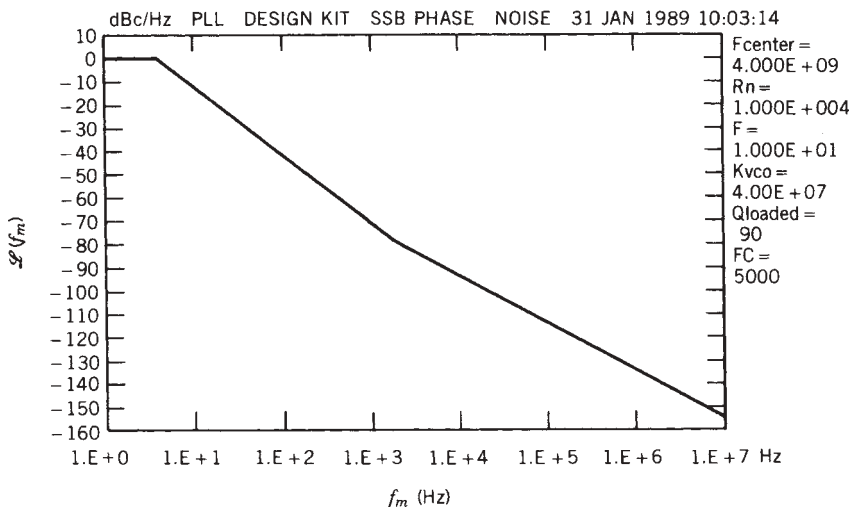
FIGURE 10.72   Single-sideband phase noise for a 4-GHz oscillator with a bipolar HBT using Table 10.6.
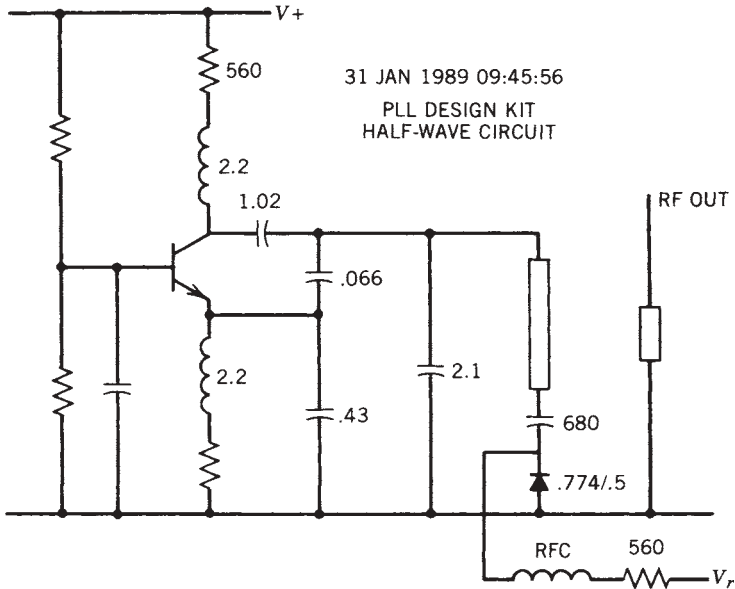
FIGURE 10.73   Circuit of a 4-GHz oscillator using Table 10.6.
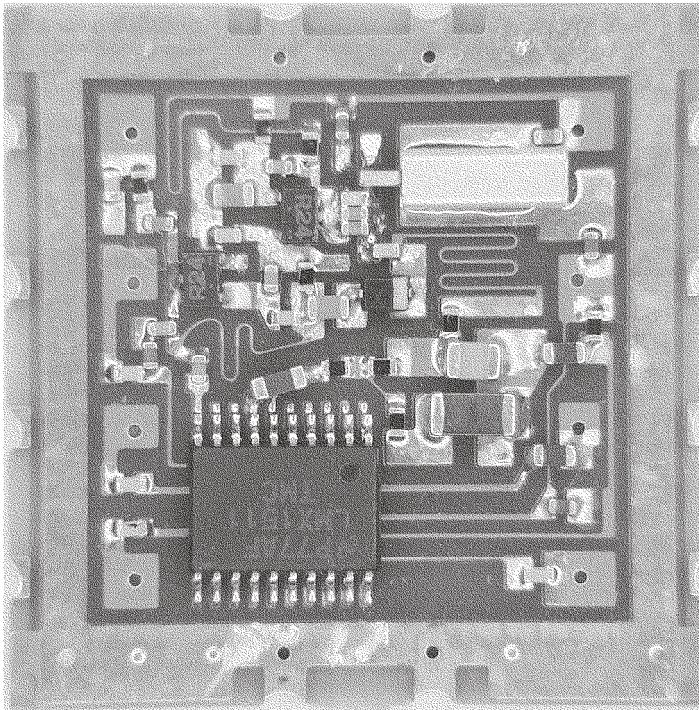
FIGURE 10.74   Miniature PLL-based synthesizer manufactured by Synergy Microwave Corporation, Paterson, NJ.

A 700- to 900-MHz VCO used in cellular telephones is shown in Figure 10.74. Figure 10.74 is a complete synthesizer consisting of a ceramic resonator-based oscillator and a PLL chip. The resonator is in the right upper corner and combines the best phase noise with the best microphonics suppression. The oscillator transistor is a Siemens 25-GHz fT.

Figures 10.75 and 10.76 show a cavity-tuned 4- to 6-GHz oscillator. In today's technology, these type of oscillators are being replaced by wide-band VCOs and stabilized with wide-band PLL systems using 1 to 10 MHz loop bandwidth.
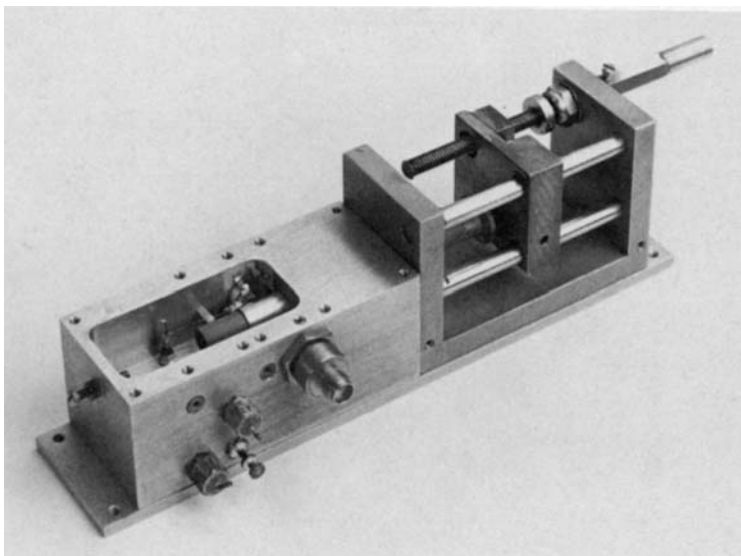
FIGURE 10.75   A 4- to 6-GHz cavity-tuned oscillator.
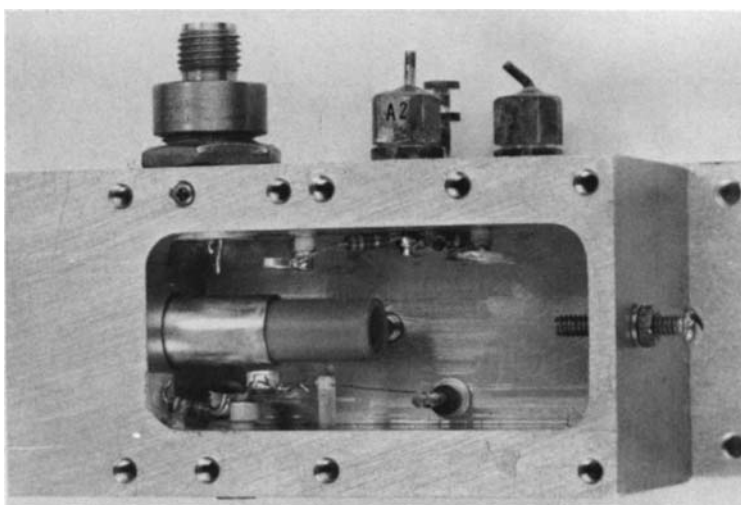
FIGURE 10.76   Close-up of Figure 10.75.

10.9   ANALYTIC APPROACH TO OPTIMUM OSCILLATOR DESIGN USING *S* PARAMETERS

Since an oscillator is often operating at the maximum output power, the small-signal parameters may not be accurate for a precise design. For this reason, designers may use a large-signal parameter set for power amplifier and oscillator designs. Usually, the most significant effect under large-signal drive is a reduction in S_{21} and changes in S_{22}.

Several oscillator design procedures have been reported [10.7–10.9, 10.30, 10.31] using large-signal parameters. Using y or z parameters, the embedding conditions given in Figure 10.77 predict the maximum output power from the oscillator. These solutions are found from the two-port equations of the networks in Figure 10.37 and the condition of maximum output power. For the Π network the y parameters are used, and the T network requires z parameters. The four degrees of freedom in the oscillator design are B_1, B_2, B_3, and G_n for the Π, or parallel, solutions and X_1, X_2, X_3, and R_n for the T, or series, solutions. This gives six oscillator designs for the active two-port without considering the load value or stability factor. We are forcing the circuit to be resonant and deliver power to a resistor (probably different from 50 Ω) [6.32].

An example of this calculation for a 500-μm GaAs MESFET at $V_{DS} = 8$ V, $I_{DS} = 50$ mA (DXL 3501A) is given in Figure 10.78 using lumped elements at 10 GHz. The S parameters for this example are

$$S_{11} = 0.66 \underline{/-143°}$$
$$S_{12} = 0.071 \underline{/117°}$$
$$S_{21} = 1.26 \underline{/46°}$$
$$S_{22} = 0.74 \underline{/-59°}$$

The series resonant case with the resistor in the gate gives nearly 50 Ω (case 4), but there is no requirement on the load resistor. Another description of these six oscillators is power out of the gate, drain, or source and power out of the gate–source, drain–source, or drain–gate.

Another analytic approach due to Gilmore and Rosenbaum [6.9] uses large-signal S parameters. The upper portion of Figure 10.79 shows a two-port network described by large-signal S parameters which represent the active element used in the oscillator. The quantity V_1^+ is the power incident on port 1 of the device; V_2^+ is the power incident on port 2.

Here, V_1^+ is fixed at the outset of the oscillator design to be equal to the amplitude used during measurement of S_{11} and S_{21}. It may be set at the point of maximum power-added efficiency as described by Pucel et al. [10.33] or Johnson [10.8] or through simulations as was done here. Similarly, V_2^+ is unknown at the outset. However, at optimum power, V_2^+ should be minimized. Hence a small level of V_2^+ should be assumed in specifying $S_{12}(V_2^+)$ and $S_{22}(V_2^+)$ at the outset. This can be checked in the final design.

The complex voltage V_2^- is a free parameter. By defining the gain

$$A = \frac{V_2^-}{V_1^+} = A_R + jA_I \tag{10.151}$$

the power delivered to the external network can be maximized as a function of A.

G_L	$C_1 + A_r C_3 + A_i C_4$	$(C_1 + A_r C_3 + A_i C_4)/|A|^2$	$(C_1 + A_r C_3 + A_i C_4)/|A - 1|^2$
B_1	$C_2 + (1 - A_r)(C_4 + C_3 A_r/A_i)$	$C_1(A_r - 1)/A_i + C_2$	$(C_1 + C_3)A_r/A_i + C_2 + C_4$
B_2	$C_3(A_r - 1)/A_i + C_4$	$[C_1(A_r - |A|^2)/A_i - A_i C_3 + A_r C_4]/|A|^2$	$-(C_1 + C_3)/A_i$
B_3	$-C_3 A_r/A_i - C_4$	C_1/A_i	$[C_1 - (1 - A_r)G_L]/A_i$

where: $C_1 = -\text{Re}(Y_{11} + AY_{12})$ $C_3 = -\text{Re}(Y_{21} + AY_{22})$ $A = A_r + jA_i$

$C_2 = -\text{IM}(Y_{11} + AY_{12})$ $C_4 = -\text{IM}(Y_{21} + AY_{22})$ $-(Y_{21} + Y_{12}^*)/2\,\text{Re}\,Y_{22}$

(a)

R_L	$D_1 + F_r D_3 + F_i D_4$	$(D_1 + F_r D_3 + F_i D_4)/|F|^2$	$(D_1 + F_r D_3 + F_i D_4)/|1 + F|^2$
X_1	$D_2 - (1 + F_r)(D_4 + D_3 F_r/F_i)$	$D_1(1 + F_r)/F_i + D_2$	$(D_1 - D_3)F_r/F_i + D_2 - D_4$
X_2	$-D_3(1 + F_r)/F_i - D_4$	$(D_1(F_r + |F|^2)/F_i - F_i D_3 + F_r D_4)/|F|^2$	$(D_1 - D_3)/F_i$
X_3	$D_3 F_r/F_i + D_4$	$-D_1/F_i$	$[(1 + F_r)(D_4 - (D_1 - D_3)F_r/F_i) - F_i D_1]/|1 + F|^2$

where: $D_1 = -\text{Re}(Z_{11} + FZ_{12})$ $D_3 = -\text{Re}(Z_{21} + FZ_{22})$ $F = F_r + jF_i$

$D_2 = -\text{Im}(Z_{11} + FZ_{12})$ $D_4 = -\text{Im}(Z_{21} + FZ_{22})$ $F = (Z_{21} - AZ_{11}/(AZ_{12} - Z_{22})$

(b)

FIGURE 10.77 Optimum embedding elements for six oscillator structures: (*a*) three shunt oscillators; (*b*) three series oscillators. (From Ref. 10.7.)

Consider the device described by its large-signal S parameters embedded in an external network as shown in Figure 10.79. The conditions for oscillation are

$$(Z_{in})\text{device}|_1 = -(Z_{in})\text{network}|_1$$

$$(Z_{in})\text{device}|_2 = -(Z_{in})\text{network}|_2$$

$$(10.152)$$
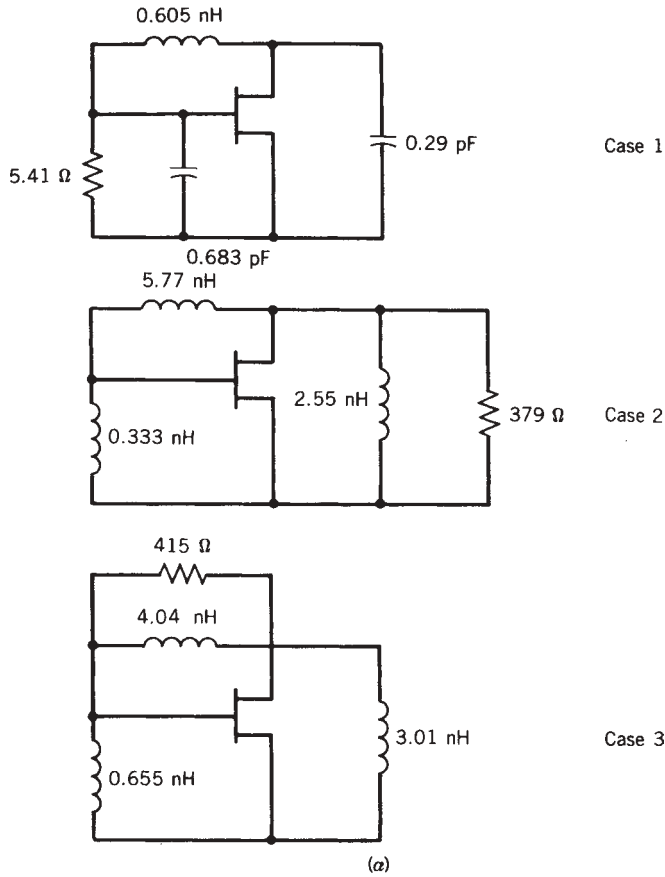
FIGURE 10.78 Six oscillator structures at 10 GHz for DXL-3501A GaAs MESFET: (*a*) three shunt oscillators; (*b*) three series oscillators.

corresponding to the conditions

$$V_{1N}^+ = V_1^- \qquad \text{and} \qquad V_{1N}^- = V_1^+ \tag{10.153a}$$

$$V_{2N}^+ = V_2^- \qquad \text{and} \qquad V_{2N}^- = V_2^+ \tag{10.153b}$$

where $(Z_{\text{in}})\text{device}|_1$ is the device input impedance at port 1 and $(Z_{\text{in}})\text{network}$ is the external embedding network input impedance at port 1. For example, port 1 might represent the gate of a common-source FET and port 2 the drain.

The device is described by its large-signal *S* parameters, each assumed to be a function of a single variable:

$$V_1^- = \mathcal{S}_{11}(V_1^+)V_1^+ + \mathcal{S}_{12}(V_2^+)V_2^+ \tag{10.153c}$$

$$V_2^- = \mathcal{S}_{21}(V_1^+)V_1^+ + \mathcal{S}_{22}(V_2^+)V_2^+ \tag{10.153d}$$

(b)
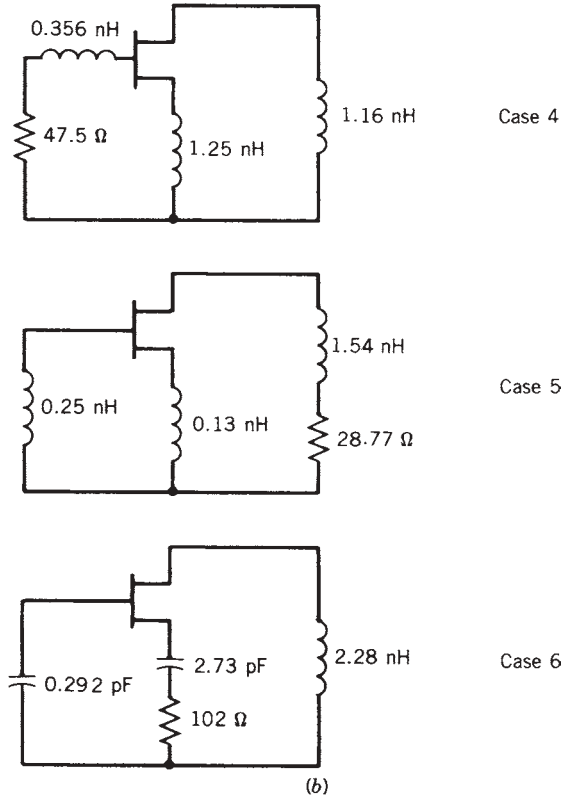
FIGURE 10.78   (*continued*)
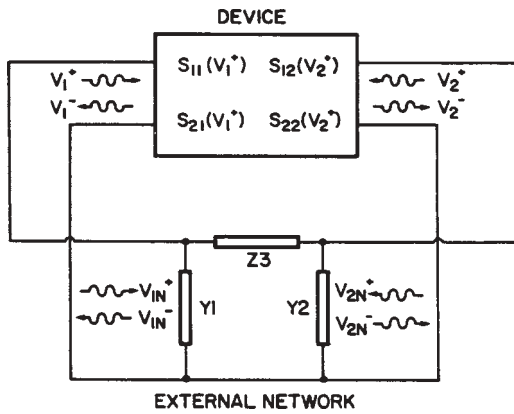
FIGURE 10.79   Shunt oscillator topology. The device is represented by large-signal *S* parameters. The incident and reflected voltage waves are shown. (From Ref. 10.9 © IEEE 1983.)

The linear embedding network is best described by inverse *S* parameters. Let $\mathcal{S}^{-1}$ represent the inverse *S* matrix of the embedding network. Then

$$V_{1N}^{+} = \mathcal{S}_{11}^{-1} V_{1N}^{-} + \mathcal{S}_{12}^{-1} V_{2N}^{-}$$
$$V_{2N}^{+} = \mathcal{S}_{21}^{-1} V_{1N}^{-} + \mathcal{S}_{22}^{-1} V_{2N}^{-}$$

(10.154)

which become, using the conditions for oscillation (10.153),

$$V_{1}^{-} = \mathcal{S}_{11}^{-1} V_{1}^{+} + \mathcal{S}_{12}^{-1} V_{2}^{+}$$
$$V_{2}^{-} = \mathcal{S}_{21}^{-1} V_{1}^{+} + \mathcal{S}_{22}^{-1} V_{2}^{+}$$

(10.155)

Substituting $V_{2}^{-} = A V_{1}^{+}$ into (10.153d) gives

$$V_{2}^{+} = \frac{A - S_{21}(V_{1}^{+})}{S_{22}(V_{2}^{+})} V_{1}^{+}$$

(10.156)

Equating (10.153c) and (10.153d) and (10.155) and using (10.156) give the design equations

$$S_{22}\mathcal{S}_{11}^{-1} + \mathcal{S}_{12}^{-1}(A - S_{21}) - S_{11}S_{22} + S_{12}S_{21} - AS_{12} = 0$$
$$S_{22}\mathcal{S}_{21}^{-1} + \mathcal{S}_{22}^{-1}(A - S_{21}) - AS_{22} = 0$$

(10.157)

This set of four equations (using real and imaginary parts) describes the condition for oscillation. Provided that *A* is suitably chosen so that the device generates power, the required network conditions are completely described by (10.157).

If it is desired to extend the reference planes of the device past the terminals at which the device was characterized (e.g., the FET bond wires), the extension is easily incorporated and can, if desired, be optimized for a given set of load conditions.

Let the length of the line added at the gate be θ_1 and at the drain θ_2. If the characteristic impedances of the lines is Z_0, the incident waves V_1^+ and V_2^+, and hence the large-signal device parameters, normalized to Z_0, are unaffected. The *S* parameters that should be used in (10.157) for the device are then

$$[S] = \begin{bmatrix} S_{11}e^{-j2\theta_1} & S_{12}e^{-j(\theta_1+\theta_2)} \\ S_{21}e^{-j(\theta_1+\theta_2)} & S_{22}e^{-j2\theta_2} \end{bmatrix}$$

(10.158)

where θ_1 and θ_2 are the electrical lengths of the lines and can be chosen as variables (if desired).

The *S* parameters of the linear network are most easily found by first cascading the transmission matrices of the three component elements, normalized to Z_0. In the example considered here, the external network is a Π (shunt) topology, as shown in Figure 10.79. The series oscillator, in which the external circuit has a T topology, can be analyzed in the same way.

For the shunt network,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y_1 & 1 \end{bmatrix}\begin{bmatrix} 1 & Z_3 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ Y_2 & 1 \end{bmatrix} = \begin{bmatrix} 1 + Z_3Y_2 & Z_3 \\ Y_1 + Y_2 + Y_1Y_2Z_3 & 1 + Y_1Z_3 \end{bmatrix}$$

(10.159a)

By conventional conversion to the S matrix and simple matrix inversion, the inverse S matrix of the embedding Π network is then

$$
\mathcal{S}^{-1} = \frac{1}{(Y_1 + Y_2) + Z_3(1 - Y_2)(1 - Y_1) - 2}
$$
$$
\times \begin{bmatrix} Z_3(1 + Y_1)(1 - Y_2) - (Y_1 + Y_2) & -2 \\ -2 & Z_3(1 - Y_1)(1 + Y_2) - (Y_1 + Y_2) \end{bmatrix}
$$
$$(10.159b)$$

After substitution of $[S]$ and $[\mathcal{S}^{-1}]$ into the four equations (10.157), four of the eight unknowns $(G_1 + jB_1,\ G_2 + jB_2,\ R_3 + jX_3,\ \theta_1,\ \theta_2)$ are determined. By arbitrarily determining the other four unknowns by circuit constraints (such as specifying the load impedance, taking the embedding elements reactive, and physical realizability constraints), the circuit can be optimized through choice of A to deliver maximum power into the load. The circuit is found simply through solution of (10.157) using standard nonlinear root-finding methods.

Optimization of $A = V_2^-/V_1^+$, keeping V_1^+ constant, requires that V_2^- be varied in both magnitude and phase until the power delivered to the external network is a maximum. Referring to Figure 10.79, the power delivered to the load is given by

$$
\begin{aligned}
P &= (|V_{1N}^+|^2 - |V_{1N}^-|^2) + (|V_{2N}^+|^2 - |V_{2N}^-|^2) \\
&= |V_1^-|^2 - |V_1^+|^2 + |V_2^-|^2 - |V_2^+|^2 \\
&= |V_1^+|^2\,|S_{11}|^2 + 2\,\mathrm{Re}\left(\frac{S_{11}^* S_{12}(A - S_{21})}{S_{22}}\right) + \frac{|S_{12}|^2 - 1}{|S_{22}|^2}(|A - S_{21}|^2) + |A|^2 - 1
\end{aligned}
$$
$$(10.160a)$$

Using $|x|^2 = x \cdot x^*$, $A = A_R + jA_I$, and (10.156), Eq. (10.16a) becomes

$$
\begin{aligned}
P &= |V_1^+|^2\,|S_{11}|^2 + \frac{S_{11}S_{12}^*}{S_{22}^*}(A_R - jA_I - S_{21}^*) + \frac{S_{12}S_{11}^*}{S_{22}} \\
&\quad \times (A_R + jA_I - S_{21}) + A_R^2 + A_I^2 - 1 \\
&\quad + \frac{|S_{12}|^2 - 1}{|S_{22}|^2} \times (A_R^2 - A_R S_{21}^* + A_I^2 - jA_I S_{21}^* - A_R S_{21} + jA_I S_{21} + |S_{21}|^2)
\end{aligned}
$$
$$(10.160b)$$

The power has a local turning point at $\partial P/\partial A_R = 0$ and $\partial P/\partial A_I = 0$, giving

$$
\mathrm{Re}\left[\frac{S_{12}^* S_{11}}{S_{22}^*}\right] + A_R\left[1 + \frac{|S_{12}|^2 - 1}{|S_{22}|^2}\right] - \left[\frac{|S_{12}|^2 - 1}{|S_{22}|^2}\right]\mathrm{Re}\,S_{21} = 0
$$
$$
\mathrm{Im}\left[\frac{S_{12}^* S_{11}}{S_{22}^*}\right] + A_I\left[1 + \frac{|S_{12}|^2 - 1}{|S_{22}|^2}\right] - \left[\frac{|S_{12}|^2 - 1}{|S_{22}|^2}\right]\mathrm{Im}\,S_{21} = 0 \quad (10.161)
$$

so that

$$
A_{\mathrm{opt}} = \frac{1}{|S_{22}|^2 + |S_{12}|^2 - 1}(|S_{12}|^2 S_{21} - S_{21} - S_{22}S_{11}S_{12}^*) \tag{10.162}
$$

Now, P is a maximum if the second derivatives are negative, which is true if

$$|S_{12}|^2 + |S_{22}|^2 < 1 \tag{10.163}$$

This condition will almost always be satisfied for the FET.

It will be noted in (10.162), on substituting for $[S]$ from (10.158), that the magnitude of A_{opt} is independent of the line lengths θ_1 or θ_2. Similarly, the coefficient of $|V_1^+|$ in (10.156) and of $|V_1^+|^2$ in (10.160a) is unchanged by the addition of lengths of line on either side of the transistor. Thus, for a given transistor, the optimum gain and power out is set solely by the FET S parameters. As would be expected intuitively, the line lengths serve only as impedance transformers.

For typical GaAs MESFET, the equation for A_{opt} can be further simplified to

$$A_{opt} \simeq \frac{S_{21}}{1 - |S_{22}|^2} \tag{10.164}$$

when S_{12} is a small number. This result states the optimum voltage gain is the S_{21} or 50-Ω voltage gain divided by the output mismatch factor, $1 - |S_{22}|^2$. For a transistor with S_{22} nearly zero, A_{opt} is simply S_{21}.

A simple computer program was written to optimize, with respect to power, the design of an FET oscillator into a 50-Ω load. For reactive embedding elements ($G_1 = R_3 = 0$) and $Y_2 = 1$, the unknown quantities are θ_1, θ_2, B_1, and X_3. Such a case is completely constrained and is illustrated in Figure 10.80.

This design is practical from the viewpoint of a carrier-mounted FET with external feedback, in which the feedback points are movable. Note further that no output load transformer is required, since Y_2 is specified directly to represent 50 Ω. A short computer program was written to calculate the device S parameters for assumed values of θ_1 and θ_2 using (10.158) and the network inverse S matrix for assumed values of B_1 and X_3 using (10.159b). These values were then substituted into (10.157) and the equations solved using a standard quasi-Newton routine as a function of the variables θ_1, θ_2, B_1, and X_3.

From the viewpoint of implementation, it is easiest to treat the feedback element Z_3 as a transmission line of some suitable characteristic impedance. The software
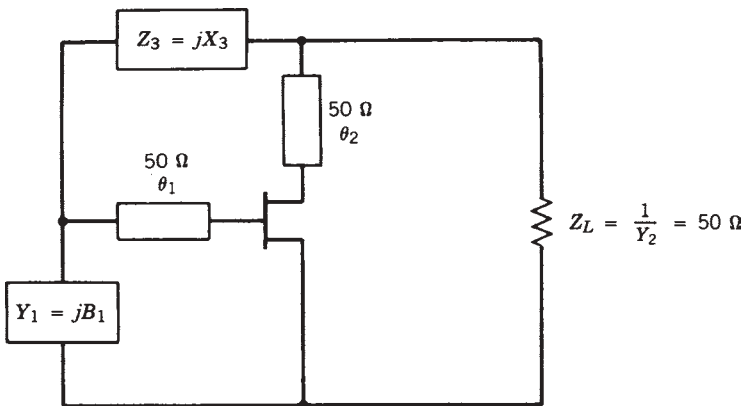
FIGURE 10.80   Generalized oscillator circuit for the design example given.

was modified so that the unknown parameter X_3 was replaced by l_3, the length of the required feedback transmission line. The network inverse S matrix (10.159b) is still easily calculable, although less simply, due to the more complicated form of the transmission matrix for a transmission line rather than a series element.

The design process then proceeds as follows:

1. The large-signal device S parameters are modeled (or measured) at a selection of incident powers at both ports.
2. A value for V_1^+ is chosen. This fixes $S_{11}(V_1^+)$ and $S_{21}(V_1^+)$. A value of V_2^+ is estimated to set $S_{12}(V_2^+)$ and $S_{22}(V_2^+)$.
3. The parameter A_{opt} is calculated from (10.162) using only the chosen device S parameters; the ratio $|V_2^+|/|V_1^+|$ can then be found from (10.156) and the ratio $Z_0 P/|V_1^+|^2$ from (10.160a). All these quantities are independent of the device reference planes (i.e., of the transmission line lengths ultimately chosen). This, then, enables the designer:
   a. To check that the output S parameters $S_{12}(V_2^+)$ and $S_{22}(V_2^+)$ that were used correspond to the actual value of V_2^+ calculated
   b. To calculate the oscillator output power at the selected value of V_1^+
   By varying the value of V_1^+ selected in step 2, a curve of output power versus incident input power (as done by Johnson [10.8] or Pucel [10.33]) may be generated. Each such output power is the maximum deliverable power to the load at the selected value of V_1^+.
4. The value of V_1^+ that gives the peak output power is used (with corresponding V_2^+) to set the S parameters at the device operating point. The external element values are then found through solution of (10.157).

A large-signal model [10.8] was used to predict the S parameters of the NEC 869177 FET employed in the construction of two oscillators which operated at 5 GHz. This transistor has a nominal I_{DSS} of 330 mA and a pinchoff voltage around 5 V. The transistor S parameters are given in Table 10.7.

Table 10.8 illustrates these steps in the design of a 5-GHz oscillator. The first column groups blocks of data according to the values of V_1^+ (incident input power) selected. The final line in each block, indicated by a check, is that for which the correct value of V_2^+ (incident power at the output) has been obtained. Thus in the first line of block 1, an incident input power of 17.7 dBm was chosen and an incident output power of 19.9 dBm estimated. This estimate for the power incident on the output port might be based on a transistor with a gain of 6 dB operating into a net output reflection

TABLE 10.7 S Parameters for NEC 869177[a]

$S_{11} = 0.73\underline{/-116°}$
$S_{21} = 1.95\underline{/85°}$
$S_{12} = 0.048\underline{/-45°}$
$S_{22} = 0.50\underline{/-42°}$

[a] At $V_{DS} = 7.5$ V, $V_{GS} = -3.0$ V, $I_{DSS} = 330$ mA, and $V_p = -5$ V.

TABLE 10.8   Design Values for the 5-GHz Oscillator

Block		Input Power Selected, $\|V_1^+\|^2$ (dBm)	Incident Power at Output, $\|V_2^+\|^2$ (dBm)		A_{opt}	$\dfrac{Z_0 P_{\text{LOAD}}}{\|V_1^+\|^2}$	Calculated P_{LOAD} (mW)
			Estimated	Calculated			
1	×	17.7	19.9	24.6	$2.77 + j1.56$	5.16	—
	√	17.7	21.2	20.9	$2.07 + j1.37$	4.00	235
2	×	19.3	19.9	26.0	$2.67 + j1.54$	4.86	—
	√	19.3	22.0	21.1	$1.82 + j1.35$	3.52	300
3	×	20.7	26.4	16.4	$0.678 + j1.45$	2.05	—
	×	20.7	19.9	26.1	$2.30 + j1.36$	3.55	—
	×	20.7	23.4	19.1	$1.27 + j1.24$	2.28	—
	√	20.7	22.0	21.3	$1.51 + j1.25$	2.55	300
4	×	22.0	23.4	19.3	$0.998 + j1.17$	1.61	—
	√	22.0	22.0	21.4	$1.25 + j1.15$	1.82	288

coefficient of 0.65. The *S* parameters are thus defined since the incident powers are known, and step 3 of the design process can be performed. From (10.162), A_{opt} is $2.77 + j1.56$; using this in (10.156) gives V_2^+ corresponding to 24.6 dBm. Since our initial estimate of V_2^+ was only 19.9 dBm, the initial guess for incident power at port 2 was modified upward in the second line of block 1, changing $S_{12}(V_2^+)$ and $S_{22}(V_2^+)$, and the cycle repeated; after recalculation, the new incident output power is found to be close to that initially assumed. As shown, the magnitude of *A* is 2.27 in this case, and the ratio $Z_0 P/\|V_1^+\|^2$, from (10.160a), is 4.00, giving a power of 235 mW delivered to the 50-Ω load for the selected V_1^+ of 17.7 dBm. This is the maximum available power from the device under the chosen terminal conditions (i.e., for the given *S* parameters used).

Blocks 2, 3, and 4 then vary the terminal conditions by selecting higher values of incident input power. The output power does not continue to increase beyond bound with V_1^+ but reaches a peak of 300 mW in blocks 2 and 3. This is then the desired operating point. Block 2 was used instead of block 3 because of the higher accuracy in the application of *S* parameters at the lower input power level, since the FET is not saturated as much. The reason for the peaking of output power can be seen in Figure 10.81, which shows the measured gain–saturation characteristics of the unmatched transistor chip. The net available power from the device, $P_{\text{out}} - P_{\text{in}}$, shown by the lower curve, indicates that the available output power will peak for some value of incident power. The shape of this experimentally measured curve correlates well with the column labeled calculated P_{LOAD} in Table 10.8, even though the matching conditions are different in the two cases.

The values of the *S* parameters at this operating point are used in a root-finding routine to solve (10.157) for these elements. The routine used here was a standard IMSL FORTRAN routine, ZXMIN. It was found that convergence to a solution was highly dependent on the initial starting guess and that multiple solutions are possible.

The design attained was readily realizable and is shown in Figure 10.82. The driving-point impedance of −50 Ω was verified using Super Compact at the load port.
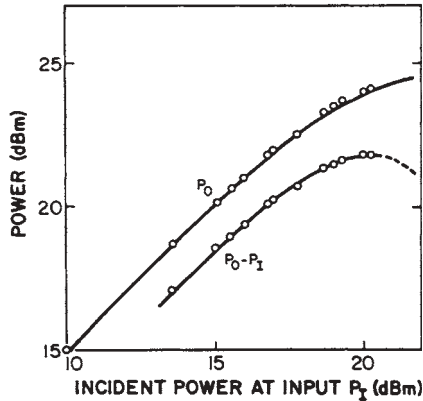
FIGURE 10.81   Measured gain–saturation characteristics of the FET chip. (From Ref. 10.9 © IEEE 1983.)
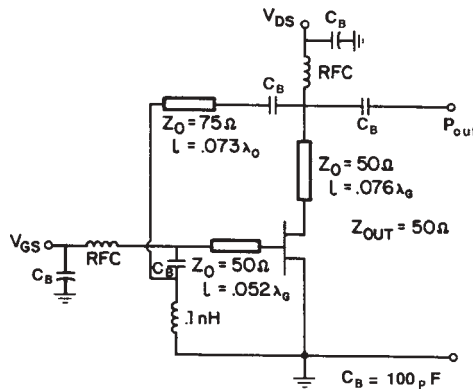
FIGURE 10.82   Optimized oscillator circuit for the topology chosen. (From Ref. 10.9 © IEEE 1983.)

The characteristic impedance of the feedback line was selected through realizability considerations. Doubling Z_0 of this line approximately halved its length, which made it too short to allow connection to the tap points. This line was implemented through a piece of copper ribbon suspended close to the substrate. The gate inductance, which has a very high admittance (and hence can be thought of as the oscillator resonator), was implemented by a short piece of copper ribbon to ground. A photograph of the oscillator is shown in Figure 10.83. The gate is on the right; the bias leads can be seen coming in at the edges of the picture; the feedback loop, shunt inductance, and chip capacitors are easily discernible.

The oscillator was operated with a gate bias of −3 V and drain voltage of 7.5 V. By slightly changing the length of the feedback loop, the frequency was adjusted to 5350 MHz. Without any tuning of the output, the power into the (designed) 50-Ω load was 23.4 dBm. By tuning around the output connector, the power out increased to 23.9 dBm, compared with the predicted output power of 24.8 dBm. The efficiency
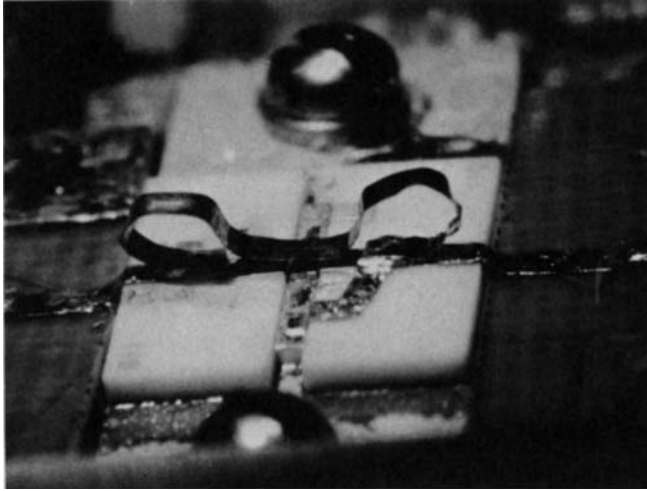
FIGURE 10.83   Photograph of 5.350-GHz oscillator. (From Ref. 10.9 © 1983 IEEE.)
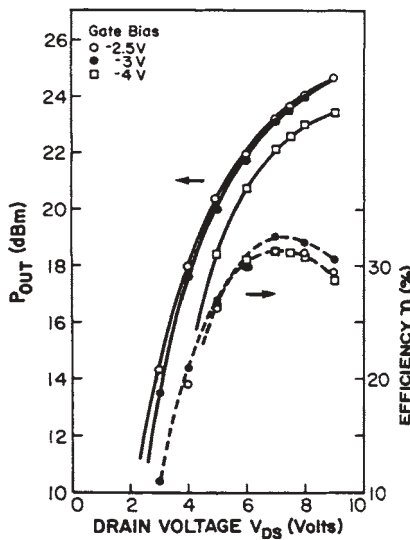
FIGURE 10.84   Oscillator efficiency and output power. (From Ref. 10.9 © 1983 IEEE.)

obtained was 34.7%, which was the maximum efficiency over all operating points. Maximum power of 25 dBm was obtained by raising the drain voltage to 9.56 V.

Figure 10.84 plots efficiency and power out as a function of drain and gate bias. Oscillations started to build up at a drain voltage of 2.2 V and were observed for gate voltages higher than −4.4 V. It can be seen that even near peak power the efficiency is still very high. Figure 10.85 shows the frequency pushing observed due to changes in the bias voltage. Sensitivity to gate voltage is about 150 MHz/V, while frequency is relatively insensitive to drain voltage variations. Although the oscillator was designed using *S* parameters at a fixed gate bias of −3 V, oscillation was still achieved over
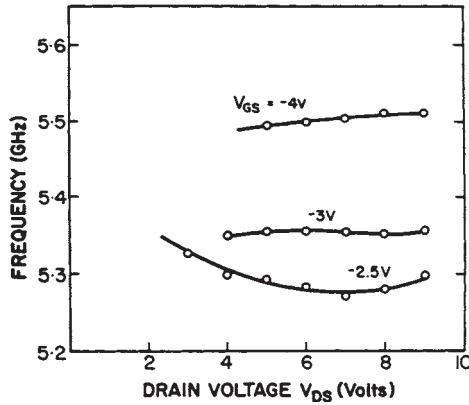
FIGURE 10.85 Oscillator frequency-pushing characteristics. (From Ref. 10.9 © 1983 IEEE.)

a wide range of bias voltages, indicating the usefulness of S parameters (which are relatively bias insensitive) in oscillator design.

Temperature variations in power and frequency at the design point are plotted in Figure 10.86. When the temperature was raised from -50 to $+125°C$, the power decreased by 1 dB. The frequency dropped by 74 MHz, giving an average temperature sensitivity of -0.42 MHz/°C.

The frequency noise was also measured in 300 Hz bandwidth, from 1 to 50 kHz off the carrier. The noise is plotted in decibels below the carrier in Figure 10.87. The gate bias was held at -2.5 V and the drain voltage at 9 V, corresponding to an output power
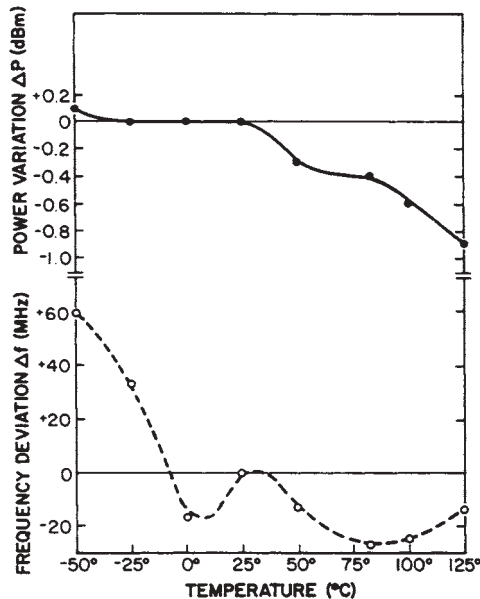
FIGURE 10.86 Oscillator frequency–temperature variation (From Ref. 10.9 © IEEE 1983.)
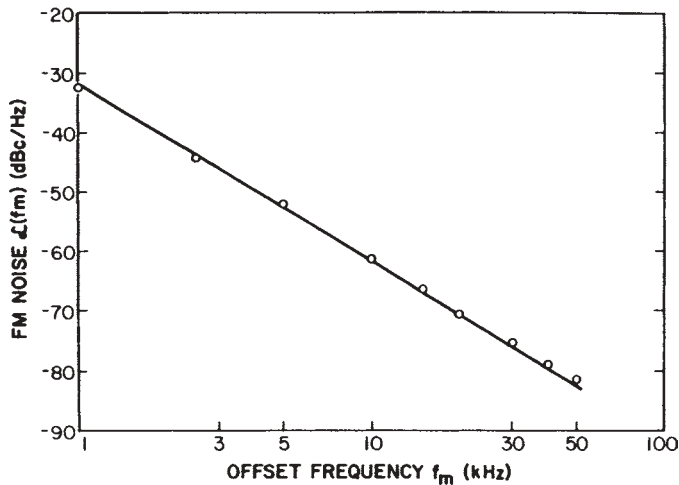
FIGURE 10.87   Oscillator FM noise. (From Ref. 10.9 © IEEE 1983.)

of +24.9 dBm, close to peak power. The external Q of the oscillator (see Section 10.7) was found to be 29 through load-pull measurements (a sliding load with VSWR of 1.5 was varied over all phases; frequency pulling was 74 MHz). Because the noise measurements are within the resonator bandwidth, the FM noise slope over frequency was 30 dB/decade.

The oscillator was also operated in the self-biased mode, with the gate RF choke (RFC) terminated by a resistor. As the drain voltage is raised, the drain current increases very rapidly at first until oscillation begins and a negative bias develops on the gate. Performance under these conditions was excellent, with peak power of 25 dBm being obtained at a drain voltage of 9.5 V at an efficiency of 30.5%. A peak efficiency of 35% was achieved at an output power of 24 dBm. Because of the self-limiting oscillation process, the harmonic power was high. However, at peak power the total harmonics were 18.4 dB down, although at lower power the ratio was much higher. Output power, harmonic power, and efficiency are plotted in Figure 10.88. The parameter is the external resistor used to develop the self-bias. Figure 10.89 presents the frequency and developed gate bias of the oscillator as a function of externally applied drain voltage. The frequency pushing is reasonably linear (+50 MHz/drain volt). The oscillator could also be used as a frequency modulator by varying the gate voltage.

Finally, to test the sensitivity of the design to the transistor S parameters, a second NEC-869177 FET was inserted into an identical circuit. The $I-V$ characteristics of this transistor were substantially different from the first (up to 30% higher drain current was observed at identical bias points). By tuning only the output connector on the drain, a slightly smaller output power of 22.7 dBm was obtained at the design bias point; the frequency was 5230 MHz. However, a much lower efficiency of 22% was recorded due to the substantially worse dc characteristics. In self-bias operation, a peak power of 24.2 dBm was obtained within the safe thermal limits of device operation.

This systematic method for oscillator design using a GaAs MESFET permits an embedding network to be derived analytically that will deliver specified power into a required load at a given frequency. The advantages of this approach are that it is a true two-port design method which requires no creation of an equivalent one-port circuit,
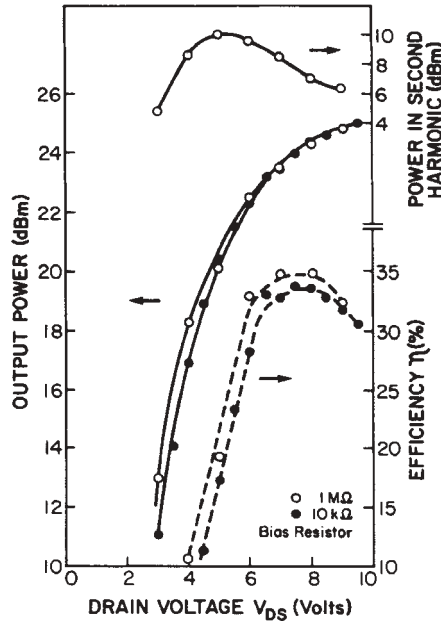
FIGURE 10.88 Oscillator characteristics in self-bias operation. (From Ref. 10.9 © IEEE 1983.)
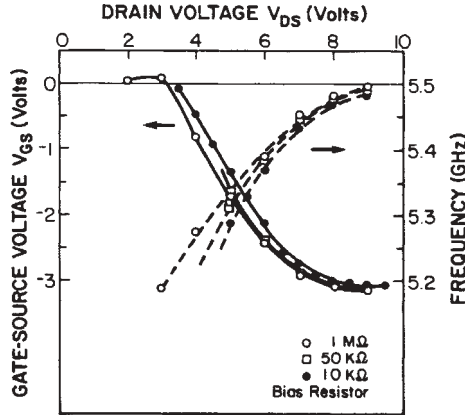
FIGURE 10.89 Oscillator frequency and gate bias in self-bias operation. (From Ref. 10.9 © IEEE 1983.)

the output load is directly specified, and power is automatically maximized for the device operating conditions. Thus no computer optimization of the circuit is necessary. Furthermore, the device is completely described only by its large-signal S parameters. No assumptions are required about the form of the nonlinearity in order to set the required load impedance for maximum power output as long as the device S parameters have the required functional dependence to be defined by large-signal methods.

10.10   NONLINEAR ACTIVE MODELS FOR OSCILLATORS

Despite several attempts by many authors such as Randy Rhea to use a linear model for designing and analyzing oscillators, nonlinear large-signal models for diodes, members of the bipolar transistor family, as well as the FET family, must be used with practical circuits to predict such performance parameters as frequency of oscillation, power output, efficiency, and phase noise. The first simulator handling nonlinear models was SPICE and harmonic balance simulators followed. The SPICE models were really low-frequency models compared to applications in microwave and millimeter-wave frequencies. Table 10.9 and Table 10.10 show large signal and splice parameters of the microwave diode. A detailed introduction in these models is given in U. L. Rohde and D. P. Newkirk, *RF/Microwave Circuit Design for Wireless Applications: Theory and Organization*, Wiley, New York, 2000.

10.10.1   Diodes with Hyperabrupt Junction

The hyperabrupt-junction diode is the device of choice as it provides a greater capacitance change for a given voltage change as well as a linear frequency-versus-voltage characteristic over a limited voltage range. This diode also follows Eq. (10.165) with the exception that n is not a function of voltage and is generally in the range of 0.5 to 2. When these requirements are satisfied, the diode capacity and diode voltage are related by

$$\frac{C(V)}{A} = K \left(\frac{N}{V + \varphi} \right)^n \tag{10.165}$$

where $C(V)$ = capacitance of diode at voltage V
   A = area of diode
   N = doping level of epitaxial layer
   V = voltage applied to diode
   φ = built-in potential of diode (0.6 to 0.8 V)
   n = slope of diode C–V curve; $n \gg 0.5$ for an abrupt-junction diode
   K = constant

The C–V curve in a hyperabrupt diode is shown in Figure 10.90 and is seen to start at a high value of capacitance per unit area at low bias (high epitaxial doping) and change to a lower value of capacitance per unit area (low epitaxial doping) at high bias. The details of the curve depend on details of the shape of the more highly doped region near the *pn* junction. Unfortunately, with a hyperabrupt diode, you must settle for a lower Q than with an abrupt-junction diode with the same breakdown voltage and same capacitance at 4 V.

It should be noted that any diode that has an n value that exceeds 0.5 at any bias voltage is, by definition, a hyperabrupt diode. Thus, the hyperabrupt diode family can have an infinite number of different C–V curves. Since the abrupt-junction diode has a well-defined C–V curve, the capacitance value at one voltage is sufficient to define the C–V capacitance at any other voltage. This is not the case for the hyperabrupt diode. To adequately define the C–V characteristics of a hyperabrupt diode, two and sometimes three points on the curve must be specified. Equation (10.165) shows that the capacitance is a nonlinear function of the voltage and therefore will cause distortion for large voltages across the junction. See Figure 10.91. Likewise, the model is lossy,
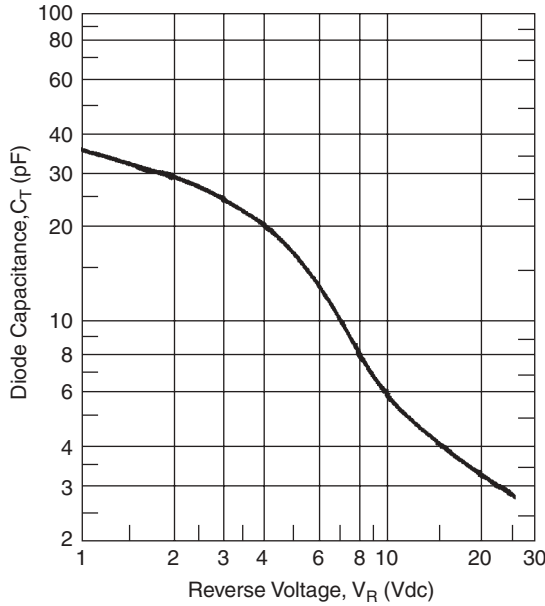
FIGURE 10.90   Capacitance versus junction bias for a hyperabrupt diode.
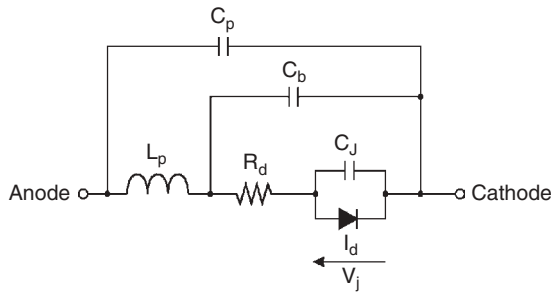
FIGURE 10.91   The large-signal microwave diode model. This model is temperature dependent.

meaning that the actual diode has distributed resistances and parasitic inductances which will determine the frequency response.

10.10.2 Silicon Versus Gallium Arsenide

Everything mentioned so far applies to both silicon and gallium arsenide (GaAs) diodes. The main difference between silicon and GaAs from a user's point of view is that higher Q can be obtained from GaAs devices. This is due to the lower resistivity of GaAs from a given doping level N. The resistivity of the epitaxial layer, or substrate, of a diode is given by

$$\rho = \frac{1}{Ne\mu} \tag{10.166}$$

TABLE 10.9   Large-Signal Microwave Diode Model

Keyword	Description	Unit	Default
	Intrinsic Model		
JS	Saturation current	A	0
ALFA	Slope factor of conduction current	V^{-1}	38.696
JB	Breakdown saturation current	A	10 mA
VB	Breakdown voltage	V	$-\infty$
E	Power law parameter of breakdown current	—	10.0
CT0	Zero-bias depletion capacitance	F	0
FI	Built-in barrier potential	V	0.8
GAMA	Capacitance power law parameter	—	0.5
GC1	Varactor capacitance polynomial coefficient 1	V^{-1}	0.0
GC2	Varactor capacitance polynomial coefficient 2	V^{-2}	0.0
GC3	Varactor capacitance polynomial coefficient 3	V^{-3}	0.0
CD0	Zero-bias diffusion capacitance (*pn* diodes)	F	0
AFAC	Slope factor of diffusion capacitance	V^{-1}	38.696
R0	Bias-dependent part of series resistance in forward-bias condition	Ω	0
T	Intrinsic time constant of depletion layer for abrupt-junction diodes		0
KF	Flicker noise coefficient	—	0.0
AF	Flicker noise exponent	—	1.0
FCP	Flicker noise frequency shape factor	—	1.0
AREA	Area multiplier	—	1.0
	Extrinsic Model		
CP	Package parasitic capacitance	F	0.0
CB	Beam-lead parasitic capacitance	F	0.0
LP	Package parasitic inductance	H	0.0

where ρ = resistivity

$\quad N$ = doping level of layer

$\quad e$ = charge on electron

$\quad \mu$ = mobility of charge carriers in layer

Gallium arsenide has a mobility about four times that of silicon and, thus, a lower resistivity and higher Q for a given doping level N. Since diode capacitance is proportional to $\sqrt{N}$, independent of resistivity, a silicon diode and a GaAs diode of equal area and doping will have a capacitance difference proportional to the square root of the dielectric constant ratio. This gives the GaAs diode a 5% higher capacitance and is thus of little practical significance. The penalty paid for using GaAs is an unpassivated diode and a more expensive diode due to higher material and processing costs. If the higher Q of the GaAs device is not really needed, a substantial price saving will be obtained by using a silicon device.

We may consider two of the terminal voltages to be independent and choose the set V_{gs} and V_{ds}, V_{gs} being the voltage across the gate capacitance and V_{ds} that across the drain conductance. If we restrict our interest to the signal frequency and ignore the

TABLE 10.10 Diode SPICE Parameters

Parameter	Unit	SMS1546	SMS3922	SMS3923	SMS3924	SMS3926	SMS3927	SMS3928	SMS7621	SMS7630
I_s	A	3×10^{-7}	3×10^{-8}	5×10^{-9}	2×10^{-11}	2.5×10^{-7}	1.3×10^{-9}	9×10^{-13}	4×10^{-8}	5×10^{-6}
R_s	Ω	4	9	11	11	4	4	4	12	30
n	—	1.04	1.08	1.05	1.08	1.04	1.04	1.04	1.05	1.05
T_d	S	1×10^{-11}	8×10^{-11}	8×10^{-11}	8×10^{-11}	1×10^{-11}	1×10^{-11}	1×10^{-11}	1×10^{-11}	1×10^{-11}
C_{J0}	pF	0.38	0.9	0.93	1.6	0.42	0.39	0.39	0.1	0.14
m	—	0.36	0.26	0.24	0.4	0.32	0.37	0.42	0.35	0.4
E_G	eV	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.69
X_{ti}	—	2	2	2	2	2	2	2	2	2
F_C	—	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
B_V	V	3	20	46	100	2	3	4	3	2
I_{BV}	A	1×10^{-5}	1×10^{-5}	1×10^{-5}	1×10^{-5}	1.00×10^{-5}	1.00×10^{-5}	1.00×10^{-5}	1×10^{-5}	0.0001
V_J	—	0.51	0.65	0.15	0.84	0.495	0.595	0.800	0.51	0.34

effects due to higher harmonic components, these voltages can be written as

$$V_{gs} = V_{gs0} + v_{gs} \cos(\omega t + \phi)$$
$$V_{ds} = V_{ds0} + v_{ds} \cos \omega t$$

$$(10.167)$$

where V_{gs0} and V_{ds0} are the dc bias voltages, v_{gs} and v_{ds} the amplitudes of signal frequency components, and ϕ the phase difference between the gate and drain voltages. The equivalent circuit for the signal frequency can now be expressed as a function of the following parameters, which are independent of time: V_{gs0}, V_{ds0}, v_{gs}, v_{ds}, ω, and ϕ.

To avoid unnecessary complexity of calculations, we limit the nonlinear behavior to five elements: gate forward conductance G_{gf}, gate capacitance C_{gs}, gate charging resistance R_i, transconductance g_m, and drain conductance G_d. This is justifiable. Here G_{gf} represents the effect of the forward-rectified current across the gate junction under large-signal operation. No voltage dependence was assumed for the parasitic elements, that is, the lead inductances (L_g, L_d, L_s) and contact resistances (R_g, R_d, R_s). Also ignored was the small voltage dependence of the drain channel capacitance C_{ds} and feedback capacitance C_{dg} because of their small values. Figure 10.92 shows the schematic of oscillator circuit and equivalent circuit of FET used in oscillator analysis [10.34].

10.10.3 Expressions for g_m and G_d

Transconductance g_m and drain conductance G_d are defined as

$$g_m = \left(\frac{i_{ds}}{v_{gs}}\right)_{v_{ds}=0} \qquad G_d = \left(\frac{i_{ds}}{v_{ds}}\right)_{v_{gs}=0}$$

$$(10.168)$$

where i_{ds} is the RF drain current amplitude. The instantaneous drain current can be written in terms of g_m and G_d as

$$I_{ds}(t) = I_{ds0} + g_m v_{gs} \cos(\omega t + \phi) + G_d v_{ds} \cos \omega t \qquad (10.169a)$$

where I_{ds0} is the dc drain current. In this expression linear superposition of the dc and RF currents is assumed.

Now, if we have a function that can simulate the nonlinear dependence of the drain current I_{ds} on V_{gs} and V_{ds}, as

$$I_{ds} = I_{ds}(V_{gs}, V_{ds}) \qquad (10.169b)$$

then under large-signal conditions the instantaneous current $I_{ds}(t)$ can be obtained by inserting (10.167) into (10.169b). By multiplying $\sin \omega t$ by (10.169a) and integrating over a complete period, g_m is obtained as

$$g_m = -\frac{\omega}{\pi v_{gs} \sin \phi} \int_0^{2\pi/\omega} I_{ds} \sin \omega t \; dt \qquad (10.170a)$$

Similarly, G_d is obtained as

$$G_d = \frac{\omega}{\pi v_{ds} \sin \phi} \int_0^{2\pi/\omega} I_{ds} \sin(\omega t + \phi) \, dt \qquad (10.170b)$$
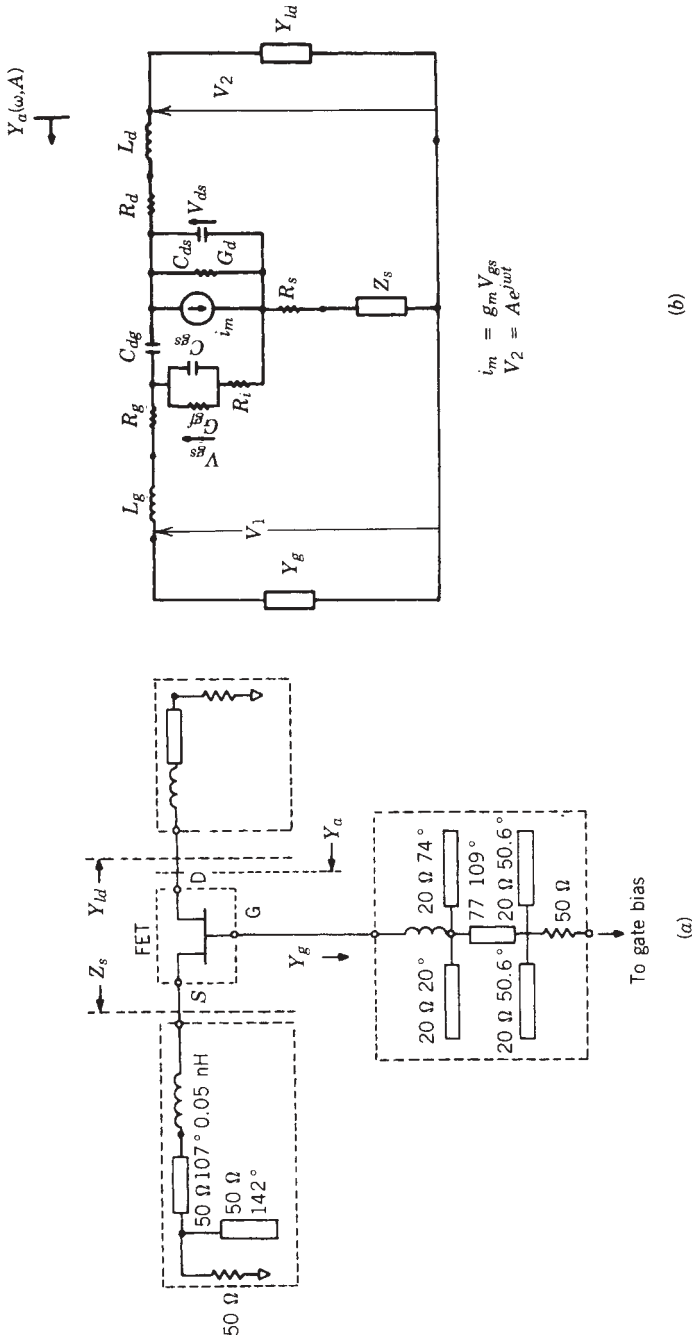
FIGURE 10.92 Schematic of oscillator circuit and equivalent circuit of FET used in oscillator analysis. (From Ref. 10.34.)

Equations (10.170a) and (10.170b) are now functions of RF amplitudes v_{gs} and v_{ds} as well as of bias voltages V_{gs0} and V_{ds0}. We turn now to a more detailed discussion of the nonlinear relation (10.169b).

The functional relation $I_{ds}(V_{gs}, V_{ds})$ was established empirically by simulating the dc $I-V$ characteristics by a nonlinear function given by

$$I_{ds}(V_{ds}, V_{gs}) = I_{d1}I_{d2} \tag{10.171}$$

$$I_{d1} = \frac{1}{k}\left\{1 + \frac{V'_{gs}}{V_p} - \frac{1}{m} + \frac{1}{m}\exp\left[-m\left(1 + \frac{V'_{gs}}{V_p}\right)\right]\right\}$$

$$I_{d2} = I_{dsp}\left\{1 - \exp\left[\frac{-V_{ds}}{V_{dss}} - a\left(\frac{V_{ds}}{V_{dss}}\right)^2 - b\left(\frac{V_{ds}}{V_{dss}}\right)^3\right]\right\}$$

$$k = 1 - \frac{1}{m}[1 - \exp(-m)]$$

$$V_p = V_{po} + pV_{ds} + V_\phi$$

$$V'_{gs} = V_{gs} - V_\phi$$

where $V_{po}(> 0)$ = pinchoff voltage at $V_{ds} \approx 0$
$\qquad V_{dss}$ = drain current saturation voltage
$\qquad V_\phi$ = built-in potential of Schottky barrier
$\qquad I_{dsp}$ = drain current when $V_{gs} = V_\phi$

and a, b, m, and p are fitting factors that can be varied from device to device.

10.10.4 Nonlinear Expressions for C_{gs}, G_{gf}, and R_i

Although the gate junction is also a function of V_{gs} and V_{ds}, we assume here that it can be approximated by a Schottky barrier diode between gate and source, with V_{gs} as the sole voltage parameter. Gate capacitance C'_{gs} and forward gate current i_{gf} can be found from Schottky barrier theory as

$$C'_{gs} = \frac{C'_{gs0}}{\sqrt{1 - V_{gs}/V_\phi}} \qquad (-V_p \le V_{gs}) \tag{10.172}$$

or

$$C'_{gs} = \frac{C'_{gs0}}{\sqrt{1 + V_p/V_\phi}} \qquad (-V_p \ge V_{gs}) \tag{10.173}$$

$$i_{gf} = i_s\exp(\alpha V_{gs} - 1) \tag{10.174}$$

where C'_{gs0} is the zero-bias gate capacitance, i_s the saturation current of the Schottky barrier, and $\alpha = q/nkT$.

When V_{gs} varies according to (10.167), the effective gate capacitance C_{gs} and gate forward conductance G_{gf} for the signal frequency are obtained from (10.172)

to (10.174) as

$$C_{gs} = \frac{1}{\pi v_{gs}} \int_0^{2\pi} \left(\int^{V_{gs}} C'_{gs}\, dv \right) \cos \omega t \, d(\omega t) \tag{10.175a}$$

$$G_{gf} = 2i_s \exp(\alpha V_{gs0}) \frac{I_1(\alpha v_{gs})}{v_{gs}} \tag{10.175b}$$

where $I_1(x)$ is the modified Bessel function of the first order.

The gate-charging resistance R_i was assumed to vary in such a way that the charging time constant was invariant with bias:

$$R_i C_{gs} = \tau_i (\text{const}) \tag{10.176}$$

Thus all nonlinear element values of the equivalent circuit can be expressed in terms of the terminal RF amplitudes and their relative phase. One may now determine more precisely the admittance $Y_a(A, \omega)$, or $Y_a(v_{gs}, v_{ds}, \omega)$, by an iteration method such as the following.

First, starting values for v_{gs} and the equivalent-circuit parameters are assumed. For the latter, small-signal values based on measured S parameters are suitable. With these parameters specified, the output voltage v_{ds} and its phase can be calculated in a straightforward manner. With the resultant value of v_{ds}, ϕ, and the initially assumed V_{gs}, the "first-cut" evaluation of the equivalent-circuit elements can be made with the help of (10.170a), (10.170b), (10.175a), (10.175b), and (10.176). The procedure above is then repeated, each time using the most recently evaluated values of v_{ds}, ϕ, and v_{gs}, until convergence is obtained. The process converges when successive iterations reproduce the equivalent-circuit parameters to within some specified error. Once convergence is achieved, such oscillator properties as power output and efficiency can be calculated.

10.10.5   Analytic Simulation of *I–V* Characteristics

The analysis begins by applying the analytic expressions [Eq. (10.171)] to the set of measured $I-V$ characteristics shown in Figure 10.93a for a 1 µm × 400 µm FET [10.34]. The fitting parameters $a = -0.2$, $b = 0.6$, $m = 3$, and $p = 0.2$ in these equations were determined and the simulated $I-V$ characteristics calculated. Figure 10.93b is the result of this simulation. Note the excellent agreement (of course, the hysteresis shown in Fig. 10.93a cannot be represented) [10.34].

10.10.6   Equivalent-Circuit Derivation

Next, the small-signal S parameters were measured over a broad frequency range (2 to 12 GHz) at the operating bias conditions for the oscillator. These were used to determine the equivalent-circuit element values (Fig. 10.94). These element values were determined by using the Super Compact computer-aided design program, which optimizes the equivalent-circuit element values to provide a "good" fit to the measured S parameters.
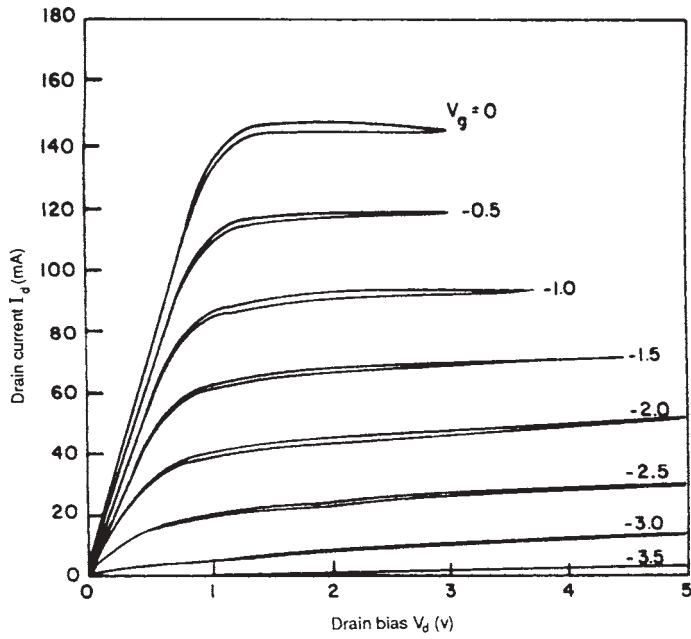
(a)
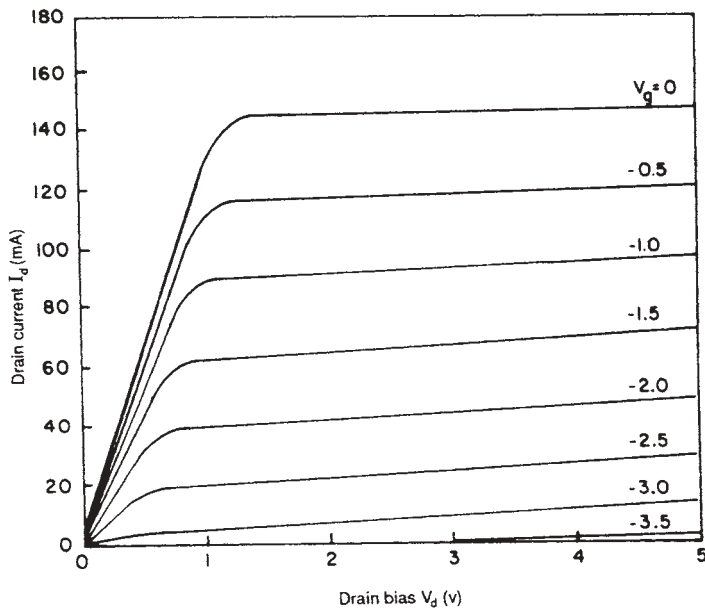
(b)

FIGURE 10.93   (a) Measured and (b) simulated $I-V$ characteristic used in nonlinear oscillator analyzer. (From Ref. 10.34.)
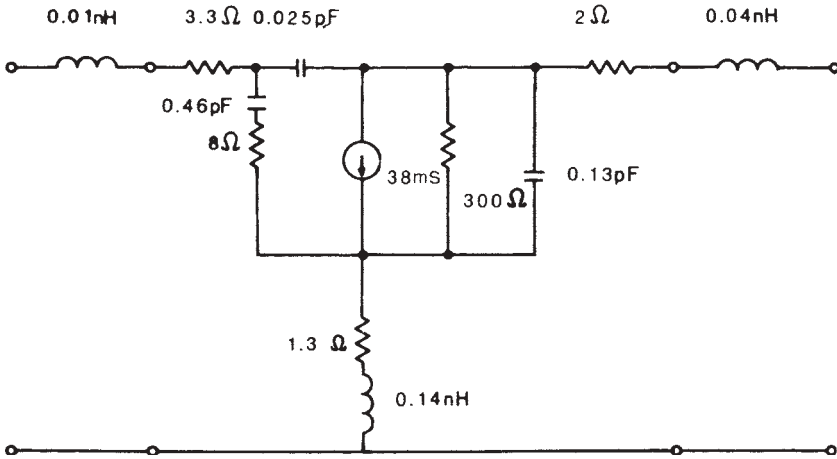
FIGURE 10.94   Equivalent circuit of FET based on measured S parameters. (From Ref. 10.34.)
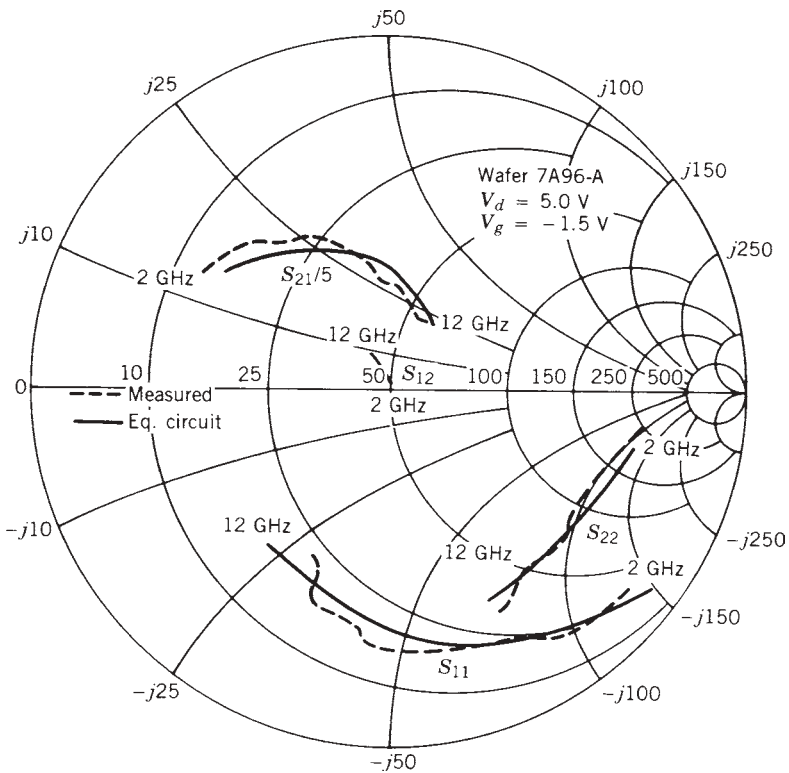
FIGURE 10.95   Comparison of measured S parameters and calculated S parameters based on equivalent circuit ($Z = 400$ μm, $L_G = 1$ μm). (From Ref. 10.34.)

Figure 10.95 illustrates the excellent agreement between measured *S* parameters and those calculated from the equivalent circuit. This establishes confidence in the equivalent-circuit element values.

The equivalent-circuit elements are used for two purposes: (1) to determine what range of circuit terminations are necessary to initiate oscillations (i.e., establish instability) and (2) to establish initial conditions for the nonlinear analysis.

10.10.7   Determination of Oscillation Conditions

The oscillation conditions, that is, the load conditions at the drain terminals necessary for oscillations to start, are delineated by the shaded regions in Figure 10.96. Shown is a plot of $-Y_a/Y_0$, where $Y_0 = 0.02$ *S* is the characteristic line admittance. This plot was obtained for the conditions where the source and gate terminals were terminated by the oscillator circuit elements established earlier (Fig. 10.92*a*). The unstable regions where oscillation is possible were determined by the Nyquist criterion. It shows that oscillation is most likely to occur close to 10 GHz, but with greater mismatch, oscillation could also occur at lower frequencies, 6 to 8 GHz. Past measurements with similar FETs have shown a tendency to hop in frequency as the circuit was tuned.
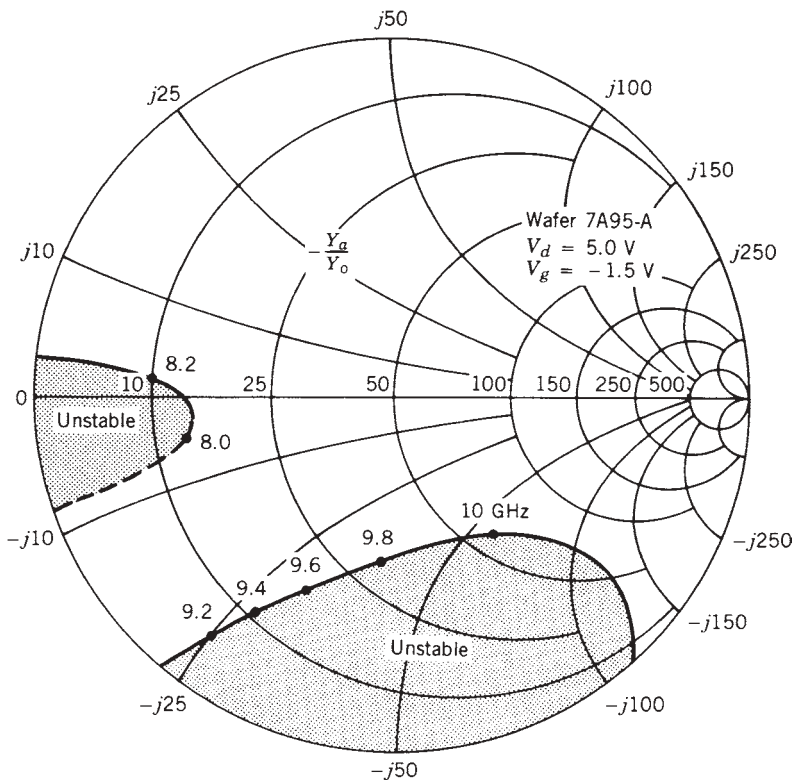
FIGURE 10.96   Domains of load admittance (shaded areas) that support oscillations in FET circuit. Reference plane for load is that marked Y_a in Figure 10.92*a*. (From Ref. 10.34.)

10.10.8 Nonlinear Analysis

Having established the oscillation conditions, we now apply the equivalent-circuit elements and the nonlinear equations from the dc $I-V$ simulation to determine the oscillator properties under steady-state oscillation conditions for the permissible range of load-terminating conditions. The result of the nonlinear analysis is shown in Figure 10.97. Shown are closed constant-output power contours (in dBm) as a function of load (drain) terminating conditions. Also shown are intersecting loci of constant-frequency contours. For example, the 10-GHz contour shows the predicted power output at various terminating admittance levels. The power levels indicated are in the range obtained experimentally, as shown by the measured data.

10.10.9 Conclusion

A large-signal model of the FET has been derived. This model has been applied to an FET embedded in an actual oscillator circuit, and the predicted performance has been shown to be consistent with experimental results [10.34].
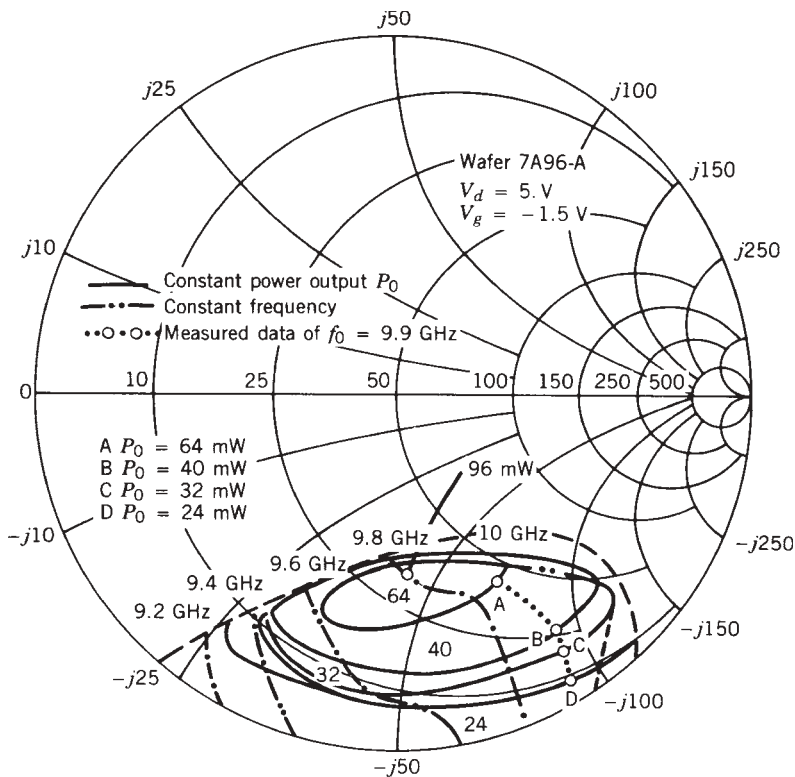
FIGURE 10.97   Calculated constant-frequency and constant-power output contours for FET oscillator circuit. These contours represent load admittance conditions at the drain which are necessary to yield the stated power output at the given frequency. All shown are measured oscillator data. (From Ref. 10.34.)

10.11   OSCILLATOR DESIGN USING NONLINEAR CAD TOOLS

The recent introduction of Flusoft Designer nonlinear computer tools such as Sonata [10.32] and Microwave Harmonica [10.35, now Flusoft Designer] allows a design engineer to produce theoretical oscillator designs to achieve given specifications. Oscillator design is an autonomous problem in which there is no external driving source. This complicates the design process considerably, as the frequency of an oscillator is then an additional degree of freedom in the circuit that must be accounted for.

Microwave Harmonica is a nonlinear CAD package using the harmonic balance technique. Because of its nonlinear optimization capabilities, it is uniquely suited to the task of oscillator design [10.36]. The example that follows, from the work of Rizzoli et al. [10.37], illustrates the design of a 5-GHz dielectric resonator oscillator using Microwave Harmonica.

The harmonic balance method seeks a solution to a steady-state nonlinear design problem by iteratively solving for a set of variables, referred to as state variables. The state variables can typically be chosen as the voltages at the linear–nonlinear interface in a circuit partitioned into linear and nonlinear segments. They are expressed as the phasor components, and their harmonics, of a sinusoidal excitation frequency. The state variables are usually found iteratively by a gradient-based technique which seeks a simultaneous solution for Kirchhoff's equations applied to the linear and nonlinear sides of the network separately.

For the nonautonomous, or driven, circuit, the driving frequency is known a priori and Kirchhoff's equations are a well-determined system of equations in which the phase and amplitude of the excitation appear on one side of the equations as forcing terms. In an autonomous circuit, the only excitation terms appearing in Kirchhoff's equations are dc sources. One stable solution to these equations for a circuit with no applied RF drive will always be the dc (or degenerate) solution, as all phasor terms at an arbitrarily chosen frequency can be set to zero and still satisfy the RF driving conditions (of zero excitation). For an autonomous circuit to have a solution to Kirchhoff's equations at nonzero frequencies, at least one additional degree of freedom is required, as there is one additional unknown in the equations—the oscillation frequency.

For oscillator analysis purposes (i.e., for a fixed circuit topology), the additional free parameter is just the unknown frequency of oscillation. For oscillator design purposes, the frequency is fixed as a design goal, and the required degree of freedom must be represented by a free circuit variable, such as a bias voltage or other tuning element. In this way, a solution can be found to the conditions for oscillation (which are just Kirchhoff's equations) by varying some circuit parameter. This parameter must be adjusted so that the equations can be satisfied at the oscillation frequency, with some set of (solution) state variables, which are determined at the same time.

The harmonic balance problem must then allow for the simultaneous solution of both the state variables and the circuit elements to satisfy Kirchhoff's equations under the chosen conditions (i.e., at the design frequency). In fact, Microwave Harmonica allows the user to set additional circuit parameters to be variables in order to optimize for other circuit responses, such as output power, efficiency, spectral purity, or distortion, while simultaneously satisfying Kirchhoff's equations. Consequently, the methodology of introducing additional degrees of freedom into the harmonic balance problem allows not only for the solution of autonomous designs but also for the optimization of all types of circuits for desired response.

As an example, Figure 10.98 shows a DRO design using the Plessey GAT6 FET ($I_{DSS} = 40$ mA) embedded in a simple microstrip circuit. The specified optimization goals were 20 mW output power at a frequency of 5 GHz. In the design, the additional degrees of freedom for the optimization problem and the oscillator synthesis were provided by the resonator diameter and the microstrip lengths together with the FET bias voltages. Prior to circuit optimization, the program automatically optimizes the DRO dimensions to resonate at the $TE_{01\delta}$ mode at 5 GHz. The preoptimization is needed to ensure that the initial starting point for the design equations is within the operating regime. A sequence of optimizations was then performed by increasing the lower bounds on the output power. The maximum power available was found to be 29 mW with an efficiency of 14.2%. The bias point was $V_D = 7.95$ V, $V_G = -0.77$ V, and $I_0 = 26$ mA. Output harmonics were 22.3 dB below the fundamental.

The circuit can also be tuned by moving the metal tuning plate over the resonator. To tune to a frequency of 5.05 GHz, the circuit must be reoptimized with the plate distance s as the only tuning variable. This change to the single circuit parameter is needed to allow there to be a solution to Kirchhoff's equations at the new oscillation frequency. The values of the state variables are, of course, also different at the new point, and the output power is reduced correspondingly.

As oscillator analysis can be performed by repetitively reoptimizing the tuning parameter s at a series of frequencies and constructing a tuning curve of oscillation frequency versus s. For an oscillator of unknown frequency, the actual oscillation frequency can be determined by entering the tuning curve at the known value of s. Note that in the case of an oscillator analysis only a single tuning variable is adjusted at each frequency point, so that a tuning curve can be constructed to give a single, unique relationship between the design frequency and the actual circuit parameter value in the circuit being analyzed.
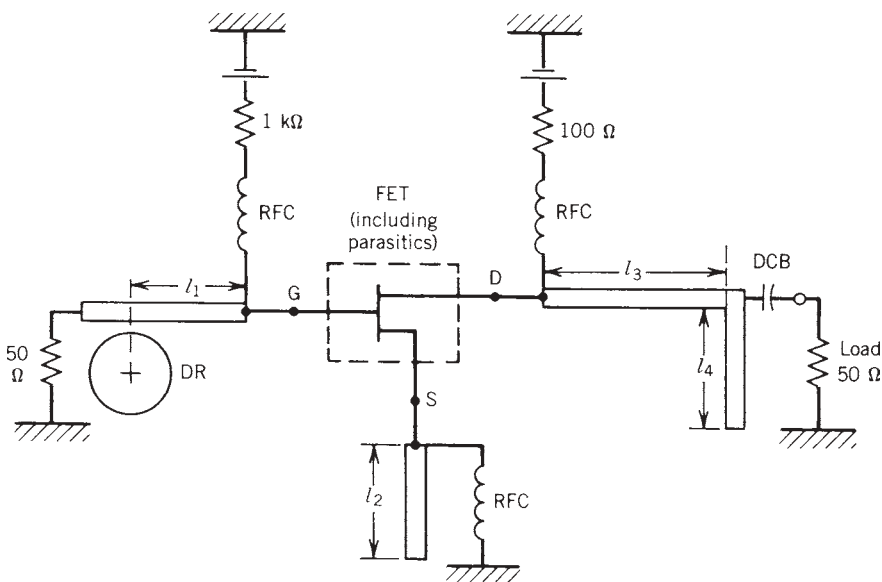
FIGURE 10.98   DRO design example. (From Ref. 10.37 with permission.)

Although the harmonic balance approach ensures that a steady-state solution exists, the buildup of oscillations and the stability of the steady-state operating point also need to be addressed. One way to provide a numerical solution to this problem is to use the principles of bifurcation theory [10.38]. Using the frequency of oscillation as a continuation parameter [10.39] and choosing the output power as a parameter to describe the circuit state, a solution path may be built by stepping the frequency through a prescribed range and performing a sequence of circuit optimizations with respect to the state variables and some other free-circuit parameter.

Figure 10.99 shows the solution path for the DRO depicted in Figure 10.98, with the distance l_1 between the DR plane and the FET gate chosen as the free-circuit variable. Both the output power and the tuning (continuation) parameter are plotted against frequency. Point A is the nominal operating point obtained by circuit optimization as just described. The critical points H_1 and H_2 are Hopf bifurcations [10.40], and all states belonging to the bifurcated branch H_1 AH_2 are stable. On the other hand, a local stability analysis about the dc bias point reveals that each dc state between H_1 and H_2 has two natural frequencies with positive real parts and is thus unstable. This guarantees oscillation buildup whenever the DRO is biased with the distance between the DR plane and the FET gate set to any values between l_1' and l_1''. The bifurcation diagram is a tuning diagram that provides full information on the DRO tuning range with respect to the circuit variable and on the power-to-frequency relationship within this range.

Figure 10.100 shows the results of a similar analysis, with the tuning plate position s now being chosen as the circuit variable. In the range of all positive s, there is only one Hopf bifurcation at point H_1, corresponding to $s = s_1$. This bifurcation is supercritical, so that the circuit is dc stable below H_1 and dc unstable above H_1 due to a couple of complex-conjugate natural frequencies with positive real part. Thus, whenever the FET is biased with the tuning plate set to any position above s_1, oscillation buildup will take place. In this case, stable oscillation is possible even if the plate is suppressed (s goes to infinity).
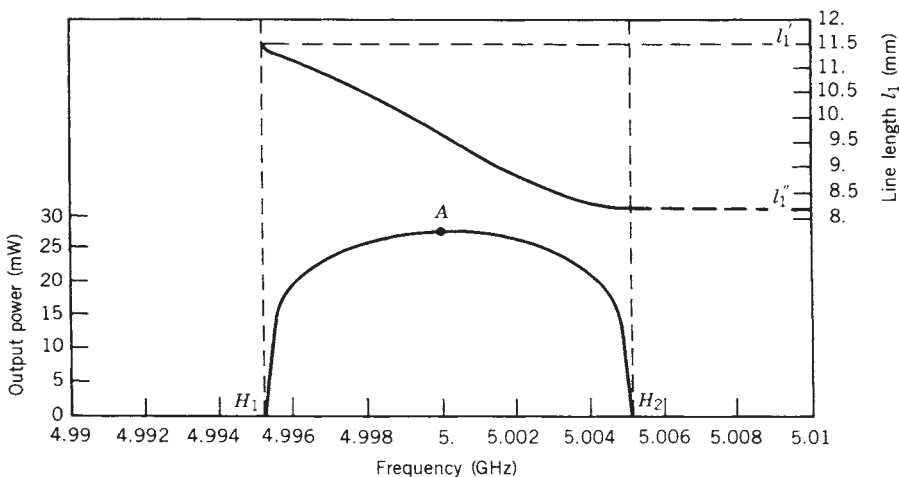
FIGURE 10.99 Oscillator performance versus l_1. (From Ref. 10.37 with permission.)
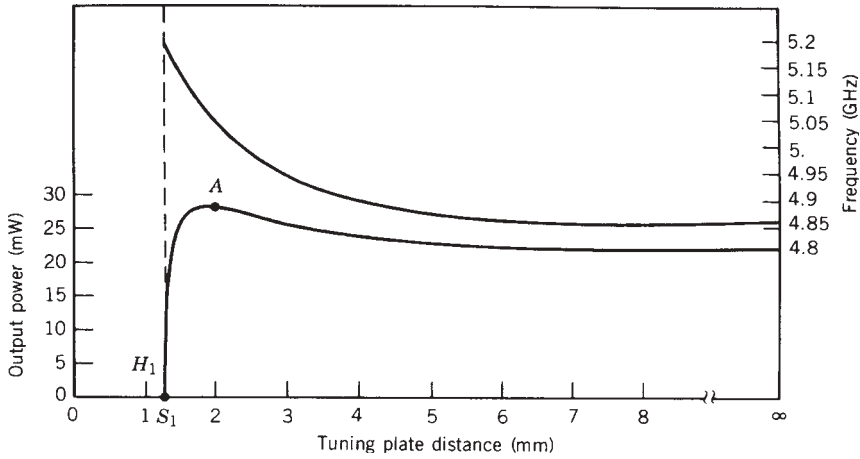
FIGURE 10.100 Oscillator performance versus tuning plate distance. (From Ref. 10.37 with permission.)
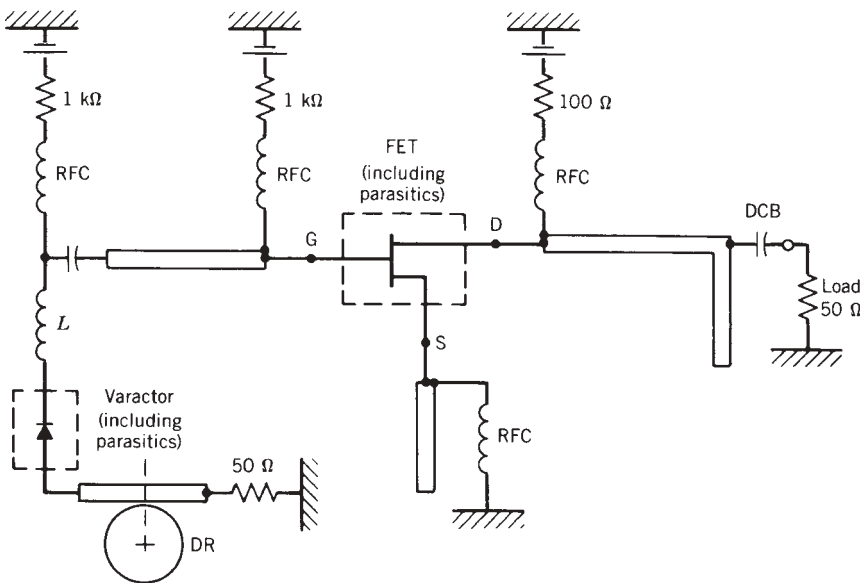
FIGURE 10.101 Varactor-tuned DRO. (From Ref. 10.37 with permission.)

Finally, the DRO may be electronically tuned by inserting a series varactor in the gate feedback circuit, as shown in Figure 10.101. An inductance was also introduced into the gate to resonate the varactor capacitance at the nominal operating frequency of 5 GHz. Figure 10.102 shows the results of the bifurcation analysis for the DRO, with the varactor bias chosen as the free-circuit parameter. A comparison of Figures 10.99, 10.100, and 10.102 clearly displays the superior tuning performance obtained by changing one of the resonator geometrical parameters over that of other types of mechanical or electronic tuning.
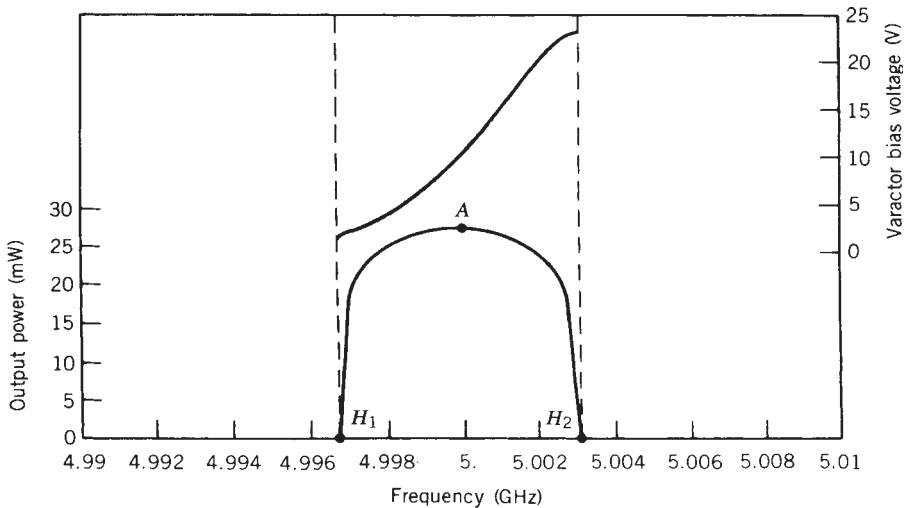
FIGURE 10.102   Oscillator performance versus varactor tuning voltage. (From Ref. 10.37 with permission.)

In summary, the advent of nonlinear CAD programs now allows the designer to verify many aspects of circuit operation not previously obtainable through linear programs alone. In this way, the levels of output power, harmonic content, dc-to-RF efficiency, device currents, and load pushing and pulling can be examined before the oscillator is constructed.

A second oscillator example described in the remainder of this section will develop the methodology needed from commencement of the nonlinear design to its completion. The $I-V$ and small-signal S-parameter data are used with a parameter extraction routine to characterize the FET for the nonlinear model used in the harmonic balance simulator. The overall design philosophy is demonstrated with the design of an oscillator–amplifier subsystem. The steps of design specification, device modeling, circuit analysis, and system optimization are illustrated by this buffered oscillator example.

10.11.1   Parameter Extraction Method

Parameter extraction of an accurate nonlinear model plays an essential part in nonlinear simulation. Conventionally, small-signal parameters are extracted from S parameters measured at a single bias point. Designers relying on this approach are often frustrated by nonunique solutions. Usually, there exists a family of solutions all of which produce a similar match between model response and measurement. As a consequence, the particular solution obtained depends on the initial guess; using a different starting point will probably result in a different solution. Additional difficulties arise for large-signal nonlinear modeling, since we need to determine parameters that may vary with bias, such as the transconductance. It is obvious that small-signal S-parameter measurements at a single bias point are not adequate for extracting bias-dependent parameters.

A common practice in an attempt at large-signal modeling is to extract the bias-dependent parameters and bias-independent parameters separately. The bias-dependent

parameters are extracted by curve fitting, while the bias-independent parameters are extracted from S parameters measured at a single bias point. Such an approach can be an improvement over conventional small-signal modeling since the extraction of the bias-independent parameters reduces the number of unknowns. However, two problems may plague such an approach: The results may not be unique, and bias-dependent parameters extracted from the dc data alone (transconductance, output conductance) may not be valid at the operating microwave frequencies.

A novel approach to nonlinear parameter extraction [10.41, 10.42] simultaneously extracts the dc, bias-dependent, and bias-independent parameters. The motivation of this method is to strengthen the model identifiability and enforce a unique solution. S-parameter measurements at multiple bias points can be utilized to achieve a robust solution applicable to dc, small-signal, and large-signal modeling.

A software package called RoMPE (Robust Model Parameter Extractor) [10.43] is commercially available to perform simultaneous extraction of dc, bias-dependent, and bias-independent parameters. The program accounts for the dependence, explicit and implicit, of small-signal parameters on the bias. It implements the theoretically established relationship between small-signal parameters and bias-dependent parameters, such as between C_{gs} and C_0 (C_{gs} at zero gate voltage) and V_B (built-in potential voltage). Extraction is performed through one of two available state-of-the-art optimizers: the l_1 or l_2 optimizers.

To illustrate the usefulness of the approach, an example will be presented. The large-signal FET model [10.44] used appears in Figure 10.103. The bias-independent parameters are identified as

$$\phi_a = [L_g, L_d, L_s, R_g, R_d, R_s, C_{dg}, C_{ds}] \tag{10.177a}$$
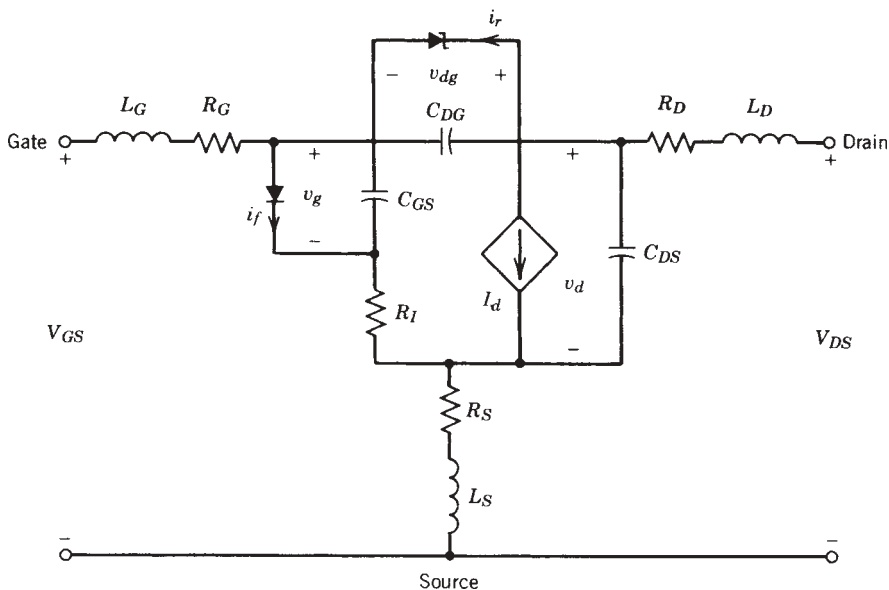
FIGURE 10.103   Large-signal FET model. (From Ref. 10.41 © IEEE 1988.)

and the bias-dependent parameters as

$$\phi_b = [C_g, I_{ds}] \tag{10.177b}$$

The constraints imposed on the ϕ_b are

$$C_{gs} = \frac{C_0}{\sqrt{1 - V_g/V_b}} \tag{10.178}$$

$$I_{ds} = I_{dss} \left(1 - \frac{V_g}{V_p}\right)^2 \tanh \frac{\alpha_d V_d}{V_g - V_p}$$

$$V_p = V_{p0} + \gamma V_d \tag{10.179}$$

The diode currents are given by

$$i_f = I_s \exp(\alpha_s v_g - 1) \tag{10.180}$$

$$i_r = I_{sr} \exp[\alpha_{sr}(V_d - V_g - V_{BR})] \tag{10.181}$$

The model parameters were then optimized such that the S parameters matched those reported in Ref. 10.41 from 2 to 18 GHz at three bias points. Starting values and model values at solution are listed in Table 10.11. The optimization required 35 iterations

TABLE 10.11   Parameter Values of the FET Model

Parameter	Units	Bias 1 Start	Bias 1 Solution	Bias 2, Solution	Bias 3, Solution
R_g	Ohm	1.0	0.0119	0.0119	0.0119
R_d	Ohm	1.0	0.0006	0.0006	0.0006
G_{ds}	S	1.0	0.004647	0.005843	0.006382
R_i	Ohm	5.0	5.855	4.164	3.642
R_s	Ohm	1.0	0.3514	0.3514	0.3514
L_s	nH	0.01	0.0107	0.0107	0.0107
C_{gs}	pF	1.0	0.7568	0.3997	0.3194
C_{dg}	pF	0.1	0.04226	0.04226	0.04226
C_{ds}	pF	0.3	0.1958	0.1958	0.1958
G	S	1.0	0.05888	0.04467	0.03048
T	ps	5.0	3.654	3.654	3.654
L_g	nH	0.05	0.1257	0.1257	0.1257
L_d	nH	0.05	0.0719	0.0719	0.0719

Coefficient	Units	Start	Solution	Coefficient	Units	Start	Solution
I_s	nA	0.5	0.5	α_d	—	4.0	3.039
α_s	V^{-1}	20.0	20.0	V_{po}	V	−4.0	−4.275
I_{sr}	nA	0.5	0.5	γ	—	−0.2	−0.3912
α_{sr}	V^{-1}	1.0	1.0	C_0	pF	1.0	0.7961
I_{dss}	A	0.2	0.191	V_b	V	1.0	0.5975

Values determined by constraints on ϕ_b.

of the l_1 optimizer and took 3 rec CPU minutes on 3000 MHz IBM PC-compatible equipment (a total of 51 frequencies, 18 optimizable variables). Figure 10.104 displays the relative S parameters over the entire frequency range for the second bias point ($V_{gs} = 1.74$ V, $V_{ds} = 4$ V). The agreement between measured and modeled responses is superb. The match at the other bias points is slightly degraded.

As a comparison to the conventional approach of parameter extraction, the dc parameters alone were first extracted to give a good match to the measured bias points. Next, the ac parameters (C_0, V_b) for the bias-dependent gate–source capacitance (C_{gs}) were extracted using (10.178). Then the bias-independent ac parameters were extracted at the second bias point and gave an excellent fit to the measured S parameters. However, when the entire model was simulated (using these bias-dependent and bias-independent parameters), the response was not acceptable, as shown in Figure 10.105. It is also worth mentioning that the parameters extracted in this way are significantly different from those extracted using the simultaneous method.
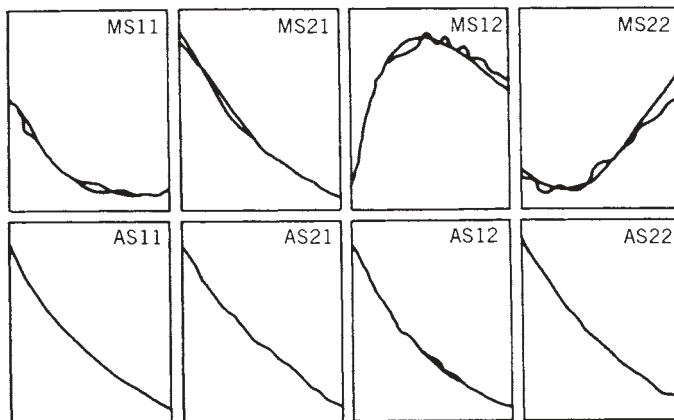
FIGURE 10.104 S-parameter match using simultaneous ac and dc parameter extraction.
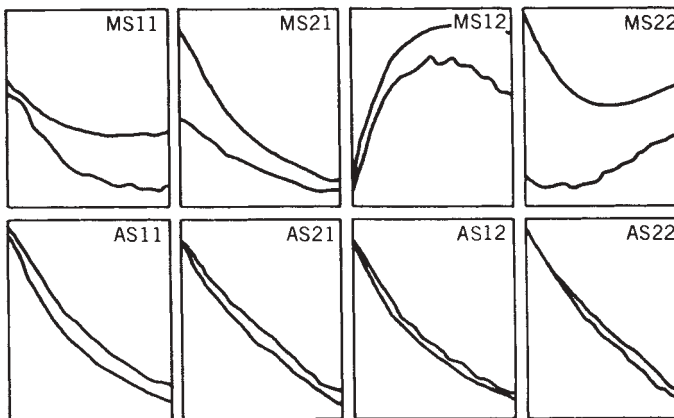
FIGURE 10.105 S-parameter match using conventional parameter extraction. (From Ref. 10.41 © IEEE 1988.)

A test of robustness was performed [10.41] by perturbing the starting point of some variables by 20% to 200%. All the variables converged to virtually the same solution. This demonstrates the uniqueness of the solution when dc and ac parameters are extracted simultaneously.

10.11.2 Example of Nonlinear Design Methodology: 4-GHz Oscillator–Amplifier

A simple example to illustrate the design steps needed to generate a buffered oscillator subsystem is presented. The steps are listed methodically to best demonstrate the overall concept of a nonlinear design rather than the details.

1. *Design Specification* A key to determining product quality is to measure its degree of conformance to specification. For this example, the simplified specification for a buffered oscillator is as follows:

Frequency	4 GHz
Output power	20 dBm or greater
Harmonic frequencies	Greater than 20 dB below fundamental
Mean time between failure	10^5 h
Frequency pulling (into 2 : 1 VSWR)	To be determined

It is instructive to note that until quite recently the design of a subsystem such as this could only have been accomplished using a linear simulator and the oscillator design could only have been achieved using a negative-resistance approach. Furthermore, none of the quantities specified (other than frequency) could be determined until the design is completed and built. The advent of nonlinear simulators allows verification of these at the design stage. This is crucial for quality considerations, as it allows conformance to specification to be designed in.

2. *Design Modeling* A parameter extraction program such as RoMPE can be used to fit the coefficients used in the model of Materka and Kacprzak [10.44], as modified in Microwave Harmonica, to the available measurement data. After selection of the FET and measurements of $I-V$ data and S-parameter data, the parasitic elements and coefficients used in the nonlinear Microwave Harmonica model can be determined. An example of the modeled $I-V$ response of the FET is shown in Figure 10.106.

3. *Component Design* The specification calls for the development of both an amplifier (for buffering) and an oscillator. The development of an amplifier is relatively simple. Figure 10.106 shows a circuit topology developed using linear circuit techniques (i.e., optimized for gain and bandwidth). For the Microwave Harmonica analysis, bias and RF sources must be added and the FET represented by the model parameters found in step 2. When driven by a 4-GHz input level of 15 dBm, the load line in Figure 10.107 results. The amplifier output power that results is 20 dBm.

The oscillator design is more difficult, as this type of circuit is now autonomous (i.e., has no external RF drive). Although the designer might derive the circuit topology shown in Figure 10.108 as a first step from linear analysis, there is no guarantee that the circuit will oscillate at precisely 4 GHz. Some additional degree of freedom (such as the 2.2-pF tuning capacitor) must be adjusted to tune the frequency.
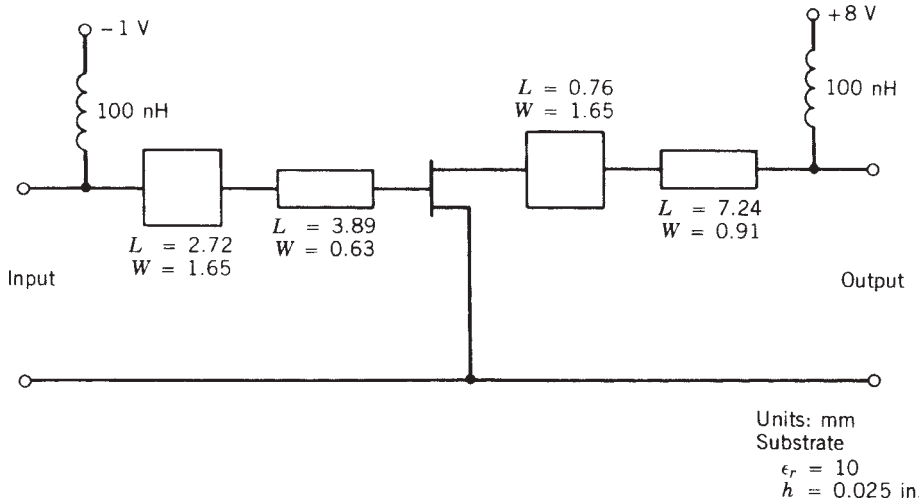
FIGURE 10.106   Amplifier design at 4 GHz. (From Ref. 6.36 © IEEE 1988.)
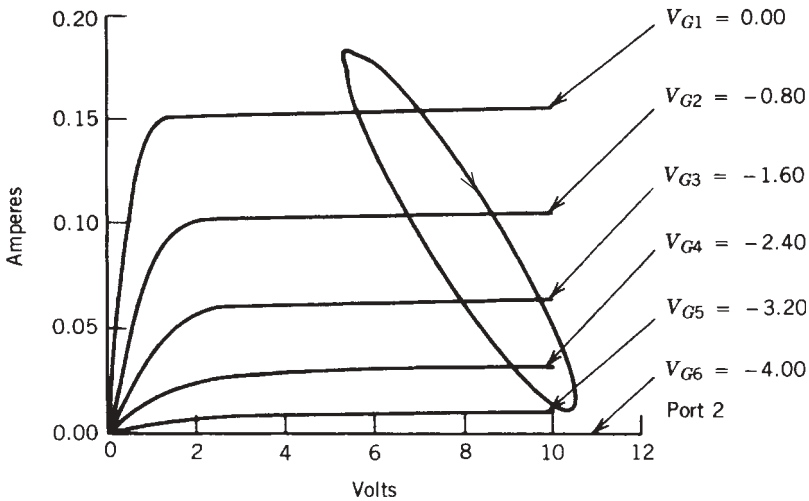
FIGURE 10.107   Amplifier load line with $P_{in} = 15$ dBm at 4 GHz. (From Ref. 10.36 © IEEE 1988.)

The design of oscillators using the harmonic balance method also requires this additional degree of freedom. The frequency, as in the specification, must first be imposed on the problem. At least one corresponding degree of freedom, such as a circuit parameter, must then be adjusted to ensure oscillation at that frequency. In Microwave Harmonica, the degree of freedom is introduced as an optimization variable, with the variable adjusted so that the harmonic balance equations (i.e., the conditions for oscillation) have a solution at the frequency imposed. Other variables and other optimization criteria, such as maximum output power, maximum spectral purity, or maximum efficiency, may also be imposed.
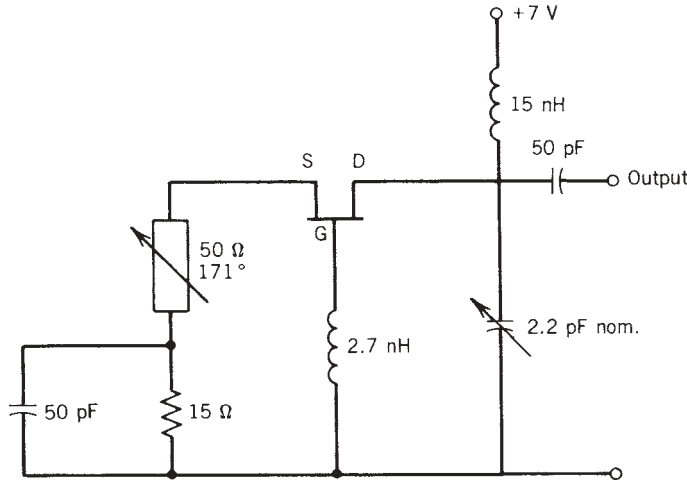
FIGURE 10.108 Oscillator design at 4 GHz. (From Ref. 10.36 © IEEE 1988.)

If a solution exists, oscillations will occur at the imposed frequency with an amplitude determined by the final values of the state variables. The output spectrum in Figure 10.109 results, with the corresponding drain current waveform shown in Figure 10.110 (over two cycles of oscillation). The load line for the oscillation is shown in Figure 10.111 and now represents a true limit cycle, with the drain current confined between slightly greater than I_{DSS} and pinchoff. The elliptical shape results because the load impedance is now reactive.

4. *Subsystem Design* The resulting oscillator–amplifier subsystem is shown in Figure 10.112. The total system is also autonomous but will no longer oscillate at precisely 4 GHz because the amplifier input loads the oscillator differently from the 50 Ω used in the initial oscillator design. Microwave Harmonica can again be used to
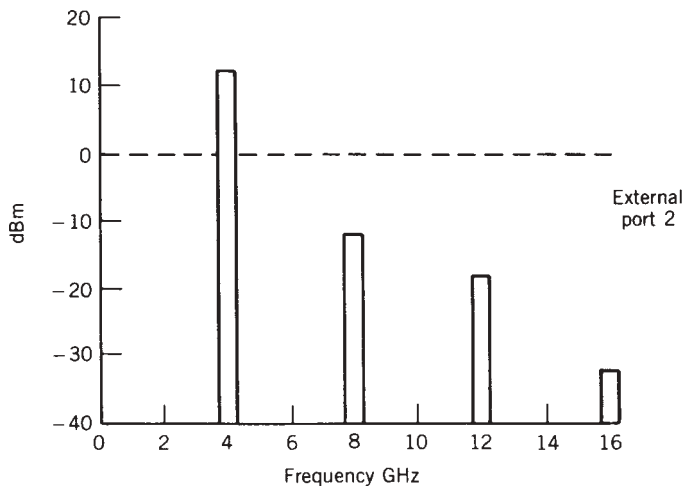
FIGURE 10.109 Oscillator power output spectrum. (From Ref. 10.36 © IEEE 1988.)
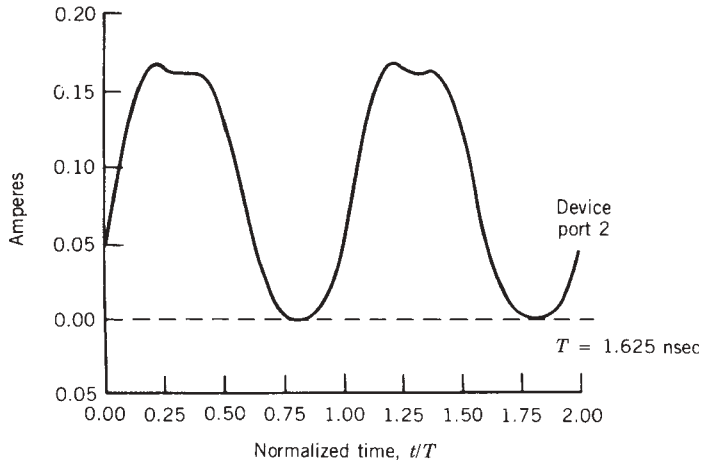
FIGURE 10.110   Oscillator drain current versus time (two cycles). (From Ref. 10.36 © IEEE 1988.)
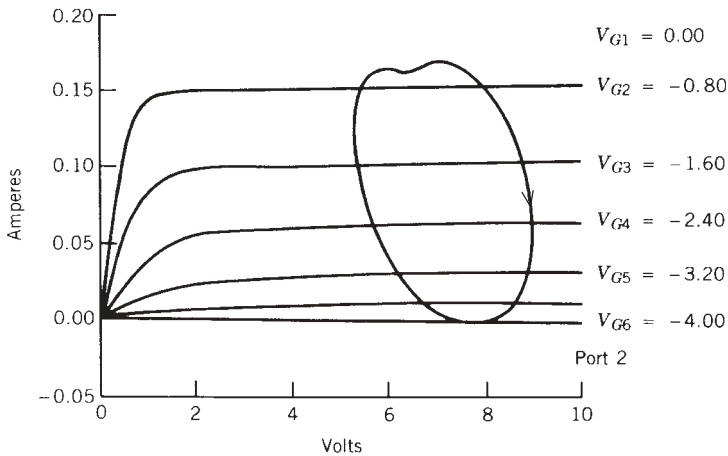
FIGURE 10.111   Oscillator load line. (From Ref. 10.36 © IEEE 1988.)

set the frequency to the desired specification frequency by adjustment of a single tuning parameter. The tuning capacitor assumes a final value of 3.14 pF after "optimization." Optimization in this case is nothing more than allowing the program's optimizer to adjust the value of the tuning element until the harmonic balance equations can be solved, at the desired frequency, with some set of (solution) state variables.

The output waveform is shown in Figure 10.113 and corresponding output spectra in Figure 10.114. The specified output power and harmonic content can be determined from this figure and additional optimization criteria added to improve the performance further. The gate current waveform in Figure 10.115 reveals substantial harmonic content with a dc offset; this would have negative implications for system reliability.
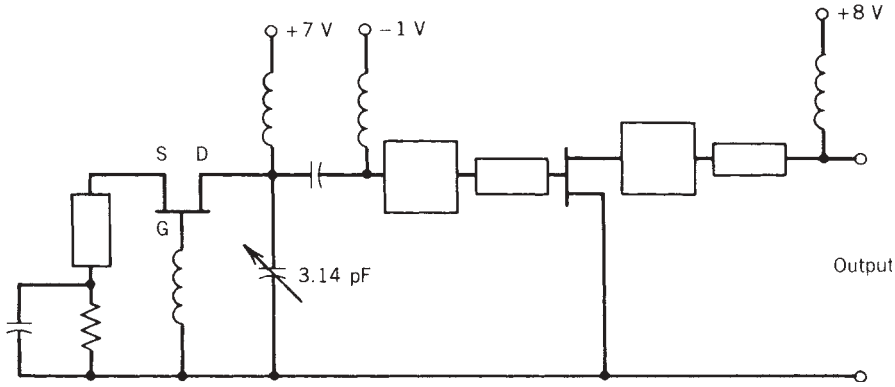
FIGURE 10.112   Buffered oscillator design. (From Ref. 10.36 © IEEE 1988.)
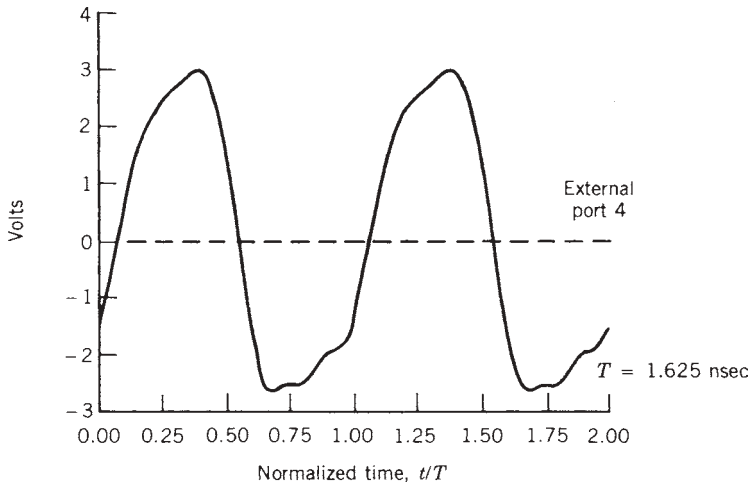
FIGURE 10.113   Buffered oscillator load voltage versus time (two cycles). (From Ref. 10.36 © IEEE 1988.)

Finally, an oscillator analysis (rather than synthesis) is required in order to determine the effect of load pull. In Microwave Harmonica this can be performed relatively easily by automatically sweeping the frequency and reoptimizing the tuning element at each step of the sweep. In this way, a tuning curve of frequency versus element value can be constructed and the frequency determined from the (fixed) value of the tuning element that is used in the actual circuit. By repeating this process for different values of the load, the effect of various loads on the oscillation frequency can be determined.

10.11.3   Conclusion

To effectively utilize any harmonic balance program, a time-domain model for the non-linear device is required. The extraction of parameters to describe devices according to the notation used in available models has always been a factor limiting the useful-ness of nonlinear circuit simulators. Programs are now available which extract these
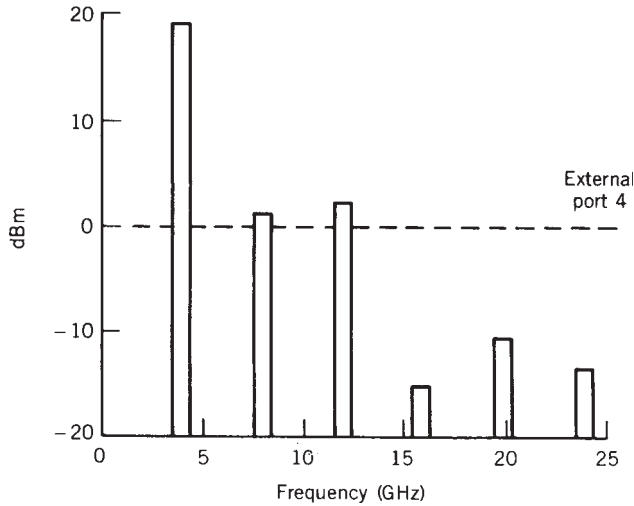
FIGURE 10.114   Buffered oscillator power output spectrum. (From Ref. 10.36 © IEEE 1988.)
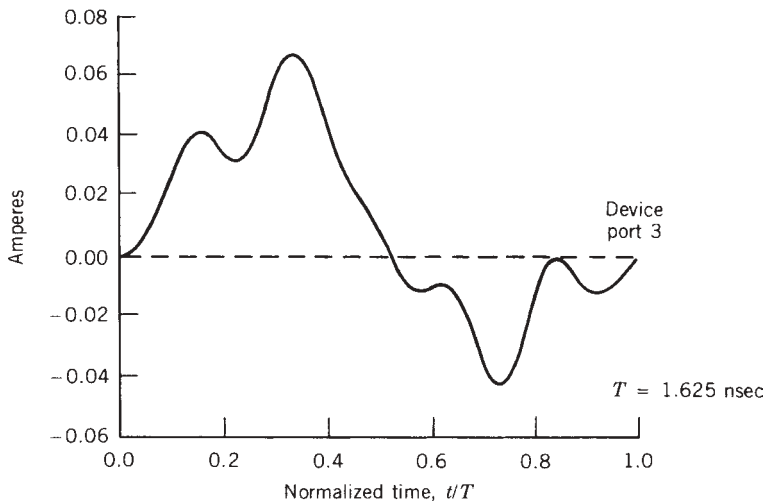
FIGURE 10.115   Gate current for amplifier FET versus time. (From Ref. 10.36 © IEEE 1988.)

parameters from $I - V$ data and small-signal S parameters measured at one or more bias conditions. Simultaneous extraction of the parasitic network and the nonlinear model parameters provides consistency between the data sets and the model. Because the equations used for device modeling are known and fixed, the adjoint technique can be used to determine sensitivities of the model elements for fitting purposes. This results in very fast execution times.

The recent advances in modeling and circuit simulation makes it possible to optimize circuits for given nonlinear responses. Mixers, oscillators, power amplifiers, limiters, and *pin* attenuators are among the types of circuits that can be quantitatively designed using the harmonic balance method. The ability to predict compressed output powers,

spectral purity, dc-to-RF and RF-to-RF efficiencies, and transducer and conversion gains under varying drive is likely to result in tremendous productivity gains as the design and optimization of nonlinear components are transferred from the computer to the workbench.

10.12 MICROWAVE OSCILLATORS PERFORMANCE

In this chapter we have looked at various aspects of oscillators. It may be useful to give readers some reference points regarding oscillator performance. Figure 10.116 shows a survey of narrow-band FET oscillators. Power output at the frequency of operation and dc-to-RF efficiency are listed. These are narrow-band VCO, DRO, or cavity-tuned circuits. For example, the 1-W oscillator at 8 GHz uses a 4000-μm-gate-width DXL 4640A-P100 GaAs MESFET on a duroid substrate with microstrip resonators [6.46].

For wide-band operation, Figure 10.117 illustrates some implementations using either varactor diodes or YIG resonators. Figure 10.118 provides an overview of the output power and tuning range for some selected oscillators. The Avantek 2- to 18-GHz YIG oscillator uses the AT22000 silicon bipolar transistor.

The noise performance is another important parameter, as we have learned, and Figure 10.119 is a graphic presentation of $\mathcal{L}(f_m)$ at $f_m = 10$ kHz. There are many
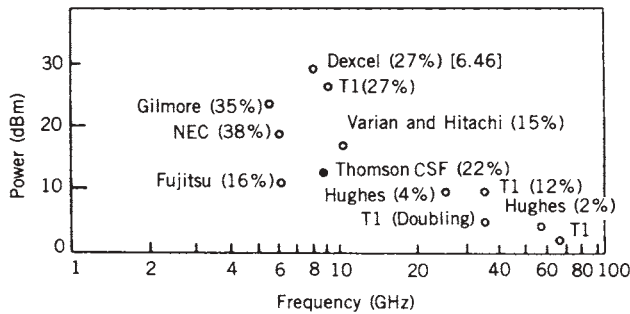
FIGURE 10.116 Survey of narrow-band FET oscillator performance. (From Ref. 10.45.)
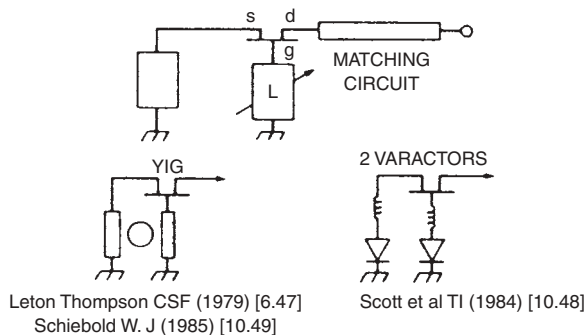
FIGURE 10.117 Wide-band tuning of an FET oscillator. (From Ref. 10.45.)
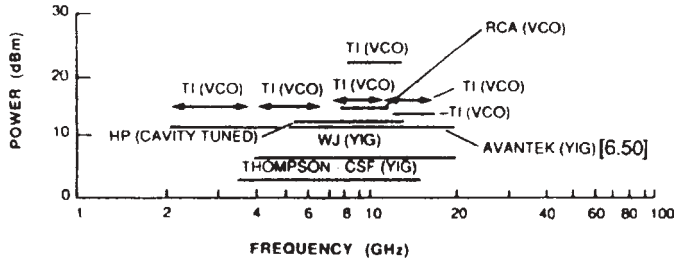
FIGURE 10.118   Survey of wide-band FET oscillator performance. (From Ref. 10.45.)
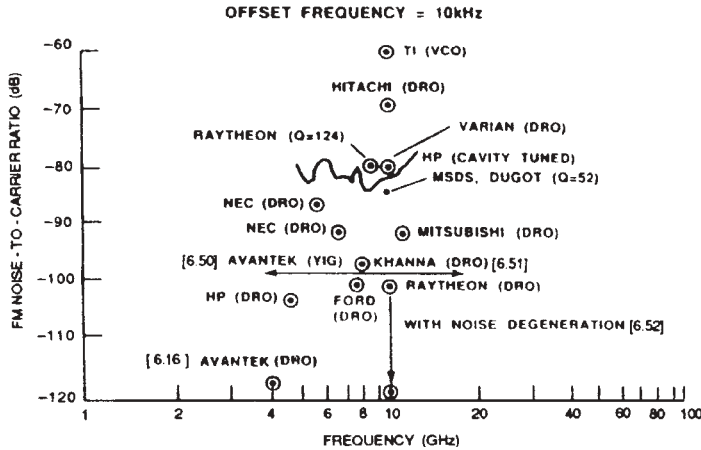
FIGURE 10.119   Survey of FET oscillator noise performance. (From Ref. 10.45.)

ways to couple a resonator to an oscillator for frequency stabilization, as shown in Figure 10.120. A very low noise DRO at 1.3 GHz using a silicon bipolar transistor gave −142 dBc/Hz at 10 kHz from the carrier [10.59]. This oscillator uses the resonator in the feedback loop and as a filter. This is similar to the crystal oscillator reported by Rohde [10.3, p. 198]. Perhaps the lowest oscillator phase noise of a 4-GHz DRO was −130 dBc/Hz at 10 kHz from the carrier [10.60] using a low-noise GaAs FET amplifier with parallel feedback. This oscillator used a two-stage GaAs amplifier with 20 dB gain and produced 11.5 dBm of output power.

The FM noise of an X-band microstrip GaAs FET oscillator is typically −65 dBc/Hz at 10 kHz offset from the carrier. Use of a dielectric resonator will reduce this noise to −100 dBc/Hz at the same offset frequency. The noise can be degenerated to a lower level by means of a frequency-locked loop, and a novel realization of such a circuit is presented in Figure 10.121.

The uniqueness of this circuit lies in its utilization of one dielectric resonator in both the basic oscillator and the discriminator within the frequency-locked loop. The resulting noise performance is given in Figure 10.122, both with and without noise degeneration. This method seems to have achieved the best carrier-to-noise ratio of an FET oscillator at the X band (10 GHz).
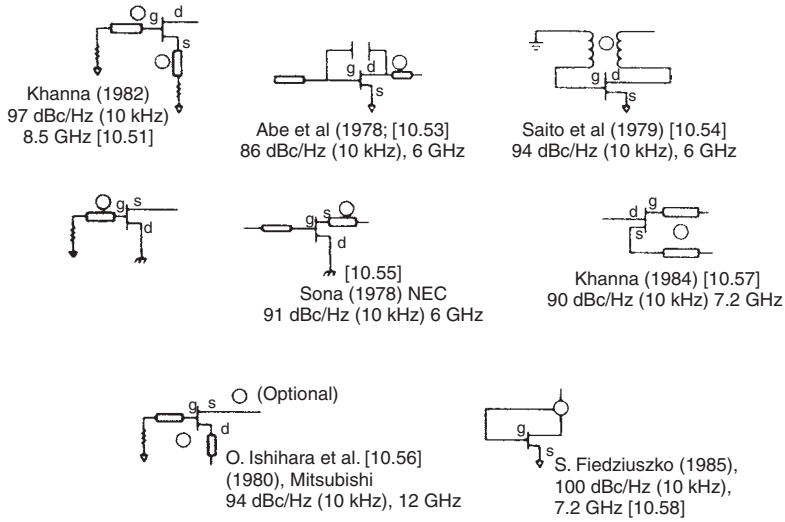
FIGURE 10.120   Methods of frequency stabilization. (From Ref. 10.45.)
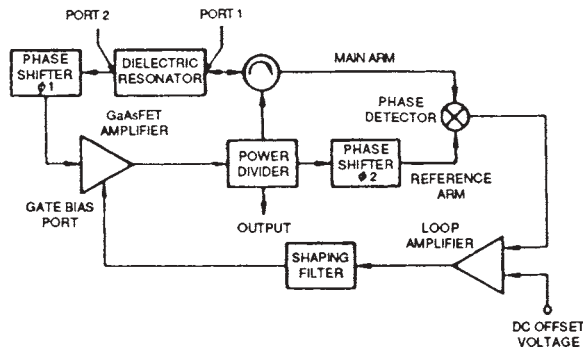
FIGURE 10.121   Circuit for noise degeneration in FET oscillators. (From Ref. 10.52.)
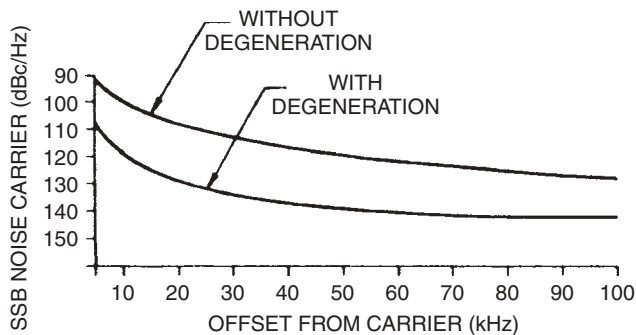
FIGURE 10.122   Noise performance of an FET oscillator with and without noise degeneration. (From Ref. 10.52.)
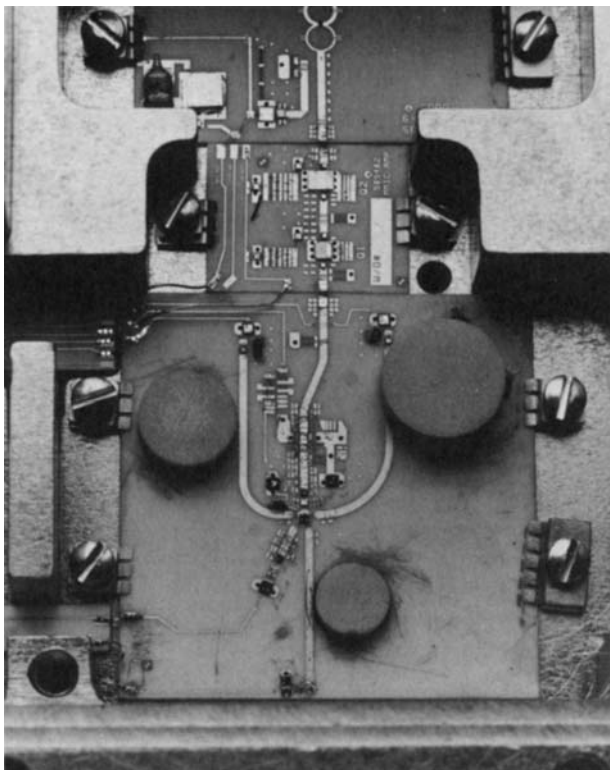
FIGURE 10.123 Photograph of an ultrafast dielectric resonator oscillator. (Courtesy of Avantek.)

Figure 10.123 is a photograph of an ultrafast switching DRO with three resonators [10.61]. This is a single GaAs MESFET switched between three resonator ports, which gives very low posttuning drift. Also, the oscillator has no spurious outputs at the unwanted oscillator frequencies.

Some recent wide-band results reported on GaAs MMIC structures indicate a bandwidth of 2.5 to 6 GHz using off-chip varactors [10.62] and 6 to 12 GHz and 10 to 20 GHz low-power oscillators with multiple integrated varactor structures [10.63, 10.64].

10.13   DESIGN OF AN OSCILLATOR USING LARGE-SIGNAL *Y* PARAMETERS

Figure 10.124 is a numerical calculation of a 3000-MHz oscillator based on the parallel-feedback case using large-signal S parameters. This example is of particular interest because it requires an inductor instead of the familiar capacitor between base and emitter, C_2. This circuit is a Colpitts oscillator.

Large-signal Y parameters measured data ($I_c = 20$ mA, $V_{ce} = 2$ V) at 3000 MHz are

$$Y_{11} = G_{11} + jB_{11} = (11.42 + j8.96) \text{ mS} \qquad (10.182)$$
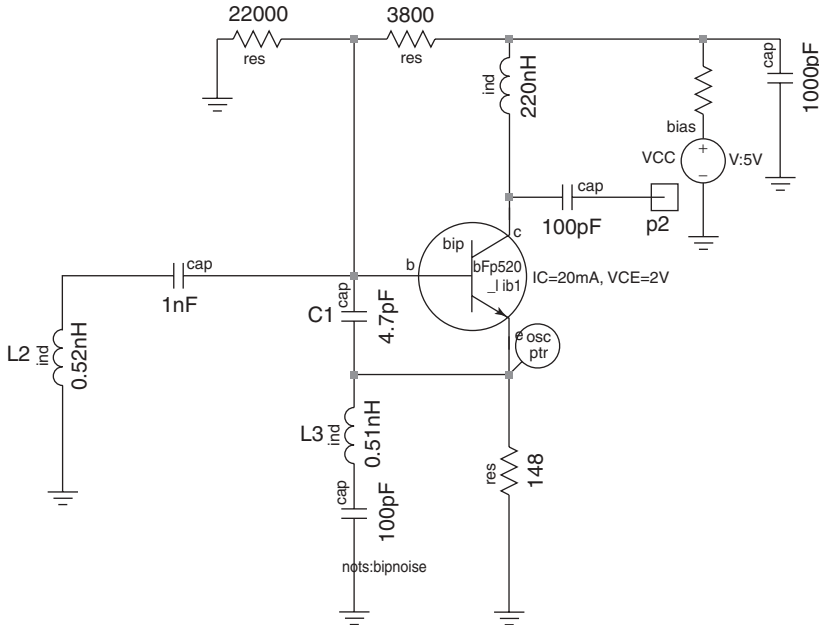
FIGURE 10.124 A 3000-MHz oscillator using a BFP520 transistor operating at 2 V and 20 mA. In this case, the capacitor C_2 needs to be replaced by an inductor L_3 that tunes out the collector–emitter capacitance to achieve the optimum value. The 1 nF on the left is a dc separation capacitor. This case is optimized for output power.

$$Y_{21} = G_{21} + jB_{21} = (4.35 - j196.64) \text{ mS} \tag{10.183}$$

$$Y_{12} = G_{12} + jB_{12} = (-433.09 - j1.5643) \text{ mS} \tag{10.184}$$

$$Y_{22} = G_{22} + jB_{22} = (4.41 + j9.10) \text{ mS} \tag{10.185}$$

The optimum values of feedback element are calculated from the given expressions of B_1^* and B_2^* as

$$B_1^* = -\left[B_{11} + \frac{B_{12} + B_{21}}{2} + \left(\frac{G_{21} - G_{12}}{B_{21} - B_{12}} \right) \left(\frac{G_{12} + G_{21}}{2} + G_{11} \right) \right] \tag{10.186}$$

$$jB_1^* = 89.8 \times 10^{-3} \tag{10.187}$$

$$jB_1^* = jwC_1 \tag{10.188}$$

$$C_1 = \frac{89.8 \times 10^{-3}}{2\pi f} = 4.77 \text{ pF} \tag{10.189}$$

$$B_2^* = \frac{B_{12} + B_{21}}{2} + \left[\frac{(G_{12} + G_{21})(G_{21} - G_{12})}{2(B_{21} - B_{12})} \right] \tag{10.190}$$

$$jB_2^* = -103.5 \times 10^{-3} \tag{10.191}$$

$$jB_2^* = \frac{1}{jwL_2} \tag{10.192}$$

$$L_2 = \frac{1}{(2\pi f) \times 103.5 \times 10^{-3}} = 0.515 \text{ nH} \tag{10.193}$$

The optimum values of the real and imaginary parts of the output admittance are

$$Y_{\text{out}}^* = G_{\text{out}}^* + jB_{\text{out}}^* \tag{10.194}$$

where G_{out}^* and B_{out}^* are given as

$$G_{\text{out}}^* = G_{22} - \frac{(G_{12} + G_{21})^2 (B_{21} - B_{12})^2}{4G_{11}} \tag{10.195}$$

$$G_{\text{out}}^* = -823.53 \times 10^{-3} \tag{10.196}$$

$$B_{\text{out}}^* = B_{22} + \frac{G_{21} - G_{12}}{B_{21} - B_{12}} - \frac{(G_{12} + G_{21})}{2} + G_{22} - G_{\text{out}}^* + \frac{B_{21} + B_{12}}{2} \tag{10.197}$$

$$B_{\text{out}}^* = -105.63 \times 10^{-3} \tag{10.198}$$

$$jB_{\text{out}}^* = \frac{1}{jwL_3} \tag{10.199}$$

$$L_3 = 0.502 \text{ nH} \tag{10.200}$$

Figure 10.125 shows the simulated response of the oscillator circuit having resonance at 3120 MHz or 5% error. The little variation in resonance frequency may be
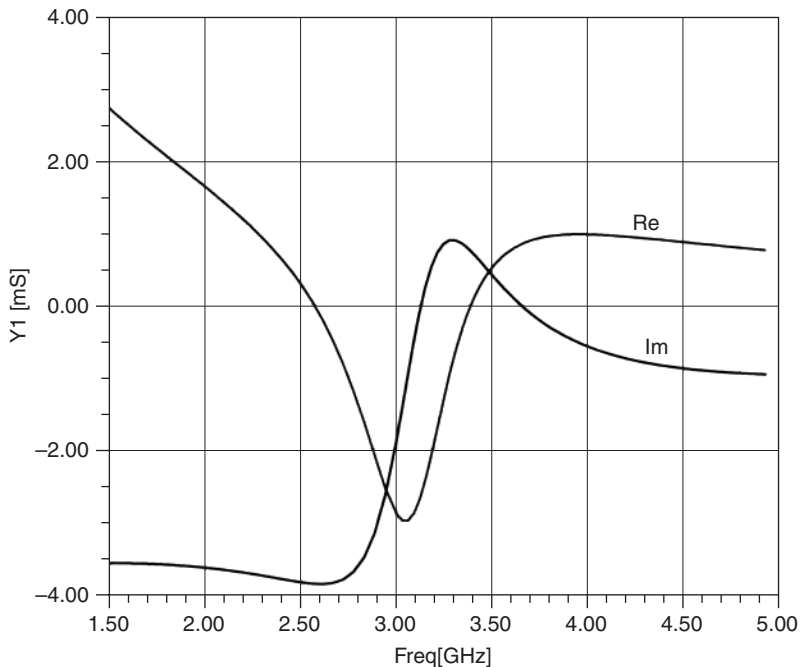
FIGURE 10.125   Real and imaginary currents for oscillation. The reactive current crosses the zero line at 3120 MHz; this is close, but not exactly at the point of most negative current.

due to the frequency-dependent packaged parameters, but it is a good starting value for tuning and optimization for the best phase noise and output power. The best phase noise at a given power output is basically dependent upon the ratio and absolute value of the feedback capacitors, which in turn depends upon the optimum drive level.

10.14   EXAMPLE FOR LARGE-SIGNAL DESIGN BASED ON BESSEL FUNCTIONS

Frequency $= 1000$ MHz

Power output $= 5$ mW

Load $= 500\ \Omega$

Figure 10.126 shows the schematic of the 1-GHz oscillator described above. The output termination is $500\ \Omega$.

Step 1: The 1000-MHz oscillator using the bipolar transistor BFP520 (Infineon) is designed based on analytical equations and is later verified with results. Based on the output power requirement and harmonics at a given load, the drive level is fixed.

The normalized drive level $x = 15$ is chosen to allow adequate drive level and to sustain oscillation and yet not produce excessive harmonic content. The normalized drive level x is defined as $\hat{V}_{be}$ over 0.026 V, where $\hat{V}_{be}$ is the ac component of V_{BE} [10.69].

For drive level $x = 15$, the fundamental peak current is given from a graph or table as

$$I_1(\text{fundamental}) = 1.932 I_{\text{dc}} \qquad (10.201)$$
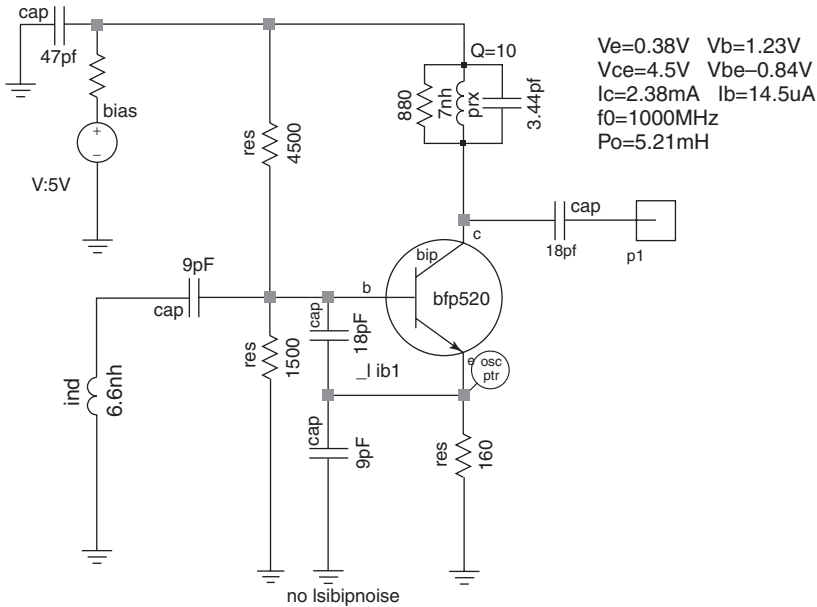
FIGURE 10.126   The 1000-MHz oscillator used in the design example.

where I_1 is the fundamental current specified by the output power needed for the designated load:

$$R_L = 500 \ \Omega \tag{10.202}$$

$$V_{\text{out}} = \sqrt{P_{\text{out}}(\text{mW}) \times 2R_L} = \sqrt{5 \times 10^{-3} \times 2 \times 500} = 2.236 \ \text{V}$$
$$\times \ (\text{no saturation voltage assumed!}) \tag{10.203}$$

$$I_1 = \frac{V_{\text{out}}}{500} = \frac{2.236}{500} = 4.472 \ \text{mA} \tag{10.204}$$

$$I_e = I_{\text{dc}} = \frac{I_1}{1.932} = \frac{4.472}{1.932} = 2.314 \ \text{mA} \tag{10.205}$$

Step 2: To avoid saturation in the transistor, select an emitter resistor R_e to maintain a sufficiently small emitter signal voltage about half the base–emitter drop. The dc emitter voltage also provides a reasonable offset to the variations in the base–emitter bias voltage. Here, R_e is set to 160 Ω. Using the common equation for biasing, the expression for the voltage at the base is given as

$$V_b = I_e \left(R_e + \frac{R_e}{\beta + 1} \right) + V_{be} = 1.23 \ \text{V} \tag{10.206}$$

where β is assumed to be around 100 and V_{be} is approximately 0.8 V. Bias resistors R_1 and R_2 are given as

$$V_b = \frac{R_2}{R_1 + R_2} V_{cc} = 1.23 \ \text{V} \Rightarrow \frac{R_1}{R_2} \approx 3 \tag{10.207}$$

$$R_1 = 1500 \ \Omega \tag{10.208}$$

$$R_2 = 4500 \ \Omega \tag{10.209}$$

$$V_{cc} = 5 \ \text{V} \tag{10.210}$$

Step 3: The large-signal transconductance is determined as

$$Y_{21} = \left. \frac{I_1}{V_1} \right|_{\text{fundamental freq}} = \frac{1.932 I_{\text{dc}}}{260 \ \text{mV}} = \frac{4.472 \ \text{mA}}{260 \ \text{mV}} = 17.2 \ \text{mS} \tag{10.211}$$

Step 4: The value of the *n*-factor is calculated from the equation above as

$$n^2(G_2 + G_3) - n(2G_3 + Y_{21}\alpha)$$
$$+ (G_1 + G_3 + Y_{21}) = 0 \tag{10.212}$$

$$G_1 = 0 \tag{10.213}$$

$$G_2 = \frac{1}{R_1 \| R_2} = 0.88 \ \text{mS} \tag{10.214}$$

$$G_3 = \frac{1}{R_e} = \frac{1}{160} = 6.25 \ \text{mS} \tag{10.215}$$

$$Y_{21} = 17.2 \ \text{mS} \tag{10.216}$$

where

$$\alpha = 0.99 \tag{10.217}$$

The quadratic equation above is reduced to

$$n^2(G_2 + G_3) - n(2G_3 + Y_{21}\alpha) + (G_1 + G_3 + Y_{21}) = 0 \tag{10.218}$$

$$n^2(0.88 + 6.25) - n(2 \times 6.25 + 17.2 \times 0.99) + (0 + 6.25 + 17.2) = 0 \tag{10.219}$$

$$7.13n^2 - 29.528n + 23.45 = 0 \tag{10.220}$$

where

$$n = \frac{29.528 \pm \sqrt{(29.528)^2 - 4 \times 7.13 \times 23.45}}{2 \times 7.13} = \frac{29.528 \pm \sqrt{871.9 - 668.794}}{2 \times 7.13} \tag{10.221}$$

$$= \frac{29.528 \pm 14.25}{14.26} \Rightarrow n_1 = 3.06 \quad \text{and} \quad n_2 = 1.071 \tag{10.222}$$

The higher value of the transformation factor n is selected, $n = 3$.

The values of C_1 and C_2 are calculated as

$$\frac{C_2}{C_1 + C_2} = \frac{1}{n} \Rightarrow C_2 = \frac{C_1}{n-1} \tag{10.223}$$

$$C_2 = \frac{C_1}{n-1} = \frac{C_1}{2} \Rightarrow \frac{C_1}{C_2} = 2 \tag{10.224}$$

The ratio of the capacitor C_1 to C_2 is 2. The absolute values of the capacitors are determined from the loop-gain condition of the oscillator as

$$Y_{21}|_{\text{large signal}} = G_m(x) = \frac{qI_{\text{dc}}}{kTx}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} = \frac{g_m}{x}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} \tag{10.225}$$

$$G_m(x) = \frac{1}{R_P}\frac{(C_1 + C_2)^2}{C_1 C_2} \tag{10.226}$$

$$\frac{g_m}{x}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} = \frac{1}{R_P}\frac{(C_1 + C_2)^2}{C_1 C_2} = \frac{1}{R_P}\frac{C_1}{C_2}\left(1 + \frac{C_2}{C_1}\right)^2 \tag{10.227}$$

$$\frac{88\ \text{mS}}{10} \times 1.932 = \frac{1}{R_P}\frac{C_1}{C_2}\left(1 + \frac{C_2}{C_1}\right)^2 \tag{10.228}$$

$$17.01 \times 10^{-3} = \frac{4.50}{R_P} \tag{10.229}$$

$$R_P = \frac{4.50}{17.01 \times 10^{-3}} = 264.5\ \Omega \tag{10.230}$$

The quality factor of the inductor is assumed to be 10 at 1000 MHz, the low-Q case.

The value of the inductor is obtained as

$$Q_T = \frac{R_P}{w_0 L} \Rightarrow L = \frac{264.5}{10 w_0} \tag{10.231}$$

$$L = \frac{264.5}{10 \times 2\pi \times 1000 \times 10^6} = 4.2 \text{ nH} \tag{10.232}$$

$$w = \sqrt{\frac{1}{L}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)} \tag{10.233}$$

$$w^2 = \frac{1}{L}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) = \frac{C_1 + C_2}{L C_1 C_2} \tag{10.234}$$

The value of the capacitor is determined as

$$C_2 = \frac{3}{w^2 \times 8.4 \times 10^{-9}} \Rightarrow C_2 = \frac{3}{331.5 \times 10^{-9}} = 9 \text{ pF} \tag{10.235}$$

$$C_1 = 2C_2 = 18 \text{ pF} \tag{10.236}$$

Step 5: The value of the coupling capacitor C_s is assumed to be 10 pF and the effect of C_s on the series reactance of the inductor L must be considered, adjusting the value of the inductor to

$$jw_0 L = jw_0 \left(L' - \frac{1}{w_0^2 C_s}\right) \tag{10.237}$$

$$jw_0 \times 4.2 \text{ nH} = jw_0 \left(L' - \frac{1}{w_0^2 \times 10 \times 10^{-12}}\right) \tag{10.238}$$

$$L' = 6.6 \text{ nH} \tag{10.239}$$

The base-lead inductance of the BFP520 is approximately 0.4 nH, and after correcting this, the effective value of the inductor is 6.2 nH.

Step 6: The harmonic content can be calculated from the table of Bessel functions as

$$x = 15 \Rightarrow I_1 = 1.932 I_{dc} \qquad I_2 = 1.742 I_{dc} \qquad I_3 = 1.272 I_{dc} \qquad I_4 = 0.887 I_{dc} \tag{10.240}$$

The parallel tank circuit at the output of the oscillator is designed to filter out higher harmonics:

$$Q = \frac{R}{wL} \tag{10.241}$$

$$= 20 \tag{10.242}$$

$$R = 880 \tag{10.243}$$

$$L = 7 \text{ nH} \tag{10.244}$$

$$C = 3.60 \text{ pF} \tag{10.245}$$
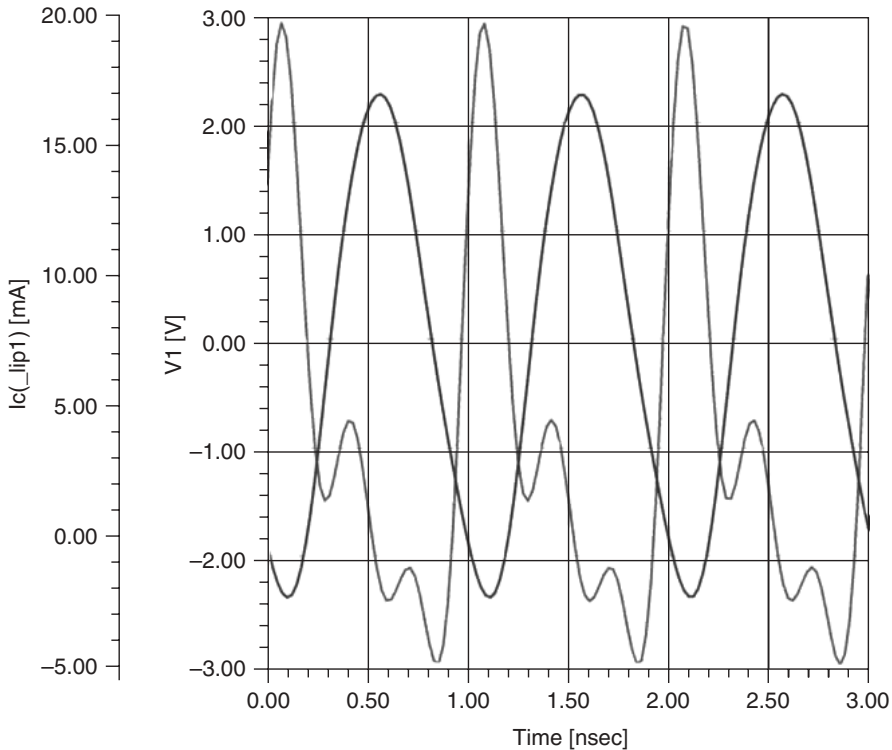
FIGURE 10.127   Base voltage and collector current of the oscillator in Figure 10.126.

The analytically calculated values are in good agreement with the simulated and published results. Figure 10.127 shows both the base–emitter voltage, which looks sinusoidal, and the collector current under the given operating condition. As previously shown, due to the harmonic content, there is a certain amount of ringing as well as negative collector current. This has to do with the tuned collector circuit.

Figure 10.128 shows the predicted phase noise as a function of the normalized drive level using values of x between levels 4 and 18. The phase noise is not the optimized phase noise for this configuration because the best phase noise can be achieved by adjusting the proper ratio and absolute values of feedback capacitors at a given drive level and required output power.

10.15   DESIGN EXAMPLE FOR BEST PHASE NOISE AND GOOD OUTPUT POWER

Figure 10.129 shows the parallel-tuned Colpitts oscillator circuit, which has to be designed with the following specifications. The unit was also built and measured. It uses a ceramic resonator and its equivalent circuit is shown. The performance for output power is given in Figure 10.130, and the predicted phase noise is given in Figure 10.131.
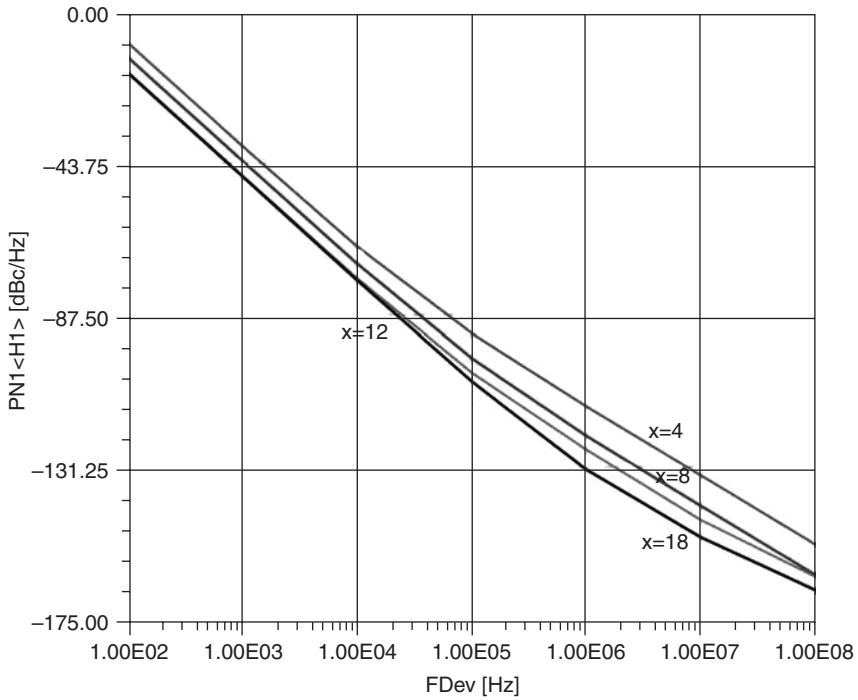
FIGURE 10.128   Predicted phase noise of the circuit shown in Figure 10.126 with different normalized drive levels.
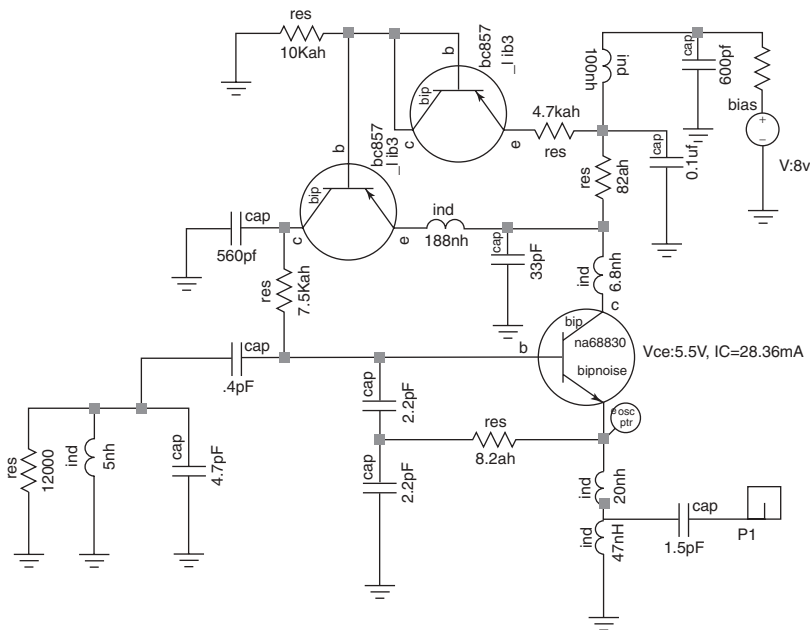
FIGURE 10.129   Schematic of the oscillator.

X1 = 1.00GHz
Y1 = 12.96
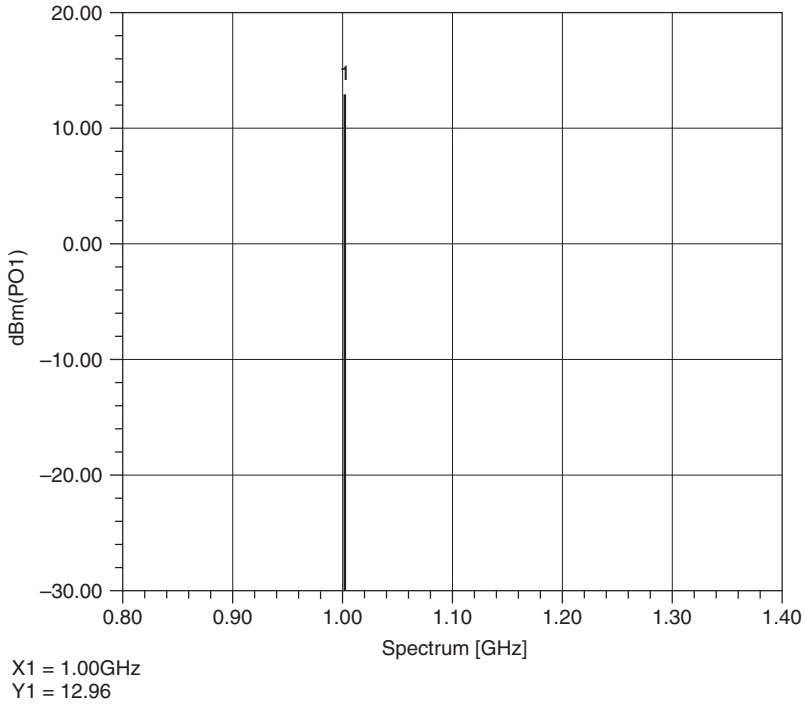
FIGURE 10.130   Predicted output power of the oscillator.

X1 = 1.00E04Hz
Y1 = −124.51dBc/Hz
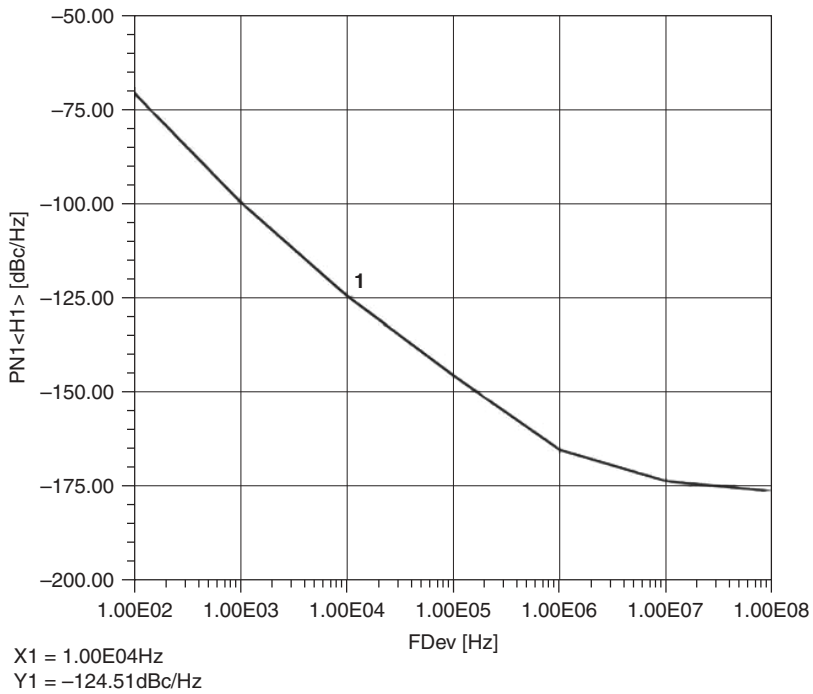
FIGURE 10.131   Predicted phase noise of the oscillator.

Requirements

- Output power requirement: 13 dBm
- Operating frequency: 1000 MHz
- Load: 50 Ω
- Phase noise: −124 dBc/Hz at 10 kHz

Design Steps   *Step 1—Calculation of operating point for fixed, normalized drive of* $x = 20$ *(high output power)*: Based on output power requirement, the following is calculated: The oscillator output voltage at the fundamental frequency is

$$V_{\text{out}}(\omega_0) = \sqrt{P_{\text{out}}(\omega_0)2R_L} = \sqrt{(20 \times 10^{-3}) \times 2 \times 50} \approx 1.414 \text{ V} \qquad (10.246)$$

The fundamental current is

$$I_{\text{out}}(\omega_0) = \frac{V_{\text{out}}(\omega_0)}{50} = \frac{1.414}{50} = 28.3 \text{ mA} \qquad (10.247)$$

The dc operating point is calculated based on the normalized drive level $x = 20$. The expression for the emitter dc can be given in terms of the Bessel function with respect to the drive level:

$$[I_E(\omega_0)] = 2I_{\text{dc}} \left[\frac{I_1(x)}{I_0(x)} \right] \qquad (10.248)$$

For the normalized drive level $x = 20$, the output emitter current at the fundamental frequency can be given as

$$[I_E(\omega_0)]_{x=20} = [I_{E1}(\omega_0)]_{x=20} + [I_{E2}(\omega_0)]_{x=20} = 2I_{\text{dc}} \left[\frac{I_1(x)}{I_0(x)} \right]_{x=20} \approx 56 \text{ mA} \qquad (10.249)$$

$$[I_{E1}(\omega_0)]_{x=20} = I_{\text{out}}(\omega_0) = 28.3 \text{ mA} \quad \text{(output current to load)} \qquad (10.250)$$

Figure 10.132 shows the oscillator circuit configuration in which dc and RF current distribution is shown and divided into its components:

$$[I_{E2}(\omega_0)]_{x=20} = [I_E(\omega_0)]_{x=20} - [I_{E1}(\omega_0)]_{x=20} = 27.3 \text{ mA} \qquad (10.251)$$

$$I_{E,\text{dc}} = \frac{[I_E(\omega_0)]_{x=20}}{2 \left[I_1(x)/I_0(x) \right]_{x=20}} = 28.3 \text{ mA} \qquad (10.252)$$

For this application, the NE68830 was selected.

Step 2—Biasing circuit: For the best phase noise close in near carrier frequency, a dc/ac feedback circuit is incorporated which provides the desired operating dc condition:

$$I_E = 28.3 \text{ mA}$$

$$V_{CE} = 5.5 \text{ V} \qquad \text{Supply voltage } V_{cc} = 8 \text{ V}$$

$$\beta = 120 \qquad I_B \approx 0.23 \text{ mA}$$
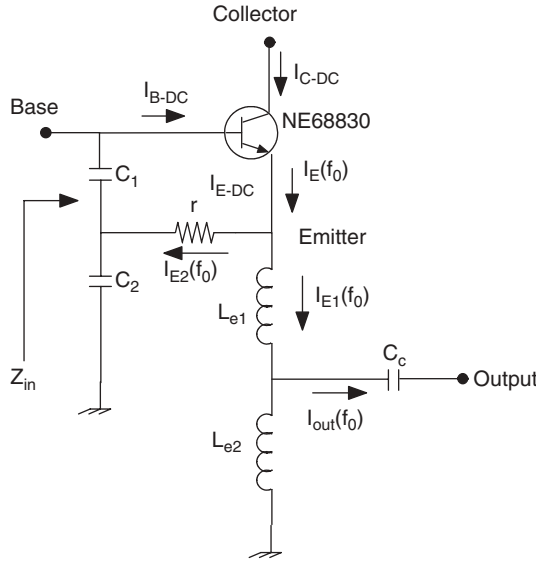
FIGURE 10.132 Output oscillator circuit configuration showing the current distribution.

Step 3—Calculation of large-signal transconductance:

$$Y_{21}|_{\text{large signal}} = G_m(x) = \frac{q I_{\text{dc}}}{kT x} \left[\frac{2 I_1(x)}{I_0(x)} \right]_{\text{fundamental}} \tag{10.253}$$

$$[Y_{21}]_{\omega=\omega_0} = \left[\frac{1.949 I_{E,\text{dc}}}{520 \text{ mV}} \right] = 0.107 \tag{10.254}$$

Step 4: The loop gain is given as

$$\text{Loop gain} = [LG]_{\text{sustained condition}} = \frac{R_P Y_{21}(x)}{n} = \left(\frac{R_P g_m}{x} \right) \left[\frac{2 I_1(x)}{I_0(x)} \right] \left(\frac{1}{n} \right) > 1 \tag{10.255}$$

$$R_{PEQ} = R_P \| \text{bias circuit} \Rightarrow 50.73 \ \Omega \tag{10.256}$$

As earlier derived, the loop gain should be 2.1 to have good starting conditions!

$$n = \frac{R_{PEQ} Y_{21}(x)}{2.1} = \frac{0.107 \times 50.73}{2.1} \approx 2.523 \tag{10.257}$$

Step 5—Calculation of feedback capacitor ratio:

$$n = 1 + \frac{C_1}{C_2} = 2.523 \Rightarrow \left[\frac{C_1}{C_2} \right]_{x=20} = 1.523 \tag{10.258}$$

Step 6—Calculation of absolute values of feedback capacitor: The expression of Z_{in} (looking in to the base of the transistor) can be given as

$$
Z_{in} \cong - \left[\left(\frac{Y_{21}}{\omega^2(C_1^* + C_p)C_2} \right) \left(\frac{1}{1 + \omega^2 Y_{21}^2 L_p^2} \right) \right]
$$
$$
- j \left[\left(\frac{C_1^* + C_P + C_2}{\omega(C_1^* + C_P)C_2} \right) - \left(\frac{\omega Y_{21} L_P}{1 + \omega^2 Y_{21}^2 L_p^2} \right) \left(\frac{Y_{21}}{\omega(C_1^* + C_P)C_2} \right) \right] \quad (10.259)
$$

where $C_P = C_{BEPKG} +$ contribution from layout $= 1.1$ pF
$\qquad L_P = L_B + L_{BX} +$ contribution from layout $= 2.2$ nH

The expression for the negative resistance R_n is given as

$$
R_{neg} = \frac{R_n}{1 + \omega^2 Y_{21}^2 L_P^2} = \frac{R_n}{1 + (2\pi \times 10^9)^2 \times (0.107)^2 \times (2.2 \text{ nH})^2} \quad (10.260)
$$

$$
R_{neg} \approx \frac{R_n}{3.65} \quad (10.261)
$$

$$
R_n = - \left[\frac{Y_{21}^+}{\omega^2 C_1 C_2} \right]_{x=20} = \frac{0.107}{(2\pi \times 10^9)^2 C_1 C_2} \quad (10.262)
$$

Here, R_n is the negative resistance without a parasitic (C_P, L_P). For sustained oscillation $\rightarrow R_{neg} \geq 2R_{PEQ} \cong 101.4 \ \Omega$:

$$
R_n = 3.65 \times 101.4 \approx 371 \ \Omega \quad (10.263)
$$

$$
C_1 C_2 = \left(\frac{1}{\omega^2} \right) \left(\frac{0.107}{371} \right) \approx 7.26 \quad (10.264)
$$

$$
\left[\frac{C_1}{C_2} \right]_{x=20} \approx 1.52 \quad (10.265)
$$

$$
C_1 = 3.3 \text{ pF} \quad (10.266)
$$

$$
C_2 = 2.2 \text{ pF} \quad (10.267)
$$

Step 7—Calculation of coupling capacitor c_e: The expression for the coupling capacitor is

$$
\frac{C}{10} > C_c > \frac{(w^2 C_1 C_2)(1 + w^2 Y_{21}^2 L_P^2)}{(Y_{21}^2 C_2 - w^2 C_1 C_2)(1 + w^2 Y_{21}^2 L_P^2)(C_1 + C_P + C_2)} \quad (10.268)
$$

$$
C_c \rightarrow 0.4 \text{ pF} \quad (10.269)
$$

Tables 10.12 and 10.13 show NE68830 nonlinear parameters and package parameters, which were taken from the NEC data sheets.

Figure 10.133 shows the transistor in the package parameters for the calculation of the oscillator frequency and loop gain.

TABLE 10.12   Nonlinear Parameters of NE68830

Parameter	Q	Parameter	Q
IS	3.8×10^{-16}	MJC	0.48
BF	135.7	XCJC	0.56
NF	1	CJS	0
VAF	28	VJS	0.75
IKF	0.6	MJS	0
NE	1.49	TF	11×10^{-12}
BR	12.3	XTF	0.36
NR	1.1	VTF	0.65
VAR	3.5	ITF	0.61
IKR	0.06	PTF	50
ISC	3.5×10^{-16}	TR	32×10^{-12}
NC	1.62	EG	1.11
RE	0.4	XTB	0
RB	6.14	XTI	3
RBM	3.5	KF	0
IRB	0.001	AF	1
RC	4.2	VJE	0.71
CJE	0.79×10^{-12}	MJE	0.38
CJC	0.549×10^{-12}	VJC	0.65

TABLE 10.13   Package Parameters of NE68830

Parameter	Values
C_{CB}	0.24×10^{-12}
C_{CE}	0.27×10^{-12}
L_B	0.5×10^{-9}
L_E	0.86×10^{-9}
C_{CBPKG}	0.08×10^{-12}
C_{CEPKG}	0.04×10^{-12}
C_{BEPKG}	0.04×10^{-12}
L_{BX}	0.2×10^{-9}
L_{CX}	0.1×10^{-9}
L_{EX}	0.2×10^{-9}

Design Calculations

1. The frequency of the oscillation is calculated as

$$\omega_0 = \sqrt{\frac{(C_1^* + C_P)C_2/(C_1^* + C_P + C_2) + C_c}{L\left\{\begin{array}{l}(C_1^* + C_P)C_2 C_c/(C_1^* + C_P + C_2) \\ +C\left[(C_1^* + C_P)C_2/(C_1^* + C_P + C_2) + C_c\right]\end{array}\right\}}} \approx 1000 \text{ MHz}$$

(10.270)

where

$$L = 5 \text{ nH} \quad \text{(inductance of parallel resonator circuit)}$$
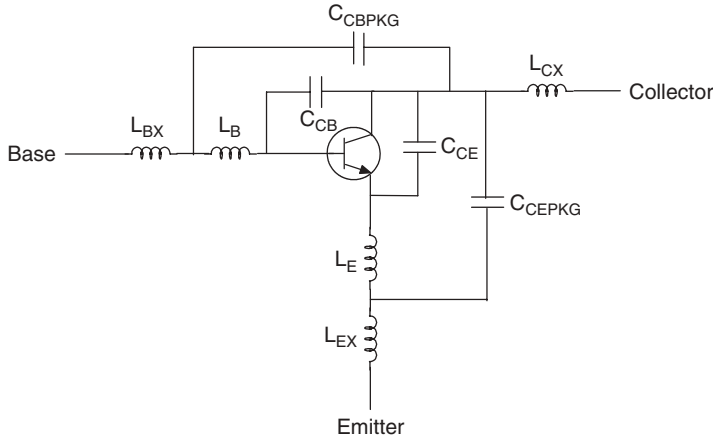
FIGURE 10.133   NE68830 with package parasitics; Q is the intrinsic bipolar transistor.

$$C_1^* = 2.2 \text{ pF} \qquad C_1 = C_1^* + C_P$$

$$C_P = 1.1 \text{ pF} \quad (C_{\text{BEPKG}} + \text{contribution from layout})$$

$$C_2 = 2.2 \text{ pF} \qquad C_c = 0.4 \text{ pF} \qquad C = 4.7 \text{ pF}$$

$$R_P = 12{,}000 \quad \text{(measured)} \qquad Q_{\text{unloaded}} = \left[\frac{R_P}{\omega L}\right] = 380$$

2. Figure 10.134 shows the phase noise contribution due to resonator (parallel loss resistance) loss resistance at 10 kHz offset. Figure 10.135 shows the phase noise contribution due to base resistance at 10 kHz offset. Figure 10.136 shows the phase noise contribution due to the base current and flicker noise contribution at 10 kHz offset. Figure 10.137 shows the phase noise contribution due to the collector current at 10 kHz offset. Figure 10.138 shows the total effect of all the four noise sources (PN_1, PN_2, PN_3, and PN_4) at 10 kHz offset.
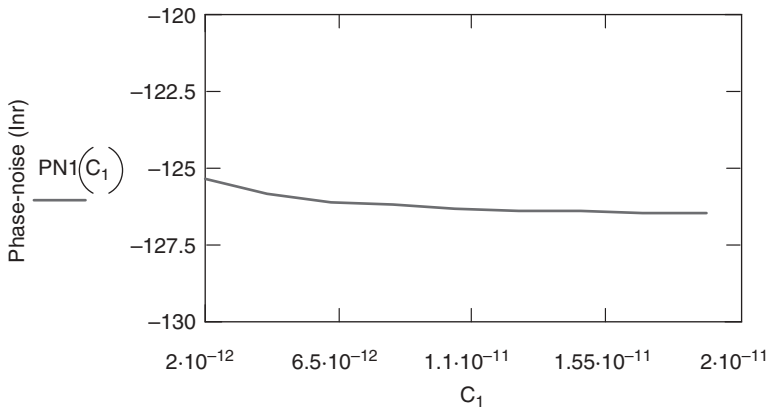
FIGURE 10.134   Phase noise contribution of lossy resonator at 10 kHz offset.
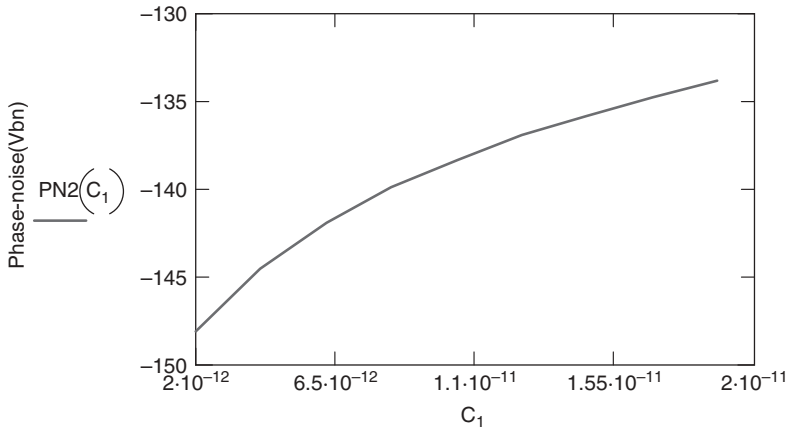
FIGURE 10.135   Phase noise contribution due to the base resistance at 10 kHz offset.
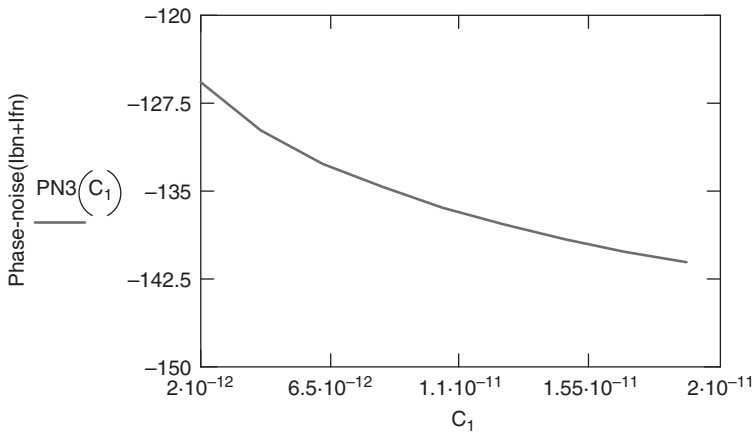
FIGURE 10.136   Phase noise contribution due to base current and flicker noise at 10 kHz offset.
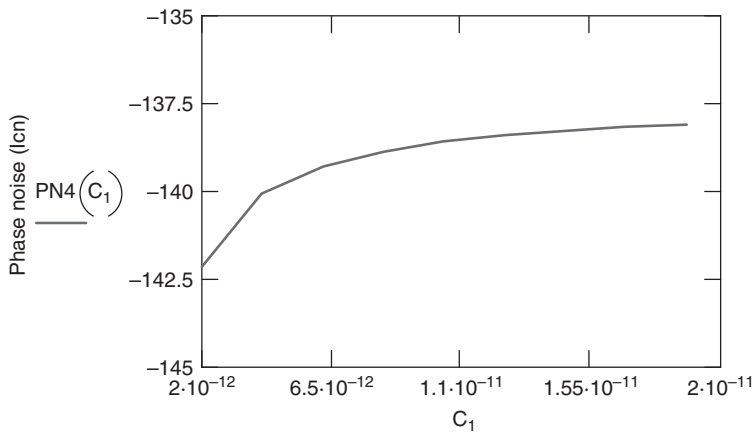
FIGURE 10.137   Phase noise contribution due to the collector current at 10 kHz offset.
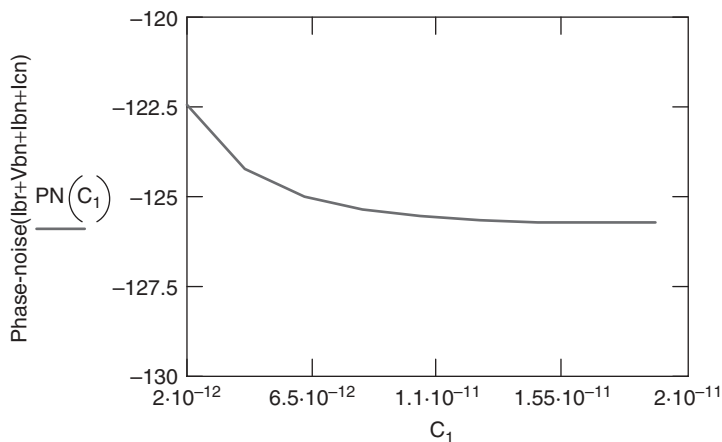
FIGURE 10.138   Total effect of all four-noise sources at 10 kHz offset.

The calculated phase noise at 10 kHz off the carrier is -124 dBc/Hz, which agrees with the measurements within 1 dB. The other values are -140 dBc/Hz at 100 kHz offset and 1 MHz offset is -160 dBc/Hz.

The important conclusion is that for the first time we have a complete mathematical synthesis procedure for best phase noise that covers both flicker noise and white noise for the oscillator. In the past most publications and dissertations have referenced an oscillator built with many shortcuts and then the author found that the measured results agree with the expectations. A complete synthesis approach has not been done.

10.16   CAD SOLUTION FOR CALCULATING PHASE NOISE IN OSCILLATORS

The following will address various important issues on noise. Noise and oscillators have already been discussed, but since many publications which have been referenced omitted a lot of important steps, it is difficult to follow the noise concept. The noise discussion has two aspects. One is a physics-based aspect and one is a mathematical-based aspect. In the earlier section, noise was explained from a physics point of view. Now all the necessary mathematical tools will be presented. The mechanism that adds the noise, both close-in noise and far-out noise, to the carrier will be mathematically described. The resulting noise figure, under large-signal condition, is an important issue. When modeling the transistors, typically the noise correlation is incomplete. This portion, which deals with the inner transistor, was discussed in Sections 7.13 and 7.14 of Chapter 7.

Two important linear noise models are necessary to understand the SSB noise. One is the Leeson phase noise equation [10.4] and the other is based on the Lee and Hajimiri noise model [10.65]. Noise theory can be divided into modulation noise and conversion noise. All of this will be explained in detail.

10.16.1 General Analysis of Noise Due to Modulation and Conversion in Oscillators

The degree to which an oscillator generates constant frequency throughout a specified period of time is defined as the frequency stability of the oscillator. The cause of frequency instability is due to the presence of noise in the oscillator circuit that effectively modulates the signal, causing a change in frequency spectrum commonly known as phase noise.

The unmodulated carrier signal is represented as

$$f(t) = A \cos(2\pi f_c t + \theta_0) \tag{10.271}$$

$$\theta = 2\pi f_c t + \theta_0 \tag{10.272}$$

$$f_c = \frac{1}{2\pi} \left(\frac{d\theta}{dt} \right) \tag{10.273}$$

For the case of an unmodulated signal, f_c is constant and is expressed by the time derivative of the phase (angle θ), but in general, this derivative is not constant and can be represented as an instantaneous frequency which can vary with time and is expressed as $f_i = (1/2\pi)(d\theta_i/dt)$ and the corresponding phase is determined as $\theta_i(t) = \int 2\pi f_i dt$. For the unmodulated carrier $\theta_i(t) = (2\pi f_c t + \theta_0)$, where $\theta_0 = \theta_i(t)|_{t=0}$.

The phase/angle of the carrier can be varied linearly by the modulating signal $m(t)$, which results in phase modulation as $\theta_i(t)$:

$$\theta_i(t) = 2\pi f_c t + k_p m(t) \tag{10.274}$$

where k_p is the phase sensitivity and its dimension is given as radians per units of the modulating signal and the instantaneous frequency w_i of the carrier is modified by modulation with the modulating signal as

$$w_i = \frac{d\theta_i}{dt} \Rightarrow w_i = w_c + k_p \frac{dm}{dt} \tag{10.275}$$

The phase-modulated signal can be expressed in the time domain as

$$s(t) = A_c \cos[2\pi f_c t + k_p m(t)] \tag{10.276}$$

10.16.2 Modulation by a Sinusoidal Signal

Consider a sinusoidal modulating signal given by $m(t) = A_m \cos(2\pi f_m t)$ and the instantaneous frequency of the modulated signal is given as

$$f_i(t) = f_c + k_f A_m \cos(2\pi f_m t) \tag{10.277}$$

$$= f_c + \Delta f \cos(2\pi f_m t) \tag{10.278}$$

$$\Delta f = k_f A_m \tag{10.279}$$

where Δf is the frequency deviation corresponding to the maximum variation of the instantaneous frequency of the modulated signal from the carrier frequency. The angle of the modulated signal is determined by integration as

$$\theta_i(t) = 2\pi \int_0^t f_i(t) \, dt \tag{10.280}$$

$$= 2\pi f_c + \frac{\Delta f}{f_m} \sin(2\pi f_m t) \tag{10.281}$$

The coefficient of the sine term is called the modulation index of the modulating signal and is denoted by $\beta = \Delta f / f_m$. The expression for the angle of the modulated signal can be written as $\theta_i(t) = 2\pi f_c + (\Delta f / f_m) \sin(2\pi f_m t)$ and the time representation of the modulated signal can be expressed as

$$s(t) = A_c \cos[\theta_i(t)] = A_c \cos[2\pi f_c t + \beta \sin(2\pi f_m t)] \tag{10.282}$$

$$= \text{Re}[A_c e^{j[2\pi f_c t + \beta \sin(2\pi f_m t)]}] \tag{10.283}$$

$$= \text{Re}[\sigma(t) A_c e^{j2\pi f_c t}] \tag{10.284}$$

where $\sigma(t)$ is the complex envelope of the frequency-modulated signal and can be given as $\sigma(t) = A_{cn} e^{j\beta \sin(2\pi f_m t)}$; it is a periodic function of time with a fundamental frequency equal to the modulating frequency f_m and can be expressed as

$$\sigma(t) = \sum_{n=-\infty}^{\infty} C_n e^{j2\pi f_m t} \tag{10.285}$$

where C_n is the Fourier coefficient given as

$$C_n = f_m \int_{-1/2\pi f_m}^{1/2\pi f_m} \sigma(t) e^{-j2\pi f_m t} \, dt \tag{10.286}$$

$$= A_c f_m \int_{-1/2\pi f_m}^{1/2\pi f_m} e^{j[\beta \sin(2\pi f_m t) - j2\pi f_m t]} \, dt \tag{10.287}$$

$$= A_c f_m \int_{-1/2\pi f_m}^{1/2\pi f_m} e^{j(\beta \sin x - nx)} \, dt \tag{10.288}$$

where $x = 2\pi f_m t$ and the expression of coefficients may be rewritten as $C_n = (A_c/2\pi) \int_{-\pi}^{\pi} e^{j(\beta \sin x - nx)} dx$. This equation is called the nth-order Bessel function of the first kind with argument β. The expressions for $\sigma(t)$ and $s(t)$ are given as

$$\sigma(t) = \sum_{n=-\infty}^{\infty} C_n e^{j2\pi f_m t} = A_c \sum_{n=-\infty}^{\infty} J_n(\beta) e^{j2\pi f_m t} \tag{10.289}$$

$$s(t) = A_c \, \text{Re}\left[\sum_{n=-\infty}^{\infty} J_n(\beta) e^{j2\pi(f_c + nf_m)t} \right] = A_c \sum_{n=-\infty}^{\infty} J_n(\beta) \cos[2\pi(f_c + nf_m)t] \tag{10.290}$$

Applying a Fourier transform to the time-domain signal $s(t)$ results in an expression for the discrete frequency spectrum of $s(t)$ as

$$s(f) = \frac{A_c}{2} \sum_{n=-\infty}^{\infty} J_n(\beta)[\delta(f - f_c - nf_m) + (f + f_c + nf_m)] \quad (10.291)$$

$$\sum_{n=-\infty}^{\infty} J_n(\beta)^2 = 1 \qquad (10.292)$$

The spectrum of the frequency-modulated signal has an infinite number of symmetrically located sideband components spaced at frequencies of $f_m, 2f_m, 3f_m, \ldots, nf_m$ around the carrier frequency. The amplitudes of the carrier component and the sideband components are the products of the carrier amplitude and a Bessel function.

10.16.3 Modulation by a Noise Signal

Consider a noise signal defined as $n(t) = r_n(t) \cos[2\pi f_c t + \theta + \Phi_n(t)]$ introduced to an oscillator circuit in a random fashion and the desired oscillator output signal is represented by $f(t) = A \cos(2\pi f_c t + \theta)$. Assume $r_n(t)$ is the coefficient of the noise signal having a Rayleighdistribution and functions of a noise signal. The phase $\Phi_n(t)$ is linearly distributed and is a distribution function of a noise signal. The output of the oscillator circuit is given as the superposition of the combined signal, which is expressed as

$$g(t) = f(t) + n(t) \tag{10.293}$$

$$= A \cos[(2\pi f_c t + \theta)] + r_n(t) \cos[2\pi f_c t + \theta + \Phi_n(t)] \tag{10.294}$$

$$= A \cos[(2\pi f_c t + \theta)] + r_n(t) \cos[\Phi_n(t)] \cos[2\pi f_c t + \theta]$$
$$\quad - r_n(t) \sin[\Phi_n(t)] \sin[2\pi f_c t + \theta] \tag{10.295}$$

$$= \cos[(2\pi f_c t + \theta)]\{A + r_n(t) \cos[\Phi_n(t)]\} - r_n(t) \sin[\Phi_n(t)] \sin[2\pi f_c t + \theta] \tag{10.296}$$

$$= \sqrt{C_1^2 + C_2^2}\left[\frac{C_1}{\sqrt{C_1^2 + C_2^2}} \cos \Phi_e(t) - \frac{C_2}{\sqrt{C_1^2 + C_2^2}} \sin \Phi_e(t) \right] \tag{10.297}$$

$$= \left[\sqrt{C_1^2 + C_2^2} \right] \cos[\psi + \Phi_e(t)] \tag{10.298}$$

where

$$\sin[\Phi_e(t)] = \frac{C_2}{\sqrt{C_1^2 + C_2^2}} \tag{10.299}$$

$$\cos[\Phi_e(t)] = \frac{C_1}{\sqrt{C_1^2 + C_2^2}} \tag{10.300}$$

$$R(t) = \sqrt{C_1^2 + C_2^2} \tag{10.301}$$

$$g(t) = C_1 \cos\psi - C_2 \sin\psi \tag{10.302}$$

$$C_1 = A + r_n(t)\cos[\Phi_n(t)] \tag{10.303}$$

$$C_2 = r_n(t)\sin[\Phi_n(t)] \tag{10.304}$$

$$\psi = 2\pi f_c t + \theta \tag{10.305}$$

The phase term $\Phi_e(t)$ is a time-variant function and can be represented as

$$\Phi_e(t) = \tan^{-1}\left[\frac{C_2}{C_1}\right] = \tan^{-1}\left[\frac{r_n(t)\sin[\Phi_n(t)]}{A + r_n(t)\cos[\Phi_n(t)]}\right] \tag{10.306}$$

For large signal-to-noise ratio (SNR), $\Phi_e(t)$ can be approximated as

$$\Phi_n(t) = \frac{r_n(t)}{A}\sin[\Phi_n(t)] \tag{10.307}$$

and the oscillator output signal can be expressed as

$$g(t) = f(t) + n(t) \Rightarrow g(t) = R(t)\cos[2\pi f_c t + \theta + \Phi_e(t)] \tag{10.308}$$

$$R(t) = \sqrt{C_1^2 + C_2^2} = \{[A + r_n(t)\cos[\Phi_n(t)]]^2 + r_n(t)\sin[\Phi_n(t)]^2\} \tag{10.309}$$

which is phase modulated due to the noise signal $n(t)$, and the resultant oscillator output signal contains modulation sidebands due to noise present in the circuit, which is called phase noise.

The amplitude of a phase modulation sideband is given by the product of the carrier amplitude and a Bessel function of the first kind and can be expressed as

$$A_{\text{SSB}} = \tfrac{1}{2}A_c[J_n(\beta)]_{n=1} \tag{10.310}$$

$$\frac{A_{\text{SSB}}}{A_c} = \tfrac{1}{2}[J_1(\beta)] \tag{10.311}$$

$$\frac{A_{\text{SSB}}}{A_c} = \frac{P_{\text{SSB}}}{P_c} \tag{10.312}$$

$$L(f) = 10\log\left[\frac{P_{\text{SSB}}}{P_c}\right] - 10\log[\text{BW}_n] \tag{10.313}$$

where $L(f)$ is phase noise due to noise modulation, A_{SSB} is the sideband amplitude of the phase modulation at offset Δf from the carrier, and BW_n is the noise bandwidth in hertz.

10.16.4 Oscillator Noise Models

At present, two separate but closely related models of oscillator phase noise exist. The first is proposed by Leeson [10.4], referred to as Lesson's model and the noise

prediction using Leeson's model is based on time-invariant properties of the oscillator such as resonator Q, feedback gain, output power, and noise figure.

Leeson has introduced a linear approach for calculation of oscillator phase noise, and his noise formula was extended by Rohde by adding $2kTRK_0^2/f_m^2$ [10.66].

Modified Lesson Phase Noise Equation

$$\mathcal{L}(f_m) = 10 \log \left\{ \left[1 + \frac{f_0^2}{(2 f_m Q_L)^2 (1 - Q_L/Q_0)^2} \right] \left(1 + \frac{f_c}{f_m} \right) \frac{FkT}{2 P_{sav}} + \frac{2kTRK_0^2}{f_m^2} \right\} \tag{10.314}$$

where $\mathcal{L}(f_m) =$ SSB noise power spectral density defined as ratio of sideband power in 1 Hz bandwidth at f_m to total power in dB, dBc/Hz

$\quad\quad f_m =$ frequency offset

$\quad\quad f_0 =$ center frequency

$\quad\quad f_c =$ flicker frequency, region between $1/f^3$ and $1/f^2$

$\quad\quad Q_L =$ loaded Q of tuned circuit

$\quad\quad Q_0 =$ unloaded Q of tuned circuit

$\quad\quad F =$ noise figure of oscillator

$\quad\quad kT = 4.1 \times 10^{-21}$ at 300 K (room temperature)

$\quad\quad P_{sav} =$ average power at oscillator output

$\quad\quad R =$ equivalent noise resistance of tuning diode

$\quad\quad K_0 =$ oscillator voltage gain

The last term of Lesson's phase noise equation is responsible for the modulation noise.

Shortcomings of Modified Leeson Noise Equation   The noise figure F is empirical, a priori, and difficult to calculate due to the linear time-variant (LTV) characteristics of the noise.

Phase noise in the $1/f^3$ region is an empirical expression with fitting parameters.

Lee and Hajimiri Noise Model [10.65]   The second noise model was proposed by Lee and Hajimiri and is based on the time-varying properties of the oscillator current waveform.

The phase noise equation for the $1/f^3$ region can be expressed as

$$\mathcal{L}(f_m) = 10 \log \left(\frac{C_0^2}{q_{\max}^2} \frac{i_n^2/\Delta f}{8 f_m^2} \frac{w_{1/f}}{f_m} \right) \tag{10.315}$$

and the phase noise equation for the $1/f^2$ region can be expressed as

$$\mathcal{L}(f_m) = 10 \log \left(\frac{\Gamma_{\text{rms}}^2}{q_{\max}^2} \frac{i_n^2/\Delta f}{4 f_m^2} \right) \tag{10.316}$$

where $C_0 =$ coefficient of Fourier series, zero order of impulse sensitivity function (ISF)

$\quad\quad i_n =$ noise current magnitude

$\quad\quad \Delta f =$ noise bandwidth

$\quad\quad w_{1/f} = 1/f$ noise corner frequency of device/transistor

q_{max} = maximum charge on capacitors in resonator
Γ_{rms} = rms value of ISF

Shortcomings of Lee and Hajimiri Noise Model

The ISF function is tedious to obtain and depends upon the topology of the oscillator. It is mathematical yet lacks practicality.

The $1/f$ noise conversion is not clearly specified.

10.16.5   Modulation and Conversion Noise

Modulation noise is defined as the noise that is generated by actually modulating the oscillator due to the tuning diode. The noise associated with the series loss resistance in the tuning diode will introduce frequency modulation, which is further translated into the oscillator phase noise, and this portion of the noise is responsible for the near-carrier noise. There is an additional phenomenon called conversion noise, which produces noise in a manner similar to the mixing process.

10.16.6   Nonlinear Approach for Computation of Noise Analysis of Oscillator Circuits

The mechanism of noise generation in autonomous circuits and oscillators combines the equivalent of modulation and frequency conversion (mixing) with the effect of AM-to-PM conversion.

Traditional approaches relying on frequency conversion analysis are not sufficient to describe the complex physical behavior of a noisy oscillator. The accuracy of this nonlinear approach is based on the dynamic range of the harmonic balance simulator and the quality of the parameter extraction for the active device.

Figure 10.139 shows a general noisy nonlinear network which is subdivided into linear and nonlinear subnetworks and noise-free multiports. Noise generation is accounted for by connecting a set of noise voltage and noise current sources at the ports of the linear and nonlinear subnetwork. It is assumed that the circuit is forced by a dc source and a set of sinusoidal sources located at the carrier harmonics $k\omega_0$ and at the sideband $\omega + k\omega_0$.

The electrical regime under this condition of the autonomous circuit will be quasiperiodic, and the nonlinear system to be solved is formulated in terms of the harmonic balance error vector E, defined as the difference between linear and nonlinear current harmonics at the common ports of the circuits.

The solution of this nonlinear algebraic system can be expressed in the form

$$E(X_B, X_H) = F \qquad (10.317)$$

$$\Rightarrow E_B, E_H \qquad (10.318)$$

where F = forcing term comprised of dc, harmonics, and sideband excitations
X_B = state-variable (SV) vectors consisting of components at sideband
X_H = (SV) vectors consisting of components at carrier harmonics
E = vector of real and imaginary parts of all HB errors
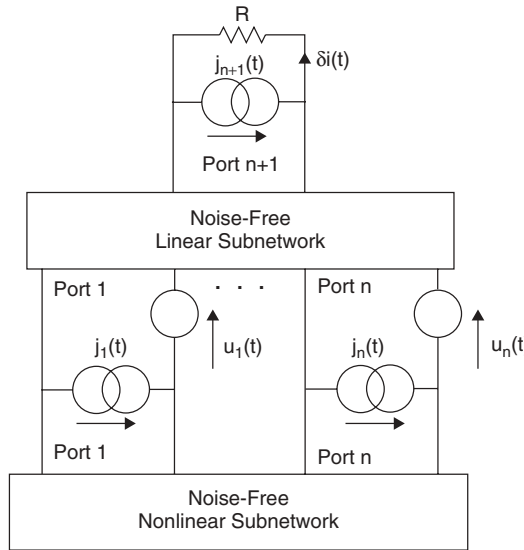
FIGURE 10.139   Shows a general noisy nonlinear network.

E_B = error subvector due to sideband
E_H = error subvector due to carrier harmonics

Under autonomous (noiseless) steady-state conditions, the forcing term F will contain only dc excitations and the possible solution for the nonlinear algebraic system $E(X_B, X_H) = F$ will have the form

$$X_B = 0 \tag{10.319}$$

$$X_H = X_H^{\text{ss}} \rightarrow \text{steady state} \tag{10.320}$$

Since the system is operating under autonomous conditions, the phase of the steady state will be arbitrary, and the carrier frequency ω_0 represents one of the unknowns of the nonlinear algebraic system above $E(X_B, X_H) = F$, so that one of the harmonics of the vector X_H is replaced by ω_0.

Now, let us assume that the steady-state condition of the autonomous (noiseless) circuit is perturbed by a set of small-signal noise sources generated inside the linear/nonlinear subnetwork ports of the circuit; this situation can be described by introducing a noise voltage and a noise current source at every interconnecting port, as shown in Figure 10.139.

Under small noise perturbations, the noise-induced deviation $[\partial X_B, \partial X_H]$ of the system state from the autonomous (noiseless) steady state $[0, X_H^{\text{SS}}]$ can be quantitatively expressed by perturbing the expression $E(X_B, X_H) = F$ in the neighborhood of the steady state as

$$\left[\frac{\partial E_B}{\partial X_B}\right]_{\text{ss}} \partial X_B + \left[\frac{\partial E_B}{\partial X_H}\right]_{\text{ss}} \partial X_H = J_B(\omega) \Rightarrow M_{BB}\partial X_B + M_{BH}\partial X_H = J_B(\omega)$$

$$\tag{10.321}$$

$$\left[\frac{\partial E_H}{\partial X_B}\right]_{ss} \partial X_B + \left[\frac{\partial E_H}{\partial X_H}\right]_{ss} \partial X_H = J_H(\omega) \Rightarrow M_{HB}\partial X_B + M_{HH}\partial X_H = J_H(\omega)$$

(10.322)

where

$$M_{BB} = \left[\frac{\partial E_B}{\partial X_B}\right]_{ss}$$

(10.323)

$$M_{BH} = \left[\frac{\partial E_B}{\partial X_H}\right]_{ss}$$

(10.324)

$$M_{HB} = \left[\frac{\partial E_H}{\partial X_B}\right]_{ss}$$

(10.325)

$$M_{HH} = \left[\frac{\partial E_H}{\partial X_H}\right]_{ss}$$

(10.326)

and M is the Jacobian matrix of the HB errors and can be expressed as

$$M = \begin{bmatrix} \left.\frac{\partial E_B}{\partial X_B}\right|_{ss} & \left.\frac{\partial E_B}{\partial X_H}\right|_{ss} \\ \left.\frac{\partial E_H}{\partial X_B}\right|_{ss} & \left.\frac{\partial E_H}{\partial X_H}\right|_{ss} \end{bmatrix}$$

(10.327)

At a steady-state condition, $X_B = 0 \Rightarrow M_{BH}$ and $M_{HB} = 0$ and the system of equations will be reduced to a set of uncoupled equations as

$$\left[\frac{\partial E_B}{\partial X_B}\right]_{ss} \partial X_B = J_B(\omega) \Rightarrow M_{BB}\partial X_B = J_B(\omega)$$

(10.328)

$$\left[\frac{\partial E_H}{\partial X_H}\right]_{ss} \partial X_H = J_H(\omega) \Rightarrow M_{HH}\partial X_H = J_H(\omega)$$

(10.329)

In the equation above, $M_{BB}\partial X_B = J_B(\omega)$ is responsible for the mechanism of the conversion noise, which is being generated by the exchange of the power between the sidebands of the unperturbed large-signal steady state through the frequency conversion in the nonlinear subnetwork/devices. The equation $M_{HH}\partial X_H = J_H(\omega)$ is responsible for the mechanism of modulation noise, which is being described as a jitter of the oscillatory steady state.

10.16.7   Noise Generation in Oscillators

The physical effects of random fluctuations taking place in the circuit are different depending on their spectral allocation with respect to the carrier:

Noise components at low-frequency deviations result in frequency modulation of the carrier through a mean-square frequency fluctuation proportional to the available noise power.

Noise components at high-frequency deviations result in phase modulation of the carrier through a mean-square phase fluctuation proportional to the available noise power.

10.16.8   Frequency Conversion Approach

The circuit has a large-signal, time-periodic, steady-state fundamental angular frequency ω_0 (carrier). Noise signals are small perturbations superimposed on the steady state, represented by families of pseudosinusoids located as the sidebands of the carrier harmonics. The noise sources are modeled as pseudosinusoids having random amplitudes, phases, and deterministic frequencies corresponding to the noise sidebands.

Therefore, the noise performance of the circuit is determined by the exchange of the power between the sidebands of the unperturbed steady state through frequency conversion in the nonlinear subnetwork. From the expression $M_{BB} \partial X_B = J_B(\omega)$, it can be seen that the oscillator noise is essentially an additive noise that is superposed on each harmonic of a lower and upper sideband at the same frequency offset.

10.16.9   Conversion Noise Analysis

Consider a set of noise current and voltage source connected to the linear/nonlinear subnetwork ports as shown in Figure 10.139. The vectors of the sideband phasor of such sources at the pth noise sideband $\omega + p\omega_0$ are represented by $J_p(\omega)$ and $U_p(\omega)$, respectively, where ω is the frequency offset from the carrier ($0 \leq \omega \leq \omega_0$). Due to the perturbative assumption, the nonlinear subnetwork can be replaced with a multi-frequency linear multiport described by a conversion matrix. The flow of noise signals can be computed by the conventional linear circuit techniques.

Assuming that the noise perturbations are small, the kth sideband phasor of the noise current through a load resistance R may be expressed through frequency conversion analysis by the linear relationship

$$\partial I_k(\omega) = \sum_{p=-nH}^{nH} T_{k,p}^J(\omega) J_p(\omega) = \sum_{p=-nH}^{nH} T_{k,p}^U(\omega) U_p(\omega) \tag{10.330}$$

For $k = 0$, upper and lower sideband noise is given as $\partial I_0(\omega)$ and $\partial I_0(-\omega) = \partial I_0^{\otimes}(\omega)$.

Here, $T_{k,p}^J(\omega)$ and $T_{k,p}^U(\omega)$ are the conversion matrices and n_H is the number of the carrier harmonics taken into account in the analysis. From the equation above, the correlation coefficient of the kth and rth sidebands of the noise delivered to the load can be given as

$$C_{k,r}(\omega) = R \langle \partial I_k(\omega) \partial I_r^*(\omega) \rangle \tag{10.331}$$

$$= R \sum_{p,q=-nH}^{nH} \{ [T_{k,p}^J(\omega) \langle J_p(\omega) J_q^{\otimes}(\omega) \rangle T_{r,q}^{J\otimes}(\omega)] \tag{10.332}$$

$$+ [T_{k,p}^U(\omega) \langle U_p(\omega) U_q^{\otimes}(\omega) \rangle T_{r,q}^{U\otimes}(\omega)] \tag{10.333}$$

$$+ [T_{k,p}^J(\omega) \langle J_p(\omega) U_q^{\otimes}(\omega) \rangle T_{r,q}^{U\otimes}(\omega)] \tag{10.334}$$

$$+ [T_{k,p}^U(\omega) \langle U_p(\omega) J_q^{\otimes}(\omega) \rangle T J_{r,q}^{J\otimes}(\omega)] \} \tag{10.335}$$

where the asterisk denotes the complex conjugate, $\otimes$ denotes the conjugate transposed, and $\langle\bullet\rangle$ denotes the ensemble average. The sideband noise sources are denoted by $J_p(\omega)$ and $U_p(\omega)$.

From the above expression of the correlation coefficient of the kth and rth sidebands $C_{k,r}(\omega)$, the power available from the noise sources is redistributed among all the sidebands through frequency conversion, and this complex mechanism of interfrequency power flow is described by the family of the sideband–sideband conversion matrices $T_{k,p}^{J}(\omega)$ and $T_{k,p}^{U}(\omega)$.

The noise power spectral density delivered to the load at $\omega + k\omega_0$ can be given as

$$N_k(\omega) = R\langle|\partial I_k(\omega)|^2\rangle = C_{k,k}(\omega) \tag{10.336}$$

10.16.10 Noise Performance Index Due to Frequency Conversion

The PM noise due to frequency conversion, AM noise-to-carrier ratio due to frequency conversion, and PM–AM correlation coefficient due to frequency conversion can be expressed in terms of a simple algebraic combination of the equations above.

PM noise for the kth harmonic can be expressed as

$$\langle|\delta\varphi_{ck}(\omega)|^2\rangle = \left[\frac{[N_k(\omega) - N_{-k}(\omega)] - 2\,\text{Re}[C_{k,-k}^{\bullet}(\omega)\exp(j2\varphi_k^{\text{ss}})]}{R|I_k^{\text{SS}}|^2}\right] \tag{10.337}$$

where $\langle|\delta\varphi_{ck}(\omega)|^2\rangle$ = PM noise at kth harmonic, subscript c indicates frequency conversion

$N_k(\omega), N_{-k}(\omega)$ = noise power spectral densities upper and lower sidebands of kth harmonics

$C_{k,-k}^{\bullet}(\omega)$ = correlation coefficient of upper and lower sidebands of kth carrier harmonics

$|I_k^{\text{SS}}|\exp(j2\varphi_k^{\text{ss}})$ = kth harmonic of steady-state current through load

R = load resistance

$\langle\bullet\rangle$ = ensemble average

AM noise for the kth harmonic can be given as

$$\langle|\delta A_{ck}(\omega)|^2\rangle = 2\left[\frac{[N_k(\omega) - N_{-k}(\omega)] + 2\,\text{Re}[C_{k,-k}^{\bullet}(\omega)\exp(j2\varphi_k^{\text{ss}})]}{R|I_k^{\text{SS}}|^2}\right] \tag{10.338}$$

where $\langle|\delta A_{ck}(\omega)|^2\rangle$ = AM noise to carrier ratio at kth harmonic, subscript c indicates frequency conversion

$N_k(\omega), N_{-k}(\omega)$ = noise power spectral densities at upper and lower sidebands of kth harmonic

$C_{k,-k}^{\bullet}(\omega)$ = correlation coefficient of upper and lower sidebands of kth carrier harmonic

$|I_k^{\text{SS}}|\exp(j2\varphi_k^{\text{ss}})$ = kth harmonic of steady-state current through load

R = load resistance

$\langle\bullet\rangle$ = ensemble average

For $k = 0$, the expression for $\partial I_k(\omega)$ can be given as

$$\partial I_k(\omega) = \sum_{p=-nH}^{nH} T_{k,p}^J(\omega) J_p(\omega) = \sum_{p=-nH}^{nH} T_{k,p}^U(\omega) U_p(\omega) \tag{10.339}$$

$$\partial I_k(\omega)|_{k=0} = \partial I_0(\omega) \Rightarrow \partial I_0^{\otimes}(\omega) \tag{10.340}$$

$$\partial I_{-k}(\omega)|_{k=0} \Rightarrow \partial I_0(-\omega) \Rightarrow \partial I_0^{\otimes}(\omega) \tag{10.341}$$

$$\varphi_k^{ss}|_{k=0} = 0, \pi \Rightarrow \langle |\delta\Phi_{c0}(\omega)|^2 \rangle = 0 \tag{10.342}$$

Here, $N_k(\omega)|_{k=0} = N_0(\omega)$, which is pure AM noise.

The PM–AM correlation coefficient for the kth harmonic can be given as

$$
\begin{aligned}
C_{ck}^{PMAM}(\omega) &= \langle \delta\Phi_{ck}(\omega)\delta A_k(\omega)^* \rangle \\
&= -\sqrt{2}\left[\frac{2\,\mathrm{Im}[C_{k,-k}^{\bullet}(\omega)\exp(j2\varphi_k^{ss})] + j[N_k(\omega) - N_{-k}(\omega)]}{R|I_k^{SS}|^2}\right]
\end{aligned} \tag{10.343}
$$

where $C_{ck}^{PMAM}(\omega) =$ PM–AM noise correlation coefficient for kth harmonic,
subscript c refers to frequency conversion

$N_k(\omega), N_{-k}(\omega) =$ noise power spectral densities at upper and lower sidebands of kth harmonic

$C_{k,-k}^{\bullet}(\omega) =$ correlation coefficient of upper and lower sidebands of kth carrier harmonic

$|I_k^{SS}|\exp(j2\varphi_k^{ss}) = k$th harmonic of steady-state current through load

$R =$ load resistance

$\langle\bullet\rangle =$ ensemble average

The frequency conversion approach frequently used has the following limitations:

The frequency conversion approach is not sufficient to predict the noise performance of an autonomous circuit. The spectral density of the output noise power, and consequently the PM noise computed by the conversion analysis, is proportional to the available power of the noise sources.

In the presence of both thermal and flicker noise sources, PM noise due to frequency conversion increases as ω^{-1} and approaches a finite limit for $\omega \to \infty$ like kT.

Frequency conversion analysis correctly predicts the far-carrier noise behavior of an oscillator, but the oscillator noise floor does not provide results consistent with the physical observations at low-frequency deviations from the carrier. This inconsistency can be removed by adding the modulation noise analysis.

10.16.11   Modulation Noise Analysis

The equation

$$\left[\frac{\partial E_H}{\partial X_B}\right]_{ss} \partial X_B + \left[\frac{\partial E_H}{\partial X_H}\right]_{ss} \partial X_H = J_H(\omega)$$

describes the noise-induced jitter of the oscillatory state, represented by the vector δX_H, and under this approach, PM noise is the result of direct frequency modulation by the noise sources present in the circuits.

The noise sources under this approach are modeled as modulated sinusoids located at the carrier harmonics with random pseudosinusoidal phase and amplitude modulation causing frequency fluctuations with a mean-square value proportional to the available power of the noise sources. The associated mean-square phase fluctuation is proportional to the available noise power divided by ω^2, and this mechanism is referred as modulation noise.

Since one of the entries of δX_H is $\delta\omega_0$, where $\delta\omega_0(\omega) =$ phasor of pseudosinusoidal components of the fundamental frequency fluctuations in a 1-Hz band at frequency ω. Equation $M_{HH}\partial X_H = J_H(\omega)$ provides a frequency jitter with a mean-square value proportional to the available noise power.

In the presence of both thermal and flicker noise, the PM noise, due to modulation, increases as ω^{-3} for $\omega \to 0$ and tends to go to zero for $\omega \to \infty$. Modulation noise analysis correctly describes the noise behavior of an oscillator at low deviations from the carrier and does not provide results consistent with physical observations at high deviations from the carrier. The combination of both phenomena explains the noise in the oscillator shown in Figure 10.140, where the near-carrier noise dominates below ω_X and far-carrier noise dominates above ω_X.

From a strict harmonic balance viewpoint, the forcing term $J_H(\omega)$ of the uncoupled equation $M_{HH}\partial X_H = J_H(\omega)$ represents a synchronous perturbation with time-independent spectral components at the carrier harmonics only, and it can be expressed in terms of sideband noise sources $J_p(\omega)$ and $U_p(\omega)$, whose correlation matrices are calculated from the following expression:

$$C_{k,r}(\omega) = R\langle \partial I_k(\omega)\partial I_r^*(\omega)\rangle \tag{10.344}$$

$$R\sum_{p,q=-nH}^{nH}\{[T_{k,p}^J(\omega)\langle J_p(\omega)J_q^\otimes(\omega)\rangle T_{r,q}^{J\otimes}(\omega)] \tag{10.345}$$

$$+ [T_{k,p}^U(\omega)\langle U_p(\omega)U_q^\otimes(\omega)\rangle T_{r,q}^{U\otimes}(\omega)] \tag{10.346}$$

$$+ [T_{k,p}^J(\omega)\langle J_p(\omega)U_q^\otimes(\omega)\rangle T_{r,q}^{U\otimes}(\omega)] \tag{10.347}$$
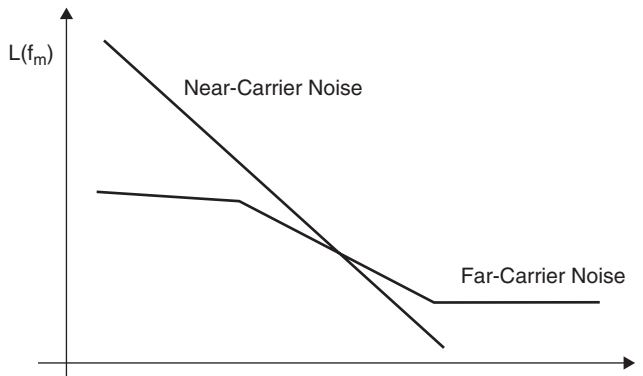
FIGURE 10.140   Oscillator noise components.

$$+ [T_{k,p}^{U}(\omega)\langle U_p(\omega)J_q^{\otimes}(\omega)\rangle T J_{r,q}^{J\otimes}(\omega)]\} \tag{10.348}$$

In a conventional (deterministic) HB analysis, $J_H(\omega)$ would contain real and imaginary parts of the synchronous perturbation phasor at $k\omega_0$. But, in reality, forcing the term $J_H(\omega)$ at the kth harmonic arises due to superposition of the upper and lower sideband noise at $\omega + k\omega_0$, and for noise analysis, the noise source waveforms may be viewed as a sinusoidal signal at frequencies $k\omega_0$ slowly modulated in both amplitude and phase at the rate of ω.

In the equation $M_{HH}\partial X_H = J_H(\omega)$, the phasors of the deterministic perturbations are replaced by the complex modulations laws, each generated by the superposition of an upper and lower sideband contribution.

Under this quasi-stationary viewpoint, the real part of the constant synchronous perturbation is replaced by the phasor of the amplitude modulation law and the imaginary part by the phasor of the phase modulation law.

Thus, the noise forcing term $J_H(\omega)$ can be expressed as

$$J_H(\omega) = \left\{\left[J_0^T(\omega)\cdots[J_k(\omega) + J_{-k}(\omega)]^T \cdots [-jJ_K(\omega) + jJ_{-K}(\omega)]^T \cdots\right]^T\right\}$$

$$(1 \le k \le n_H) \tag{10.349}$$

where T denotes the transpose and the equivalent Norton phasor of the noise source sidebands is given as

$$J_k(\omega) = -[J_{Lk}(\omega) + J_{Nk}(\omega) + Y(\omega + k\omega_0)U_{Nk}(\omega)] \tag{10.350}$$

where $Y(\omega + k\omega_0)$ = linear subnetwork admittance matrix

$J_{Lk}(\omega), J_{Nk}(\omega)$ = forcing terms corresponding to linear and nonlinear sub network

$J_k(\omega), U_k(\omega)$ = phasors of pseudosinusoids representing noise components in 1 Hz bandwidth located in neighborhood of sidebands $\omega + k\omega_0$

In phasor notation with a rotating vector $\exp(j\omega t)$, the forcing term $J_H(\omega)$ can be given as

$$J_H(\omega) = \begin{bmatrix} J_0(\omega) \\ \cdots \\ J_K(\omega) + J_{-K}(\omega) \\ -jJ_K(\omega) + jJ_{-K}(\omega) \\ \cdots \end{bmatrix} \quad (1 \le k \le n_H) \tag{10.351}$$

After replacing the forcing term $J_H(\omega)$ in the earlier given uncoupled equation $M_{HH}\partial X_H = J_H(\omega)$ by $[J_0^T(\omega)\cdots[J_k(\omega) + J_{-k}(\omega)]^T \cdots [-jJ_K(\omega) + jJ_{-K}(\omega)]^T \cdots]^T$, the entries of the perturbation vector ∂X_H become a complex phasor of the pseudosinusoidal fluctuations of the corresponding entries of the state vector δX_H at frequency ω.

The solution of the equation $M_{HH}\partial X_H = J_H(\omega)$ for δX_H and for $\partial\omega_0$ can be given by introducing the row matrix $S = [000\cdots 1\cdots 0]$, where the nonzero element corresponds to the position of the entry $\partial\omega_0$ in the vector δX_H, and we obtain

$$\partial\omega_0(\omega) = S[M_{HH}]^{-1}J_H(\omega) = T_F J_H(\omega) \tag{10.352}$$

where $\partial\omega_0$ (ω) represents the phasor of the pseudosinusoidal component of the fundamental frequency fluctuations in a 1-Hz band at frequency ω and T_F is a row matrix.

Furthermore, a straightforward perturbative analysis of the current of the linear subnetwork allows the perturbation on the current through the load resistor R to be linearly related to the perturbation on the state vector, δX_H is obtained from equation $M_{HH}\,\partial X_H = J_H(\omega)$, and the phasor of the pseudosinusoidal component of the load current fluctuations in a 1-Hz band at a deviation ω from $k\omega_0$ can be given as

$$\partial I_k(\omega) = T_{AK}\,J_H(w) \tag{10.353}$$

where T_{AK} is a row matrix and J_H (w) is a forcing term of the uncoupled equation.

10.16.12   Noise Performance Index Due to Contribution of Modulation Noise

PM noise due to noise modulation, AM noise due to noise modulation, and the PM–AM correlation coefficient due to noise modulation can be expressed in terms of a simple algebraic combination of the equations above.

PM noise for the kth harmonic due to modulation is given as

$$\langle|\partial\Phi_k(\omega)|^2\rangle = \frac{k^2}{\omega^2}[T_F\langle|J_H(\omega)J_H^{\otimes}(\omega)|\rangle T_F^{\otimes}] \tag{10.354}$$

where $\langle|\delta\varphi_{mk}(\omega)|^2\rangle =$ PM noise at kth harmonic, subscript m refers to modulation
mechanism
$\langle|J_H(\omega)J_H^{\otimes}(\omega)|\rangle =$ correlation matrix
$T_F^{\otimes} =$ conjugate transpose
$J_H(w) =$ forcing term
$\langle\bullet\rangle =$ ensemble average

For AM noise due to modulation contribution, the kth harmonic of the steady-state current through the load can be expressed as

$$I_k^{SS} = Y_R(k\omega_0)V_k(X_H) \tag{10.355}$$

where $I_k^{SS} = k$th harmonic of steady-state current through load
$Y_R(k\omega_0) =$ transadmittance matrix
$V_k =$ vector representation of kth harmonics of voltages at nonlinear
subnetwork ports

By perturbing I_k^{SS} in the neighborhood of the steady state, the phasor of the pseudosinusoidal component of the kth-harmonic current fluctuations at frequency ω can be expressed as a linear combination of the elements of the perturbation vector δX_H. From the equations

$$\left[\frac{\partial E_H}{\partial X_H}\right]_{ss}\partial X_H = J_H(\omega) \Rightarrow M_{HH}\,\partial X_H = J_H(\omega) \qquad \partial I_k(\omega) = T_{AK}\,J_H(w)$$

the modulation contribution for the kth-harmonic AM noise-to-carrier ratio at frequency ω can be expressed as

$$\langle \partial |A_{mk}(\omega)|^2 \rangle = \frac{2}{|I_k^{SS}|^2} [T_{Ak} \langle |J_H(\omega) J_H^{\otimes}(\omega)| \rangle T_{Ak}^{\otimes}] \tag{10.356}$$

where $\langle |\delta A_{mk}(\omega)|^2 \rangle$ = AM noise to carrier ratio at kth harmonic, subscript m refers to modulation mechanism

$\langle |J_H(\omega) J_H^{\otimes}(\omega)| \rangle$ = correlation matrix

$J_H(w)$ = forcing term

T_{Ak} = row matrix

$T_{Ak}^{\otimes}$ = conjugate transpose

10.16.13 PM–AM Correlation Coefficient

From the equation

$$\left[\frac{\partial E_H}{\partial X_H} \right]_{ss} \partial X_H = J_H(\omega) \Rightarrow M_{HH} \partial X_H = J_H(\omega)$$

the information of the RF phase is lost and it is not possible to calculate the phase of the PM–AM correlation coefficient from the expressions above. To calculate the PM–AM correlation, the first-order approximation of the normalized kth-harmonic PM–AM normalized correlation coefficient $C_{ck}(\omega)$ computed from frequency conversion analysis is given as

$$C_{ck}(\omega) = \left[\frac{C_{ck}^{PM-AM}(\omega)}{\sqrt{\langle |\delta \Phi_{ck}(\omega)|^2 \rangle \langle |\delta A_{ck}(\omega)|^2 \rangle}} \right] \tag{10.357}$$

and can be correctly evaluated from frequency conversion analysis even for $\omega \to 0$, where $C_{ck}(\omega)$ is the normalized PM–AM correlation coefficient, which compensates for the incorrect dependency of $\langle |\delta \Phi_{ck}(\omega)|^2 \rangle$ of the frequency at low-frequency offsets from the carrier. From the PM–AM correlation coefficient above due to modulation contribution, the kth harmonic can be given as

$$C_{mk}^{PM-AM}(\omega) = C_{ck}(\omega) \left[\sqrt{\langle |\delta \Phi_{mk}(\omega)|^2 \rangle \langle |\delta A_{mk}(\omega)|^2 \rangle} \right] \tag{10.358}$$

$$C_{mk}^{PM-AM}(\omega) \cong \langle \delta \Phi_k(\omega) \delta A_k(\omega)^* \rangle = \frac{k\sqrt{2}}{j\omega |I_k^{SS}|} [T_F \langle J_H(\omega) J_H^{\otimes}(\omega) \rangle T_{Ak}^{\otimes}] \tag{10.359}$$

Now, the near-carrier noise power spectral density $N_k(\omega)$ of the oscillator due to modulation contribution at an offset ω from $k\omega_0$ ($-n_H \leq k \leq n_H$) can be given as

$$N_k(\omega) = \frac{1}{4} R \left[\frac{k^2}{\omega^2} \left| I_k^{SS} \right|^2 T_F \left\langle J_H(\omega) J_H^{\otimes}(\omega) \right\rangle T_F^{\otimes} \right] \tag{10.360}$$

$$+ \frac{1}{4} R [T_{AK} [J_H(\omega) J_H^{\otimes}(\omega)] T_{Ak}^{\otimes}] \tag{10.361}$$

$$+ \frac{kR}{2\,\omega} \left| I_k^{SS} \right| \mathrm{Re} [T_F \left\langle J_H(\omega) J_H^{\otimes}(\omega) \right\rangle T_{Ak}^{\otimes}] \tag{10.362}$$

$$\Rightarrow N_k(\omega) = \frac{1}{4} R \left| I_k^{\text{SS}} \right|^2 \left[\left\langle |\delta \Phi_{mk}(\omega)|^2 \right\rangle + \frac{1}{2} \left\langle |\delta A_{mk}(\omega)|^2 \right\rangle - \frac{k}{|k|} \sqrt{2} \, \text{Im}[C_{mk}^{\text{PMAM}}(\omega)] \right] \tag{10.363}$$

where $J_H(\omega)$ = vector of Norton equivalent of noise sources

$\quad T_F$ = frequency transfer matrix

$\quad R$ = load resistance

$\quad I_k^{\text{ss}}$ = kth harmonic of steady-state current through load

10.17   VALIDATION CIRCUITS

The mathematical background for optimizing microwave oscillators has been shown. The next step is to validate the synthesis of the circuits. The following circuits have been chosen for validation:

A: 1000-MHz bipolar transistor-based oscillator with ceramic resonator

B: 4100-MHz bipolar transistor-based oscillator with transmission line resonators

C: 2000-MHz GaAs FET-based oscillator with transmission line resonators

10.17.1   1000-MHz Ceramic Resonator Oscillator (CRO)

Many applications require a very low noise microwave oscillator in the 1000-MHz region, and this is best accomplished with a ceramic resonator. An operating Q in the vicinity of 500 is available in this material. An oscillator using an NEC transistor-type NE68830 has been selected because of its superior flicker noise contribution. The Colpitts oscillator uses an 8.2-Ω resistor between the emitter and the capacitive feedback. Rather than take the RF signal at the collector, it is taken from a tap of the emitter inductor. The collector circuit, using *pnp* transistors, has been designed to set the dc current.

Class A common-emitter amplifiers are usually very sensitive to stray impedance in the emitter circuit. Any small inductance in series with the emitter will cause instability; for this reason the emitter needs to be grounded as directly as possible, and bias components in the emitter are generally undesirable. In the schematic in Figure 10.141, Q_1 is the RF amplifier and Q_2 provides the base current required for a constant-voltage difference across R_c. This constant-voltage difference then ensures constant collector current.

Diode D_1 provides some measure of temperature compensation, and R_b should be high in order not to affect base impedance but not high enough to cause Q_2 to saturate over temperature and β_1 variations. Neglecting the base current of Q_2, the design equations are [10.67]

$$I_c = \frac{R_1(A^+ - V_d)}{R_c(R_1 + R_2)} \tag{10.364}$$

$$V_c = A^+ - I_c R_c \tag{10.365}$$
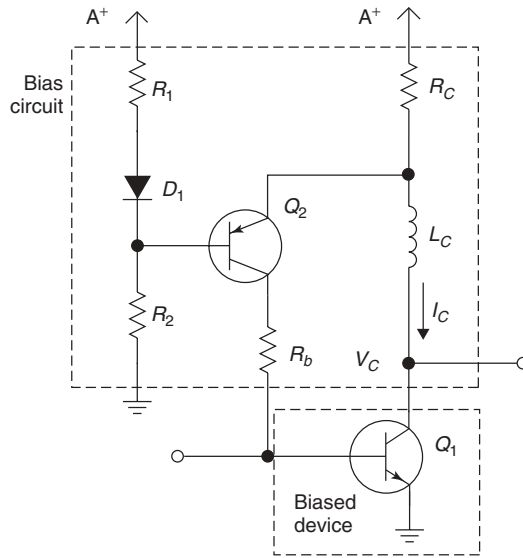
FIGURE 10.141   Active bias network for a common-emitter RF amplifier stage.

Assuming that we are designing the bias circuit to provide a certain device bias current I_c and collector voltage V_c, select a convenient $A^+ > V_c$. The component values are then supplied by the following equations:

$$R_c = \frac{A^+ - V_c}{I_c} \tag{10.366}$$

$$R_1 = \frac{A^+ - V_c}{I_d} \tag{10.367}$$

$$R_2 = \frac{V_c - V_d}{I_d} \tag{10.368}$$

$$R_b < \beta_{\min} \frac{V_c - V_d - 0.2}{I_c} \tag{10.369}$$

where I_c = desired collector current of Q_1 (A)

$\quad V_c$ = desired collector voltage of Q_1 (V)

$\quad V_d$ = diode, or base–emitter voltage drop, nominally 0.7 (V)

$\quad A^+$ = chosen supply voltage (V)

$\quad R_i$ = resistor values as shown in Figure 10.141

$\quad I_d$ = bias current through $R_1, R_2,$ and D_1 (A)

$\quad \beta_{\min}$ = minimum beta of Q_1

The bias circuit shown has to be carefully bypassed at both high and low frequencies. There is one inversion from base to collector of Q_1, and another inversion may be introduced by L_c matching components and stray capacitances, resulting in positive feedback around the loop at low frequencies. Low ESR electrolytic or tantalum capacitor from the collector of Q_2 to ground is usually adequate to ensure stability.

The ceramic resonator is coupled loosely to the transistor with a capacitor of 0.9 pF. The resonator has a parallel capacitor of 0.6 pF, which reduces the manufacturing tolerances of the resonator. The tuning diode assembly, two diodes in parallel, is coupled to the resonator with 0.8 pF. The reason for using two diodes was that there was not one single diode available with the necessary capacitance and Q. Figure 10.142 shows the schematic of the oscillator.

It has been pointed out that the best operating condition for this will be the case where the most negative resistance occurs at the point of resonance to achieve best phase noise. This is shown in Figure 10.143. The Im curve starting below zero shows the imaginary current, which resonates at 1000 MHz, while the green-Re curve shows the negative resistance. Its maximum negative peak occurs at exactly 1000 MHz, as it should be.

Figure 10.144 shows the measured phase noise of this oscillator. The measurements were done with the Aeroflex Euro Test system. At 1 kHz the phase noise is approximately 95 dBc/Hz and at 10 kHz it is approximately 124 dBc/Hz. This is a 30-dB/decade slope, which is triggered by the flicker corner frequency of the transistor. From 10 to 100 kHz, the slope is 20 dB/decade with a phase noise of -145.2 dBc/Hz at 100 kHz. At 1 MHz off the carrier, it is -160 dBc/Hz.

Because of the narrow tuning range and the loose coupling of the tuning diode, the noise contribution of the diode is negligible.

This circuit has been designed using the synthesis procedure and also has been analyzed with the harmonic balance simulator Microwave Harmonica from Ansoft. Figure 10.145 shows the predicted performance of the phase noise.

The circuit layout arrangement is shown in Figure 10.146. The ceramic resonator can be found easily.

10.17.2   4100-MHz Oscillator with Transmission Line Resonators

For less demanding applications, it is possible to design oscillators using transmission line resonators. Its Q depends on the material and implementation of the resonator. Figure 10.147 shows the circuit of the oscillator. While the previous example was a
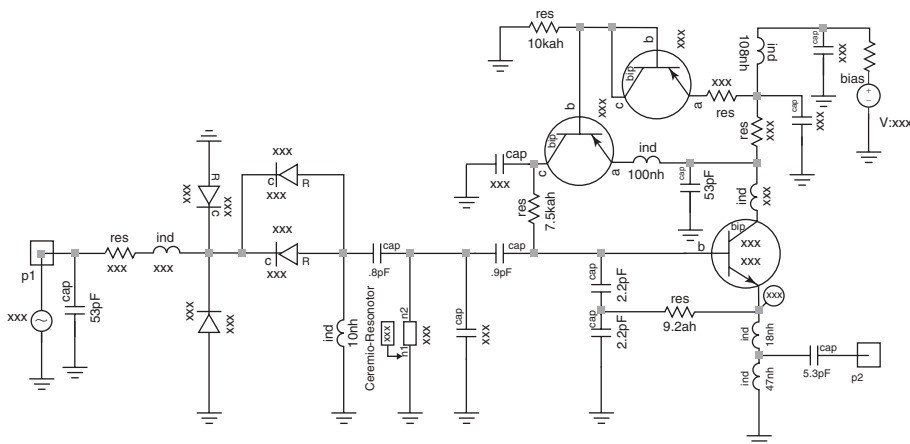
FIGURE 10.142   A 1000-MHz ceramic resonator oscillator.
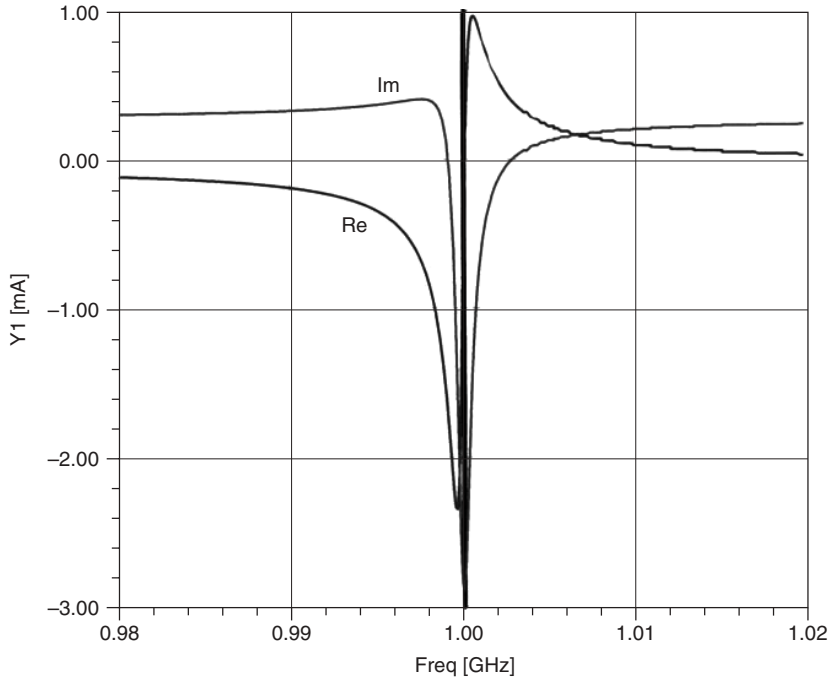
FIGURE 10.143   Plot of real and imaginary oscillator currents as a function of frequency.
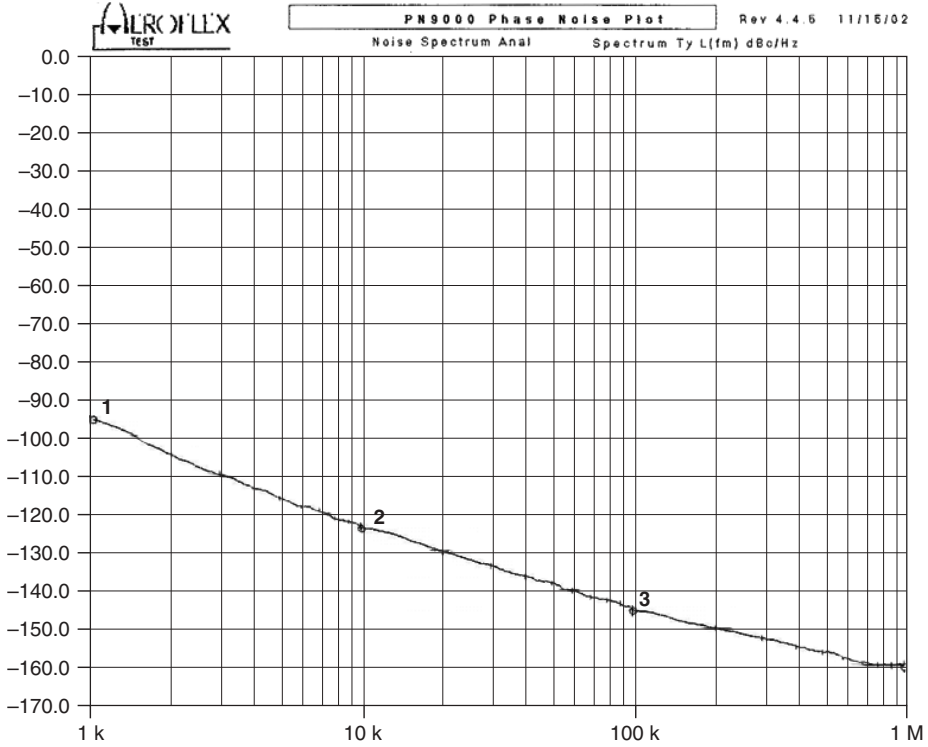
FIGURE 10.144   Measured phase noise of the 1000-MHz ceramic resonator oscillator.

X1 = 1.00EHz   X2 = 1.00E06Hz
Y1 = −96.30dBc/Hz   Y2 = −160.67dBc/Hz
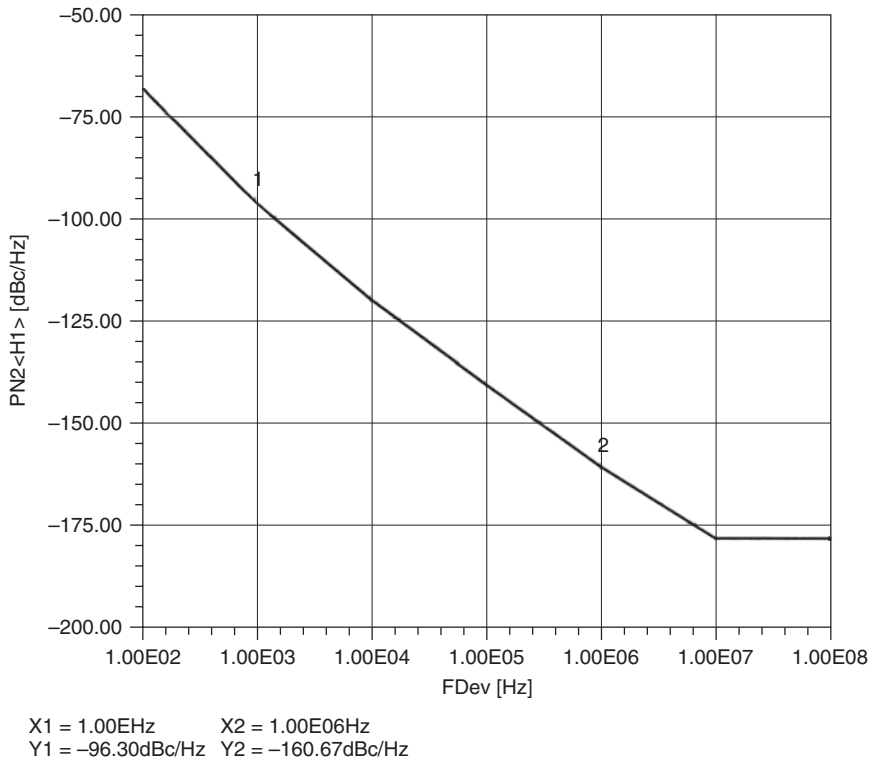
FIGURE 10.145   Predicted phase noise of the CRO at 1 GHz shown in Figure 10.142.
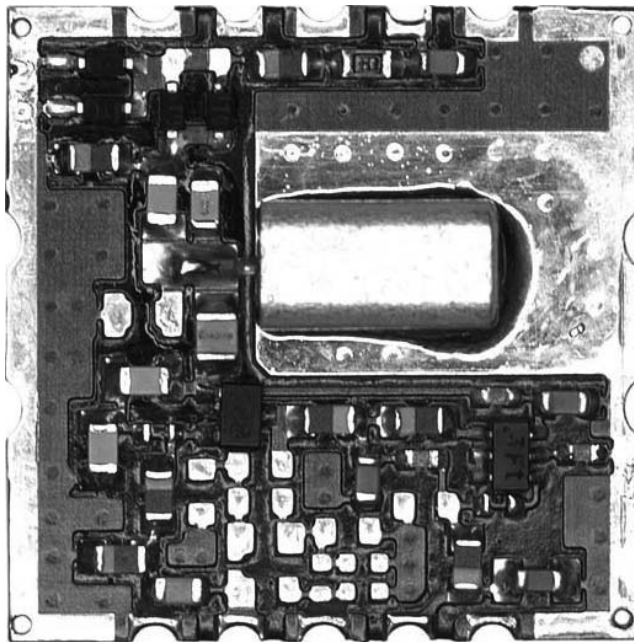
FIGURE 10.146   Photograph of the 1-GHz CRO of the schematic shown in Figure 10.142.
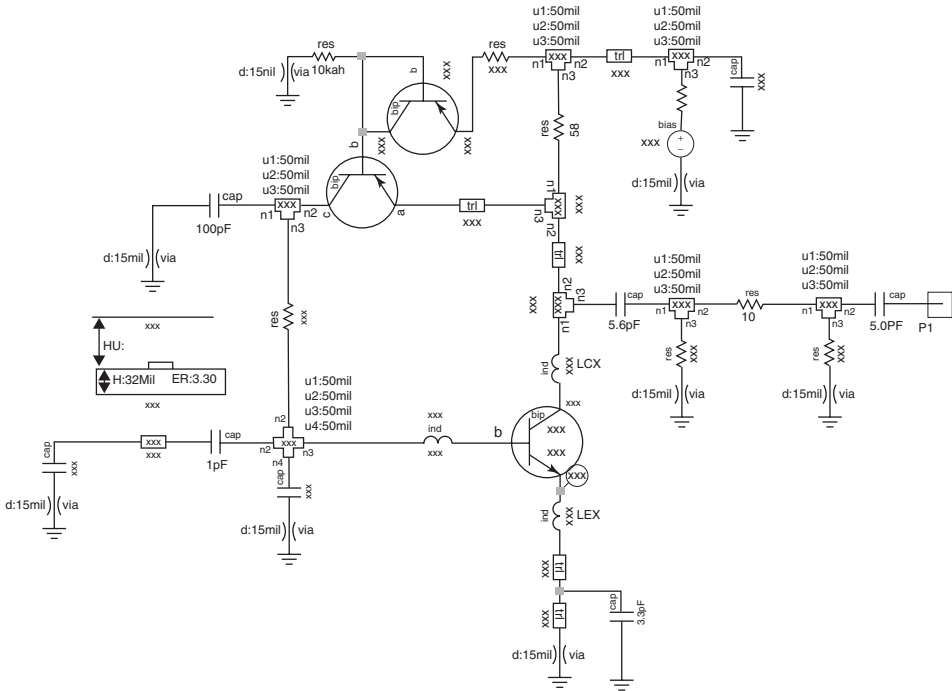
FIGURE 10.147   Circuit diagram of the 4.1-GHz oscillator.

Colpitts, parallel resonant circuit, this circuit operates in the series resonant mode. The *npn* transistor NE68830 has an inductor in the emitter, base, and collector lines. For the purpose of accurate modeling, tee and cross junctions were used as well as transmission lines where applicable. The dc stabilization circuit uses the same technique as shown in Figure 10.141. This time the RF power is taken from the collector and uses a 10-dB attenuator to minimize frequency pulling. The ground connections for the capacitors are done via holes. A via hole is the electrical equivalent of a small inductor. The phase noise of this oscillator was simulated using the values of the synthesis program. Figure 10.148 shows the predicted phase noise of the oscillator shown in Figure 10.147.

The output power of this oscillator is 6.8 dBm. This oscillator was built and measured. Figure 10.149 shows the printed circuit board of the oscillator.

Because of the padlike microstrip, the simulation needs to be done very carefully, and the soldering of the component is also very critical. This frequency range makes the assembly very difficult because it is not high enough for an RFIC and still needs to be done on a printed circuit board. The measured phase noise is shown in Figure 10.150. It agrees well with the predicted phase noise. At 100 kHz the difference is about 3 dB. The same is valid at 10 kHz. At 1 kHz there is a larger difference. The flicker corner frequency of the actual device is different than the simulation.

10.17.3   2000-MHz GaAs FET-Based Oscillator

Low-cost applications are frequently implemented as an RFIC. For further validation, a GaAs FET-based 2000-MHz Colpitts oscillator was designed and built. Figure 10.151

X1 = 1.00E05Hz
Y1 = −116.17dBc/Hz
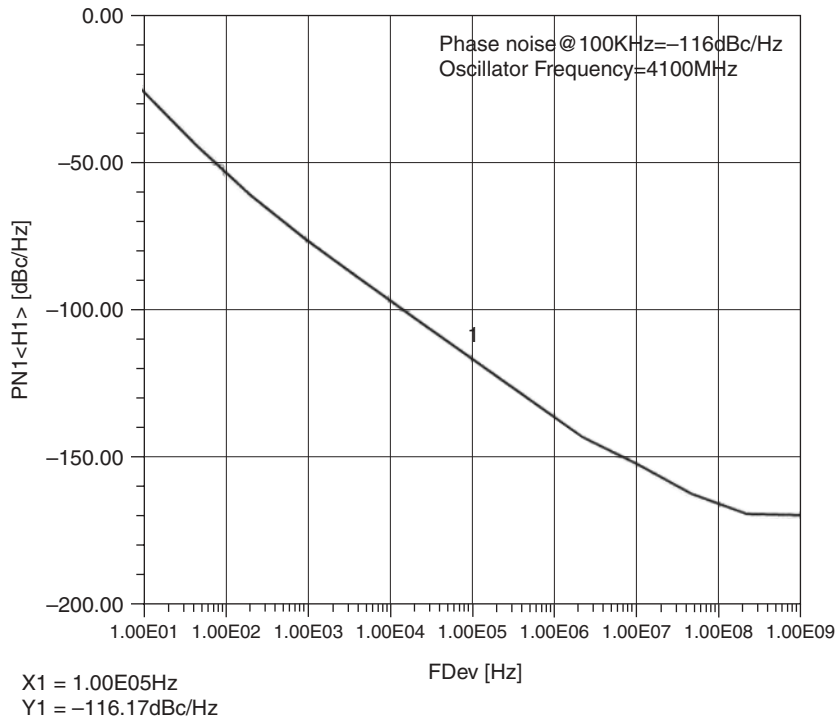
FIGURE 10.148   Predicted phase noise of the 4.1-GHz oscillator.
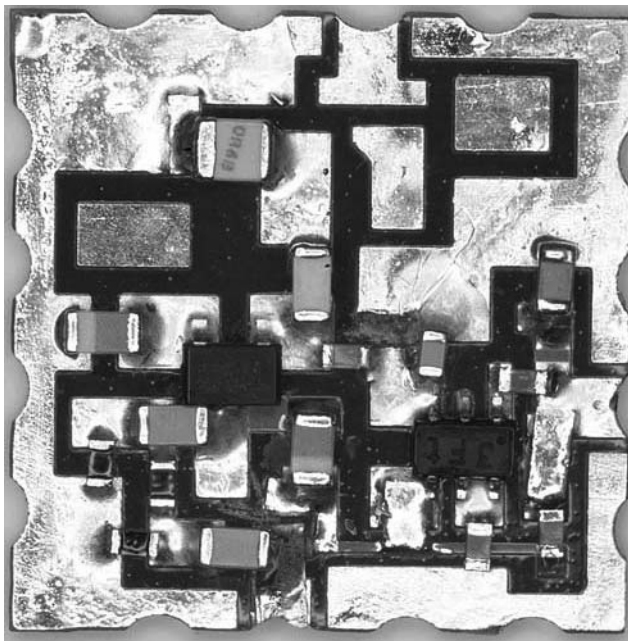
FIGURE 10.149   Printed circuit board of the 4.1-GHz oscillator shown in Figure 10.147.
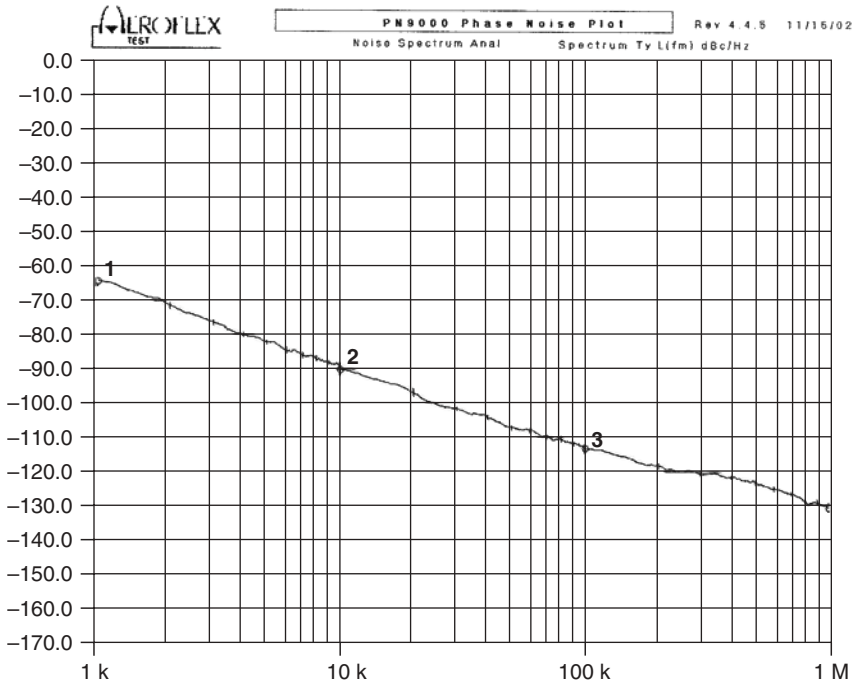
FIGURE 10.150   Measured phase noise of the 4.1-GHz oscillator.
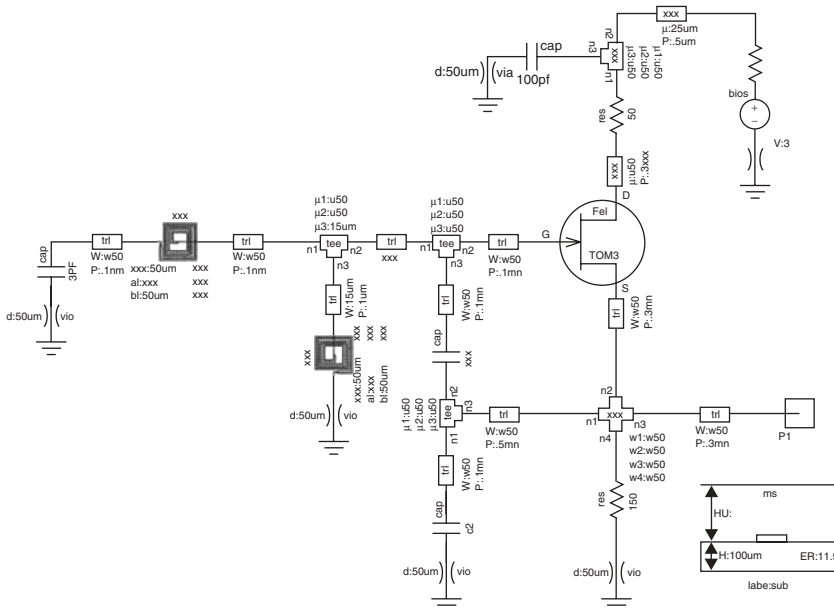
FIGURE 10.151   Circuit diagram of the 2-GHz GaAs FET oscillator.

shows the circuit diagram of the oscillator. As mentioned, it is a Colpitts oscillator using a combination of transmission lines and rectangular inductors as resonators. The inductor in the middle of the schematic in Figure 10.151, connected to a via hole, is need as a dc return.

If a tuning diode is connected to the capacitor on the left of the schematic in Figure 10.151, then a dc control voltage can be applied, and the center inductor becomes an RF choke. The output is taken again from the source. Because of the dc coupling, an additional external dc decoupling capacitor will be needed. The transistor and the circuit were constructed using the TriQuint GaAs Foundry and the transistor was optimized for dc. Figure 10.152 shows the predicted phase noise of this oscillator.

It is interesting to see the load line of this oscillator, which is shown in Figure 10.153. This circuit is operated in a fairly linear range.

Figure 10.154 shows the layout of the 2-GHz GaAs FET oscillator. Its output power is 1.8 dBm.

10.18   ANALYTICAL APPROACH FOR DESIGNING EFFICIENT MICROWAVE FET AND BIPOLAR OSCILLATORS (OPTIMUM POWER)

For large-signal operation, it is necessary to obtain the exact nonlinear device parameters of the active two-port network and calculate the external feedback elements of

X1 = 1.00E05Hz   X2 = 1.00E06Hz   X3 = 1.00E07Hz
Y1 = −98.04dBc/Hz Y2 = −122.22dBc/Hz Y3 = −142.68dBc/Hz
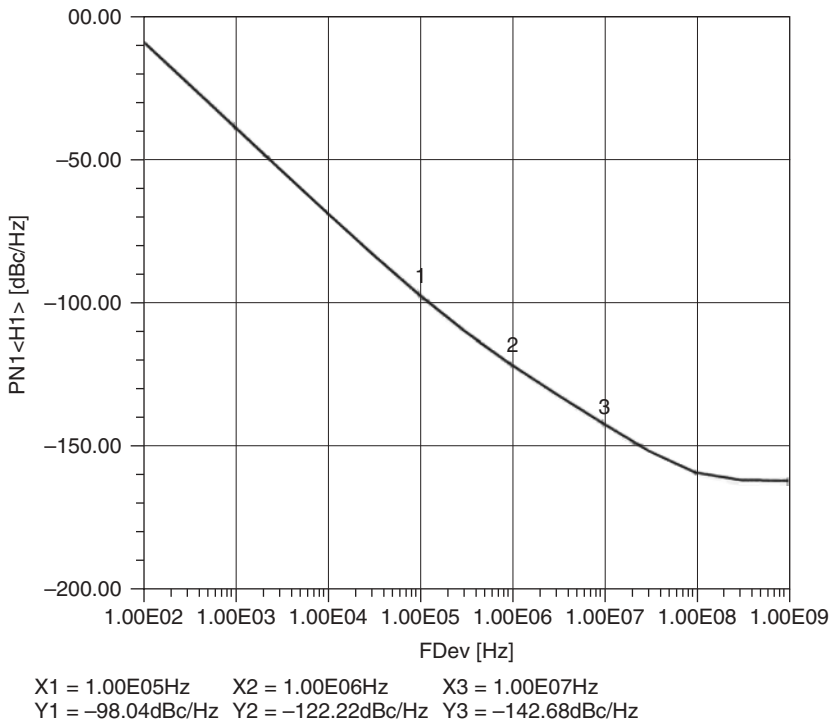
FIGURE 10.152   Predicted phase noise of the oscillator shown in Figure 10.151. The measured values were 100 dBc/Hz at 100 kHz and 120 dBc/Hz at 1 MHz. There is a deviation of about 2 dB compared to simulation.
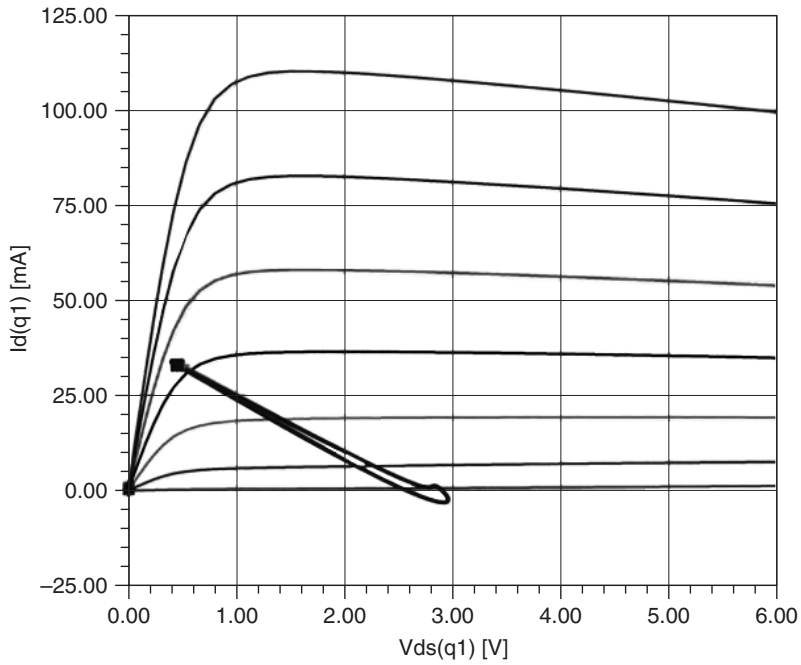
FIGURE 10.153   The dc $I-V$ and the load line for the GaAs FET oscillator.
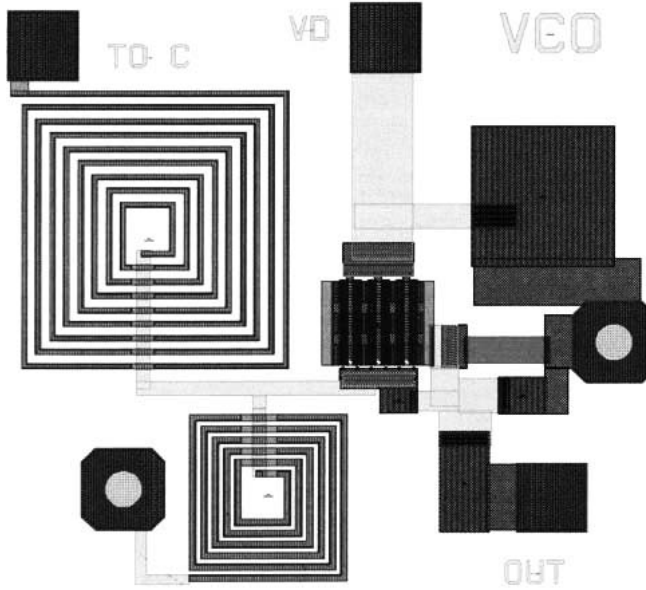
FIGURE 10.154   Layout of the 2-GHz GaAs FET oscillator.

the oscillator circuits. Initially, the feedback element values are unknown. There is no good or efficient experimental solution for this task, only a small-signal approach, which does not handle power and noise.

10.18.1   Series Feedback (MESFET)

The best way to calculate series or parallel feedback oscillators with external elements is to use an analytical approach to designing a microwave oscillator that determines the explicit expression for the optimum feedback elements and the load impedance in terms of the transistor equivalent circuit parameters. These equations also provide better understanding of the fundamental limitation in obtaining high output power for a given topology of the microwave oscillator.

Furthermore, maximizing the oscillator output power and the oscillator efficiency is of interest in many ongoing applications such as active phase-array antennas.

Figure 10.155 shows the series feedback topology of the oscillator using a MESFET. External feedback elements Z_1, Z_2, and Z_3 are shown outside the dashed line [10.69].

The optimum values of the feedback elements Z_1, Z_2, and Z_3 are given as

$$Z_1^{\text{opt}} = R_1^* + jX_1^* \tag{10.370}$$

$$Z_2^{\text{opt}} = R_2^* + jX_2^* \tag{10.371}$$

$$Z_3^{\text{opt}} = Z_L^{\text{opt}} = R_3^* + jX_3^* \tag{10.372}$$

$$Z_{\text{out}}^{\text{opt}} + Z_L^{\text{opt}} \Rightarrow 0 \tag{10.373}$$

$$Z_{\text{out}}^{\text{opt}} = R_{\text{out}}^* + jX_{\text{out}}^* \tag{10.374}$$

The general approach for designing an oscillator corresponding to the maximum output power at a given frequency is based on the optimum values of the feedback element and the load under steady-state large-signal operation. The steady-state oscillation condition
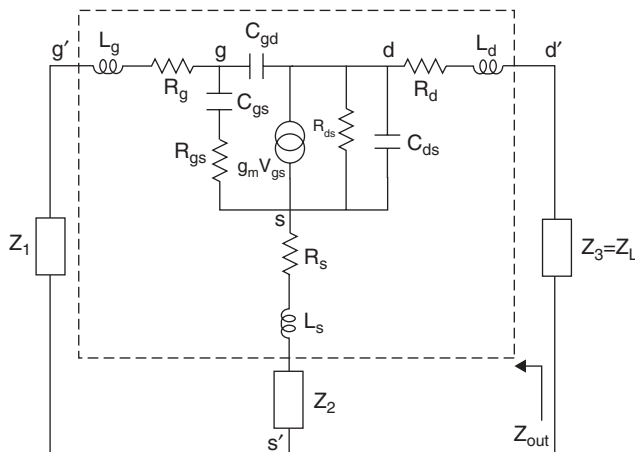
FIGURE 10.155   Series feedback topology.

for a series feedback configuration can be expressed as

$$[Z_{\text{out}}(I_0, w) + Z_L(w)]_{w=w_0} = 0 \tag{10.375}$$

where I_0 is the amplitude of the load current and w_0 is the oscillator frequency. Assuming that the steady-state current entering the active circuit is near the sinusoidal, medium- to high-Q case, the output impedance $Z_{\text{out}}(I_0, w_0)$ and the load impedance $Z_L(w_0)$ can be expressed in terms of real and imaginary part as

$$Z_{\text{out}}(I_0, w_0) = R_{\text{out}}(I_0, w_0) + jX_{\text{out}}(I_0, w_0) \tag{10.376}$$

$$Z_L(w) = R_L(w) + jX_L(w) \tag{10.377}$$

where $Z_{\text{out}}(I_0, w_0)$ is the current amplitude and the frequency-dependent function and $Z_L(w)$ is a function of the frequency. The common-source $[Z]$ parameter of the MESFET is given as

$$[Z]_{cs} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}_{cs} \tag{10.378}$$

with

$$Z_{11} = R_{11} + jX_{11} \tag{10.379}$$

$$R_{11} = R_{gs}\left[\frac{a}{a^2+b^2} + \frac{bwR_{ds}C_{ds}(1+C_{gd}/C_{ds})}{a^2+b^2}\right]$$
$$+ \left[\frac{awR_{ds}C_{ds}(1+C_{gd}/C_{ds})}{wC_{gs}(a^2+b^2)} - \frac{b}{wC_{gs}(a^2+b^2)}\right] \tag{10.380}$$

$$X_{11} = R_{gs}\left[\frac{awR_{ds}C_{ds}(1+C_{gd}/C_{ds})}{a^2+b^2} - \frac{b}{a^2+b^2}\right]$$
$$- \left[\frac{a}{wC_{gs}(a^2+b^2)} + \frac{bwR_{ds}C_{ds}(1+C_{gd}/C_{ds})}{wC_{gs}(a^2+b^2)}\right] \tag{10.381}$$

$$Z_{12} = R_{12} + jX_{12} \tag{10.382}$$

$$R_{12} = \frac{aR_{ds}C_{gd}}{C_{gs}(a^2+b^2)} + \frac{bwR_{ds}C_{gd}R_{gs}}{a^2+b^2} \tag{10.383}$$

$$X_{12} = \frac{awR_{ds}C_{gd}R_{gs}}{a^2+b^2} - \frac{bR_{ds}C_{gd}}{C_{gs}(a^2+b^2)} \tag{10.384}$$

$$Z_{21} = R_{21} + jX_{21} \tag{10.385}$$

$$R_{21} = R_{ds}\left[\frac{C_{gd}}{C_{gs}}\frac{a}{a^2+b^2} + \frac{bwR_{gs}C_{gd}}{a^2+b^2} + \frac{g_m(b\cos w\tau + a\sin w\tau)}{wC_{gs}(a^2+b^2)}\right] \tag{10.386}$$

$$X_{21} = R_{ds}\left[\frac{awR_{gs}C_{gd}}{a^2+b^2} - \frac{C_{gd}}{C_{gs}}\frac{b}{a^2+b^2} + \frac{g_m(a\cos w\tau - b\sin w\tau)}{wC_{gs}(a^2+b^2)}\right] \tag{10.387}$$

$$Z_{22} = R_{22} + jX_{22} \tag{10.388}$$

$$R_{22} = R_{ds}\left(\frac{a}{a^2+b^2} + \frac{C_{gd}}{C_{gs}}\frac{a}{a^2+b^2} + \frac{b}{a^2+b^2}wR_{gs}C_{gd}\right) \tag{10.389}$$

$$X_{22} = R_{ds} \left(\frac{aw R_{gs} C_{gd}}{a^2 + b^2} - \frac{C_{gd}}{C_{gs}} \frac{b}{a^2 + b^2} - \frac{b}{a^2 + b^2} \right) \qquad (10.390)$$

where

$$a = 1 + \frac{C_{gd}}{C_{gs}}(1 - w^2 R_{gs} C_{gs} R_{ds} C_{ds}) + \frac{g_m R_{ds} C_{gd}}{C_{gs}} \cos(w\tau) \qquad (10.391)$$

$$b = w(R_{ds} C_{ds} + R_{ds} C_{gd}) + w \frac{C_{gd}}{C_{gs}}(R_{gs} C_{gs} + R_{ds} C_{ds}) - \frac{g_m R_{ds} C_{gd}}{C_{gs}} \sin(w\tau) \qquad (10.392)$$

The expression of the output impedance Z_{out} can be written as

$$Z_{out} = \left[(Z_{22} + Z_2) - \frac{(Z_{12} + Z_2)(Z_{21} + Z_2)}{(Z_{11} + Z_1 + Z_2)} \right] \qquad (10.393)$$

$$Z_{out} + Z_3 \Rightarrow Z_{out} + Z_L = 0 \qquad (10.394)$$

where Z_{ij} $(i, j = 1, 2)$ are the Z parameters of the transistor model and can be expressed as

$$\lfloor Z_{i,j} \rfloor_{i,j=1,2} = [R_{ij} + jX_{ij}]_{i,j=1,2} \qquad (10.395)$$

According to the criterion for the maximum output power at a given oscillator frequency, the negative real part of the output impedance Z_{out} has to be maximized, and the optimal values of the feedback reactance under which the negative value of R_{out} is maximized is given by the following conditions:

$$\frac{\partial \text{Re}}{\partial X_1}[Z_{out}(I, w)] = 0 \Rightarrow \frac{\partial}{\partial X_1}[R_{out}] = 0 \qquad (10.396)$$

$$\frac{\partial \text{Re}}{\partial X_2}[Z_{out}(I, w)] = 0 \Rightarrow \frac{\partial}{\partial X_2}[R_{out}] = 0 \qquad (10.397)$$

The values of X_1 and X_2 which will satisfy the differential equations above are given as X_1^* and X_2^* and can be expressed in terms of a two-port parameter of the active device (MESFET) as

$$X_1^* = -X_{11} + \frac{X_{12} + X_{21}}{2} + \left(\frac{R_{21} - R_{12}}{X_{21} - X_{12}} \right) \left(\frac{R_{12} + R_{21}}{2} - R_{11} - R_1 \right) \quad (10.398)$$

$$X = \frac{1 - w\tau_g \tan w\tau}{w C_{gs}(a - b \tan w\tau)} - \frac{(b + a \tan w\tau)(R_1 + R_g)}{a - b \tan w\tau}$$

$$- \left[\frac{R_{ds} C_{ds}(w\tau_g + \tan w\tau)}{C_{gs}(a - b \tan w\tau)} - \frac{g_m R_{ds}}{2w C_{gs} \cos w\tau (a - b \tan w\tau)} \right] \qquad (10.399)$$

where τ is the transit time in the MESFET channel and $\tau_g = R_{gs}$, $\tau_d = R_{ds}$:

$$X_2^* = -\frac{X_{12} + X_{21}}{2} - \frac{(R_{21} - R_{12})(2R_2 + R_{12} + R_{21})}{2(X_{21} - X_{12})} \qquad (10.400)$$

$$X = \frac{R_{ds} C_{gd}(w\tau_g + \tan w\tau)}{C_{gs}(a - b \tan w\tau)} - \frac{(b + a \tan w\tau)(R_2 + R_s)}{a - b \tan w\tau}$$

$$- \frac{g_m R_{ds}}{(a - b \tan w\tau)2wC_{gs} \cos w\tau} \tag{10.401}$$

where $\lfloor R_{i,j} \rfloor_{i,j=1,2}$ and $= [X_{ij}]_{i,j=1,2}$ are the real and imaginary parts of the $[Z_{i,j}]_{i,j=1,2}$ of the transistor.

The output impedance can be given as $Z_{\text{out}}(I, w) = R_{\text{out}}(I, w) + X_{\text{out}}(I, w)$ and the corresponding optimum output impedance for the given oscillator frequency can be derived analytically by substituting values of the optimum values of susceptance under which a negative value of R_{out} is maximized:

$$[Z_{\text{out}}^*(I, w)]_{w-w_0} = [R_{\text{out}}^*(I, w) + X_{\text{out}}^*(I, w)]_{w=w_0} \tag{10.402}$$

$$[R_{\text{out}}^*(I, w_0)]_{X_1^*, X_2^*} = R_2 + R_{22} - \frac{(2R_2 + R_{21} + R_{12})^2 + (X_{21} - X_{12})^2}{4(R_{11} + R_2 + R_1)} \tag{10.403}$$

$$X_{\text{out}}^*(I, w) = \frac{X_{22} - X_{12} - X_{21}}{2} - \frac{(R_{21} - R_{12})(2R_2 + R_{12} + R_{21})}{2(X_{21} - X_{12})}$$

$$- \frac{(R_{21} - R_{12})(R_{\text{out}}^* - R_2 - R_{22})}{X_{21} - X_{12}} \tag{10.404}$$

$$[X_{\text{out}}^*(I, w)]_{X_1^*, X_2^*} = X_2^* + X_{22} - \left(\frac{R_{21} - R_{12}}{X_{21} - X_{12}}\right)(R_{\text{out}}^* - R_2 - R_{22}) \tag{10.405}$$

$$X_{\text{out}}^* = \frac{R_{ds}}{a - b \tan w\tau}\left(\tan w\tau - \frac{g_m}{2wC_{gs} \cos w\tau}\right) - \frac{(b + a \tan w\tau)R_{\text{out}}^*}{a - b \tan w\tau} \tag{10.406}$$

where X_1^* and X_2^* are the optimal values of the external feedback susceptance.

For easier analysis, the effects of the transit time and the gate–drain capacitance are neglected for preliminary calculation of an optimum value of the feedback element and the simplified expressions are given as

$$X_1^* = \frac{1}{wC_{gs}} + R_{ds}\left[-wC_{ds}(R_1 + R_g + R_{gs}) + \frac{g_m}{2wC_{gs}}\right] \tag{10.407}$$

$$X_2^* = -R_{ds}\left[wC_{ds}(R_2 + R_s) + \frac{g_m}{2wC_{gs}}\right] \tag{10.408}$$

$$X_{\text{out}}^* = -R_{ds}\left(wC_{ds} R_{\text{out}}^* + \frac{g_m}{2wC_{gs}}\right) \tag{10.409}$$

$$R_{\text{out}}^* = (R_2 + R_s) + \frac{R_{ds}}{1 + (wC_{ds} R_{ds})^2}\left[1 - \frac{R_{ds}}{R_g + R_s + R_1 + R_2 + R_{gs}}\left(\frac{g_m}{2wC_{gs}}\right)^2\right] \tag{10.410}$$

The simplified expressions above show accuracy with the harmonic balance–based simulated results for a gate length less than 1 μm at an operating frequency range up to 20 GHz.

The differential drain resistance R_{ds} can be expressed in terms of the optimum output resistance as

$$R_{ds} = \frac{1 + \sqrt{1 - 4(R_{\text{out}}^* - R_2 - R_s)G_{ds0}}}{2G_{ds0}} \tag{10.411}$$

where

$$G_{ds0} = \frac{1}{R_g + R_s + R_2 + R_{gs}} \left(\frac{g_m}{2wC_{gs}}\right)^2 + (R_{\text{out}}^* - R_2 - R_s)(wC_{ds})^2 \tag{10.412}$$

Alternatively, a differential drain resistance can be obtained from a quasi-linear analysis. Under large-signal operation, the transistor parameters vary with the drive level. If we restrict our interest to the fundamental signal frequency component, then V_{gs} and V_{ds} can be expressed as

$$V_{gs}(t) = V_{gs0} + V_{gs} \sin(wt + \varphi) \tag{10.413}$$

$$V_{ds}(t) = V_{ds0} + V_{ds} \sin(wt) \tag{10.414}$$

where V_{gs0} and V_{ds0} are the dc operating bias voltages, V_{gs} and V_{ds} are the amplitudes of the signal frequency components, and φ is the phase difference between the gate and drain voltages.

The drain current I_d can be expressed as

$$I_{ds} = I_{ds}(V_{gs}, V_{ds0}) \tag{10.415}$$

Under the assumption of linear superposition of the dc and RF currents, an instantaneous drain current can be expressed as

$$I_{ds}(t) = I_{ds0} + g_m v_{gs} \cos(wt + \varphi) + G_d v_{ds} \cos(wt) \tag{10.416}$$

where I_{ds0} is the dc bias drain current.

The transconductance g_m and the drain conductance are defined as

$$g_m = \left[\frac{I_{ds}}{V_{gs}}\right]_{V_{ds}=0} \tag{10.417}$$

$$G_D = \left[\frac{I_{ds}}{V_{gs}}\right]_{V_{gs}=0} \tag{10.418}$$

Under large-signal conditions, the transconductance and the drain conductance are given as

$$g_m = \frac{w}{\pi V_{gs} \sin\varphi} \int_0^{2\pi/w} I_{ds} \sin(wt)\, dt \tag{10.419}$$

$$G_d = \frac{w}{\pi V_{ds} \sin\varphi} \int_0^{2\pi/w} I_{ds} \sin(wt + \varphi)\, dt \tag{10.420}$$

The drain current can be expressed in terms of V_{gs}, V_p, and V_{ds} as

$$I_d = I_{dss} \left(1 - \frac{V_g}{V_p} \right)^2 \tanh \left(\frac{\alpha V_d}{V_g - V_p} \right) \tag{10.421}$$

$$V_p = V_{p0} + \gamma V_d \tag{10.422}$$

where I_{dss} is the saturation current, V_p is the gate pinchoff voltage, and α, γ, and V_{p0} are the model parameters of the MESFET.

Applying a Taylor series expansion of the equation about the operating dc point and considering the fundamental frequency component terms, the large-signal drain resistance as a function of the small-signal drain voltage amplitude can be given as

$$R_{DS}|_{\text{large signal}} = \frac{R_{ds}}{1 + AV_d^2} \tag{10.423}$$

where R_{DS} and R_{ds} are the large and small signal differential resistances.

Let A be defined as

$$A = \frac{3 \tanh^2[\alpha V_{d0}/(V_{g0} - V_p)] - 1}{4[(V_{g0} - V_p)/\alpha]^2} \tag{10.424}$$

Let R_{ds} be given as

$$R_{ds} = \frac{\cosh^2[\alpha V_{d0}/(V_{g0} - V_p)]}{I_{dss}(1 - V_{g0}/V_p)^2} \left[\frac{V_{g0} - V_p}{\alpha} \right] \tag{10.425}$$

From the expression above, $R_{DS}|_{\text{large signal}}$ has a maximum in the absence of the RF drive signal and gets smaller as the amplitude of the RF signal increases. Consequently, the oscillator output impedance and the oscillator output power are a function of the change in the drain resistance under large-signal operation. To support the steady-state operation mode, the amplitude and the phase balance conditions can be written as

$$[R_{\text{out}}^*(I, w) + R_L(w)]_{w=w_0} = 0 \tag{10.426}$$

$$[X_{\text{out}}^*(I, w) + X_L^*(w) = 0]_{w=w_0} = 0 \tag{10.427}$$

The output power of the oscillator can be expressed in terms of load current and load impedance as

$$P_{\text{out}} = \tfrac{1}{2} I_{\text{out}}^2 \, \text{Re}[Z_L] \tag{10.428}$$

where I_{out} and V_{out} are the corresponding load current and drain voltage across the output.

$$I_{\text{out}} = \left[\frac{Z_{11} + Z_1 + Z_2}{Z_{22}(Z_{11} + Z_1 + Z_2) - Z_{21}(Z_{12} + Z_2)} \right] V_{\text{out}} \tag{10.429}$$

$$P_{\text{out}} = \frac{1}{2} I_{\text{out}}^2 \, \text{Re}[Z_L] \Rightarrow \frac{1 + \left[(R_{21} - R_{12})/(X_{21} - X_{12}) \right]^2}{(R_{22} + R)^2 + (X_{22} + X)^2} (R_{\text{out}} + R_d) \frac{V_d^2}{2} \tag{10.430}$$

where

$$R = \frac{X_{21}(X_{12} + X_2^*) - R_{21}(R_{12} + R_2 + R_s) - X_{22}(X_{11} + X_1^* + X_2^*)}{R_{11} + R_1 + R_2 + R_g + R_s} \quad (10.431)$$

$$X = \frac{R_{21}(X_{11} + X_1^* + X_2^*) - R_{21}(X_{12} + X_2^*) - X_{21}(R_{12} + R_2 + R_s)}{R_{11} + R_1 + R_2 + R_g + R_s} \quad (10.432)$$

10.18.2 Parallel Feedback (MESFET)

Figure 10.156 shows the parallel feedback topology of the oscillator using the MES-FET, in which the external feedback elements Y_1, Y_2, and Y_3 are shown outside the dashed line. The optimum values of the feedback element Y_1, Y_2, and Y_3 are given as

$$Y_1^{\text{opt}} = R_1^* + jX_1^* \quad (10.433)$$

$$Y_2^{\text{opt}} = R_2^* + jX_2^* \quad (10.434)$$

$$Y_3^{\text{opt}} = Z_L^{\text{opt}} = R_3^* + jX_3^* \quad (10.435)$$

$$Y_{\text{out}}^{\text{opt}} + Z_L^{\text{opt}} \Rightarrow 0 \quad (10.436)$$

$$Y_{\text{out}}^{\text{opt}} = R_{\text{out}}^* + jX_{\text{out}}^* \quad (10.437)$$

The common-source $[Y]$ parameter of the MESFET is given as

$$[Y]_{cs} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \quad (10.438)$$
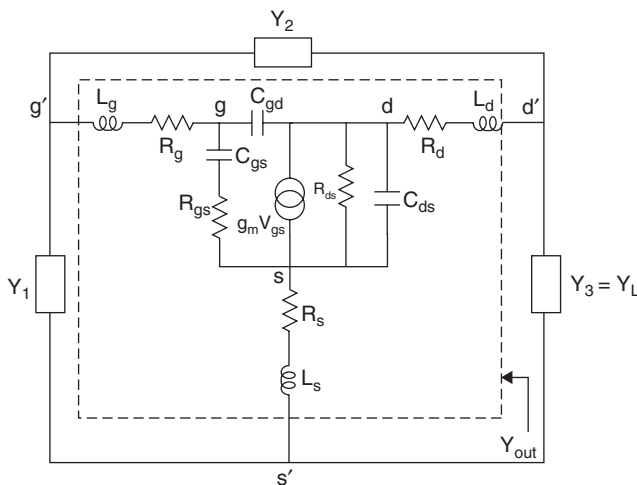
FIGURE 10.156   Parallel feedback topology.

$$Y_{11} = \frac{jwC_{gs}}{1 + jwC_{gs}R_{gs}} + jwC_{gd} \Rightarrow G_{11} + jB_{11} \tag{10.439}$$

$$Y_{21} = \frac{g_m \exp(-jw\tau)}{1 + jwC_{gs}R_{gs}} - jwC_{gd} \Rightarrow G_{21} + jB_{21} \tag{10.440}$$

$$Y_{12} = -jwC_{gd} \Rightarrow G_{12} + jB_{12} \tag{10.441}$$

$$Y_{22} = \frac{1}{R_{ds}} + jw(C_{ds} + C_{gd}) \Rightarrow G_{22} + jB_{22} \tag{10.442}$$

The optimum values of the output admittance Y_{out}^* and the feedback susceptances B_1^* and B_2^* can be expressed in terms of the two-port Y parameter of the active device:

$$B_1^* = -B_{11} + \frac{B_{12} + B_{21}}{2} + \left(\frac{G_{21} - G_{12}}{B_{21} - B_{12}}\right)\left(\frac{G_{12} + G_{21}}{2} + G_{11}\right) \tag{10.443}$$

$$= \frac{g_m}{2wC_{gs}R_{gs}} \tag{10.444}$$

$$B_2^* = \frac{B_{12} + B_{21}}{2} + \frac{(G_{12} + G_{21})(G_{21} - G_{12})}{2(B_{21} - B_{12})} \tag{10.445}$$

$$= -wC_{dg} - \frac{g_m}{2wC_{gs}R_{gs}} \tag{10.446}$$

The optimum value of the real and imaginary part of the output admittance is

$$Y_{\text{out}}^* = (G_{\text{out}}^* + jB_{\text{out}}^*) \tag{10.447}$$

where

$$G_{\text{out}}^* = G_{22} - \frac{(G_{12} + G_{21})^2(B_{21} - B_{12})^2}{4G_{11}} \tag{10.448}$$

$$= \frac{1}{R_{ds}} - \frac{1}{R_{gs}}\left(\frac{g_m}{2wC_{gs}}\right)^2 \tag{10.449}$$

$$B_{\text{out}}^* = B_{22} + \frac{G_{21} - G_{12}}{B_{21} - B_{12}} - \frac{(G_{12} + G_{21})}{2} + G_{22} - G_{\text{out}}^* + \frac{B_{21} + B_{12}}{2} \tag{10.450}$$

$$= wC_{gd} - \frac{1}{R_{gs}}\left(\frac{g_m}{2wC_{gs}}\right)\left(1 - \frac{1}{R_{gs}}\frac{1}{wC_{gs}}\frac{g_m}{2wC_{gs}}\right) \tag{10.451}$$

The value of the output susceptance B_{out}^* may be positive or negative, depending on the values of the transistor transconductance and $\tau_{gs} = R_{gs}C_{gs}$.

The voltage feedback factor n and phase φ_n can be expressed in terms of transistor Y parameters as

$$n\left(\frac{V_{ds}}{V_{gs}}\right) = \frac{\sqrt{(G_{12} + G_{21} - 2G_2)^2 + (B_{21} - B_{12})^2}}{2(G_{12} + G_{21} - G_2)} \Rightarrow \frac{1}{2}\sqrt{1 + (wR_sC_{gs})^2} \tag{10.452}$$

$$\Phi_n(\text{phase}) = \tan^{-1} \frac{B_{21} - B_{12}}{G_{12} + G_{21} - 2G_2} \Rightarrow -\tan^{-1}(wR_sC_{gs}) \tag{10.453}$$

The output power of the oscillator can be expressed in terms of the load current and the load impedance as

$$P_{\text{out}} = \tfrac{1}{2}I_{\text{out}}^2 \text{ Re}[Z_L] \tag{10.454}$$

where I_{out} and V_{out} is the corresponding load current and drain voltage across the output.

$$I_{\text{out}} = \left[\frac{Z_{11} + Z_1 + Z_2}{Z_{22}(Z_{11} + Z_1 + Z_2) - Z_{21}(Z_{12} + Z_2)} \right] V_{\text{out}} \tag{10.455}$$

10.18.3 Series Feedback (Bipolar)

Figure 10.157 shows the series feedback oscillator topology for deriving explicit analytical expressions for the optimum values of the external feedback elements and the load impedance for maximum power output at a given oscillator frequency through $[Z]$ parameters of a bipolar transistor.

Figure 10.157 shows the series feedback topology of the oscillator using a bipolar transistor, in which external feedback elements Z_1, Z_2, and Z_3 are shown outside the dashed line.

The optimum values of the feedback elements Z_1, Z_2, and Z_3 are given as

$$Z_1^{\text{opt}} = R_1^* + jX_1^* \tag{10.456}$$

$$Z_2^{\text{opt}} = R_2^* + jX_2^* \tag{10.457}$$

$$Z_3^{\text{opt}} = Z_L^{\text{opt}} = R_3^* + jX_3^* \tag{10.458}$$

$$Z_{\text{out}}^{\text{opt}} + Z_L^{\text{opt}} \Rightarrow 0 \tag{10.459}$$

$$Z_{\text{out}}^{\text{opt}} = R_{\text{out}}^* + jX_{\text{out}}^* \tag{10.460}$$
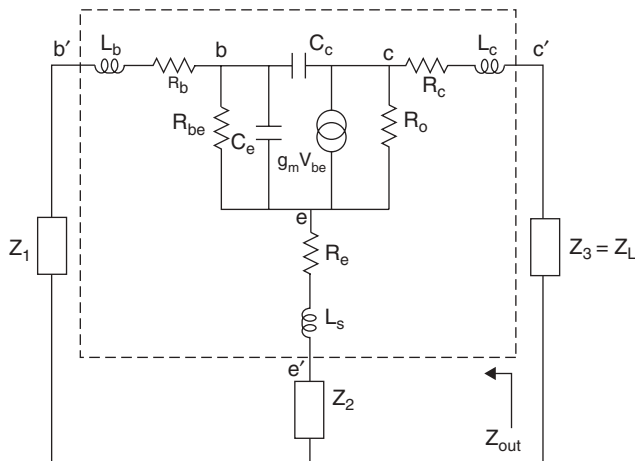
FIGURE 10.157   Series feedback topology of the oscillator using bipolar transistor.

The $[Z]$ parameters of the internal bipolar transistor in a common-emitter, small-signal condition are given as

$$[Z]_{ce} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \tag{10.461}$$

$$Z_{11} = R_{11} + jX_{11} \Rightarrow a\left[\frac{1}{g_m} + r_b\left(\frac{w}{w_T}\right)^2\right] - ja\frac{w}{w_T}\left(\frac{1}{g_m} - r_b\right) \tag{10.462}$$

$$Z_{12} = R_{12} + jX_{12} \Rightarrow a\left[\frac{1}{g_m} + r_b\left(\frac{w}{w_T}\right)^2\right] - ja\frac{w}{w_T}\left(\frac{1}{g_m} - r_b\right) \tag{10.463}$$

$$Z_{21} = R_{21} + jX_{21} \Rightarrow a\left[\frac{1}{w_T C_c} + \frac{1}{g_m} + r_b\left(\frac{w}{w_T}\right)^2\right] - ja\frac{w}{w_T}\left(\frac{1}{g_m} - \frac{1}{w_T C_c} - r_b\right) \tag{10.464}$$

$$Z_{22} = R_{22} + jX_{22} \Rightarrow a\left[\frac{1}{w_T C_c} + \frac{1}{g_m} + r_b\left(\frac{w}{w_T}\right)^2\right] - ja\frac{w}{w_T}\left(\frac{1}{g_m} + \frac{1}{w_T C_c} - r_b\right) \tag{10.465}$$

where

$$a = \frac{1}{1 + (w/w_T)^2} \tag{10.466}$$

$$w_T = 2\pi f_T \tag{10.467}$$

$$f_T = \frac{g_m}{2\pi C_e} \tag{10.468}$$

According to the optimum criterion for the maximum power output at a given oscillator frequency, the negative real part of the output impedance Z_{out} has to be maximized and the possible optimal values of the feedback reactance, under which the negative value of R_{out} is maximized, is given by the following:

$$\frac{\partial \operatorname{Re}}{\partial X_1}[Z_{out}(I, w)] = 0 \Rightarrow \frac{\partial}{\partial X_1}[R_{out}] = 0 \tag{10.469}$$

$$\frac{\partial \operatorname{Re}}{\partial X_2}[Z_{out}(I, w)] = 0 \Rightarrow \frac{\partial}{\partial X_2}[R_{out}] = 0 \tag{10.470}$$

The values of X_1 and X_2 which will satisfy the differential equations above are given as X_1^* and X_2^* and can be expressed in terms of a two-port parameter of the active device (bipolar):

$$X_1^* = -X_{11} + \frac{X_{12} + X_{21}}{2} + \left(\frac{R_{21} - R_{12}}{X_{21} - X_{12}}\right)\left(\frac{R_{12} + R_{21}}{2} - R_{11} - R_1\right) \tag{10.471}$$

$$= \frac{1}{2wC_c} - r_b\frac{w}{w_T} \tag{10.472}$$

$$X_2^* = -\frac{X_{12} + X_{21}}{2} - \frac{(R_{21} - R_{12})(2R_2 + R_{12} + R_{21})}{2(X_{21} - X_{12})} \Rightarrow -\frac{1}{2wC_c} - r_e\frac{w}{w_T} \tag{10.473}$$

$$= -\frac{1}{2wC_c} - r_e\frac{w}{w_T} \tag{10.474}$$

By substituting the values of X_1^* and X_2^* into the equation above, the optimal real and imaginary parts of the output impedance Z_{out}^* can be expressed as

$$Z_{\text{out}}^* = R_{\text{out}}^* + X_{\text{out}}^* \tag{10.475}$$

$$R_{\text{out}}^* = R_2 + R_{22} - \frac{(2R_2 + R_{21} + R_{12})^2 + (X_{21} - X_{12})^2}{4(R_{11} + R_2 + R_1)} \tag{10.476}$$

$$R_{\text{out}}^* = r_c + \frac{r_b}{r_b + r_e + R_{11}}\left(r_e + R_{11} + \frac{a}{w_T C_e}\right) - \frac{a}{r_b + r_e + R_{11}}\left(\frac{1}{2wC_e}\right) \tag{10.477}$$

$$X_{\text{out}}^* = X_2^* + X_{22} - \left(\frac{R_{21} - R_{12}}{X_{21} - X_{12}}\right)\left(R_{\text{out}}^* - R_2 - R_{22}\right) \tag{10.478}$$

$$X_{\text{out}}^* = \frac{1}{2wC_e} - (R_{\text{out}}^* - r_c)\frac{w}{w_T} \tag{10.479}$$

Thus, in the steady-state operation mode of the oscillator, the amplitude and the phase balance conditions can be written as

$$R_{\text{out}}^* + R_L = 0 \tag{10.480}$$

$$X_{\text{out}}^* + X_L^* = 0 \tag{10.481}$$

The output power of the oscillator can be expressed in terms of load current and load impedance as

$$P_{\text{out}} = \tfrac{1}{2}I_{\text{out}}^2 \, \text{Re}[Z_L] \tag{10.482}$$

Let I_{out} and V_{out} be the corresponding load current and drain voltage across the output:

$$I_{\text{out}} = \left[\frac{Z_{11} + Z_1 + Z_2}{Z_{11}Z_2 - Z_{12}(Z_1 + Z_2)}\right]V_{be} \tag{10.483}$$

$$V_{\text{out}} = V_c = \left[\frac{Z_{22}(Z_{11} + Z_1 + Z_2) - Z_{21}(Z_2 + Z_{12})}{Z_{12}(Z_1 + Z_2) - Z_{11}Z_2}\right]V_{be} \tag{10.484}$$

$$P_{\text{out}} = \tfrac{1}{2}I_{\text{out}}^2 \, \text{Re}[Z_L] \tag{10.485}$$

$$= aG_m^2(x)R_{\text{out}}^* \frac{r_b + r_e + R_{11}}{r_b + r_c - R_{\text{out}}^*}\frac{V_1^2}{2} \tag{10.486}$$

Then assume V_1 is the signal voltage and x is the drive level across the base–emitter junction of the bipolar transistor. The large-signal transconductance $G_m(x)$ is given as

$$G_m(x) = \frac{q I_{dc}}{kTx} \left[\frac{2I_1(x)}{I_0(x)} \right]_{n=1} = \frac{g_m}{x} \left[\frac{2I_1(x)}{I_0(x)} \right]_{n=1} \tag{10.487}$$

$$V_1|_{peak} = \frac{kT}{q} x \tag{10.488}$$

$$g_m = \frac{I_{dc}}{kT/q} \tag{10.489}$$

where g_m is the small-signal transconductance.

10.18.4 Parallel Feedback (Bipolar)

Figure 10.158 shows the parallel feedback topology of the oscillator using a bipolar transistor in which the external feedback elements Y_1, Y_2, and Y_3 are shown outside the dashed line. The optimum values of the feedback elements Y_1, Y_2, and Y_3 are given as

$$Y_1^{opt} = R_1^* + jX_1^* \tag{10.490}$$

$$Y_2^{opt} = R_2^* + jX_2^* \tag{10.491}$$

$$Y_3^{opt} = Z_L^{opt} = R_3^* + jX_3^* \tag{10.492}$$

$$Y_{out}^{opt} + Z_L^{opt} \Rightarrow 0 \tag{10.493}$$

$$Y_{out}^{opt} = R_{out}^* + jX_{out}^* \tag{10.494}$$

The common-source $[Y]$ parameters of the bipolar transistor are given as

$$[Y]_{cs} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{10.495}$$
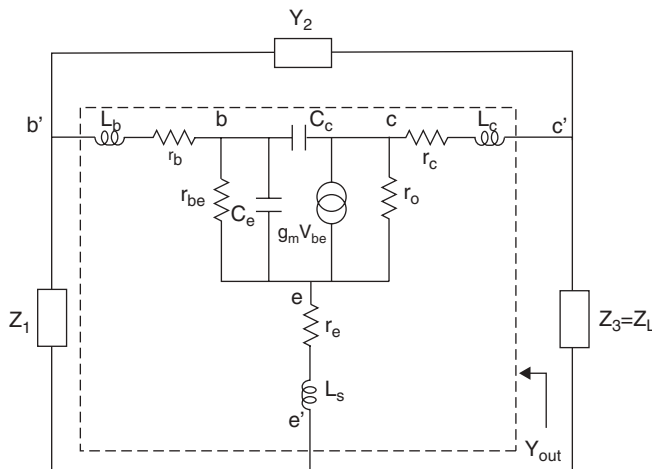
FIGURE 10.158 Parallel feedback topology of the oscillator using a bipolar transistor.

$$Y_{11} = G_{11} + jB_{11} \tag{10.496}$$

$$Y_{21} = G_{21} + jB_{21} \tag{10.497}$$

$$Y_{12} = G_{12} + jB_{12} \tag{10.498}$$

$$Y_{22} = G_{22} + jB_{22} \tag{10.499}$$

The optimum values of the output admittance Y_{out}^* and feedback susceptances B_1^* and B_2^* can be expressed in terms of the two-port Y parameter of the active device:

$$B_1^* = -B_{11} + \frac{B_{12} + B_{21}}{2} + \left(\frac{G_{21} - G_{12}}{B_{21} - B_{12}}\right)\left(\frac{G_{12} + G_{21}}{2} + G_{11}\right) \tag{10.500}$$

$$B_2^* = \frac{B_{12} + B_{21}}{2} + \frac{(G_{12} + G_{21})(G_{21} - G_{12})}{2(B_{21} - B_{12})} \tag{10.501}$$

The optimum value of the real and imaginary part of the output admittance is

$$Y_{\text{out}}^* = G_{\text{out}}^* + jB_{\text{out}}^* \tag{10.502}$$

where

$$G_{\text{out}}^* = G_{22} - \frac{(G_{12} + G_{21})^2(B_{21} - B_{12})^2}{4G_{11}} \tag{10.503}$$

$$B_{\text{out}}^* = B_{22} + \frac{G_{21} - G_{12}}{B_{21} - B_{12}} - \frac{(G_{12} + G_{21})}{2} + G_{22} - G_{\text{out}}^* + \frac{B_{21} + B_{12}}{2} \tag{10.504}$$

The output power of the oscillator can be expressed in terms of the load current and the load impedance as

$$P_{\text{out}} = \tfrac{1}{2}I_{\text{out}}^2 \, \text{Re}[Z_L] \tag{10.505}$$

where I_{out} and V_{out} are the corresponding load current and drain voltage across the output:

$$I_{\text{out}} = \left[\frac{Z_{11} + Z_1 + Z_2}{Z_{22}(Z_{11} + Z_1 + Z_2) - Z_{21}(Z_{12} + Z_2)}\right] V_{\text{out}} \tag{10.506}$$

10.18.5   An FET Example

Figure 10.159 shows a 950-MHz MESFET oscillator circuit configuration [10.68, 10.69] and the analytical approach for optimum operating conditions for maximum oscillator output power.

The analysis is based on a quasi-linear approach and is experimentally supported with a conversion efficiency of 54%, which is the maximum conversion efficiency published for this topology. However, the publication does not give any emphasis on the optimum phase noise, which is the key parameter for the oscillator design.
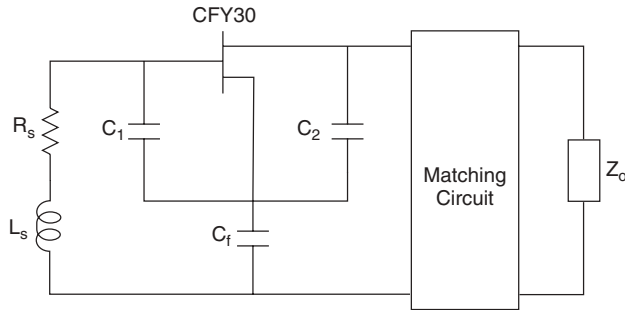
FIGURE 10.159 A 950-MHz MESFET oscillator circuit configuration.
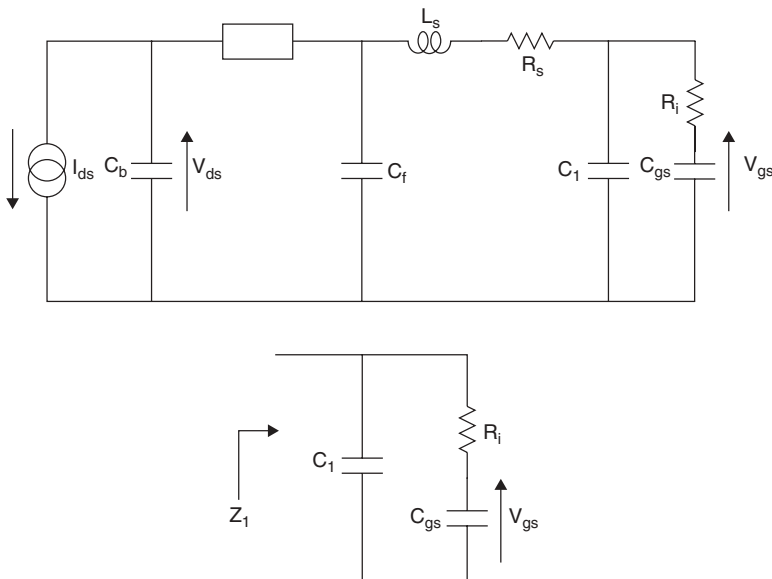
FIGURE 10.160 Equivalent circuit of the open model MESFET oscillator.

In the power optimization of a GaAs 950-MHz MESFET oscillator, the derivation of the analytical expressions is based on the open-loop model of the oscillator. Figure 10.160 shows an equivalent circuit of the oscillator. Assume Z_1 can be expressed as

$$Z_1 = \frac{(R_i + 1/jwC_{gs})(1/jwC_1)}{R_i + 1/jwC_{gs} + 1/jwC_1} = \frac{-jR_i/wC_1 + 1/w^2C_{gs}C_1}{R_i - j(1/wC_{gs} + 1/wC_1)} \tag{10.507}$$

Multiplying the numerator and the denominator by the conjugate yields

$$Z_1 = \frac{\begin{array}{c}(-jR_i^2/wC_1 - R_i/w^2C_{gs}C_1) + (R_i/w^2C_1)(1/C_1 + 1/C_{gs}) \\ -(j/w^3C_{gs}C_1)(1/C_1 + 1/C_{gs})\end{array}}{R_i^2 + (1/wC_{gs} + 1/wC_1)^2} \tag{10.508}$$

The following assumptions are made for simplification purposes:

$$\frac{R_i}{w^2 C_{gs} C_1} \ll \frac{R_i}{w^2 C_1} \left(\frac{1}{C_1} + \frac{1}{C_{gs}} \right) \tag{10.509}$$

$$\frac{j R_i^2}{w C_1} \ll \frac{j}{w^3 C_{gs} C_1} \left(\frac{1}{C_1} + \frac{1}{C_{gs}} \right) \tag{10.510}$$

$$R_i \ll \frac{1}{w C_{gs}} + \frac{1}{w C_1} \tag{10.511}$$

Then modified Z_1 can be represented as

$$Z_1 = \frac{(R_i/w^2 C_1)(1/C_1 + 1/C_{gs}) - (j/w^3 C_{gs} C_1)(1/C_1 + 1/C_{gs})}{(1/w C_{gs} + 1/w C_1)^2} \tag{10.512}$$

$$= \frac{R_i/C_1}{1/C_1 + 1/C_{gs}} - \frac{j}{w[C_1 + C_{gs}]} \tag{10.513}$$

defining the three new variables as [10.69]

$$C_a = C_1 + C_{gs} \tag{10.514}$$

$$C_b = C_2 + C_{ds} \tag{10.515}$$

$$R_a = R_s + \frac{C_{gs}^2}{C_a^2} R_i \tag{10.516}$$

$$X_a = w L_s - \frac{1}{w C_a} \tag{10.517}$$

$$w(X_a = 0) = \frac{1}{\sqrt{L_s C_a}} \tag{10.518}$$

Figure 10.161 shows a simplified open-loop model of the oscillator for easy analysis. In this open-loop model, the parasitic elements of the device are absorbed into the corresponding embedding impedances:

$$Z = R_a + \frac{1}{jw C_a} \Rightarrow R_s + \frac{C_{gs}^2}{C_a^2} R_i - \frac{j}{w C_a} \tag{10.519}$$

$$Z + jw L_s = R_s + \frac{C_{gs}^2}{C_a^2} R_i - \frac{j}{w C_a} + jw L_s \Rightarrow \left(R_s + \frac{C_{gs}^2}{C_a^2} R_i \right) + j \left(w L_s - \frac{1}{w C_a} \right) \tag{10.520}$$

$$Z_a = Z + jw L_s \Rightarrow R_a + j X_a \tag{10.521}$$

$$R_a = R_s + \frac{C_{gs}^2}{C_a^2} R_i \tag{10.522}$$
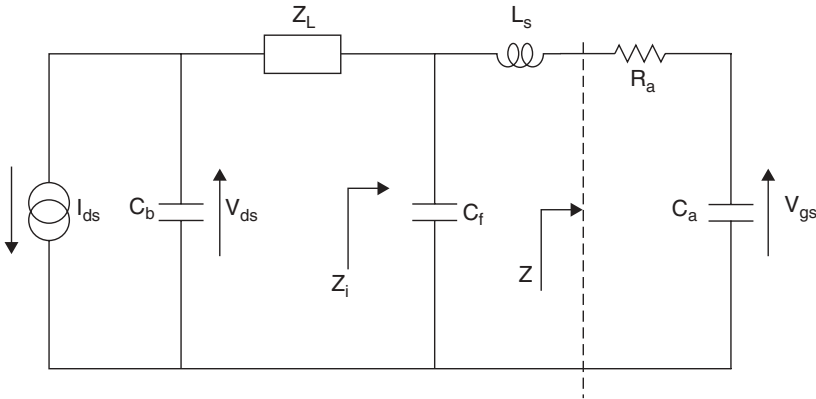
FIGURE 10.161 A simplified open loop model of the oscillator.

$$X_a = wL_s - \frac{1}{wC_a} \tag{10.523}$$

$$Z_i = Z_a \| C_f \Rightarrow (Z + jwL_s)\| C_f \tag{10.524}$$

$$Z_i = \frac{-j[(R_a + jX_a)/wC_f]}{R_a + jX_a - j/wC_f} \Rightarrow \frac{R_a + jX_a}{1 + jR_awC_f - wC_fX_a} = \frac{R_a + jX_a}{1 + jwC_f(R_a + jX_a)} \tag{10.525}$$

The circuit model of the oscillator is shown in Figure 10.162, in which the output current through Z_L is given as

$$I = \frac{I_{ds}}{1 + jwC_b(Z_i + Z_L)} \tag{10.526}$$

The voltage across Z_i is given as

$$V_{zi} = IZ_i = -I_{ds}\left[\frac{R_a + jX_a}{1 + jwC_f(R_a + jX_a)}\right]\left[\frac{1}{1 + jwC_b(Z_i + Z_L)}\right] \tag{10.527}$$
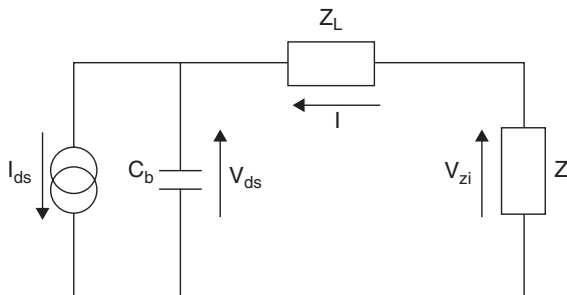
FIGURE 10.162 Circuit model of an oscillator.

Applying the voltage divider in Figure 10.160, V_{gs} can be expressed as

$$V_{gs} = -I_{ds}\left[\frac{1}{jwC_b(R_a + jX_a)}\right]\left[\frac{Z_i}{1 + jwC_b(Z_i + Z_L]}\right) \tag{10.528}$$

Steady-state oscillation occurs when $I_{ds}(t) = I_I$ and $V_{gs} = V_p$. Consequently, the equation above can be written as

$$1 + jwC_b(Z_i + Z_L) = -\frac{I_{ds}}{V_{gs}}\frac{Z_i}{jwC_a(R_a + jX_a)} \tag{10.529}$$

$$1 + jwC_b(Z_i + Z_L) = \frac{-g_{mc}Z_i}{jwC_a(R_a + jX_a)}$$

$$\Rightarrow \frac{-g_{mc}(R_a + jX_a)}{jwC_a(R_a + jX_a)[1 + jwC_f(R_a + jX_a)]} \tag{10.530}$$

$$1 + jwC_b(Z_i + Z_L) = \frac{-g_{mc}}{jwC_a[1 + jwC_f(R_a + jX_a)]}$$

$$= \frac{g_{mc}}{w^2C_fC_a - j(wC_a - w^2C_fC_aX_a)} \tag{10.531}$$

$$Z_L = Z_i\frac{g_{mc}}{w^2C_bC_a(R_a + jX_a)} - Z_i - \frac{1}{jwC_b} \tag{10.532}$$

$$Z_L = \frac{g_{mc}(R_a + jX_a)}{[1 + jwC_f(R_a + jX_a)][w^2C_bC_a(R_a + jX_a)]}$$

$$- \frac{R_a + jX_a}{1 + jwC_f(R_a + jX_a)} - \frac{1}{jwC_b} \tag{10.533}$$

$$= \frac{g_{mc}}{w^2C_bC_a[1 + jwC_f(R_a + jX_a)]}$$

$$- \frac{R_a + jX_a}{1 + jwC_f(R_a + jX_a)} - \frac{1}{jwC_b} \tag{10.534}$$

where

$$g_{mc} = \frac{I_1}{V_p} = \frac{I_{max}}{2V_p} \tag{10.535}$$

In addition, V_{ds} can be determined by calculating I_{cb}, the current through C_b, with the help of Figure 10.162:

$$I_{cb} = I_{ds}\frac{Z_L + Z_i}{Z_L + Z_i + 1/jwC_b} \tag{10.536}$$

Based on the last result, we can conclude that

$$V_{ds} = I_{cb}\frac{j}{wC_b} = \frac{Z_L + Z_i}{Z_L + Z_i + 1/jwC_b}I_1 \tag{10.537}$$

or, in square magnitude form,

$$V_{ds}^2 = \frac{(Z_L + Z_i)^2}{[1 + jwC_b(Z_L + Z_i)]^2} I_1^2 \tag{10.538}$$

Also, $\mathrm{Re}[Z_L]$ can be defined as follows:

$$\mathrm{Re}[Z_L] = \frac{g_{mc}(1 - wC_f X_a - jwC_f R_a)}{w^2 C_b C_a[(1 - wC_f X_a)^2 + w^2 C_f^2 R_a^2]}$$
$$- \frac{(R_a + jX_a)(1 - wC_f X_a - jwC_f R_a)}{(1 - wC_f X_a)^2 + w^2 C_f^2 R_a^2} \tag{10.539}$$

$$= \frac{g_{mc}(1 - wC_f X_a - jwC_f R_a)}{-w^2 C_b C_a(R_a + jX_a)(1 - wC_f X_a - jwC_f R_a)}{w^2 C_b C_a[(1 - wC_f X_a)^2 + w^2 C_f^2 R_a^2]} \tag{10.540}$$

$$= \frac{g_{mc}(1 - wC_f X_a) - w^2 C_b C_a R_a + w^3 C_b C_a C_f X_a}{-w^3 C_b C_a C_f R_a}{w^2 C_b C_a[(1 - wC_f X_a)^2 + w^2 C_f^2 R_a^2]} \tag{10.541}$$

The power delivered to the load Z_L and the magnitude of V_{ds} can be determined by

$$P_{\mathrm{out}} = \frac{1}{2} I^2 \, \mathrm{Re}[Z_L] \tag{10.542}$$

$$= \frac{1}{2} I_1^2 \frac{\mathrm{Re}[Z_L]}{[1 + jwC_b(Z_L + Z_i)]^2} \tag{10.543}$$

$$V_{ds}^2 = \frac{(Z_L + Z_i)^2}{[1 + jwC_b(Z_L + Z_i)]^2} I_1^2 \tag{10.544}$$

$$[1 + jwC_b(Z_i + Z_L)]^2 = \frac{g_{mc}^2}{[w^2 C_f C_a R_a - j(wC_a - w^2 C_f C_a X_a)]} \times [w^2 C_f C_a R_a + j(wC_a - w^2 C_f C_a X_a)] \tag{10.545}$$

$$= \frac{g_{mc}^2}{(w^2 C_f C_a R_a)^2 + (wC_a - w^2 C_f C_a X_a)^2}$$

$$= \frac{g_{mc}^2}{w^2 C_a^2[(1 - w^2 C_f C_a X_a)^2 + (w^2 C_f C_a R_a)^2]} \tag{10.546}$$

Based on the equations above, the output power can be estimated as

$$P_{\mathrm{out}} = \frac{1}{2} I^2 \, \mathrm{Re}(Z_L) \tag{10.547}$$

$$= \frac{1}{2} I_1^2 \frac{\mathrm{Re}(Z_L)}{[1 + jwC_b(Z_L + Z_i)]^2} \tag{10.548}$$

$$
\begin{aligned}
&= \frac{1}{2} I_1^2 \frac{\dfrac{g_{mc}(1 - wC_f X_a) - w^2 C_b C_a R_a + w^3 C_b C_a C_f X_a - w^3 C_b C_a C_f R_a)}{w^2 C_b C_a [(1 - wC_f X_a)^2 + w^2 C_f^2 R_a^2]}}{\dfrac{g_{mc}^2}{w^2 C_a^2 [(1 - w^2 C_f C_a X_a)^2 + (w^2 C_f C_a R_a)^2]}}
\end{aligned}
$$

$$(10.549)$$

$$
= \frac{1}{2} I_1^2 C_a \frac{[(1 - wC_f X_a) - w^2 C_b C_a R_a + w^3 C_b C_a C_f X_a - w^3 C_b C_a C_f R_a)]}{g_{mc} C_b}
$$

$$(10.550)$$

Below 5 GHz, it is valid to ignore some of the terms by assuming that [10.69]

$$
w^2 C_b C_a R_a \gg w^3 C_b C_a C_f X_a \tag{10.551}
$$

$$
\gg w^3 C_b C_a C_f R_a \tag{10.552}
$$

The power output is now expressed as

$$
P_{\text{out}} = \frac{1}{2} I_1^2 C_a \frac{g_{mc}(1 - wC_f X_a) - (w^2 C_b C_a C_f R_a)}{g_{mc}^2 C_b} \tag{10.553}
$$

$$
= \frac{1}{2} I_1^2 \left(C_a w \frac{1 - wC_f X_a}{wC_b} - \frac{w^2 C_a^2 R_a}{g_{mc}^2} \right) \tag{10.554}
$$

$$
= \frac{1}{2} I_1^2 \left(\alpha \frac{1 - wC_f X_a}{wC_b} - \alpha^2 R_a \right) \tag{10.555}
$$

$$
\alpha = \frac{wC_a}{g_{mc}} \tag{10.556}
$$

In a similar manner,

$$
V_{ds}^2 = I_1^2 \left[\frac{\alpha^2 (1 - wC_f X_a)^2 + (1 - wC_f R_a)^2}{w^2 C_b^2} \right] \tag{10.557}
$$

Both the output power and V_{ds} depend on C_b if the other parameters are fixed.

This is a limitation for the maximum value. However, a maximum value of the current and the voltage a transistor can take before burnout. Therefore, by setting $|V_{ds}| = V_{dsm}$, an optimal condition according to the author is given by

$$
\frac{|V_{ds}|^2}{I_1^2} = \frac{|V_{dsm}|^2}{I_1^2} = \frac{\alpha^2 (1 - wC_f X_a)^2 + (1 - wC_f R_a)^2}{w^2 C_b^2} \tag{10.558}
$$

The optimum load impedance that the device needs to see to deliver the highest power is defined as

$$
\frac{|V_{ds}|}{I_1} = \frac{2|V_{dsm}|}{I_{\text{max}}} = R_{\text{opt}} \tag{10.559}
$$

leading to the definition

$$wC_b R_{\text{opt}} = \sqrt{\alpha^2(1 - wC_f X_a)^2 + (1 - wC_f R_a)^2} \tag{10.560}$$

Using the result above, the optimum P_{out} is, therefore, given by

$$P_{\text{out}} = \frac{V_{dsm} I_{dsm}}{4} \alpha \frac{1 - wC_f X_a}{\sqrt{\alpha^2(1 - wC_f X_a)^2 + (1 - wC_f R_a)^2}} - (wC_a V_p)^2 \frac{R_a}{2} \tag{10.561}$$

The first term is the power available from the current source and the second term is the power absorbed by R_a. This also indicates that a high-Q inductor minimizes the absorbed power, increasing the power available from the current source. At the oscillation frequency P_{out} simplifies further since $X_a \approx 0$:

$$P_{\text{out}} = \frac{V_{dsm} I_{dsm}}{4} \alpha \frac{1}{\sqrt{\alpha^2 + (1 - \alpha wC_f R_a)^2}} - (wC_a V_p)^2 \frac{R_a}{2} \tag{10.562}$$

The above analytical analysis gives the following important results:

1. Maximum output power is attained if we set

$$C_f = \frac{1}{\alpha w R_a} \tag{10.563}$$

and

$$P_{\text{out}}(\text{max}) = \frac{V_{dsm} I_{\text{max}}}{4} \left(1 - \frac{1}{G}\right) \tag{10.564}$$

$$\frac{1}{G} = \frac{P_f}{P_{\text{av}}} = w^2 C_a^2 R_a \frac{2V_{p^2}}{V_{dsm} I_{\text{max}}} \tag{10.565}$$

Accordingly, the dc/RF conversion efficiency is calculated by

$$P_{\text{dc}} = \frac{V_{DS} I_{\text{max}}}{\pi} \tag{10.566}$$

$$\eta_{\text{max}} = \frac{P_{\text{out}}(\text{max})}{P_{\text{dc}}} \tag{10.567}$$

$$= \left(1 - \frac{1}{G}\right) \frac{V_{dsm}}{V_{DS}} \tag{10.568}$$

To maximize the oscillator output power and efficiency, the loss resistance R_a of the input circuit has to be reduced (increasing G), and an optimal biasing condition V_{DS} has to be selected.

2. Let

$$C_b = \frac{(1 - wC_f R_a)C_a}{g_{mc} R_{\text{opt}}} \tag{10.569}$$

$$C_b(C_f = 0) = \frac{C_a}{g_{mc} R_{\text{opt}}} \tag{10.570}$$

3. Combining the above equation leads to the following expression for Z_L:

$$Z_L = \frac{1 + j\alpha}{1 + \alpha^2} R_{\text{opt}} \qquad (10.571)$$

From these analytical calculations, the results achieved are given below. Finally, a circuit simulation of the oscillator was done using a nonlinear Materka model.

Figure 10.163 shows the schematic diagram of a practical oscillator operating at 950 MHz. A simple high-pass filter consisting of L_T and C_T is used to transfer the $Z_0/50$-Ω load to the required Z_L value.

From the above expression all the effective components of the oscillator can be given as follows [10.69]:

1. Bias condition:
$$V_{DS} = 5 \text{ V} \qquad I_{DS} = 18 \text{ mA}$$

2. Device parameters:
$$I_{\max} = 45 \text{ mA} \qquad V_P = 1.25 \text{ V} \qquad V_K \text{(knee voltage)} = 0.5 \text{ V}$$

3. Device parasitic:
$$C_{gs} = 0.5 \text{ pF} \qquad C_{ds} = 0.2 \text{ pF} \qquad C_{gd} = 0.0089 \text{ pF}$$

4. Oscillator parameters:

$$w = \frac{1}{\sqrt{L_s C_a}} \Rightarrow f = 950 \text{ MHz}$$

$$C_1 = 6 \text{ pF} \qquad C_2 = 1.5 \text{ pF} \qquad C_f = 20 \text{ pF}$$

$$L_s = 3.9 \text{ nH} \qquad C_a = C_1 + C_{gs} = 6.5 \text{ pF} \qquad C_b = C_2 + C_{ds} = 1.7 \text{ pF}$$

$$L'_f = 18 \text{ nH} \qquad C'_f = 15 \text{ pF} \qquad R_a = R_s + \frac{C_{gs}^2}{C_a^2} R_i = 4 \text{ } \Omega$$
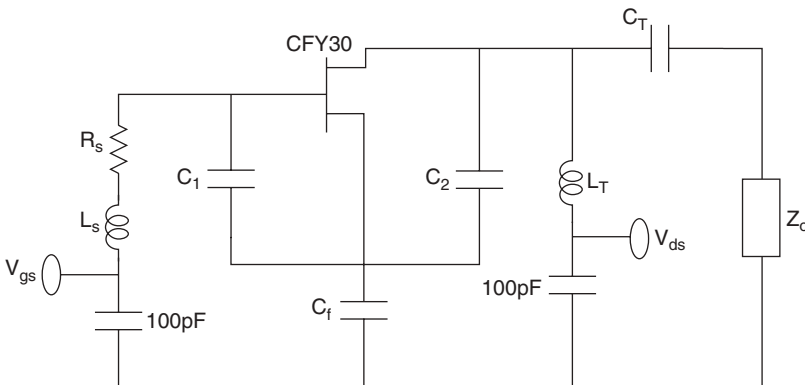
FIGURE 10.163   Schematic diagram of the oscillator operating at 950 MHz.

5. Output matching circuit:

$$L_d(\text{package}) = 0.7 \text{ nH} \qquad L_T = 8.9 \text{ nH} \qquad L'_T = 8.9 \text{ nH} - L_d = 8.7 \text{ nH}$$
$$C_T = 1.91 \text{ pF}$$

6. Calculation of R_{opt}:

$$I_{\text{dc}} = \frac{I_{\text{max}}}{\pi} \qquad I_1 = \frac{I_{\text{max}}}{2} = 22.5 \text{ mA}$$
$$R_{\text{opt}} = \frac{V_{dsm}}{I_1} = \frac{V_{DS} - V_K}{I_1} = \frac{5 \text{ V} - 0.5 \text{ V}}{22.5 \text{ mA}} = 200 \text{ } \Omega$$

7. Calculation of Z_L:

$$Z_L = \frac{1 + j\alpha}{1 + \alpha^2} R_{\text{opt}}$$
$$g_{mc} = \frac{I_1}{V_p} = \frac{I_{\text{max}}}{2V_p} = \frac{45 \text{ mA}}{2 \times 1.25} = 18.8 \text{ mS}$$
$$\alpha = \frac{w_0 C_a}{g_{mc}} = \frac{2 \times \pi \times (950 \times 10^6)(6.5 \times 10^{-12})}{0.0188} = 2.0$$
$$Z_L = \frac{1 + j\alpha}{1 + \alpha^2} R_{\text{opt}} = \frac{1 + j2}{1 + 4} \times 200 = 40 + j80 \text{ } \Omega$$

8. Output power:

$$P_{\text{out}}(\text{max}) = \frac{V_{dsm} I_{\text{max}}}{4} \left(1 - \frac{1}{G}\right)$$
$$= 16.6 \text{ dBm} \qquad \frac{1}{G} = \frac{P_f}{P_{\text{av}}} = w^2 C_a^2 R_a \frac{2V_p^2}{V_{dsm} I_{\text{max}}}$$

9. dc–RF conversion efficiency:

$$P_{\text{dc}} = \frac{V_{DS} I_{\text{max}}}{\pi} = \frac{5 \times 45 \text{ mA}}{\pi} = 71.62 \text{ mW}$$
$$\eta_{\text{max}} = \frac{P_{\text{out}}(\text{max})}{P_{\text{dc}}} = \frac{45.7 \text{ mW}}{71.62 \text{ mW}} = 0.64$$
$$= 64\%$$

10.18.6 Simulated Results

Figures 10.164 to 10.169 show the oscillator test circuit and simulated results. After the oscillator circuit is analyzed in the harmonic balance program, the oscillator frequency is found to be 1.08 GHz and some tuning is required to bring the oscillator frequency back to the required value by changing L_s from 3.9 to 4.45 nH. The slight shift in the oscillator frequency may be due to the device parasitic. The simulated power
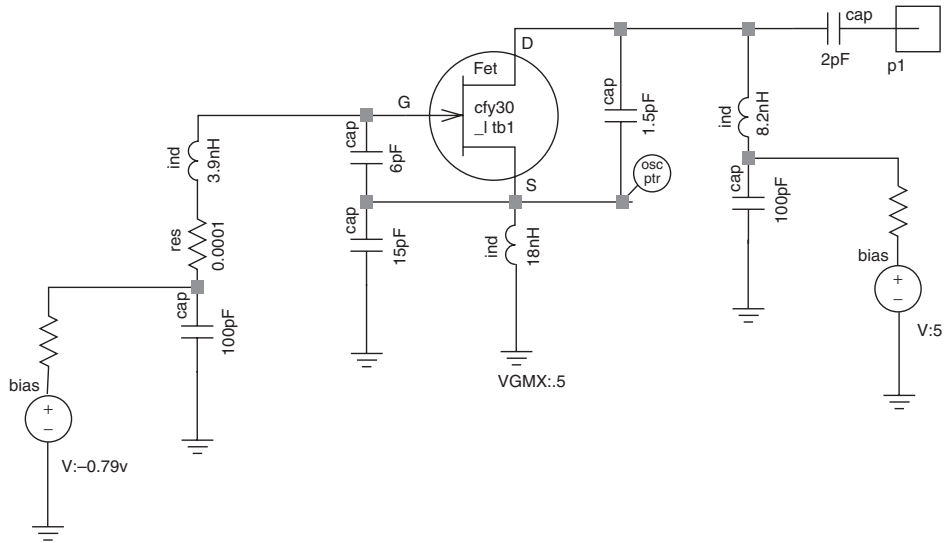
FIGURE 10.164   Schematic of the test oscillator.
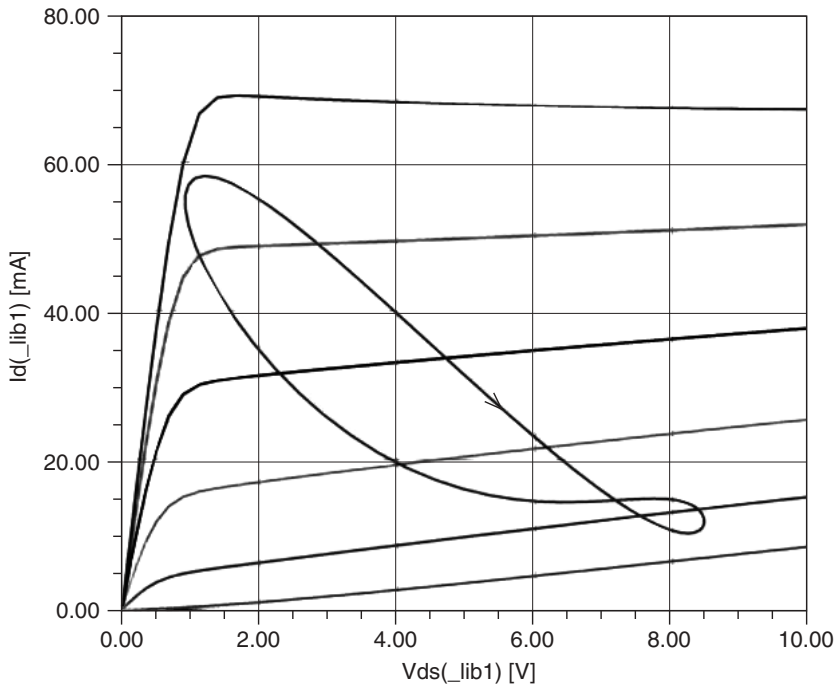
FIGURE 10.165   Load line of the oscillator shown in Figure 10.164. Because the load is a tuned circuit, the "load line" is a curve and not a straight line [10.69].
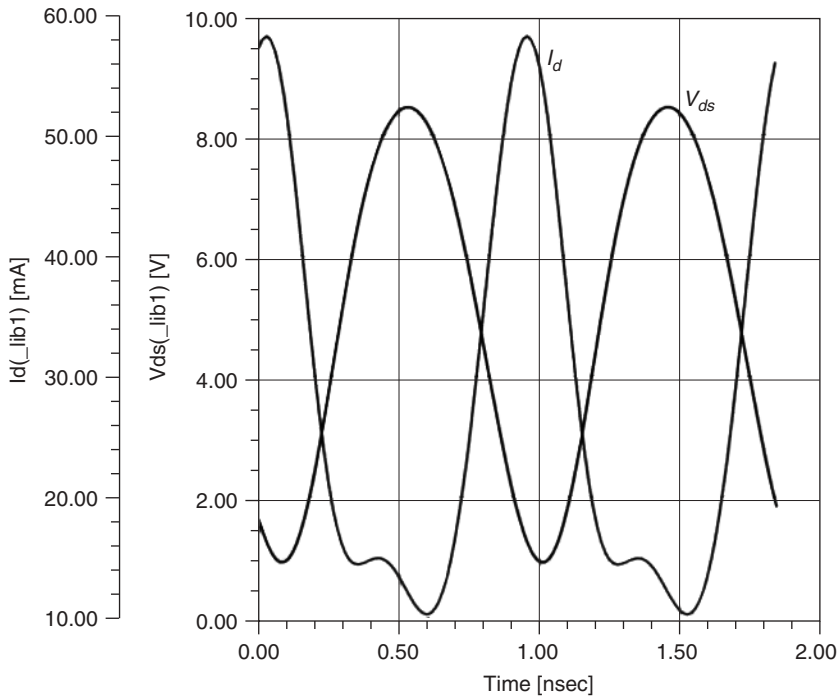
FIGURE 10.166 Plot of drain current and drain source voltage as a function of time.
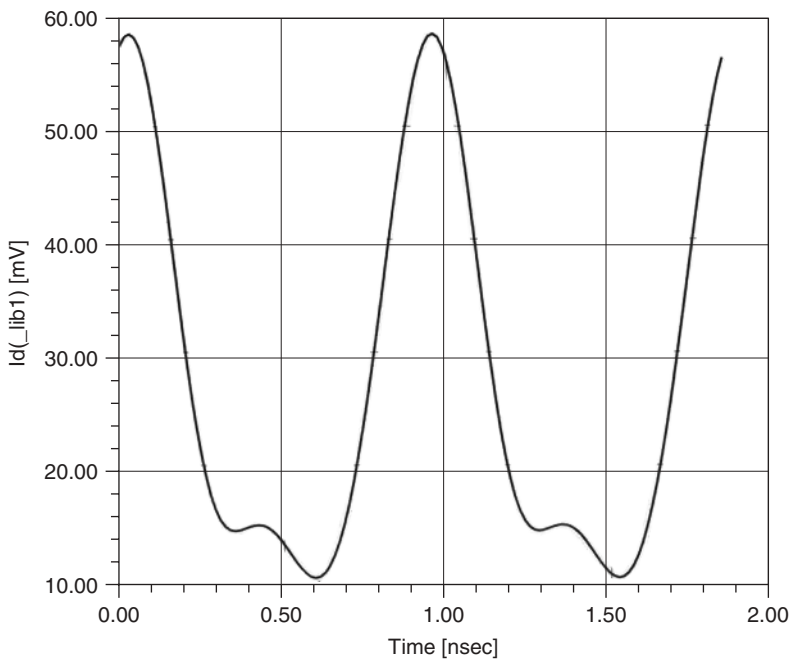
FIGURE 10.167 The ac drain current simulated for Figure 10.164.
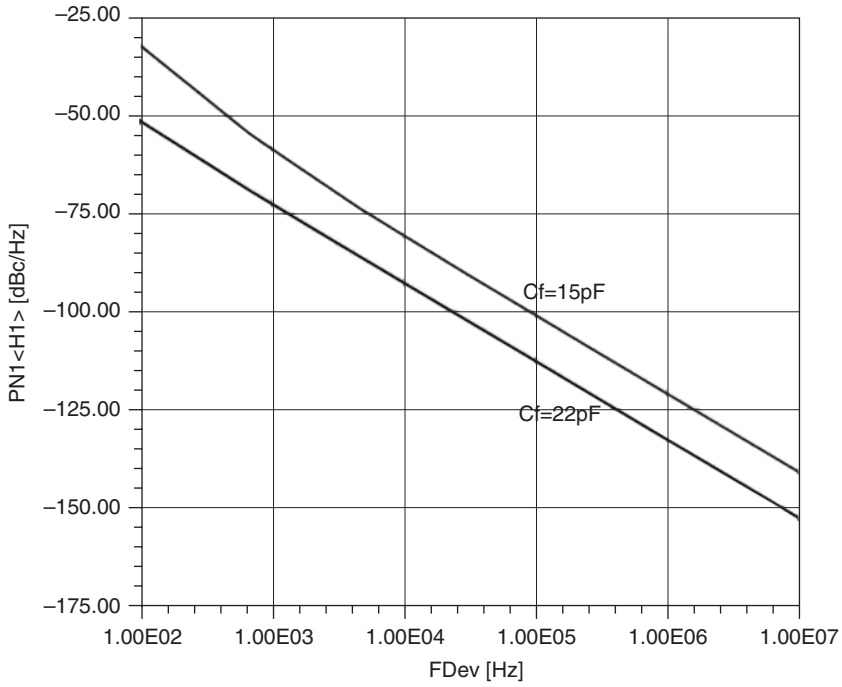
FIGURE 10.168   Simulated noise figure of the circuit shown in Figure 10.164. An increase of the feedback capacitor from 15 to 22 pF improves the phase noise.
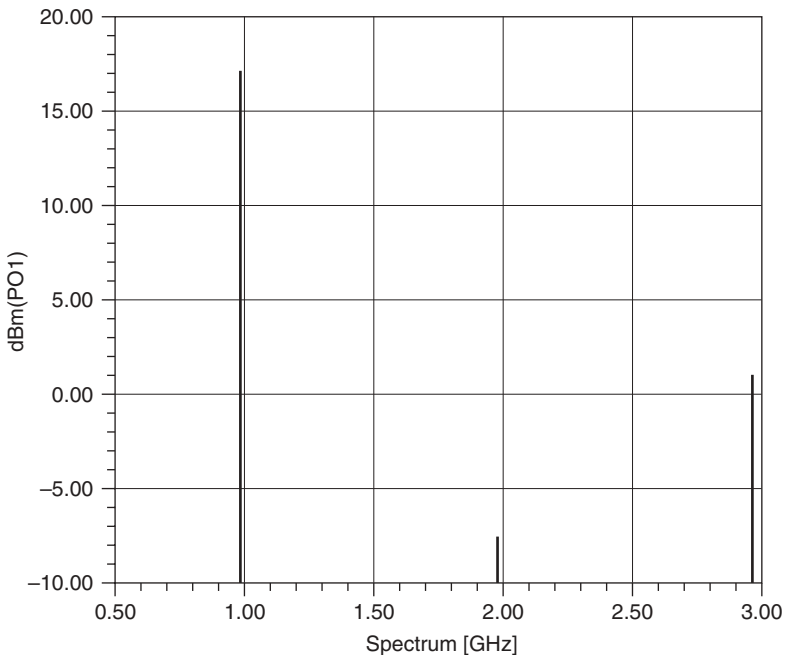
FIGURE 10.169   Simulated output power of the oscillator shown in Figure 10.164.

output is 17.04 dBm, which is about the same as the measured value given else where [10.68]. The dc-to-RF conversion efficiency at the fundamental frequency is 55%. The calculation in Ref. 10.68, as well as the calculation here, assumes an ideal transistor. By finding a better value between C_1 and C_2, the efficiency was increased to 64%, compared to the published result of 55%. This could mean that the circuit in Ref. 10.68 was not properly optimized.

Taking the published experimental results [10.68] into consideration, the analytical expression gives excellent insight into the performance of the oscillator circuit.

The maximum achievable output power and efficiency for a given active device can be predicted through the closed-form expressions without the need of a large-signal device characterization and an HB simulation. The publication [10.68] has not addressed the power optimization and best phase noise, which is a very important requirement for the oscillator. By proper selection of the feedback ratio at the optimum drive level, the noise is improved by 8 dB, keeping the output power approximately the same.

10.18.7 Synthesizers

While beyond the scope of this book, because of its substantial material, it needs to be mentioned that these oscillators are typically part of an oscillator. The book *Microwave and Wireless Synthesizers: Theory and Design* by U. L. Rohde (2000, Wiley) covers this material in great detail and is highly recommended for this topic.
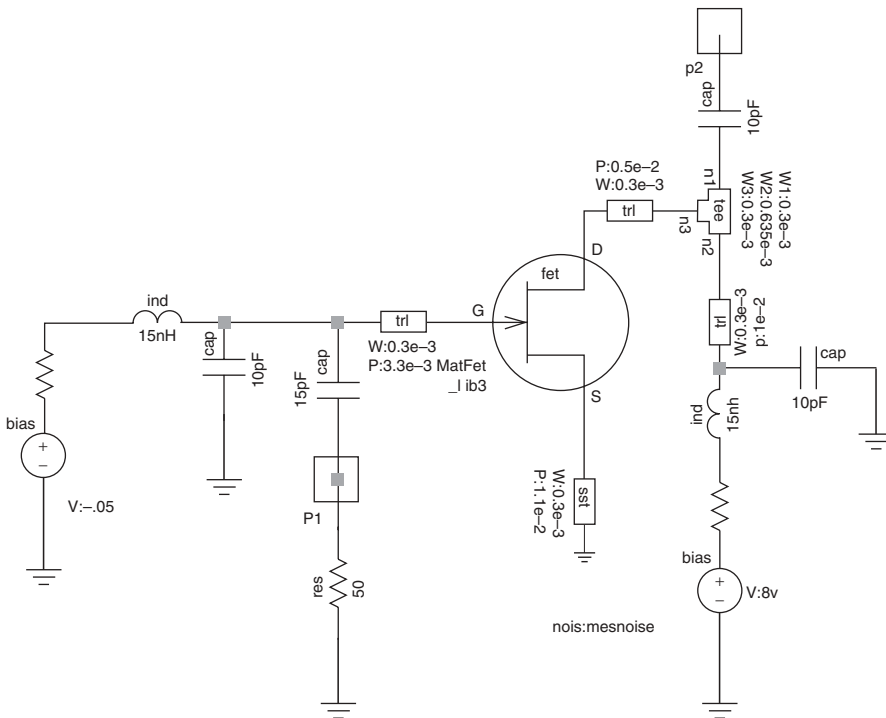
FIGURE 10.170   Schematic of the self-oscillating mixer.
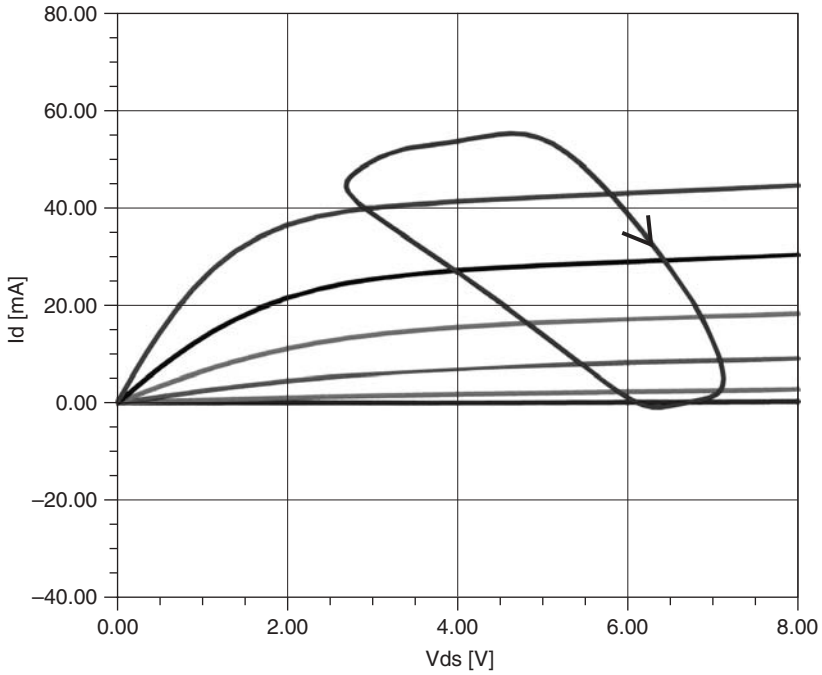
FIGURE 10.171   Load line in the oscillator mode of the self-oscillating mixer.
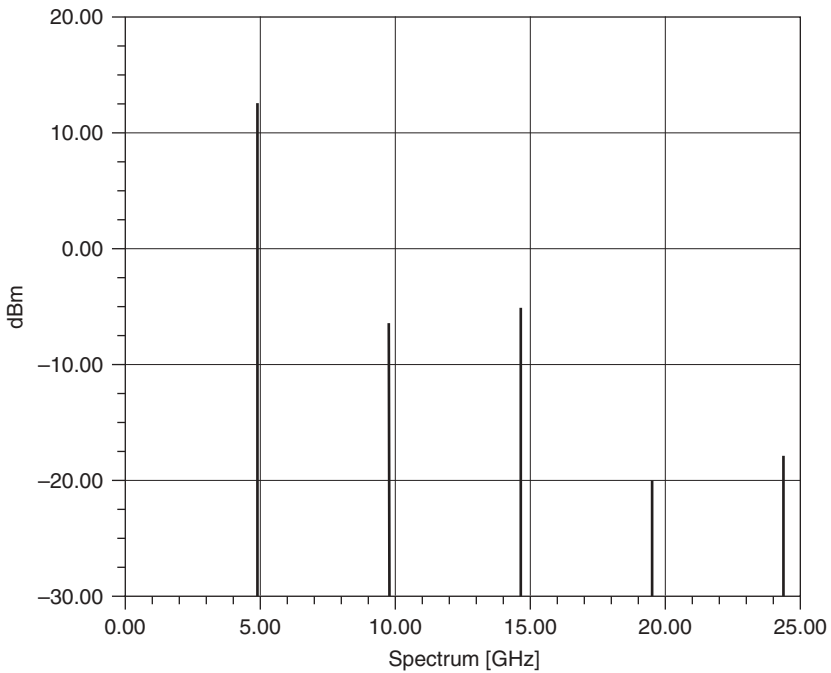
FIGURE 10.172   RF power of the self-oscillating mixer.
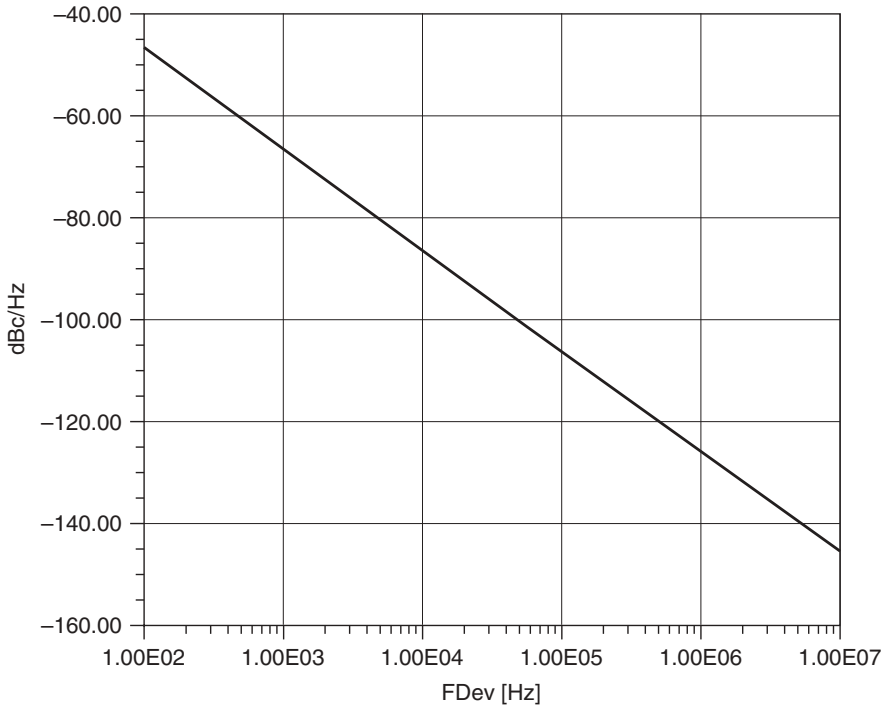
FIGURE 10.173   Predicted phase noise of the self-oscillating mixer.

10.18.8   Self-Oscillating Mixer

This section deals with mixers and a particularly interesting application is a mixer which is also an oscillator. The drawback of these circuits is the pulling of the frequency when a large signal is added.

Figure 10.170 shows the schematic of such a self-oscillating mixer. The transmission lines at the gate source and drain are responsible for the instability-causing oscillation and the RF signal is fed in at the point P_1. A straightforward analysis of the Ansoft Designer shows the operating point in Figure 10.171. The load line for the oscillator/mixer is a deformed circle. The deformation comes from the asymmetrically stored energy. The output power of the oscillator portion is 12 dBm and is shown in Figure 10.172. The resulting phase noise is shown in Figure 10.173. Since the oscillator transistor is a GaAs FET, the flicker noise contribution is very high and the total noise is not very good. These types of circuits are infrequently used but are shown as a handover to the following mixer chapter.

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PROBLEMS

10.1 The *S* parameters are given below for a HXTR-5001 silicon bipolar transistor, including parasitic bonding inductances ($L_B = 0.3$ nH, $L_E = 0.1$ nH). Design an oscillator at 5 GHz which delivers power to a 50-Ω load. Design the dc bias circuit. Give the complete RF and dc schematic. Assume that a 28-V dc supply is available.

S parameters at $f = 5.0$ GHz ($V_{CE} = 18$ V, $I_C = 30$ mA)

Oscillator	S_{11}	S_{21}	S_{12}	S_{22}	k
Common emitter	$0.54\underline{/167°}$	$1.45\underline{/52°}$	$0.120\underline{/44°}$	$0.49\underline{/42°}$	1.41
Common base	$0.83\underline{/141°}$	$1.58\underline{/-87°}$	$0.162\underline{/115°}$	$1.10\underline{/-53°}$	−0.45

10.2 The *S* parameters of the NE567 bipolar transistor are given for the common-emitter and common-base oscillators ($V_{CE} = 10$ V, $I_{CE} = 40$ mA), $f = 8$ GHz.
   (a) Design a common-emitter oscillator with a power-out collector.
   (b) Design a common-base oscillator with a power-out collector.

Common Emitter		Common Base	
$0.85\underline{/117°}$	$0.142\underline{/88°}$	$1.32\underline{/88°}$	$0.595\underline{/99°}$
$0.87\underline{/24°}$	$0.68\underline{/-59°}$	$1.47\underline{/172°}$	$1.03\underline{/-96°}$

$$S = \begin{bmatrix} 0.85\underline{/117°} & 0.142\underline{/88°} \\ 0.87\underline{/24°} & 0.68\underline{/-59°} \end{bmatrix} \quad S = \begin{bmatrix} 1.32\underline{/88°} & 0.595\underline{/99°} \\ 1.47\underline{/172°} & 1.03\underline{/-96°} \end{bmatrix}$$

$k = 0.33$ $\qquad\qquad\qquad$ $k = 0.24$
$G_{ms} = 7.9$ dB $\qquad\qquad$ $G_{ms} = 3.9$ dB

Use lumped elements for these designs.

10.3 Design a common-base bipolar oscillator at 4 GHz using lumped elements.

$$S = \begin{bmatrix} 0.707\underline{/-30°} & 0.35\underline{/45°} \\ 1.414\underline{/45°} & 0.50\underline{/-60°} \end{bmatrix} \qquad \begin{aligned} V_{CE} &= 10 \text{ V} \\ I_C &= 10 \text{ mA} \\ (h_{FE})_{min} &= 30 \end{aligned}$$

If the supply voltage is 15 V, give the dc bias circuit. Draw a complete RF and dc schematic.

10.4 The S parameters of a common-base bipolar transistor are given and the input resonator has been selected. Design the load circuit for an oscillator ($f = 10$ GHz) using distributed elements.

$$S = \begin{bmatrix} \sqrt{2}\underline{/90°} & 0.707\underline{/90°} \\ \sqrt{2}\underline{/180°} & 1\underline{/-90°} \end{bmatrix} \qquad \Gamma_G = 1\underline{/-90°}$$
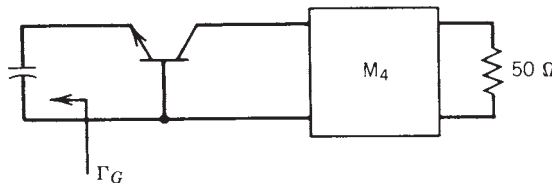
10.5 Design an oscillator using a common-collector NE219 bipolar transistor at $f = 4$ GHz, $V_{CE} = 8$ V, $I_{CE} = 40$ mA.

$$S = \begin{bmatrix} 0.91\underline{/-135°} & 0.67\underline{/-30°} \\ 1.41\underline{/-90°} & 0.60\underline{/90°} \end{bmatrix} \qquad k = 0.389$$

Give the RF design and schematic using lumped elements (ignore dc design).

10.6 A common-collector NEC 645 bipolar transistor (*npn*) was selected for an oscillator design at $f = 10$ GHz, $V_{CE} = 8$ V, $I_{CE} = 20$ mA. The power supply is $+15$ V.

$$S_{11} = 0.56\underline{/92°} \qquad S_{12} = 0.89\underline{/-119°} \qquad k = 0.49$$
$$S_{21} = 0.92\underline{/177°} \qquad S_{22} = 0.47\underline{/-56°}$$

Draw the complete RF and dc schematic using 50-Ω microstripline elements for the RF design.

10.7 Given S parameters of a common-source FET at $f = 6$ GHz,

$$S = \begin{bmatrix} 0.95\underline{/-45°} & 0.25\underline{/45°} \\ 1.414\underline{/45°} & 0.50\underline{/-45°} \end{bmatrix} \qquad \begin{array}{l} V_{DD} = 12 \text{ V} \\ V_{DS} = 6 \text{ V} \\ V_{GS} = -1 \text{ V} \\ I_{DS} = 10 \text{ mA} \end{array}$$

(a) Calculate k.
(b) Give the RF design of an oscillator with a 50-Ω load; use lumped elements.
(c) Give the dc design.
(d) Prepare a complete schematic.

10.8 Given the S parameters of a common-source or common-gate GaAs FET at $f = 12$ GHz (DXL-2502A chip).

FET	S_{11}	S_{21}	S_{12}	S_{22}	k
Common source	$0.52\underline{/-139°}$	$1.47\underline{/60°}$	$0.039\underline{/140°}$	$0.75\underline{/-40°}$	2.44
Common gate	$0.32\underline{/155°}$	$1.38\underline{/-75°}$	$0.226\underline{/50°}$	$1.19\underline{/-34°}$	-0.12

Design an oscillator using distributed 50-Ω microstripline elements which delivers power to a 50-Ω load. Assuming a $+15$-V power supply, design the dc bias network for the operating point

$$I_{DS} = 0.30 \text{ A} \qquad V_{DS} = 6.0 \text{ V} \qquad V_{GS} = -1.0 \text{ V}$$

Finally, draw the entire oscillator schematic (RF and dc).

10.9 Given the following S parameters of a common-source GaAs MESFET at 2 GHz:

$$S_{11} = 0.93\underline{/-43°} \qquad k = 0.53$$
$$S_{21} = 2.72\underline{/146°} \qquad V_{DS} = 5.0 \text{ V}$$
$$S_{12} = 0.022\underline{/69°} \qquad I_{DS} = 40 \text{ mA}$$
$$S_{22} = 0.77\underline{/-9°} \qquad V_{GS} = -2 \text{ V}$$
$$V_{DD} = +12 \text{ V}$$

Data on stability circles at 2 GHz:

Γ_G Plane			Γ_L Plane		
Center	Radius	Stable Region	Center	Radius	Stable Region
$1.10\underline{/50°}$	0.17	Outside	$1.60\underline{/38°}$	0.83	Outside

(a) Design an oscillator that delivers power from the drain–source port to a 50-Ω load.
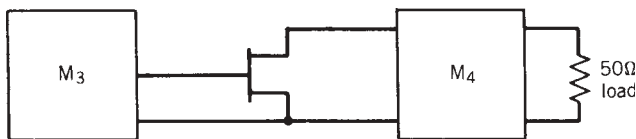
(b) Design the dc bias circuit.

(c) Draw the complete RF and dc circuit schematic.

10.10 Use a silicon varactor diode modeled by

$$C = C_{min} \left(\frac{V_B + \phi}{V_R + \phi} \right)^{\gamma}$$

where

$$\phi = 0.7 \text{ V (for Si)} \qquad V_B = 20 \text{ V}$$

$$\gamma = 0.71 \qquad\qquad V_R = \text{reverse voltage applied}$$

$$C_{min} = 0.35 \text{ pF}$$

The capacitance versus voltage is shown on the following plot, which shows a capacitance range of better than $10:1$ over 0.7 to 20.7 V. Design a 2- to 6-GHz circuit with this diode and the silicon bipolar transistor shown below. Suggested topology: a common base with varactor at input port.
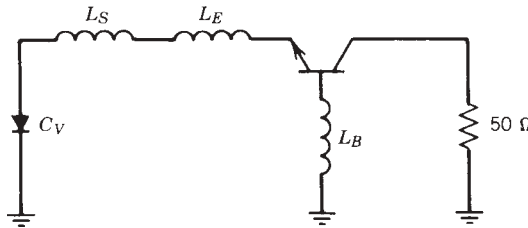
	S_{11}		S_{21}		S_{12}		S_{22}	
Frequency (GHz)	Magni-tude	Angle	Magni-tude	Angle	Magni-tude	Angle	Magni-tude	Angle
0.1	0.56	−60	39.07	152	0.009	69	0.87	−18
0.5	0.54	−145	15.00	104	0.023	56	0.49	−28
1.0	0.54	−170	8.03	90	0.033	65	0.42	−23
1.5	0.55	179	5.30	82	0.045	72	0.41	−22
2.0	0.56	170	4.04	76	0.058	75	0.41	−23
2.5	0.56	165	3.24	72	0.070	78	0.40	−23
3.0	0.58	159	2.75	65	0.083	79	0.40	−25
3.5	0.59	154	2.37	62	0.096	82	0.41	−26
4.0	0.60	149	2.06	57	0.108	83	0.42	−28
4.5	0.61	145	1.87	53	0.124	84	0.42	−33
5.0	0.62	142	1.67	49	0.136	83	0.43	−36
5.5	0.64	137	1.54	44	0.150	85	0.42	−40
6.0	0.65	134	1.40	41	0.165	84	0.44	−45

S parameters, CE AT-41400, silicon bipolar transistor chip ($V_{CE} = 8$ V, $I_C = 25$ mA, $L_B \approx 0.5$ nH, $L_E \approx 0.2$ nH).

10.11 Design a wide-band buffered VCO using the AT-10600 FET at 6 to 12 GHz. The perfect varactor would be

$$C = C_{\min} \left(\frac{V_B + \phi}{V_R + \phi} \right)^{\gamma}$$
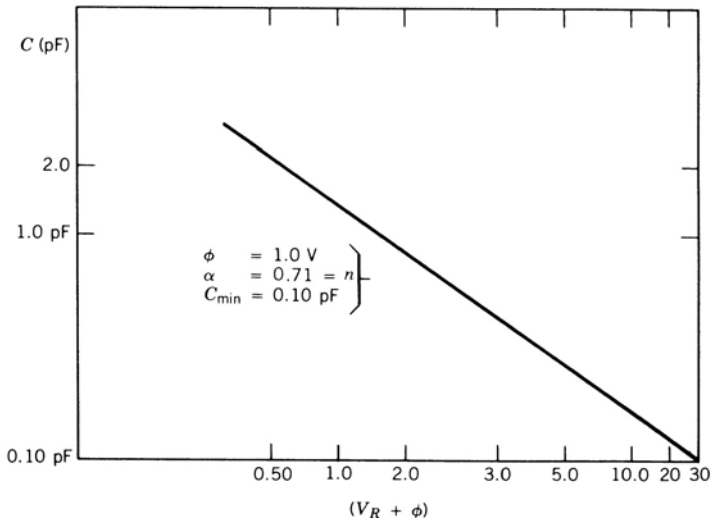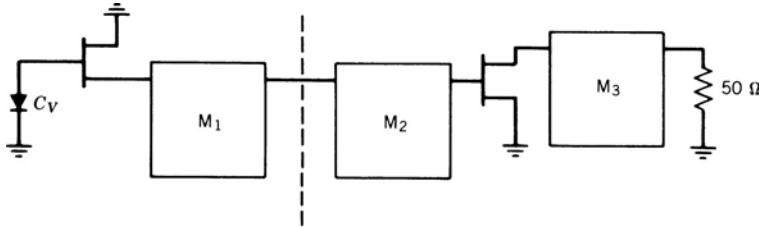
where

$$\gamma = 0.71 \qquad V_B = 30 \text{ V}$$

$$C_{\min} = 0.10 \text{ pF} \qquad \phi = 1.0 \text{ (for GaAs)}$$

Suggested topology: a common-drain oscillator and common-source amplifier. Use 3 V, 10 mA for the oscillator; 5 V, 30 mA for the amplifier. Give the tuning voltage versus frequency curve.

Typical scattering parameters, common source ($V_{DS} = 3$ V, $I_{DS} = 10$ mA):

Frequency (GHz)	S_{11} Magnitude	S_{11} Angle	S_{21} dB	S_{21} Magnitude	S_{21} Angle	S_{12} dB	S_{12} Magnitude	S_{12} Angle	S_{22} Magnitude	S_{22} Angle
5.0	.90	−47	6.9	2.22	131	−21.5	.084	69	.61	−13
6.0	.86	−59	7.1	2.27	120	−19.9	.101	64	.57	−17
7.0	.80	−72	7.2	2.29	110	−18.6	.117	59	.52	−23
8.0	.74	−83	7.3	2.32	100	−17.7	.130	54	.48	−28
9.0	.68	−97	7.3	2.33	89	−16.9	.143	48	.43	−36
10.0	.61	−114	7.3	2.31	77	−16.1	.156	42	.38	−46
11.0	.55	−133	7.1	2.27	66	−15.6	.166	35	.33	−56
12.0	.52	−153	6.8	2.18	54	−15.2	.174	28	.28	−66
13.0	.49	−174	6.4	2.10	44	−14.9	.180	21	.24	−78

Typical scattering parameters, common source ($V_{DS} = 5$ V, $I_{DS} = 30$ mA):

Frequency (GHz)	S_{11} Magnitude	S_{11} Angle	S_{21} dB	S_{21} Magnitude	S_{21} Angle	S_{12} dB	S_{12} Magnitude	S_{12} Angle	S_{22} Magnitude	S_{22} Angle
5.0	.81	−59	9.7	3.05	124	−25.8	.051	76	.65	−11
6.0	.74	−72	9.5	2.98	112	−24.7	.058	74	.62	−14
7.0	.68	−86	9.1	2.86	101	−23.4	.068	72	.60	−18
8.0	.63	−100	8.9	2.80	91	−22.5	.075	70	.57	−22
9.0	.56	−113	8.8	2.76	82	−21.7	.082	69	.55	−26
10.0	.51	−130	8.4	2.62	72	−20.6	.096	68	.53	−30
11.0	.46	−143	8.0	2.52	62	−20.0	.100	66	.51	−40
12.0	.42	−156	7.8	2.45	54	−19.6	.105	64	.47	−49
13.0	.41	−168	7.5	2.37	46	−18.9	.114	60	.46	−54

10.12 Find Γ_L and S'_{22} for the 15.6-GHz oscillator shown below. Also find Γ_G and S'_{11} for the oscillator; assume a common-base configuration.
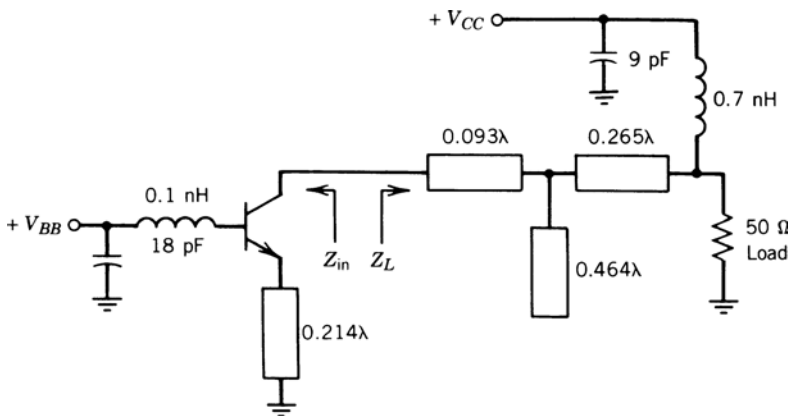
CHAPTER 11

MICROWAVE MIXER DESIGN

11.1 INTRODUCTION

For many years the key element in receiving systems has been the crystal detector or diode mixer. At the beginning of the twentieth century, RF detectors were crude, consisting of a semiconductor crystal contacted by a fine wire ("whisker"), which had to be adjusted periodically so that the detector would keep functioning. With the advent of the triode, a significant improvement in receiver sensitivity was obtained by adding amplification in front of and after the detector. A real advance in performance came with the invention by Edwin Armstrong of the superregenerative receiver. Armstrong was also the first to use a vacuum tube as a frequency converter (mixer) to shift the frequency of an incoming signal to an intermediate frequency (IF), where it could be amplified and detected with good selectivity. The superheterodyne receiver, which is the major advance in receiver architecture to date, is still employed in virtually every receiving system.

The development of microwave mixers was fostered during World War II with the development of radar. At the beginning of the war, single-diode mixers exhibited poor noise figure performance; but, by the end of the 1950s, system noise figures of 7 dB could be obtained. Today, single-diode mixers exhibit this type of performance at frequencies in excess of 200 GHz. The burden of establishing receiver sensitivity and dynamic range is still largely dependent on the mixer throughout the upper microwave and millimeter-wave frequency range. Below 100 GHz, low-noise GaAs FET amplifiers are being used to improve the system noise figure, but above this frequency, the diode is almost the only device that can be used for low-noise frequency conversion amplifications.
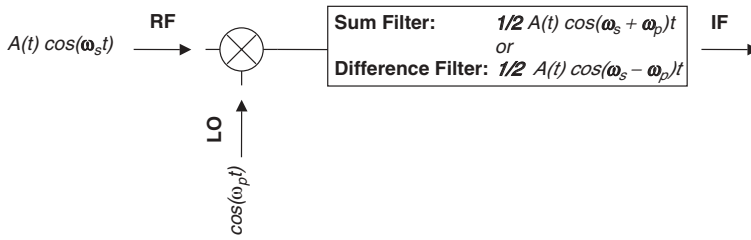
FIGURE 11.1   Ideal multiplier model showing both up- and down-converter performance.

The mixer, which can consist of any device capable of exhibiting nonlinear performance, is essentially a multiplier or a chopper. That is, if at least two signals are present, their product will be produced at the output of the mixer. This concept is illustrated in Figure 11.1. The RF signal applied has a carrier frequency of ω_s with modulation $M(t)$, and the local oscillator signal (LO or pump) applied has a pure sinusoidal frequency of ω_p. From basic trigonometry we know that the product of two sinusoids produces a sum and difference frequency.

For example, the voltage-current relationship for a diode can be described as an infinite power series,

$$I = a_0 + a_1 V + a_2 V^2 + a_3 V^3 + \cdots \tag{11.1}$$

where V is the sum of both input signals and I is the total signal current. If the RF signal is substantially smaller than the LO signal and modulation is ignored, the frequency components of the current I are

$$\omega_d = n\omega_p \pm \omega_s \tag{11.2}$$

As mentioned above, the desired component is usually the difference frequency $|\omega_p - \omega_s|$ or $|f_p - f_s|$, but sometimes the sum frequency $(f_s + f_p)$ is desired when building an up converter or a product related to a harmonic of the LO can be selected.

A mixer can also be analyzed as a switch that is commutated at a frequency equal to the pump frequency ω_p. This is a good first-order approximation of the mixing process for a diode since it is driven from the low-resistance state (forward bias) to the high-resistance state (reverse bias) by a high-level LO signal.

A mixer can also be analyzed as a switch that is commutated at a frequency equal to the pump frequency ω_p. This is a good first-order approximation of the mixing process for a diode, since it is driven from the low-resistance state (forward bias) to the high-resistance state (reverse bias) by a high-level LO signal. The simplified diode model is shown in Figure 11.2. With this switching action in mind, a single-ended mixer can be represented by the circuit shown in Figure 11.3a. In this example, the RF signal appearing at the IF load is interrupted by the switching action of the diode, which is caused by the pump. From the modulation theorem it can be shown that the sum and difference frequencies, as well as many other products, appear at the IF port. It should be remembered that a dc component is also present and must not be suppressed in a physical diode mixer if proper operation is to be obtained. The circuit shown in Figure 11.3b is equivalent to a double-balanced mixer. In this instance, the time average of the RF signal and the LO dc component does not appear at the IF
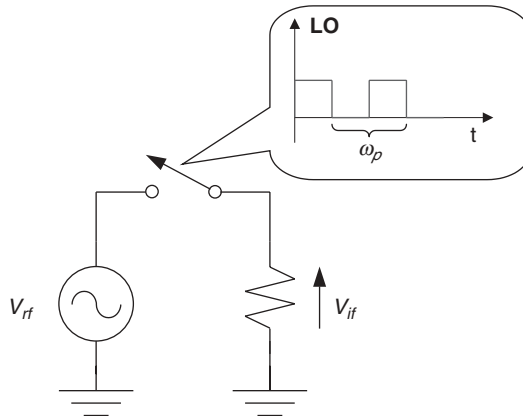
FIGURE 11.2   Single-ended mixer employing diode switching model.
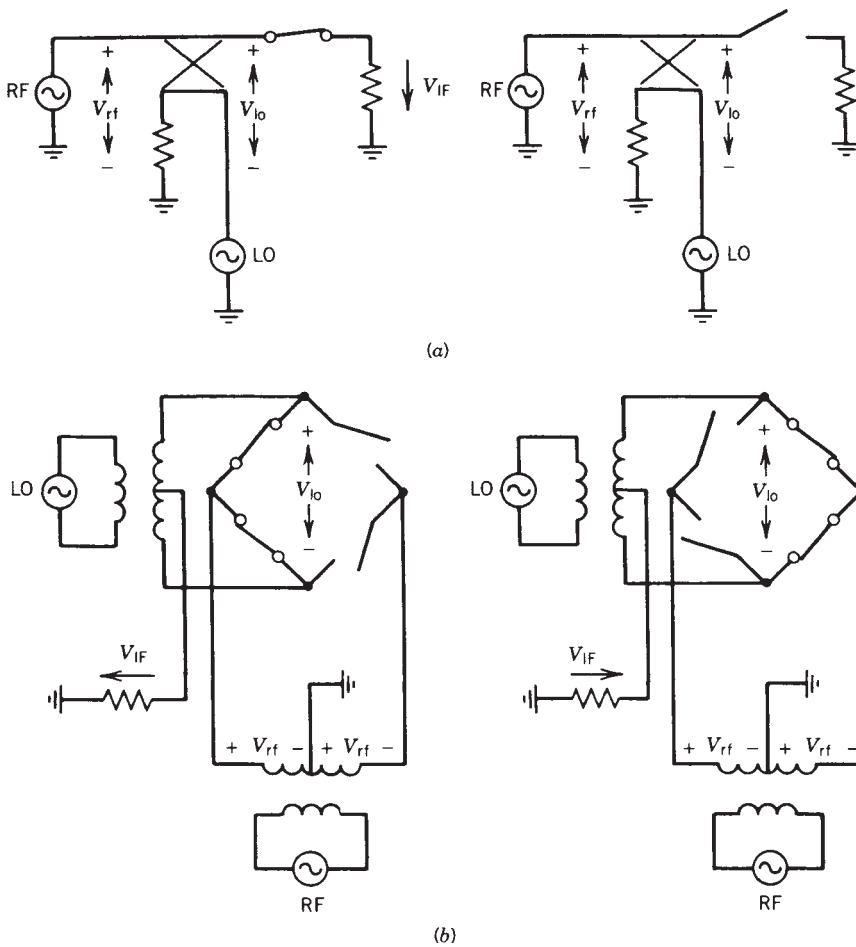
FIGURE 11.3   Typical mixer circuits employing diode switching model depicting IF voltage (or current) as a function of LO polarity; (*a*) single-ended mixer; (*b*) double-balanced mixer.

port. Since there is no LO dc component in the LO waveform, there is no switching product at the LO port with the frequency component of the fundamental RF signal. Hence the mixer also has LO-to-RF port isolation without requiring filters as in the single-ended case.

The concept of the switching mixer model can also be applied to FETs when used as voltage-controlled resistors. In this mode, the drain-to-source resistance can be changed from a few ohms to many thousands of ohms simply by changing the gate-to-source potential. At frequencies below 1 GHz, virtually no pump power is required to switch the FET, and since no dc drain bias is required, the resulting FET mixer is passive. However, as the operating frequency is raised above 1 GHz, passive FET mixers require LO drive powers comparable to diode or active FET designs.

Regardless of the nonlinear or switching elements employed, mixers can be divided into several classes: (1) single ended, (2) single balanced, or (3) double balanced. Depending on the application and fabrication constraints, one topology can exhibit advantages over the other types. The simplest topology (Fig. 11.4a) consists of a single diode and filter networks. Although there is no isolation inherent in the structure (balance), if the RF, LO frequency, and IF are sufficiently separated, the filter (or diplexer) networks can provide the necessary isolation. In addition to simplicity, single-diode mixers have several advantages over other configurations. Typically, the best conversion loss is possible with a single device, especially at frequencies where balun or transformer construction is difficult or impractical. Local oscillation requirements are also minimal since only a single diode is employed and dc biasing can easily be accomplished to reduce drive requirements further. The disadvantages of the topology are (1) sensitivity to terminations, (2) no spurious response suppression, (3) minimal
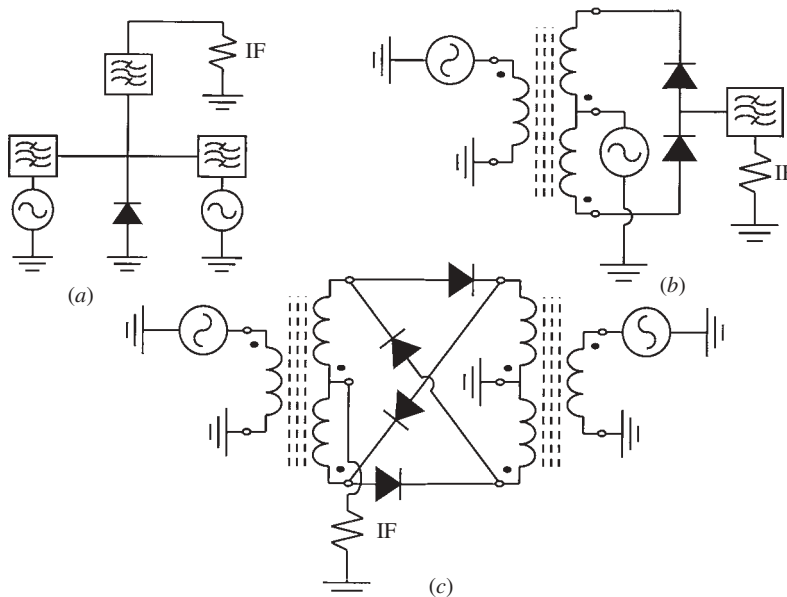
FIGURE 11.4   Common mixer topologies: (*a*) single ended; (*b*) single balanced; (*c*) double balanced.

TABLE 11.1   Mixer Topology Performance Considerations

Parameter	Single Ended	Single Balanced	Double Balanced
Conversion gain	High	Moderate	Low
Spurious performance	None	Moderate	High
Dynamic range	Low	Moderate	High
Isolation	None	Moderate	High
Pump power	Low	Moderate	High
Complexity	Low	Moderate	High
Bandwidth	Narrow	Wide	Wide

tolerance to large signals, and (4) narrow bandwidth due to spacing between the RF filter and mixer diode.

The next topology commonly used is the single-balanced structure shown in Figure 11.4b. These structures tend to exhibit slightly higher conversion loss than that of a single-ended design, but since the RF signal is divided between two diodes, the signal power-handling ability is better. However, more diodes require more LO power. Since the structure is balanced, some isolation between ports is obtained and there is some spurious suppression for RF or LO products, depending on which is balanced.

The double-balanced structure is the topology most commonly employed between 2 and 18 GHz. It exhibits the best large signal-handling capability, port-to-port isolation, and spurious rejection. Alas, double-balanced mixers usually exhibit the poorest conversion loss characteristics and require the most LO drive. However, in strong signal environments such as the EW arena, spurious rejection and large-signal performance usually outweigh the 1 dB or so loss in sensitivity. Some high-level mixer designs can employ multiple-diode rings with several diodes per leg in order to achieve the ultimate in large-signal performance. Such designs can easily require hundreds of milliwatts of pump power. A general performance comparison for various mixer topologies is shown in Table 11.1. It should be noted that these performance traits are quite general and are highly dependent on balun design, diode quality, and operating frequency.

11.2   DIODE MIXER THEORY

The simple metal–semiconductor junction, first investigated by Braun in 1874, exhibits a nonlinear impedance as a function of voltage, making it an ideal candidate for mixer applications. Although other semiconductor junctions, such as the p–n junction, also exhibit nonlinear behavior, the metal–semiconductor diode (Schottky barrier) is primarily a majority-carrier device, making it essentially free of minority-carrier effects such as reverse recovery time problems and high charge storage capacitance. Because of the inherently low junction capacitance and high switching speed, Schottky diodes [11.1], typically the point contact type, operate well into the millimeter-wave frequency range with cutoff frequencies exceeding 2000 GHz. Most practical diodes employ either Si (silicon) or GaAs (gallium arsenide) as the semiconductor material, with the most common metals being Cu (copper), Pt (platinum), Ag (silver), Al (aluminum), Ti (titanium),

and Au (gold). Since n-type GaAs exhibits a mobility many times greater than that of p-type material, n-type structures using Pt, Au, or Ti are most prevalent.

There have been many models explaining the operation of metal–semiconductor junctions, but the original model described by W. Schottky in 1942 [11.2] has endured and amply describes diode operation. As mentioned above, diode operation is based on majority-carrier injection into the metal (anode) from the semiconductor (cathode), made possible because of free electrons present in the doped semiconductor. Diode operation is easily illustrated by first considering the metal and semiconductor properties separately and then combining the two.

Figure 11.5 depicts various energy levels for both the isolated metal and n-type semiconductor at equilibrium. From the electron gas theory for metals, we know that the average energy to remove an electron from the Fermi level and place it at rest in free space is $e\psi_m$, where ψ_m is the thermionic or vacuum work function. Values for ψ_m are on the order of several volts and are unique for each metal. However, the work function can vary depending on the metal surface conditions. Similarly, a work function ψ_s exists for the semiconductor, which not only is a function of surface conditions but also is influenced by the position of the Fermi level ψ_{fs}, which is dependent on doping level. The quantities ψ_v and ψ_c denote the positions of the valance and conduction band energy levels. Depending on the distribution and type of surface states of the semiconductor, a net positive or negative charge may exist at the surface, thus distorting the conduction and valance band energy levels, as shown in Figure 11.5b. The energy required to remove an electron from the conduction band to free space is e_χ, where χ is the electron affinity, which is a constant for each material and does not vary with doping level.

As the metal and semiconductor, which are joined by an external conductor, are brought together, a shift in energy levels must occur because equilibrium must be maintained for the combined system. Thus, from thermodynamics, the Fermi levels for both the metal and semiconductor must then coincide. Hence a potential difference Δ between the metal and semiconductor, due to the difference between their work functions, will result. This is known as the barrier potential or contact potential and varies depending on the materials used. As δ becomes sufficiently small (at or near
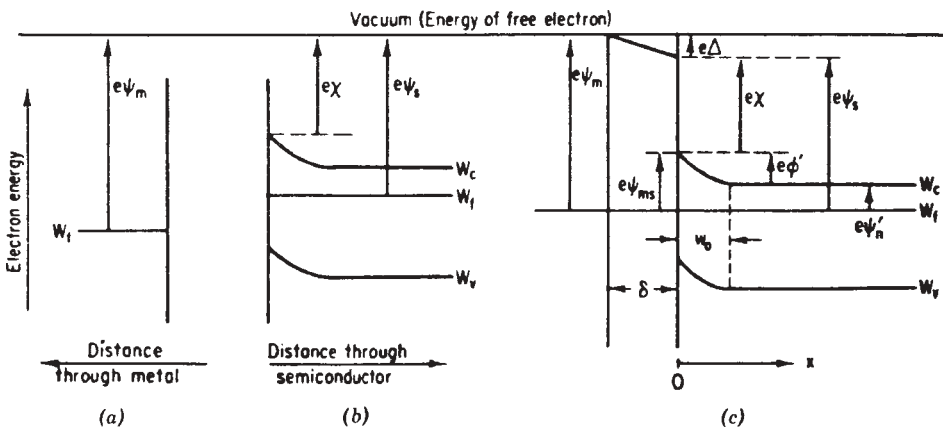
FIGURE 11.5   Energy levels for a metal and a semiconductor: (a) isolated metal; (b) isolated semiconductor; (c) metal and semiconductor in contact.

contact), charge will be transferred between the two materials. In this case, electrons will be transferred from the semiconductor to the metal because of its lower Fermi level, leaving behind a positively charged depletion region and creating a negatively charged metal surface; hence a junction capacitance is created via the contact potential.

However, it should be remembered that the barrier height, which is defined as

$$\psi_{ms} = \psi_m - X' \tag{11.3}$$

where $X' = X - \Delta$, is not predicted by the original Schottky theory, since surface states, which imply that W is nonzero, were not considered. With this assumption the barrier height would be simply the difference between ψ_m and X. This is the case when the surface state density is very low, but for materials such as GaAs, ψ_{ms} is almost metal independent but has a strong dependence on the surface state density. It should also be noted that the model above does not take into account image forces on the electron at the junction.

Several other characteristics of the junction can also be determined by solving Poisson's equation throughout the junction and depletion regions. The solution can begin by assuming that the charge density in the depletion region can be approximated by $\rho = eN_d$ for $x = 0$ to $x = w_0$ and zero elsewhere, where N_d is the donor density. The electric field, which is a simple triangle function, can be written as

$$E(x) = -\left(\frac{eN_d}{\varepsilon_s}\right)(w_0 - x) \tag{11.4}$$

The voltage across the junction can then be found by integrating the electric field and applying the boundary conditions at $x = 0$. At that point, we know that the voltage must then be equal to $-\phi_{bi}$. Hence the voltage can be written as

$$V(x) = \left(\frac{eN_d}{\varepsilon_s}\right)[w_0 x - (0,5)x^2] - \psi_{ms} \tag{11.5}$$

It can then be shown that the quantity ϕ_{bi}, which is the degree of band bending in the semiconductor (built-in potential), can be related to the depletion width as

$$\phi_{bi} = \frac{eN_d w_0^2}{2\varepsilon_s} \tag{11.6}$$

When a voltage V is applied to the diode (Fig. 11.6), Eq. (11.6) is still valid provided that ϕ_{bi} is replaced by $\phi_{bi} - V$ and w_0 is replaced by w. Hence the depletion width is a function of applied voltage. Diode conduction properties can also be illustrated by examining Figure 11.6.

During forward-bias conditions, the barrier height is lowered by an amount equal to the applied voltage. Thus it becomes easier for electrons to travel from the n-type semiconductor to the metal. However, the potential barrier for electrons traveling in the reverse direction is unaffected. The greater the applied voltage, the easier it becomes for forward charge flow and the thinner the depletion region becomes. When reverse bias is applied, the potential barrier for forward-traveling electrons becomes large; hence there is a small probability that an electron with sufficient thermal energy will cross the junction.
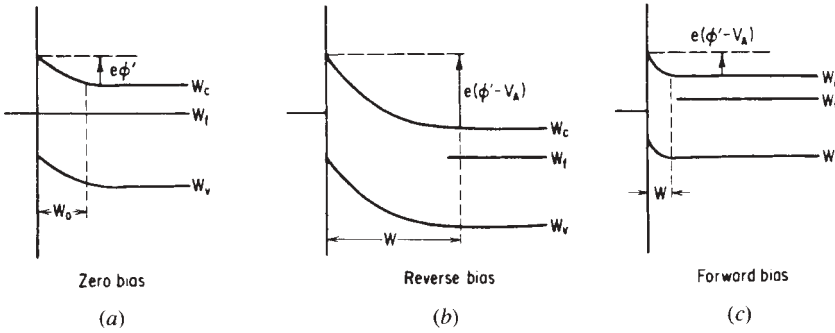
FIGURE 11.6 Energy-level diagram of Schottky barrier as a function of applied bias: (*a*) zero bias; (*b*) reverse bias; (*c*) forward bias.

The capacitance of the diode is also a function of applied voltage and can be found by first determining the total junction charge, which is $eN_d \times A$ (area) $\times w$ (depletion width). Using the relation

$$w = \left(\frac{2(\phi_{bi} - V)\varepsilon_s}{eN_d} \right)^{1/2} \tag{11.7}$$

$$Q = \text{junction charge} = [2(\phi_{bi} - V)eN_d\varepsilon_s]^{1/2} \qquad \text{A} \tag{11.8}$$

Then, by taking the partial derivative of the charge Q with respect to the applied voltage, the capacitance becomes

$$C(V) = A \left(\frac{q\varepsilon_s N_d}{2(\phi_{bi} - V)} \right)^{1/2} \tag{11.9}$$

which can be put in the form

$$C(V) = \frac{C_{j0}}{(1 - V/\phi_{bi})^{1/2}} \tag{11.10}$$

where C_{j0} is the capacitance at zero bias.

The current–voltage relationship for the metal–semiconductor diode can be derived from a variety of theories which lead to the same basic exponential relationship. The model formulated by Bethe [11.3], called the diode or thermionic emission model, assumes that the junction depletion region is small and electrons do not suffer collisions when traversing the junction. Hence the charge carriers are affected primarily by the barrier potential and traverse the junction only if the carriers possess sufficient thermal energy (velocity) to overcome the barrier height. It is also assumed that at zero bias equal numbers of electrons cross the junction in both directions, yielding a net current of zero.

The other common approach to determining the diode's $I-V$ characteristics is based on the diffusion theory proposed by Schottky. In this approach, the depletion region length is assumed to be large and the charge carriers (electrons) suffer numerous collisions. Passage across the barrier is determined partly by diffusion and carrier concentrations are assumed to be independent of current.

As mentioned above, both approaches yield essentially the same $I-V$ relationship, which has the dominant characteristic

$$I(V) = I_0 \left[\exp\left(\frac{eV}{kT} \right) - 1 \right] \tag{11.11}$$

where k is Boltzmann's constant (1.37×10^{-23} J/K), T is the absolute temperature, and V is the applied voltage. However, to account for the nonideal behavior of real diodes, the ideal diode equation of (11.11) can be modified by adding the factor n to the relationship as follows:

$$I(V) = I_0 \left[\exp\left(\frac{eV}{nkT} \right) - 1 \right] \tag{11.12}$$

where n is a number close to unity, usually between 1.05 and 1.4. The factor n, sometimes called the diode ideality factor or slope parameter, can usually be selected so that the $I-V$ relationship obtained from (11.12) matches measured diode performance.

There are a variety of reasons why physical diodes do not follow the ideal diode equation, such as imperfections in fabrication and factors not included in either simple model. Some of these factors are (1) series resistance, (2) surface imperfections, (3) image forces, (4) edge effects, and (5) tunneling. The most important of these with respect to mixer performance is diode series resistance.

Unfortunately, the fabrication requirements for producing a Schottky barrier diode somewhat contradict the requirements for low series resistance, which is essential for optimum mixer performance. Generally, Schottky barriers require lightly doped semiconductors, but fabricating diode contacts with low series resistance requires highly doped material. Therefore, diodes are usually fabricated by growing a lightly doped epitaxial layer on top of a highly doped substrate to achieve the best junction versus ohmic contact performance. Series resistance is minimized, but there is still a contribution from the lightly doped epitaxial layer, which must be made thick enough to contain the depletion region during reverse-bias conditions. These conflicting requirements make it difficult to fabricate high-Q diodes using an ion implantation process, which is becoming very popular in the manufacture of high-volume MMICs.

RF skin resistance is the other main contributor to the total series resistance of the diode. This component of resistance cannot be measured at dc, as is most manufacturers' data, but must be measured at RF frequencies. The skin effects of connecting beams or wires further complicate measurements and estimates of the true value of R_s. The DeLoach [11.4, 11.5] method, described in Chapter 5, can be used to determine diode Q but cannot separate the values of C_j and R_s. However, by measuring or estimating C_j at low frequencies, a good approximation of R_s can be obtained.

Neither theory presented above includes the effects of image forces on the electrons in the depletion region. This force arises from the electron's negative charge, which is positively imaged in the metal, thus attracting charge carriers to the metal side of the junction, effectively lowering the barrier height. This phenomenon produces a voltage-dependent deviation from the ideal diode current characteristic.

Quantum mechanical tunneling can also cause charge carriers to traverse the junction by tunneling through the barrier. Tunneling is more prevalent at low temperatures,

where thermionic emission has been reduced, and, when doping levels are high, can sometimes degrade the noise performance of some mixers. Up to this point, imperfections in diode performance were attributed to material and fabrication quantities, with little regard to operating temperature. However, at commercial or military temperature ranges, diode characteristics change enough to affect mixer performance. As the temperature is lowered, the diode becomes more sensitive to applied voltage, with the diode knee increasing in voltage. If the LO power is marginal and no bias control is employed, large changes in conversion loss can occur. If LO power is varied as a function of temperature, mixer performance can be held constant, but in broadband designs, which are typically unbiased with wide variations in LO power as a function of frequency, the controlling of LO power as a function of temperature is completely impractical. Stable performance can be accomplished by overdriving the mixer diodes. This technique can usually limit mixer conversion loss variations to within 0.5 dB at any given frequency.

The junction capacitance of a diode remains essentially constant as a function of temperature but can increase slightly because of shifts in knee voltage. This may cause a slight degradation in conversion loss performance of a mixer at the low end of its temperature range. However, operation of a properly designed mixer at very low temperatures can result in extremely good noise figure performance. Mixers for very low noise radio-astronomy applications are commonly operated at cryogenic temperatures as low as 4.8 K.

Now that the junction current and capacitance characteristic are known, a large-signal model of the pumped diode can be formulated. As we have learned, when a diode is pumped with an LO signal, an infinite number of products, including a dc component, are generated. If a second signal is added, the simple set of LO and harmonic frequencies becomes much larger, since products of the signal and pump, as well as products that include harmonics of both frequencies, are generated. If we now assume that the signal amplitude is substantially smaller than the pump (LO), which is commonly the case, a small-signal mixing spectrum (Fig. 11.7) is generated [11.6]. It should be remembered that all mixing product frequencies exist in the diode and it does not matter which of the two signals is the larger. Short circuiting the diode at a particular mixing product frequency eliminates the product's voltage component across the diode terminals, but a current component can still exist. In a similar manner, open circuiting a voltage component of a mixing product across the diode terminals eliminates the current component, but the product's voltage is still present. However, it will be seen later that a performance difference will arise for a particular circuit application whether a mixing product is open circuited or short circuited.

We can now investigate the effects of pumping on junction current and capacitance and combine these effects to form both a large- and a small-signal diode model (Fig. 11.8). From Eq. (11.12) for diode current as a function of voltage, the $I-V$ relationship for the ideal diode component of the large-signal model is obtained, since that expression is valid for any junction voltage. Similarly, the expression for junction capacitance (11.9) was obtained from the charge in the depletion region by the relation

$$C(V) = \frac{dQ_d}{dV} \tag{11.13}$$
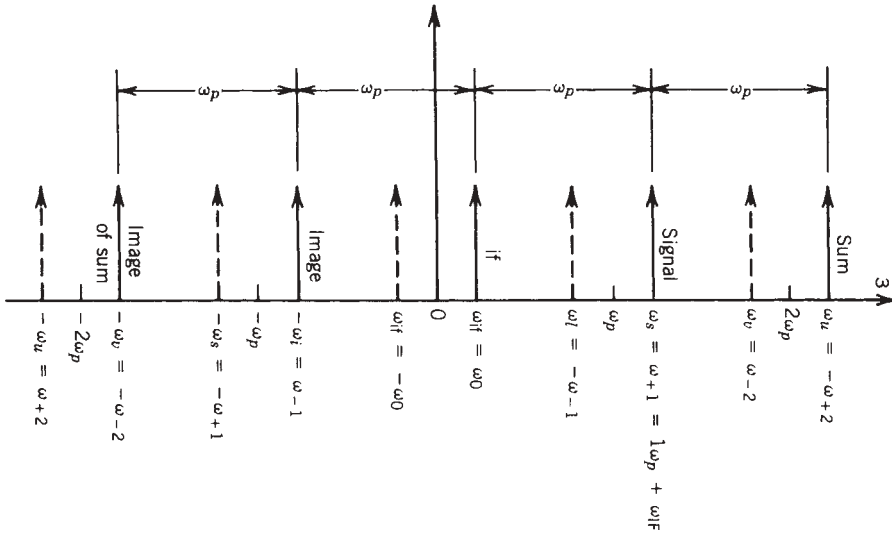
FIGURE 11.7   Modulation spectra for a pumped nonlinear element allowing for both positive and negative frequencies.
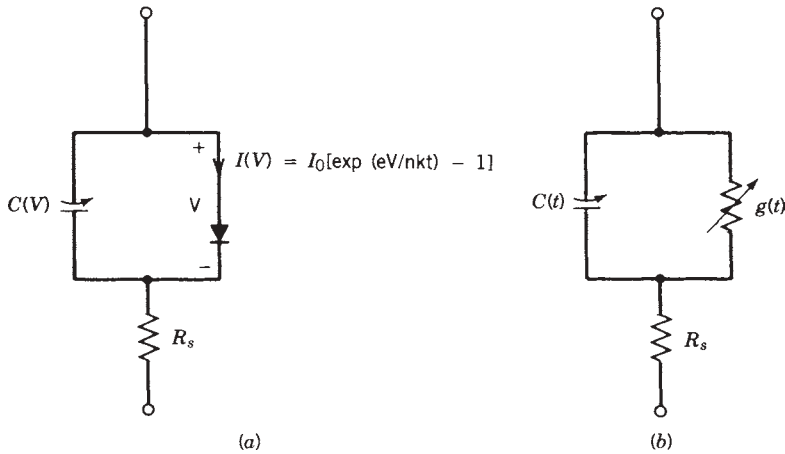
FIGURE 11.8   (*a*) Large-signal and (*b*) small-signal diode models.

The current in the capacitor is defined as

$$I_c(t) = \frac{dQ_d}{dt} = \frac{dQ_d}{dV}\bigg|_{V=V_j(t)} \frac{dV_j(t)}{dt} \tag{11.14}$$

$$= C(V_j(t))\left(\frac{dV_j(t)}{dt}\right) \tag{11.15}$$

where $V_j(t)$ is the large-signal junction voltage.

It is this quantity, $V_j(t)$, that must be determined prior to the solution of the small-signal problem. The solution for $V_j(t)$ must include the effects of the diode embedding network at both the pump frequency ω_p and its harmonics as well as at dc. The analysis assumes that the RF signal is negligible and circuit performance is determined solely by the LO or pump signal. A circuit representation of the LO analysis is shown in Figure 11.9 [11.7]. The circuit performance of the diode model and embedding network shown in the figure can also be described in terms of the Fourier coefficients [11.8–11.11] of the diode's junction voltage and circuit current as

$$V_j(t) = \sum_{k=-\infty}^{\infty} V_k e^{jk\omega pt} \tag{11.16}$$

where $V_k = V_{-k}^*$ and

$$I_e(t) = I_c(t) + I_d(t) = \sum_{k=-\infty}^{\infty} I_{ek} e^{jk\omega pt} \tag{11.17}$$

where $I_{ek} = I_{e-k}^*$. The circuit solution must also satisfy the boundary conditions. The first condition is best applied in the time domain and is imposed by the diode currents I_d and I_c. The second condition, which is imposed by the embedding network, can be described as

$$V_k = -I_{ek}[Z_e(k\omega_p) + R_s(k\omega_p)] \tag{11.18}$$

where $k = \pm1, \pm2, \ldots$. Equation (11.18) can then be written as

$$V_{\pm1} = V_p - I_{e\pm1}(Z_{10})$$
$$Z_{10} = Z_e(\pm\omega_p) + R_s(\pm\omega_p) \tag{11.19}$$
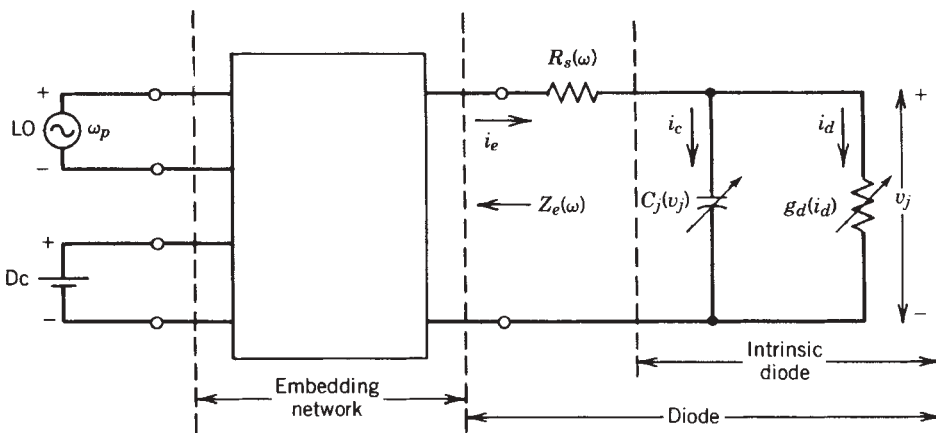
FIGURE 11.9 Equivalent circuit for mixer LO analysis with the large-signal diode model characterized in the time domain and the series resistance R_s and embedding network Z_e represented in the frequency domain.

at the pump frequency (ω_p), where V_p is the LO voltage, and as

$$V_0 = V_{dc} - I_{dc}[Z_e(0) + R_s(0)] \tag{11.20}$$

where V_{dc} is the dc bias voltage. The boundary conditions for the circuit relationships above are best applied in the frequency domain, where the embedding network, which is usually composed of linear lumped and distributed elements, is easily described by analytical functions not requiring differentiation or integration. However, to solve the harmonic balance diode/network problem efficiently, the number of LO harmonics must be truncated. Typically, a value of $n = 5$ provides a good compromise between execution speed and numerical efficiency.

Once the LO voltage waveform has been determined, a small-signal conductance and capacitance can be defined. The diode incremental conductance is obtained from the expression for current (11.12). Thus

$$g(t) = \frac{dI_d}{dV_j} = \frac{I_0}{nKT} \frac{eV_j(t)}{1} \exp\left[\frac{eV_j(t)}{nKT}\right] \simeq \frac{eV_j(t)}{nKT} I_d(t) \tag{11.21}$$

Hence the diode conductance presented to a small signal (RF) for any instant of time during the LO cycle can be found. Similarly, for a small-signal analysis, the junction capacitance can be treated as a linear time-variant capacitance. With this assumption,

$$C(t) = C(V_j(t)) \tag{11.22}$$

and

$$
\begin{aligned}
i_c(t) &= \frac{d[C(t)v(t)]}{dt} \\
&= C(t)\frac{dv(t)}{dt} + v(t)\frac{dC(t)}{dt}
\end{aligned}
\tag{11.23}
$$

where $v(t)$ is the small-signal junction voltage.

The mixing process in a diode mixer is due to the periodic modulation of junction conductance and reactance by the pump signal. Although the variation in diode conductance can change by several orders of magnitude during the LO cycle, the $3:1$ or $4:1$ variation in capacitive reactance that occurs can still influence mixer performance and must be included in the small-signal analysis.

As in the large-signal model, the small-signal admittance components can be expressed by their Fourier coefficients. Thus

$$g_d(t) = \sum_{k=-\infty}^{\infty} G_k e^{jk\omega pt} \tag{11.24}$$

$$c_j(t) = \sum_{k=-\infty}^{\infty} C_k e^{jk\omega pt} \tag{11.25}$$

and

$$i_d(t) = \sum_{k=-\infty}^{\infty} I_k e^{jk\omega pt} \tag{11.26}$$

where $G_k = G_{-k}^*$, $C_k = C_{-k}^*$, and $I_k = I_{-k}^*$. These quantities, in conjunction with the embedding impedance $Z_e(\omega)$, can be used to determine the small-signal mixer characteristics and used to develop a conversion matrix for the diode.

The components of the conversion matrix, which relates the various small-signal components of voltage to current at each sideband frequency, can be constructed from the foregoing nonlinearities. For the intrinsic diode (Fig. 11.10), the admittance matrix Y relates the current and voltage at port m, corresponding to a sideband frequency of $\omega_0 + m\omega_p$, to the current and voltage at port n, which corresponds to a sideband frequency of $\omega_0 + n\omega_p$. Although these ports are not physical, the model can be treated as a multiport circuit since each port is at a different frequency. The ports, instead of being different sets of terminals at the same frequency, are the same set of terminals at different sideband frequencies.

The square conversion matrix $[Y]$, which is of the form

$$
\begin{bmatrix}
& \vdots & \vdots & \vdots & \\
\cdots & Y_{11} & Y_{10} & Y_{1-1} & \cdots \\
\cdots & Y_{01} & Y_{00} & Y_{0-1} & \cdots \\
\cdots & Y_{-11} & Y_{-10} & Y_{-1-1} & \cdots \\
& \vdots & \vdots & \vdots &
\end{bmatrix}
$$

is the admittance matrix of the intrinsic diode; hence the current–voltage relationship for the circuit must obey Ohm's law. Thus

$$[i] = [Y][v] \tag{11.27}$$
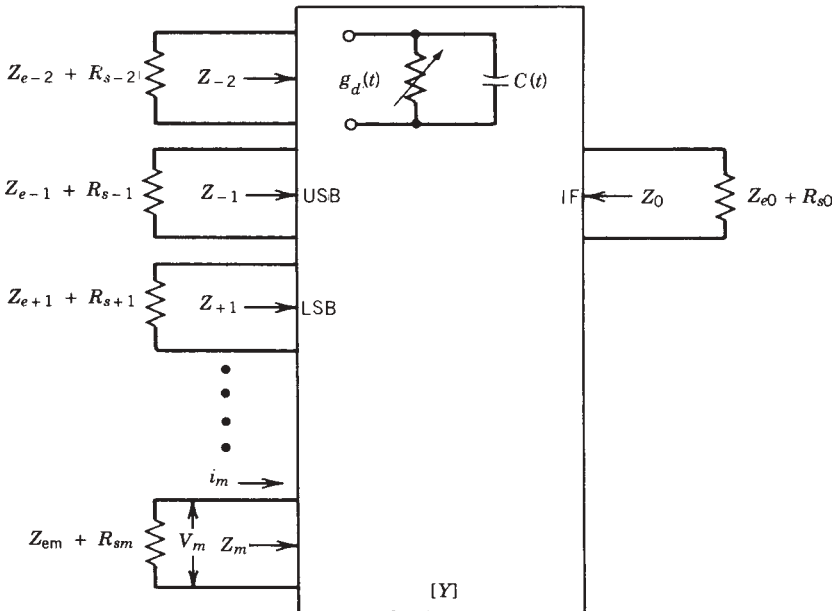
FIGURE 11.10 Multiport model of pumped intrinsic diode.

where $[i] = [\ldots, i_1, i_0, i_{-1}, \ldots]^T$ and $[v] = [\ldots, v_1, v_0, v_{-1}, \ldots]^T$ are the small-signal voltage and current components at each port. For the intrinsic diode, it can be shown that the elements of the $[Y]$ matrix are given by

$$Y_{mn} = G_{m-n} + j(\omega_0 + m\omega_p)C_{m-n} \tag{11.28}$$

where G_{m-n} and C_{m-n} are the Fourier coefficients of the diode's small-signal conductance and capacitance defined in (11.24) and (11.25). The series resistance and the effects of the embedding network, as shown in Figure 11.11, can now easily be added. This can be done by forming a new conversion matrix, $[Y']$, which is the admittance of the total mixer. This augmented network (Fig. 11.12) for the pumped mixer allows one external source, v_1, which is the RF input. However, the augmented matrix includes all external terminating impedances Z_{em}. The new matrix is of the form

$$\begin{bmatrix} & \vdots & \vdots & \vdots & \\ \cdots & Y'_{11} & Y'_{10} & Y'_{1-1} & \cdots \\ \cdots & Y'_{01} & Y'_{00} & Y'_{0-1} & \cdots \\ \cdots & Y'_{-11} & Y'_{-10} & Y'_{-1-1} & \cdots \\ & \vdots & \vdots & \vdots & \end{bmatrix}$$

and can be defined as

$$[Y'] = [Y] + \text{diag}\left[\frac{1}{Z_{em} + R_{sm}}\right] \tag{11.29}$$
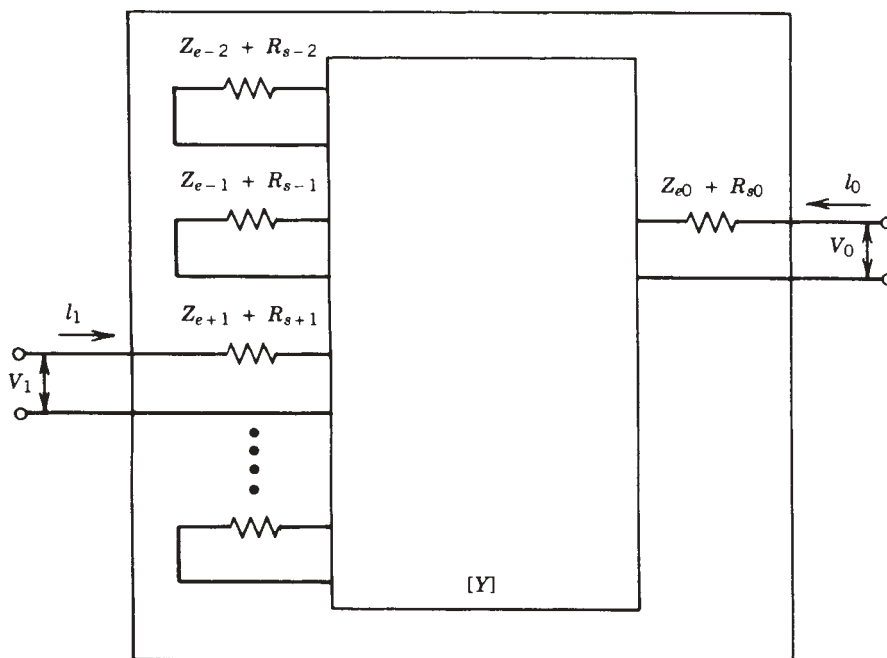
FIGURE 11.11 Augmented Y' matrix for complete mixer.

$$\overline{V}_t^2 = kT_{eq}\,R_s\,\Delta f$$

(a)

$$i_t^2 = \frac{kT_{eq}\,R_S\,\Delta f}{|R_S + Z_E|}$$

(b)
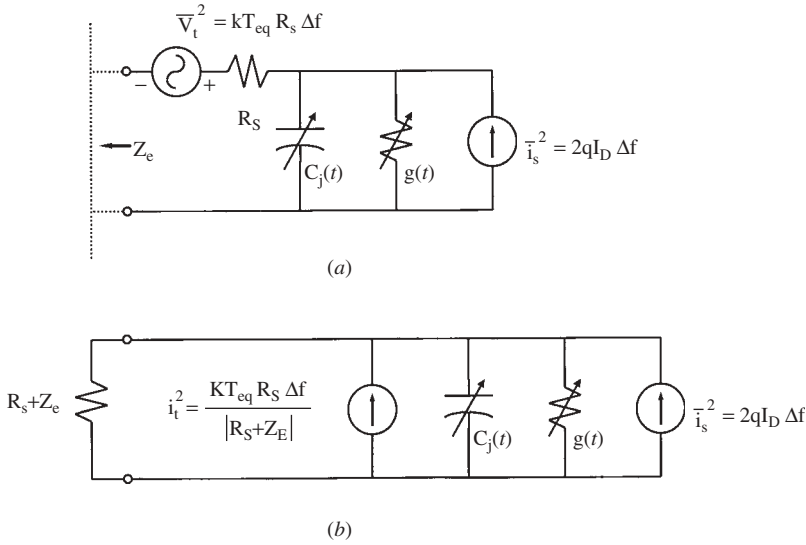
FIGURE 11.12   Mixer diode noise model: (*a*) voltage representation from thermal noise source in R_s; (*b*) noise source converted to a current source via Thévenin's theorem. (© IEEE 1978, [7.9].)

assuming that

$$[i'] = [Y'][v] \tag{11.30}$$

At this point the entire mixer circuit can be evaluated since the embedding impedances are determined from the mixer topology, but only two ports are of interest, the signal and the IF output. All other ports are terminated and contained within the new matrix $[Y']$. The addition to the intrinsic diode admittance matrix $[Y]$ of the diagonal matrix above is the first step in converting the $(2n + 1)$-port network into a two-port. To complete the conversion, the voltages at the unwanted ports are set to zero, effectively placing the embedding impedances Z_{em} in series with their respective ports. However, the IF load impedance Z_{e0} is not defined or absorbed but in the physical mixer can be adjusted for optimum performance by matching. Hence a conjugately matched load can be assumed.

The conversion matrix can also be expressed in terms of impedance by inverting $[Y']$; thus

$$[Z'] = [Y']^{-1} \tag{11.31}$$

With this in mind, we can now define the ratio of available power transferred from the RF source Z_{e1} to the IF load Z_{01} (conversion loss). The conversion loss property of a real mixer can be considered to be composed of three main components: (1) the conversion loss of the intrinsic diode without R_s, (2) the loss contribution at the IF by R_s, and (3) the loss associated with R_s at the signal frequency. The embedding network and matching network are assumed to be lossless. It should be noted how important the diode parameter R_s is to mixer performance since it contributes loss twice, once at the RF and again at the IF. Thus it is also important in determining noise performance.

For the case when the RF signal is defined as ω_1 and the IF signal is defined as ω_0, the input and output impedances, as well as the conversion loss characteristics, can be

calculated from two-port network theory. The conversion loss contribution due to R_s at the IF and RF can be shown to be

$$K_0 = \frac{\text{Re}[Z_{e0} + R_{s0}]}{\text{Re}[Z_{e0}]} \tag{11.32}$$

and

$$K_1 = \frac{\text{Re}[Z_{e1} + R_{s1}]}{\text{Re}[Z_{e1}]} \tag{11.33}$$

while the conversion loss component from the intrinsic diode is

$$L' = \frac{1}{4|Z'_{01}|^2} \frac{|Z_{e0} + R_{s0}|^2}{\text{Re}[Z_{e0} + R_{s0}]} \frac{|Z_{e1} + R_{s1}|^2}{\text{Re}[Z_{e1} + R_{s1}]} \tag{11.34}$$

From (11.32)–(11.34), the total conversion loss becomes

$$L = \frac{1}{4|Z'_{01}|^2} \frac{|Z_{e0} + R_{s0}|^2}{\text{Re}[Z_{e0}]} \frac{|Z_{e1} + R_{s1}|^2}{\text{Re}[Z_{e1}]} \tag{11.35}$$

We may now generalize the expression above to obtain the conversion loss from any sideband j to any other sideband i. Thus (11.35) becomes

$$L_{ij} = \frac{1}{4|Z'_{ij}|^2} \frac{|Z_{ei} + R_{si}|^2}{\text{Re}[Z_{ei}]} \frac{|Z_{ej} + R_{sj}|^2}{\text{Re}[Z_{ej}]} \tag{11.35a}$$

The noise properties of microwave mixers, starting from the earliest Schottky diodes and later to vacuum tubes, were well verified and understood for many years. But until the 1970s, an accurate noise model did not exist [11.12]. An accurate mixer noise model not only must include the effecs of shot noise, thermal noise, and phonon scattering but also must encompass circuit interactions, correlation properties from other mixing products, and nonlinear junction capacitance effects. The theory that will be presented was developed by Held and Kerr [11.9, 11.10] and agrees well with experimental results.

As mentioned above, the main noise sources in Schottky mixers are (1) the thermal noise contribution from the diode series resistance; (2) shot noise generated by the random flow of charge carriers across the barrier, which is analogous to shot noise in vacuum tubes; and (3) noise due to phonon scattering and, in the case of GaAs, intervalley scattering. The first two noise sources are almost always the dominant contributors, with scattering noise becoming more pronounced at very high frequencies such as for radio-astronomy applications at several hundred gigahertz.

The thermal noise component of the mixer diode model, which is present when any power-dissipating element is involved at a temperature above absolute zero, is determined by the total diode series resistance. The noise, which is attributed to the random motion of charge carriers (in this case electrons), can be assumed to be frequency independent and linearly related to temperature. Hence the noise power from a resistor can be modeled as a noiseless resistor of value R with a noise voltage source in series with it which has a magnitude of

$$\overline{v_t^2} = 4kTBR \tag{11.36}$$

The noise power generated in bandwidth B is then

$$P_n = kTB \qquad (11.37)$$

where k is Boltzmann's constant and T is temperature in kelvin. Shot noise, which is also significant, occurs because the current through the Schottky barrier is not constant. This is true even for the dc-biased case since the charge carriers are discrete points of charge (electrons) and are not continuous. This concept can easily be understood if the current is assumed to be a series of random impulses of charge traversing the junction. That is, at any instant of time, the current is made up of discrete charge carriers that randomly transit the junction, giving rise to different values of current at any instant of time. However, the average number of discrete pulses of charge per unit time, provided that the time unit is substantially longer than the junction transit time, is proportional to a constant dc current. The fluctuations in the diode current that result from this random impulse process cause a noise current component with a mean-squared magnitude proportional to dc junction current. Thus the noise current in a forward-biased diode can be shown to be

$$\overline{i_s^2} = 2eI_d B \qquad (11.38)$$

where e is the electron charge, B the bandwidth, and I_d the junction current.

A diode noise model can now be formulated by adding these Gaussian noise sources to the diode model shown in Figure 11.9. The new diode equivalent circuit is shown in Figure 11.12a. To be more compatible with the mixer circuit shown in Figure 11.10, the thermal noise voltage source can be converted to a current source by using Thévenin's theorem. The current source model (Fig. 11.12b) is more practical for noise analysis.

The thermal and shot noise sources, although both Gaussian in nature, act quite differently when LO power is applied to the diode. The thermal noise components from R_s, when down converted from the desired and undesired products to the IF, are uncorrelated since R_s is assumed to be time invariant. With just a dc component in the diode, the noises centered at mixing frequencies of $\omega_0 + n\omega_p$ are independent and therefore, when mixed down to the IF frequency of ω_0, will be uncorrelated (Fig. 11.13a). However, when an LO voltage is applied to the diode, the shot noise components at each mixing product frequency are translated to the IF band (Fig. 11.13b). In addition, the noise components from any mixing frequency include up- and down-converted noise components from other mixing frequencies since they are all related to the same LO and its harmonics. The correlation occurs because the converted noise modulation is due to the same random process.

By using an analysis method similar to the previous small-signal conversion analysis, correlation matrices for thermal and shot noise can be found. For thermal noise, which is uncorrelated, the matrix is simply a diagonal. Thus

$$C_{tmn} = \begin{cases} \dfrac{4kTR_s B}{(Z_{em} + R_s)^2} & m = n \\[3mm] \dfrac{4kTR_s B}{(Z_0)^2} & m = 0 \\[3mm] 0 & \text{elsewhere} \end{cases} \qquad (11.39)$$
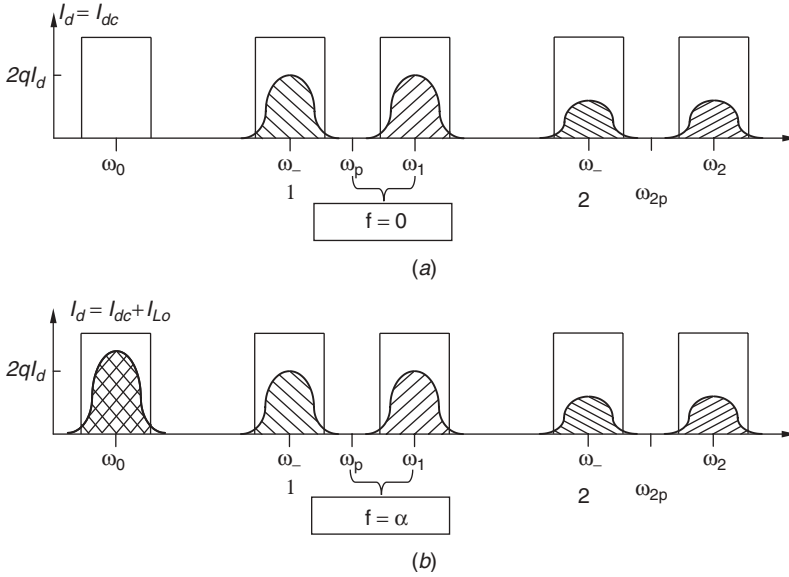
FIGURE 11.13 Noise correlation illustration: (*a*) IF output noise for a dc-biased diode; (*b*) down-converted correlated noise for LO-driven diode.

Similarly, the correlation matrix for shot noise is

$$C_{smn} = 2eI_{m-n}B \tag{11.40}$$

where I_{m-n} is the Fourier coefficient of the $(m - n)$th term for the series representing the LO diode current. It can then be shown that the noise power dissipated in the output termination Z_{em} is

$$P_m = \frac{|V_m|^2 \, \text{Re}[Z_{em}]}{|Z_{em} + R_s|^2} \tag{11.41}$$

where the voltage at ω_m is the sum of the shot and thermal noise and is defined as

$$\langle V_m^2 \rangle = Z_m (C_s + C_t) Z_m^* t \tag{11.42}$$

It should be noted that Z_m is the row of the conversion matrix Z_e corresponding to ω_m. If the conversion matrix Z' defined in (11.31) is known, the single-sideband noise figure can be defined as

$$F_{\text{ssb}} = 1 + \frac{T_m}{T_0} \tag{11.43}$$

where $T_0 = 290$ K and

$$T_m = \frac{\langle V_0^2 \rangle}{4 \, kB} \frac{|Z_{e1} + R_{s1}|^2}{|Z_{01}'|^2 \, \text{Re}[Z_{e1}]} \tag{11.44}$$

The analysis techniques outlined above should give the design engineer insight into the conversion loss and noise figure mechanisms and limitations for most practical

mixers. However, design engineers cannot be expected to develop computer algorithms to evaluate conversion and correlation matrices in order to conduct their daily design activities. Therefore, several design methods will be presented in the following sections which can be executed with commercially available software. Designs conducted in this manner can give excellent results, especially when diodes rather than transistors are used as the nonlinear element. This is in part due to the fact that diodes are very forgiving; that is, they are very tolerant of matching errors, LO drive variations, and temperature excursions. Also, most mixer requirements do not demand state-of-the-art performance in regard to noise figure and conversion loss characteristics.

11.3   SINGLE-DIODE MIXERS

The single-diode mixer, although fondly remembered for its use as an AM "crystal" radio or radar detector during World War II, has become less popular due to demanding broadband and high-dynamic-range requirements encountered at frequencies below 20 GHz. However, there are still many applications at millimeter-wave frequencies, as well as consumer applications in the microwave portion of the spectrum, which are adequately served by single-ended designs. The design techniques presented can also be applied to single-ended or balanced mixers using planar or waveguide approaches.

In this chapter we focus on a more "hands-on" design approach than previously presented, with emphasis on microstrip applications. Matching considerations, circuit approximations, and design philosophy for all types of mixers are developed. Commercially available design tools will also be used to determine nonlinear and linear circuit and diode characteristics.

The design of single-diode mixers can be approached in the same manner as multiport network design. The multiport network contains all mixing-product frequencies regardless of whether they are ported to external terminations or terminated internally. With simple mixers, the network's main function is frequency-component separation; impedance matching requirements are secondary. Hence, in the simplest approach, the network must be capable of selecting the LO frequency, RF, and IF (Fig. 11.14).

However, before a network can be designed, the impedance presented to the network by the diode at various frequencies must be determined. Unfortunately, the diode is a nonlinear device; hence, determining its characteristics is more involved than determining an unknown impedance with a network analyzer. Since the diode impedance is time varying, it is not readily apparent that a stationary impedance can be found. Stationary impedance values for the RF, LO frequency, and IF can be measured or determined if sufficient care in analysis or evaluation is taken.

The first impedance to measure or determine is the diode's LO impedance. As we have learned, this impedance is a function of LO drive power, dc bias, frequency, and physical diode characteristics; thus impedance measurements must be conducted at the correct bias and drive power, which correspond to the expected mixer environment. Typically, S_{11} (large signal) is measured as a function of frequency for several values of LO power. This information allows the design engineer to optimize the network characteristics to the expected LO power variation so that the resulting mixer will exhibit the best performance traits, such as conversion loss, noise figure, VSWR, and so on. The large-signal LO impedance can also be simulated numerically with a harmonic balance or time-domain simulator. Figure 11.15 illustrates typical LO impedance characteristics for a beam-lead diode as a function of frequency and pump power. It should
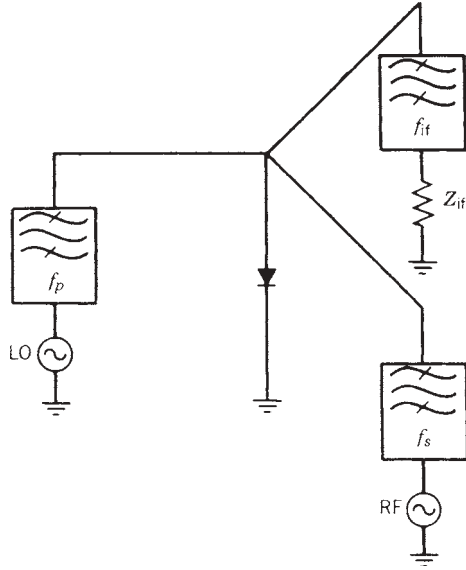
FIGURE 11.14   Three main frequency components and filtering requirements for single-diode mixer.
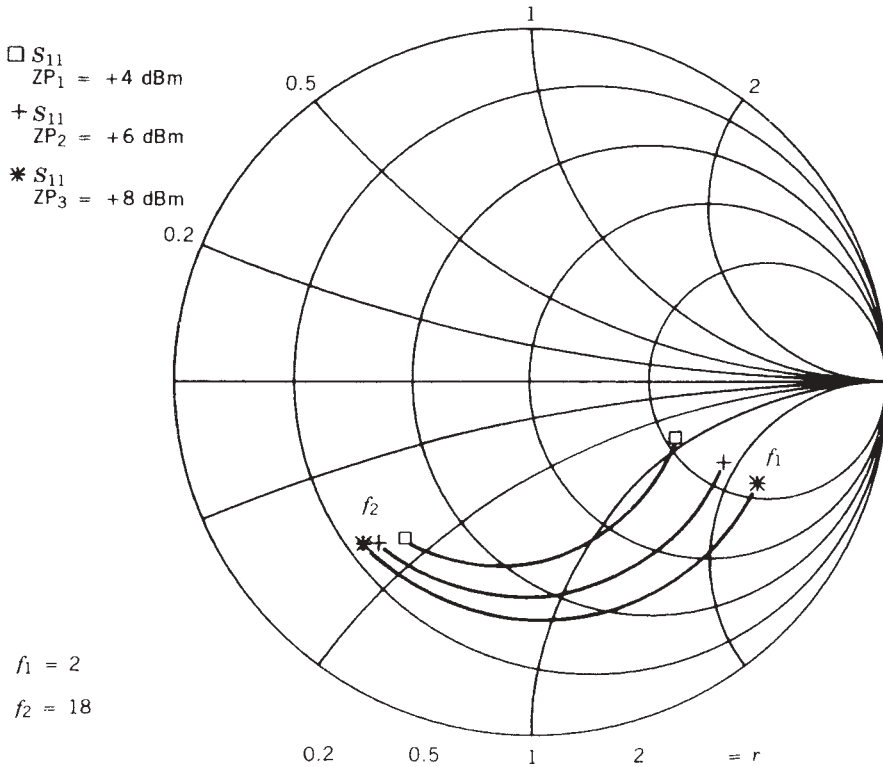
FIGURE 11.15   LO impedance as a function of pump power.

be remembered that, when measuring the diode's LO impedance, a dc return path must be present even if fixed dc bias is not employed (Fig. 11.16).

Measuring or determining the RF and IF impedances is somewhat more difficult in that the LO drive must be present. When computer simulation is employed, the problem is numerically difficult but conceptually easy for the user. By adding a second signal to the analysis and evaluating the voltages and currents in the circuit, the conjugate matched impedance values for the embedding network can be determined. A computer program such as microwave SPICE is ideal for such analyses. Measuring such parameters is a bit more tricky.

An approximate value for RF impedance can be obtained with the measurement setup shown in Figure 11.17. With this arrangement, LO power is injected by means of a directional coupler. The RF impedance is measured by using a second source and network analyzer. Sometimes there are problems with this approach, in that the LO signal interferes with the network analyzer measurements. Usually, this is when the LO and RF signals are very close in frequency. As mentioned above, measurements of this type are only approximate, because the diode is not presented with the terminating impedances that it will see in the final mixer circuit at all product frequencies. The IF impedance can be measured in a similar manner, or if the IF is sufficiently far removed from the RF or LO frequencies, a slide screw tuner can be placed at the diode's IF output port and adjusted for optimum conversion loss. The tuner and load can then be measured. The tuner/load combination will be the conjugate of the diode's IF impedance. This measurement configuration is shown in Figure 11.18. Although the measured impedance values determined by the foregoing method are only approximate, they are typically sufficiently accurate for most design problems.
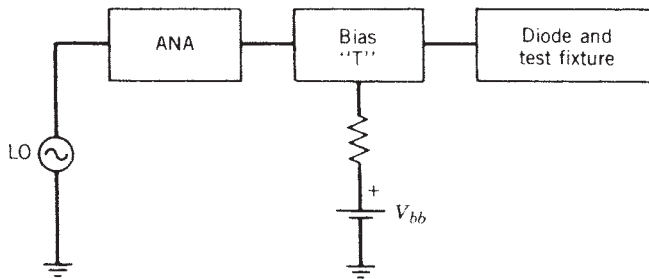
FIGURE 11.16   Measurement setup for determining diode LO impedance.
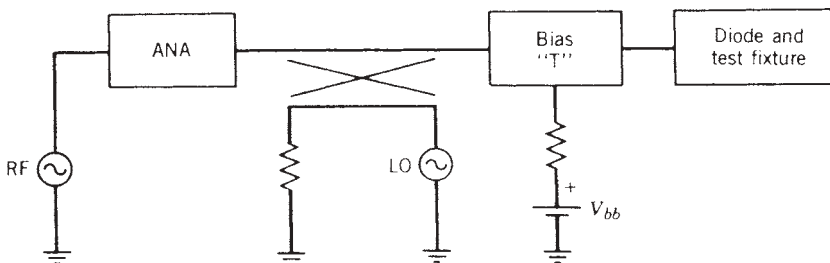
FIGURE 11.17   Diode RF impedance measurement setup.
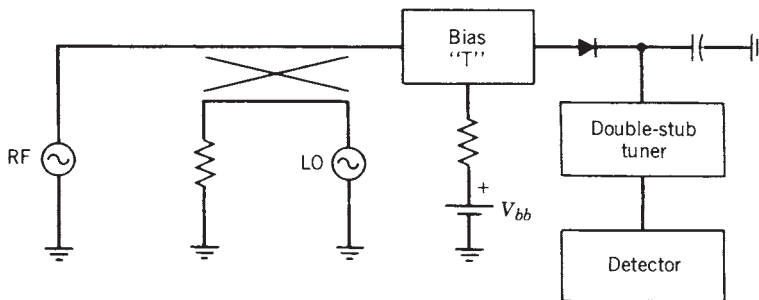
FIGURE 11.18   IF impedance measurement setup using a double-stub tuner.

With the diode impedance data obtained, we can now continue with the network design problem. The problem proceeds as a multiport network design where key impedance terminations and sources are external to the network. Each port of the network is at a different frequency, not necessarily a different physical location (Fig. 11.19). Hence, as one of the source frequencies is changed, a new set of network conditions result. When broadband performance is desired, this analysis method can become a bit cumbersome.

When both the large-signal (LO) and small-signal (RF and IF) impedances are known, the design problem can be reduced to the solution of linear two-port networks. That is, a two-port network can be constructed for each frequency component, such as the LO-to-diode matching network, image termination-to-diode matching network, and so on. This concept is illustrated in Figure 11.20. The dashed lines between each network in the figure denote the fact that each network is not independent but is composed of at least some of the identical elements. Thus during computer optimization of the network performance, a change, for example, in the value of a capacitor that is common to all signal paths must be made identical from network to network. This is easily accomplished by employing the variable element block when using either Super-Compact or Touchstone.
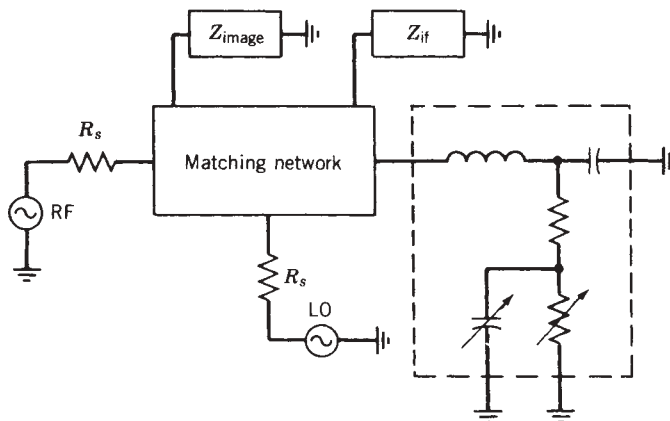
FIGURE 11.19   Matching circuit for single-diode mixer with external ports at separate frequencies.
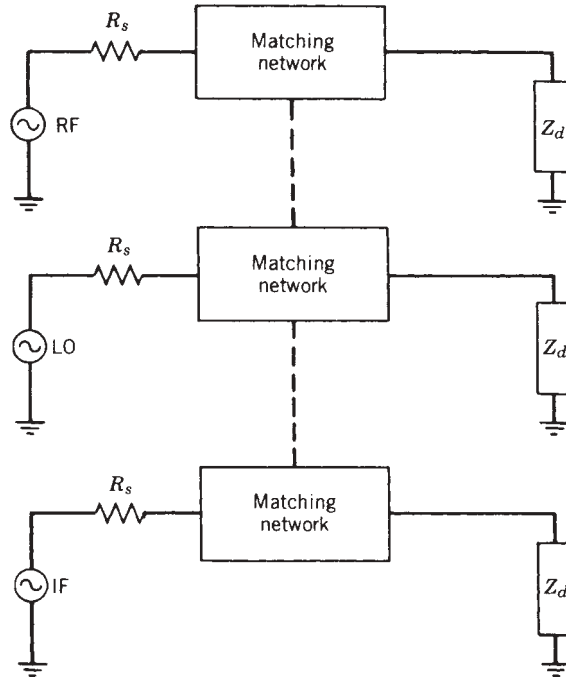
FIGURE 11.20 Multiport matching network for single-diode mixer reduced to three coupled two-port networks. A linear simulator can yield a good design approximation if the small- and large-signal impedances are substituted for Z_d in the appropriate analyses.

If a nonlinear simulator is available, such as Libra Microwave SPICE, and a diode model is formulated using the methods outlined in Chapter 5 for GaAs FETs, the complete problem can be solved using a single network. Provided that a sufficient number of LO and signal harmonics or a sufficiently small time step is employed, excellent simulation accuracy can be obtained. The nonlinear simulator has the added advantage of being able to predict intermodulation and conversion gain compression characteristics.

Although the design approach outlined above can be straightforward and is well defined, the problems encountered when selecting a diode are sometimes ignored. Selecting the proper mixer diode for a particular application is dependent on a variety of factors, such as conversion loss, cost, intermodulation characteristics, LO drive power, frequency of operation, and the desired transmission line media.

The actual mechanical characteristic of the diode is probably the first parameter to be considered. This parameter is influenced not only by the transmission line media involved but also by performance, cost, and the final application environment. For example, better mixer performance will almost always be obtained when unpackaged devices are employed rather than chip or beam-lead diodes, due to package parasitics and losses. However, packaged diodes are much easier to handle, and product assembly can be accomplished without expensive soldering, welding, or bonding equipment. A good illustration of the use of packaged diodes for low-cost products are the vast variety of commercially available broadband mixers constructed with ribbon-lead diodes on soft substrate material.

As the frequency of operation becomes higher and soft substrate materials are replaced by fused silica or alumina, performance requirements usually dictate the use of either beam-lead or chip devices. However, there are vast performance differences between diodes, which are due to semiconductor type, barrier potential, and junction area. Typically, a figure of merit is defined for a diode, analogous to the parameter f_t for an active device, called the cutoff frequency f_c, which is defined as

$$f_c = \frac{1}{2\pi R_s C_{j0}}$$
(11.45)

The cutoff frequency is an important parameter since it can be shown that a degradation in conversion loss performance δ_1 from the ideal case at the RF [11.13] can be defined as

$$\delta_1 = 1 + \frac{R_s}{r_{dr}} + \frac{r_{dr}}{R_s}\left(\frac{f}{f_c}\right)^2$$
(11.46)

where r_{dr} is the nonlinear impedance of the diode junction at the RF. At the IF, a finite R_s also degrades conversion loss; thus a degradation factor δ_2 can also be defined as

$$\delta_2 = \frac{2R_s}{r_{di}} + 1$$
(11.47)

where r_{di} in this case is the nonlinear impedance of the diode junction at the IF. Equation (11.46) can also be written in the form

$$\delta_1 = 1 + \frac{R_s}{r_{dr}} + R_s r_{dr}(\omega C_{j0})^2$$
(11.48)

Hence it becomes easy to see that as the $R_s C_{j0}$ product becomes large, the conversion loss degrades rapidly. Equation (11.48) also illustrates that an optimum diode size exists for a given frequency. This can be seen if one examines the last term in (11.48). At low frequencies, C_{j0} cannot be made arbitrarily large in an attempt to minimize R_s. Also, as the operating frequency is increased, the $(\omega)^2$ term begins to dominate. Unfortunately, the relationship between R_s and C_{j0} for any diode geometry is inversely related; that is, as the junction area is reduced so that C_{j0} can be minimized, R_s increases. Thus a minimum in conversion loss occurs for a given frequency as the diode junction area is varied. As the operating frequency is raised, the minimum occurs at smaller and smaller junction areas; the absolute value of conversion loss deteriorates with frequency. In Figure 11.21a the parasitic conversion loss contribution due to the diode parasitics for diodes fabricated using a high-quality silicon process is shown. A similar plot of conversion loss degradation for ion-implanted GaAs diodes fabricated using a conventional FET process is illustrated in Figure 11.21b. For both cases it was assumed that the $R_s C_{j0}$ product remains constant as the diode size is scaled. This problem is always a challenge to the diode designer, who invariably is asked to fabricate a diode with minimum C_{j0} and minimum R_s. It should be noted that, when selecting a diode for a particular frequency range, the largest C_{j0} should be chosen. This will minimize performance sensitivity due to diode variations and will usually give the best overall results.
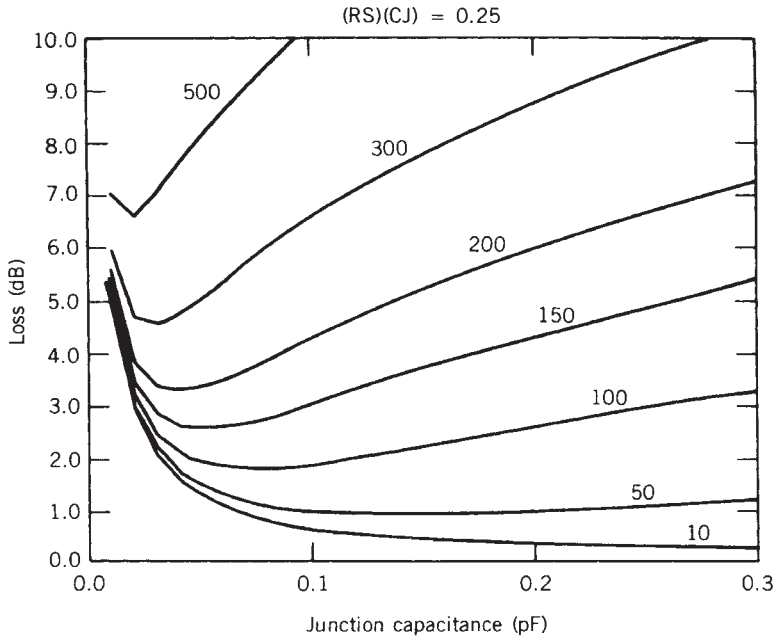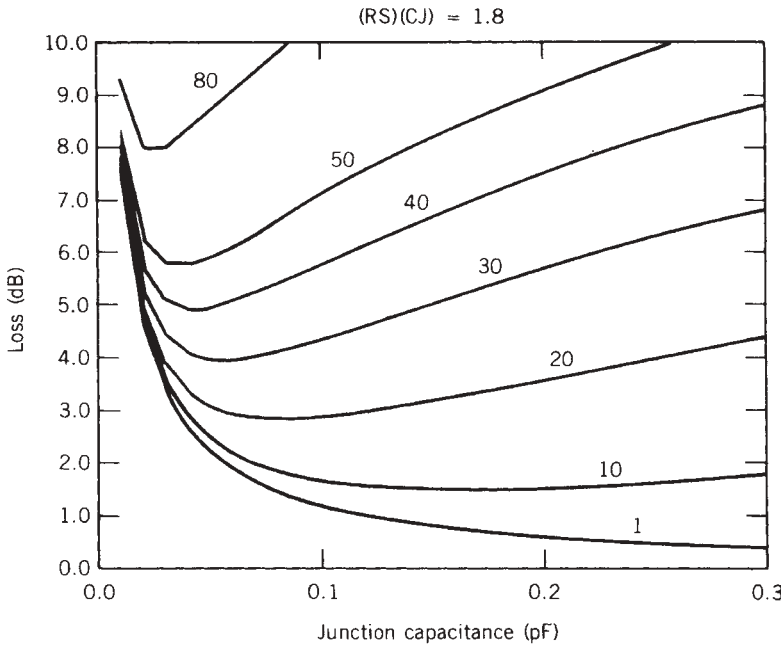
FIGURE 11.21   Conversion loss degradation due to diode parasitics as a function of junction capacitance and frequency (GHz): (*a*) high-quality silicon diode; (*b*) GaAs ion-implanted planar diode.

The junction area and the semiconductor material also influence the nonlinear diode impedance at various product frequencies. The diode size can be chosen for ease in matching, rather than for conversion loss performance, as is sometimes done in waveguide designs or broadband applications. Generally, GaAs diodes exhibit higher impedances than comparably sized silicon devices [11.14] and typically have lower values of R_s but are usually more costly. Two diode models for Si and GaAs devices driven into LO saturation are shown in Figure 11.22. As can be seen, the junction resistance is quite different even though the parasitic element values are similar.

The final major consideration in diode selection is intermodulation performance. This key characteristic is directly related to LO power and barrier potential. Most commercial diode manufacturers offer silicon mixer diodes with various barrier potentials. Low-barrier Si devices require only about 0.3 V for 1 mA diode current, while high-barrier diodes may require as much as 0.7 V for the same current. If the LO impedances are similar, about 6 dB more LO power is required with high-barrier devices. As the input RF signal to the diode approaches the pump power level, the converted product levels begin to saturate; that is, the converted signal level is no longer related to the input RF signal power. The 1-dB compression point occurs when the input signal power is approximately 6 dB less than the LO power level. Increasing the LO or pump power increases the compression point until the diode is fully saturated. This occurs when the LO waveform drives the diode well into the conduction region, which for a high-barrier Si diode is about 0.7 to 0.8 V of peak forward voltage. For GaAs diodes the saturation level may even be slightly greater. The third-order intercept point is also related to the barrier height and LO power in the same manner. A common "rule of thumb" is that the third-order intercept point (IP3) is 10 dB above the 1-dB compression point; however, the designer should not be surprised if the IP3 level of a particular mixer is on the order of the LO power. Product terminations, especially the image termination, greatly influence the distortion characteristics of any mixer.

To illustrate the foregoing design concepts and circuit interactions, the design of a single-diode microstrip mixer for the frequency range (RF) 9.0 to 10.2 with an IF of 500 MHz will now be described. If we select alumina as the substrate material and desire a simple matching structure capable of reasonable bandwidth performance, either
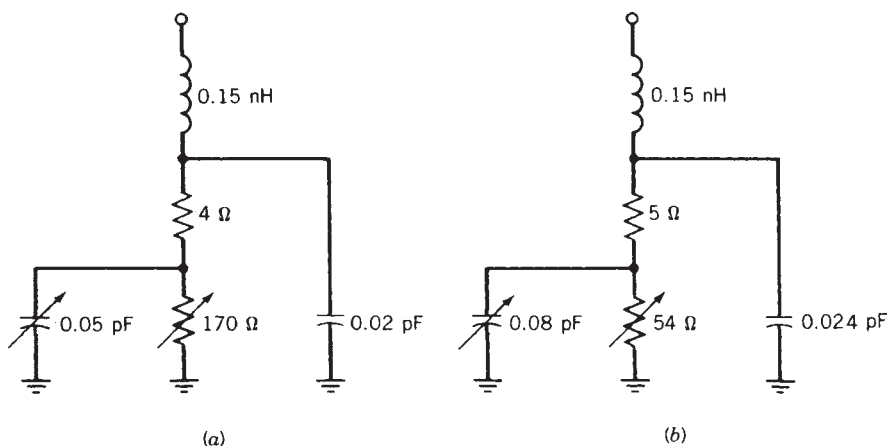
FIGURE 11.22   Parasitic element values for (*a*) GaAs and (*b*) silicon beam-lead diodes.

a beam-lead or chip diode should be employed. In addition, for X-band operation, the diode cutoff frequency should be in excess of 100 GHz, and R_s should be less than 10 Ω to assure good mixer performance. Also, C_{j0} must be less than 0.3 pF so that optimum performance can be obtained. LO pump power is minimized by selecting a low-barrier Si diode.

The design begins by determining the LO, RF, and IF impedances at the desired LO power level for the diode. This can be accomplished by using numerical techniques or laboratory measurements. Figure 11.23 illustrates the LO, RF, and IF impedances of a typical silicon beam-lead diode driven at the onset of LO saturation. The element values for a simple diode model are shown in Figure 11.24.

The unmatched return loss impedance characteristics for LO and RF signals in the frequency range 9.0 to 10.7 GHz are shown in Figure 11.25. Because of the semiconductor material (Si) and diode size, the impedances are relatively close to 50×. However, some improvement in conversion loss performance can be obtained by matching. A simple matching network topology that separates the IF signal from the LO and RF signals and provides a dc and IF return path is shown in Figure 11.26. The new RF and LO return loss performances for the total structure are shown in Figure 11.27. It was assumed the the LO and RF signal separation would be accomplished with the aid of a directional coupler. It should also be noted that although the
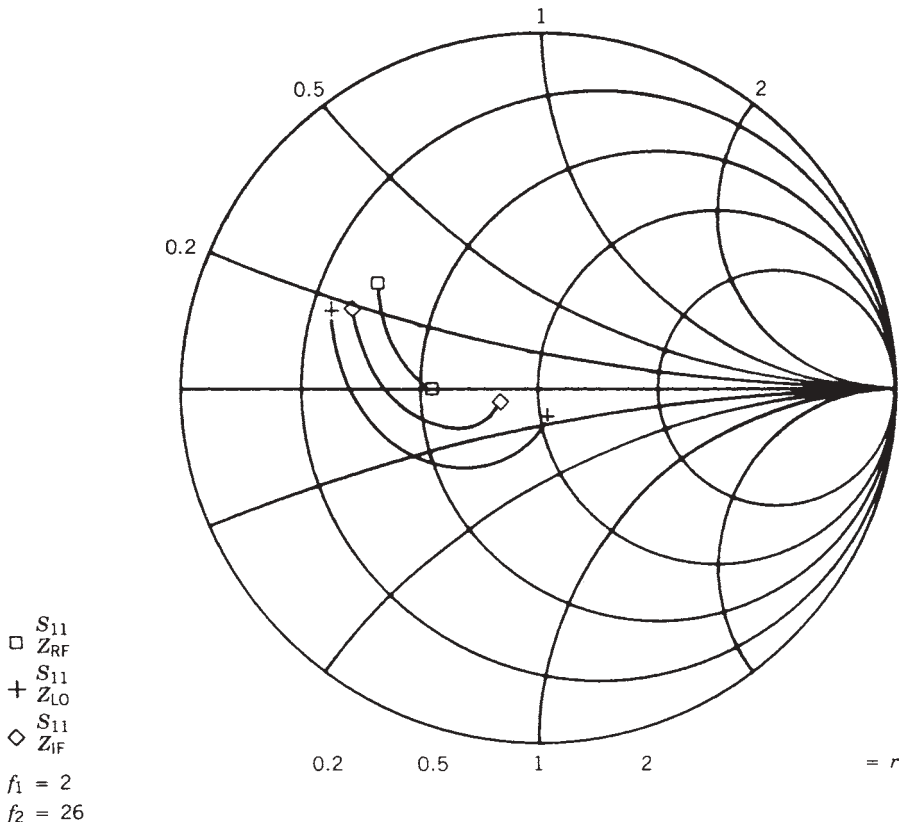
FIGURE 11.23   LO, RF, and IF impedances of typical silicon beam-lead diode.

	RF	LO	IF
R_s	8	8	8
R_D	19	46	33
C_{JO}	0.28	0.3	0.28
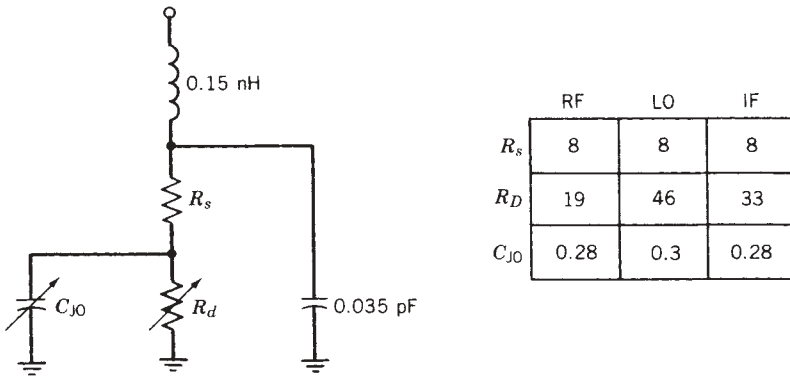
FIGURE 11.24   Element values for silicon beam-lead diode used in mixer example.
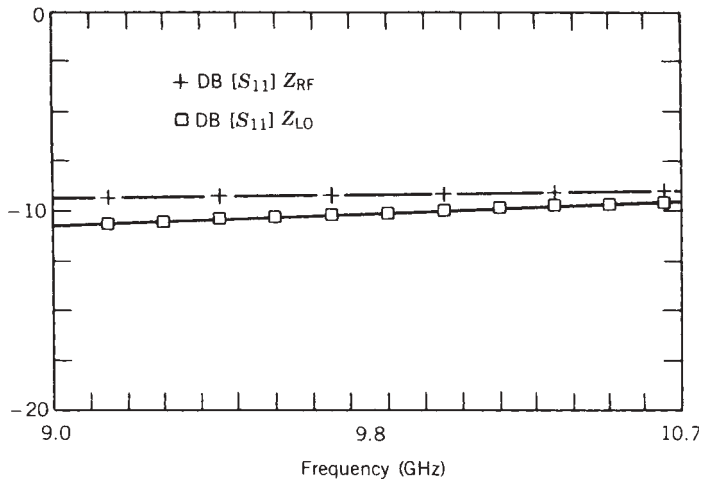
FIGURE 11.25   Return loss of LO and RF impedances of unmatched diode.

DIM: mils
SUB: $H = 15$, $\epsilon_r = 9.9$ $T = 0.1$
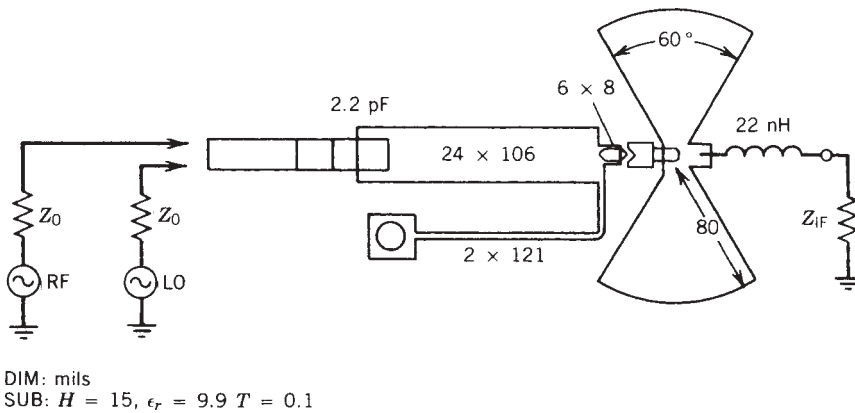
FIGURE 11.26   Single-diode mixer microstrip circuit layout with beam-lead silicon diode.
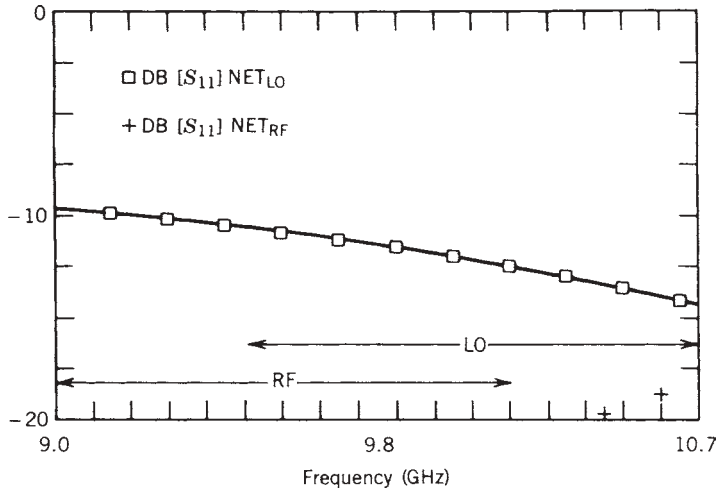
FIGURE 11.27   LO and RF return loss performance of single-diode and matching network.

RF return loss is greater than 20 dB, the LO return loss was slightly degraded from the unmatched case. This type of VSWR trade-off in favor of the RF port is common. IF port matching at 500 MHz can be accomplished with lumped-element techniques.

Although the example above is somewhat simple, it does illustrate the design methodology, device selection, and circuit trade-offs. The single-diode mixer design problem also forms the basis for many other topologies which are illustrated in the following sections.

11.4   SINGLE-BALANCED MIXERS

The simplicity and performance of the single-diode mixer presented in Section 11.3 make it very attractive in terms of cost, producibility, and conversion loss, but it exhibits some serious drawbacks for broadband high-dynamic-range applications. Probably its greatest disadvantage is the difficulty in injecting LO energy while still being able to separate the LO, RF, and IF signals in the embedding network. Without the aid of some form of balun or hybrid structure, this problem becomes even more difficult as the mixer operating bandwidth is increased. Aside from circuit design considerations, balanced mixers offer some unique advantages over single-ended designs such as LO noise suppression and rejection of some spurious products. The dynamic range can also be greater because the input RF signal is divided between several diodes, but this advantage is at the expense of increased pump power. However, balanced mixers tend to exhibit higher conversion loss and are more complex. Both the increase in complexity and conversion loss can be attributed to the hybrid or balun and to the fact that perfect balance and lossless operation cannot be achieved.

There are essentially only two design approaches for single-balanced mixers; one employs a 180° hybrid, while the other employs some form of quadrature structure. The numerous variations found in the industry are related to the transmission line media employed and the ingenuity involved in the design of the hybrid structure. The most common designs for the microwave frequency range employ a branch line, Lange, or

"rat-race" hybrid structure. At frequencies below about 5 GHz, broadband transformers are very common, while at frequencies above 40 GHz, waveguide structures become prevalent, although GaAs monolithics are beginning to encroach in the 44-, 60-, and 94-GHz frequency ranges.

Before we can analyze or design a single-balanced mixer, we must understand the operation and realization of the 180° or 90° hybrid. Ideal representations illustrating the performance characteristics of both hybrid types are shown in Figure 11.28. The ideal performance of the quadrature hybrid illustrated in Figure 11.28a can be described with the aid of an *S*-parameter matrix. Assuming that the ports are defined as in the figure, the matrix can be defined as

$$S_{90} = \frac{1}{(2)^{1/2}} \begin{bmatrix} 0 & -j & 0 & 1 \\ -j & 0 & 1 & 0 \\ 0 & 1 & 0 & -j \\ 1 & 0 & -j & 0 \end{bmatrix} \tag{11.49}$$

Similarly, the performance of an ideal 180° hybrid (or balun) can be described as

$$S_{180} = \frac{1}{(2)^{1/2}} \begin{bmatrix} 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 \end{bmatrix} \tag{11.50}$$

As can be seen in the relationships above, the zero-valued diagonal terms indicate that the hybrids are perfectly matched, and the nondiagonal zero-valued terms indicate infinite reverse isolation.

A popular form of the quadrature hybrid described above is the Lange coupler, illustrated in Figure 11.29. The coupler is used in microstrip applications because of its ability, due to the interdigitated structure, to obtain very tight coupling values (approximately −6 to −1.25 dB). Because of this ability, couplers are commonly designed
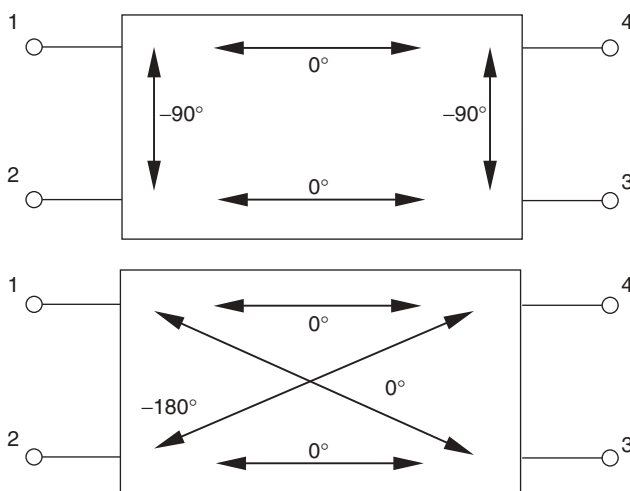
FIGURE 11.28   Ideal hybrid performance: (*a*) quadrature coupler (90°); (*b*) balun (180°).
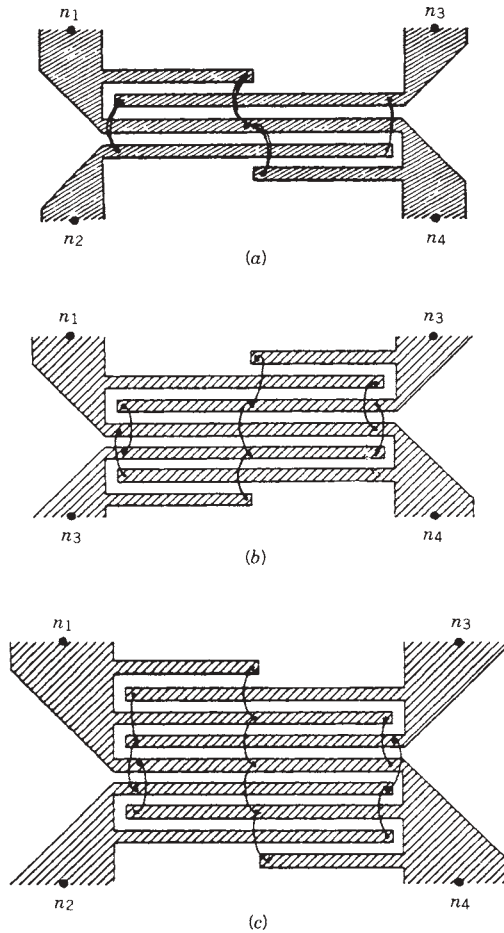
FIGURE 11.29   Microstrip Lange coupler configurations: (*a*) four-strip; (*b*) six-strip; (*c*) eight-strip.

overcoupled (about −2.5 dB), thus achieving very broadband performance for a single-section structure. Typical broadband amplitude and phase performance for a four-strip coupler fabricated on an alumina substrate is shown in Figure 11.30. As can be seen, the phase performance is very close to 90° throughout a considerable frequency range. The amplitude balance, although not perfect, is also very respectable. Couplers with similar performance can also be realized in a three-layer stripline by using parallel-plate coupling. Quadrature coupler performance can also be obtained in a stripline or microstrip over a limited bandwidth with a branch line coupler (Fig. 11.31). The amplitude and phase performances for a typical coupler are shown in Figure 11.32. Although the single-section branch line coupler exhibits narrow-band performance, multisection couplers can be constructed for 40% bandwidth applications.

Realizing a 180° hybrid at microwave frequencies is somewhat more difficult. However, the ring or rat-race hybrid, illustrated in Figure 11.33, is easy to construct and offers good performance for narrow-band applications. The coupler ring is realized with a 70.7-Ω transmission line which is 1.5 wavelengths in circumference. The four

(a)
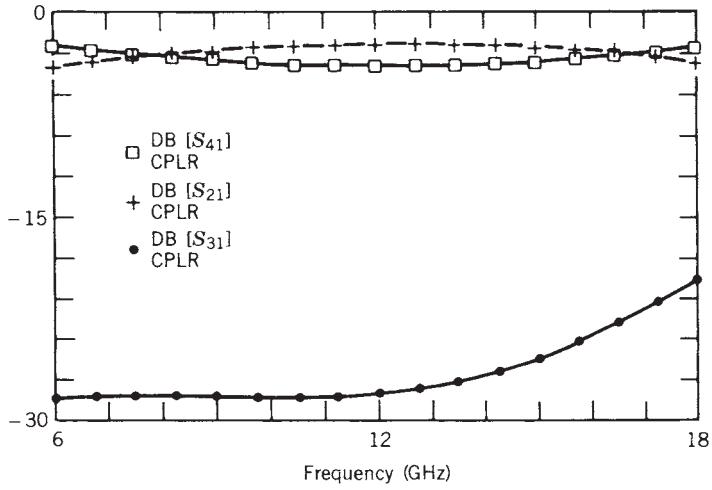
(b)
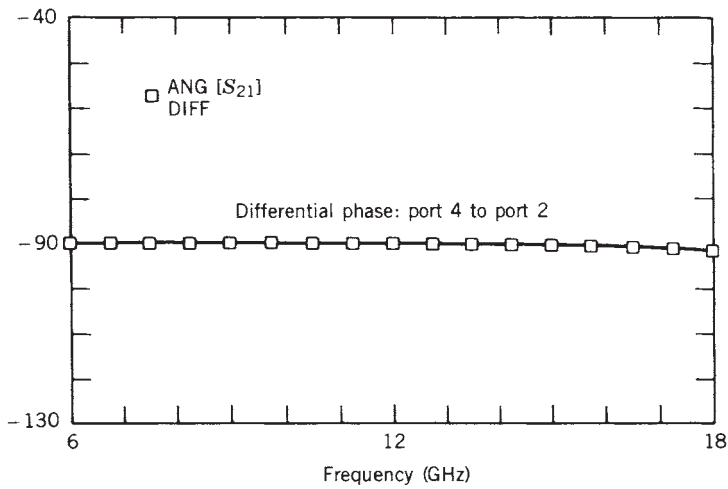
(c)

FIGURE 11.30   Microstrip Lange coupler fabricated on an alumina substrate: (*a*) coupler strip dimensions with nodel connections; (*b*) amplitude response; (*c*) phase performance.
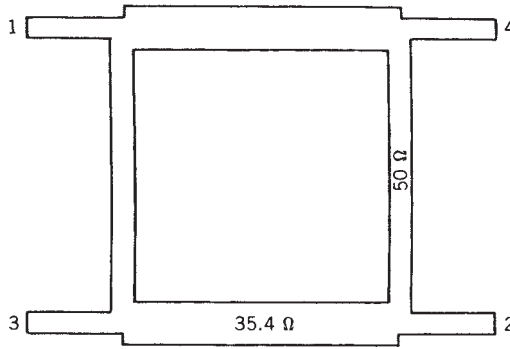
FIGURE 11.31   Branch line hybrid for 50-Ω system.
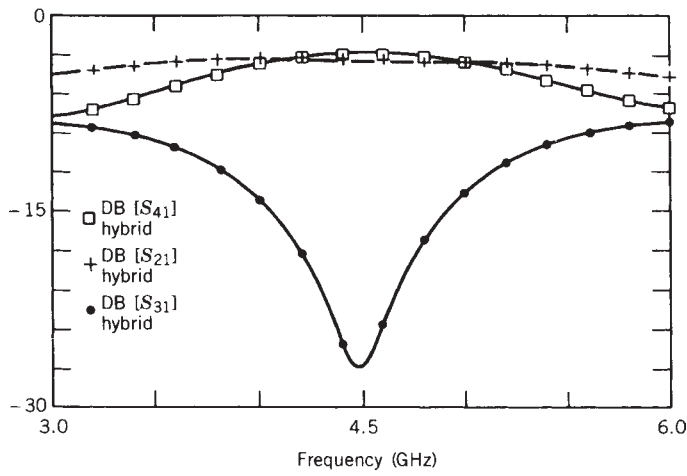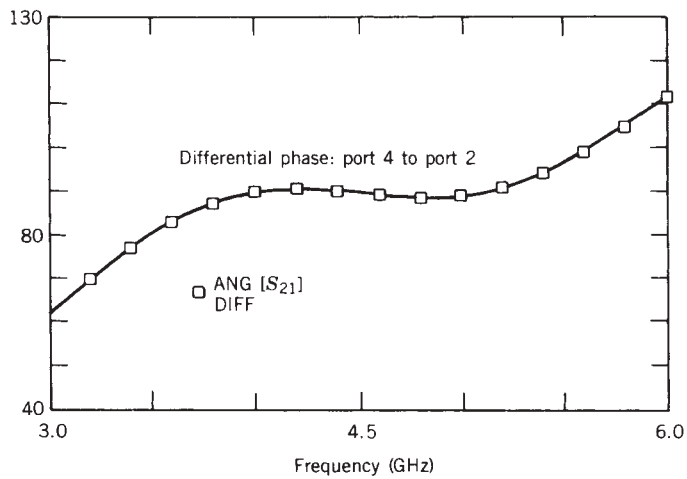
FIGURE 11.32   Microstrip branch line coupler performance: (*a*) amplitude response; (*b*) differential phase performance.
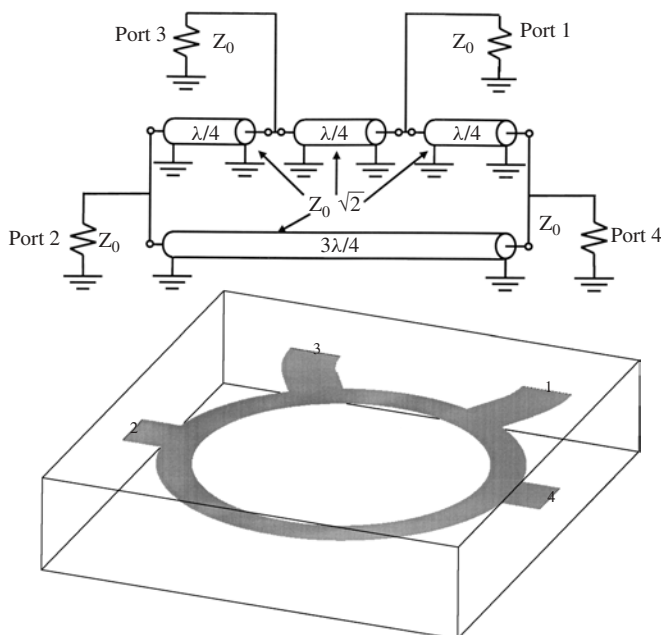
FIGURE 11.33   Hybrid ring ("Rat-race") general circuit model and stripline topology.

50-Ω ports are connected to the ring in such a manner that two of them are separated by 0.75 wavelength, with the remaining two being separated by 0.25 wavelength.

The operation of the $180°$ hybrid is simple and is illustrated in Figure 11.34. If a signal is injected into port 1, the voltage appearing at port 2 is zero, since the path lengths differ by 0.5 wavelength; thus port 2 can be treated as a virtual ground. Hence the transmission line portions of the ring between ports 3 and 2 and ports 4 and 2 act as short-circuited stubs connected across the loads presented at ports 3 and 4. For center-frequency operation, these stubs appear as open circuits. Similarly, the transmission line lengths between ports 1 and 3 and ports 1 and 4 transform the 50 Ω load impedances (Z_0) at ports 3 and 4 to 100 Ω ($2Z_0$). When combined at port 1, these transformed impedances produce the 50 Ω input impedance seen at port 1. A similar analysis can be applied at each port, thus showing that the hybrid exhibits a matched impedance of 50 Ω or Z_0 at all nodes. It should be noted that, when port 1 is driven, the outputs at ports 3 and 4 are equal and in phase, while ideally there is no signal at port 2. However, when port 2 is driven, the output signals appearing at ports 3 and 4 are equal but exactly out of phase. Also, no signal appears at port 1. Hence ports 1 and 2 are isolated. Unfortunately, the hybrid performance is narrow band, although modifications to the ring by replacing 0.5 wavelength of transmission line between ports 2 and 4 by a constant $180°$ phase "flip" (Fig. 11.35) does improve the bandwidth considerably, but realizing the necessary transmission line, since it must be very tightly coupled, is difficult. Parallel suspended coupled strips or a Lange coupler can be used for this application, with good results. The performances of both hybrids are shown in Figures 11.36 and 11.37.

Another form of a four-port $180°$ hybrid is the trifilar wound center-tapped transformer [11.15]. These types of transformers, which are typically wound on ferrite
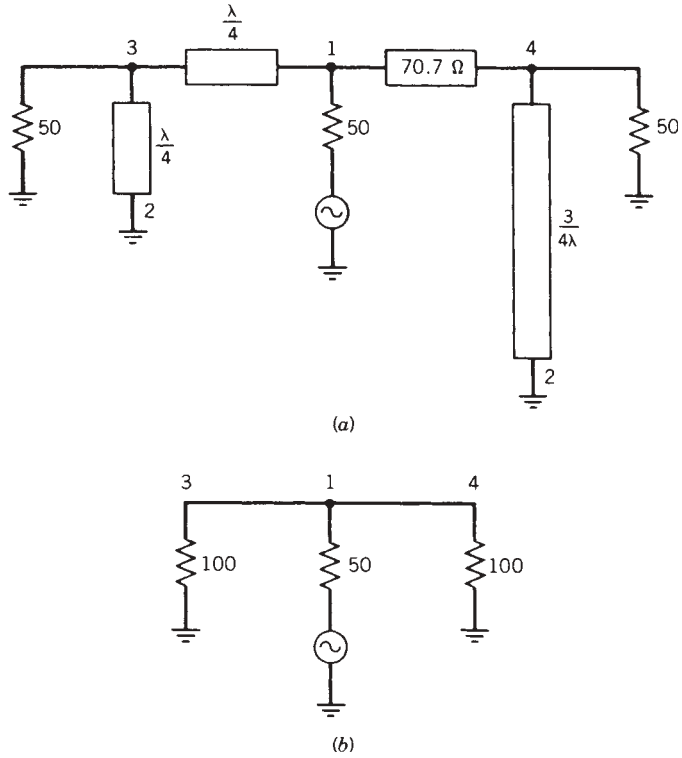
FIGURE 11.34 Equivalent circuit of ring hybrid with port 1 excited and with ports 3 and 4 as outputs: (*a*) transmission line model with port 2 as a virtual ground; (*b*) equivalent circuit at center frequency.
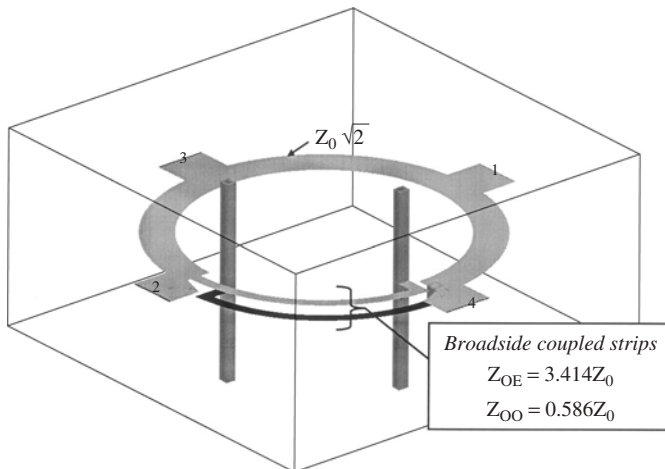
FIGURE 11.35 Multilayer stripline topology for a broadband ring hybrid employing an inversely connected transmission line in order to achieve an ideal 180° phase shift ("flip").
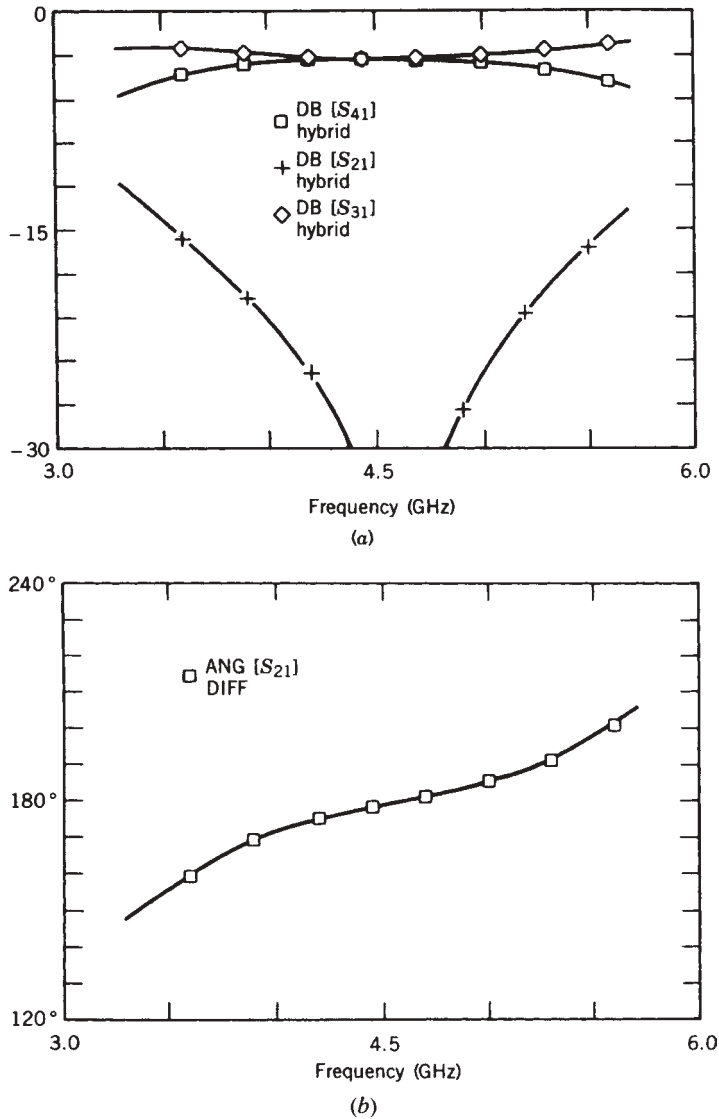
FIGURE 11.36 Microstrip ring (rat-race) hybrid performance: (*a*) amplitude response; (*b*) differential phase performance.

cores (beads or toroids), can be designed to exhibit extremely broadband performance. Although the transformer performance is influenced by a variety of factors, such as wire size and winding length, core material, and size and aspect ratio, transformers that can operate from 10 mHz to 4 GHz can be constructed. Typical construction of a trifilar wound transformer with a 2 : 1 turns ratio is illustrated in Figure 11.38.

The performance of a transformer hybrid is similar to the rat race described previously if it is connected as shown in Figure 11.39, with the exception that all four ports do not have the same driving-point impedance. This condition will always exist regardless of the turns ratio of the transformer because the secondary winding will
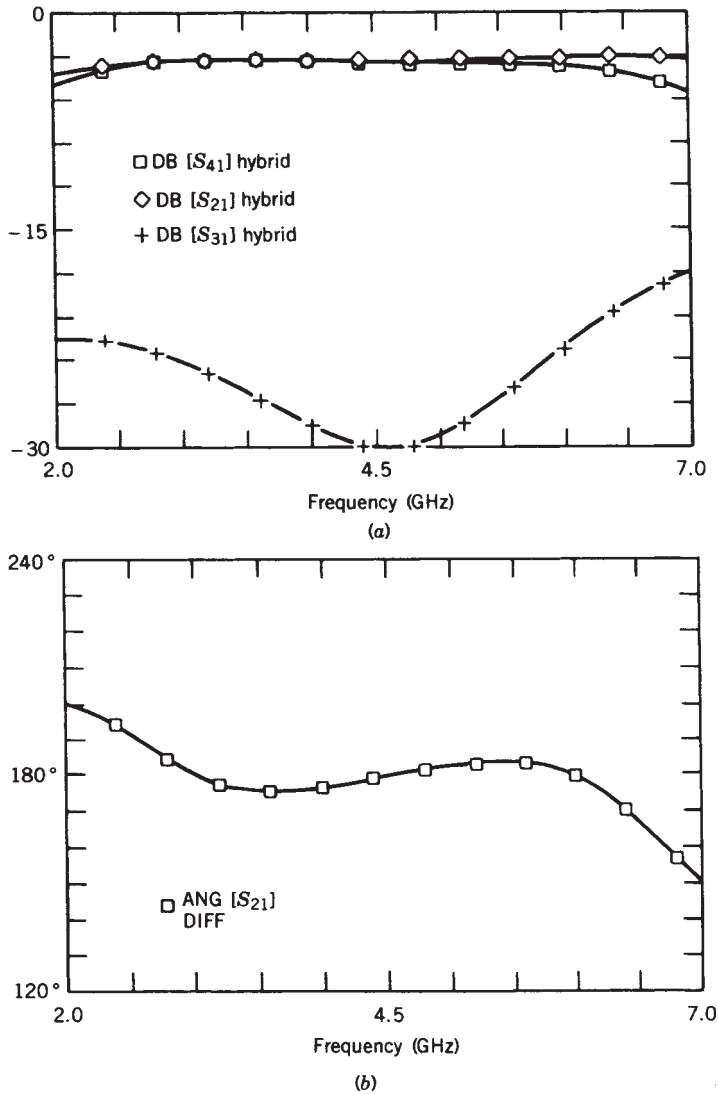
FIGURE 11.37 Enhanced bandwidth microstrip ring (rat-race) hybrid performance: (*a*) amplitude response; (*b*) differential phase performance.

always be center tapped. The operation of the transformer is easily explained with the aid of Figure 11.40.

If a voltage source of 2 V with impedance Z_0 is connected to the transformer's primary winding (port 4), the current I will induce a current of $I/2$ in the secondary with a voltage of V across each winding. When ports 1 and 2 are terminated with an impedance of $2Z_0$, voltage V and $-V$ appear across the outputs. By summing the voltages around the loop, it is found that no voltage appears at port 3; thus port 3 is a virtual ground.

A similar analysis can be used to describe the hybrid's operation when port 3 is driven. In this case, because of symmetry in the transformer, the current is
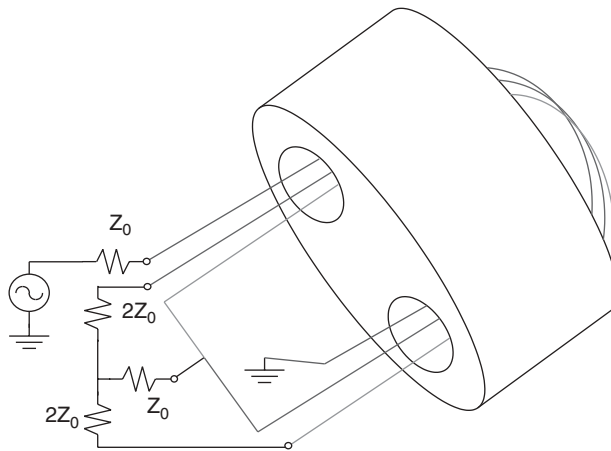
FIGURE 11.38 Transformer hybrid constructed on a binocular ferrite core with trifilar windings.
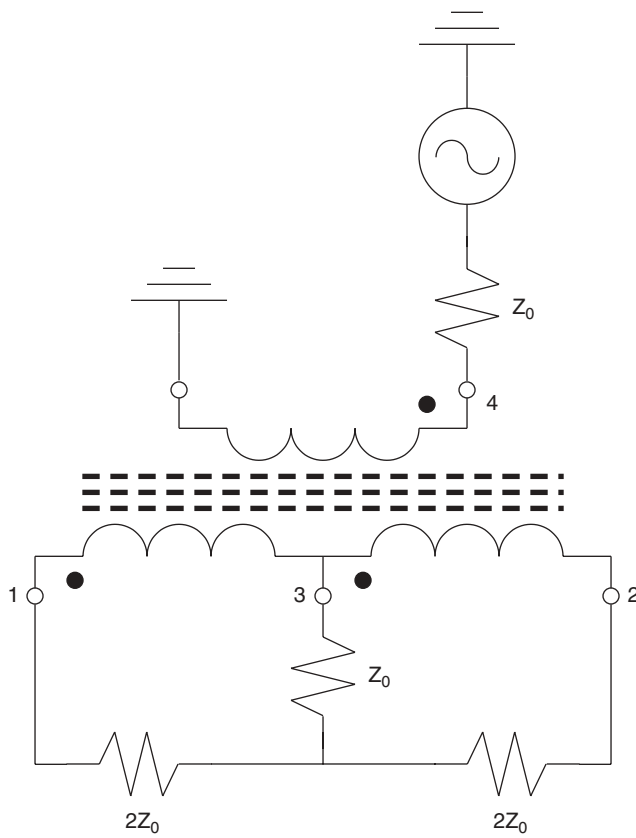
FIGURE 11.39   Wire diagram of 180° transformer hybrid.
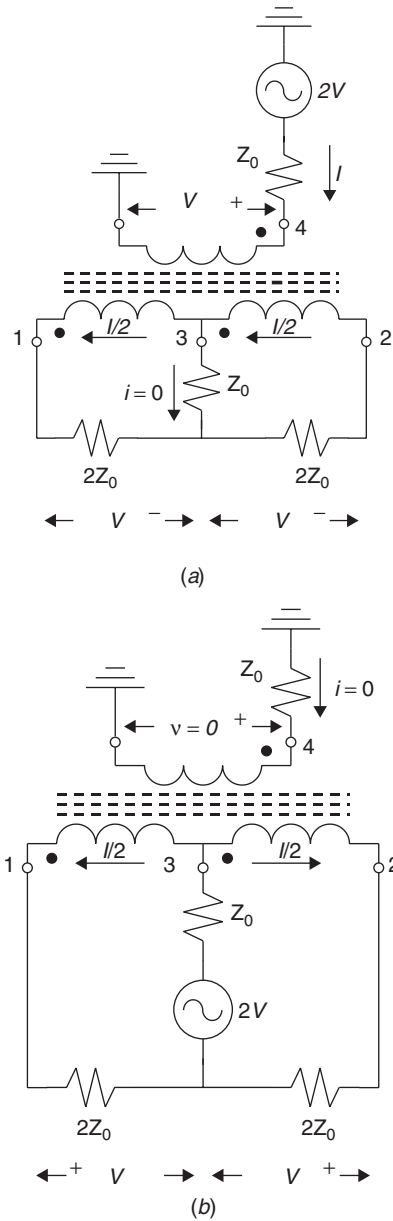
FIGURE 11.40   Voltage and current conditions in a transformer hybrid for various port excitations: (*a*) voltage source at port 4; (*b*) voltage source at port 3; (c) voltage at port 2; (d) voltage at port 1.

divided equally between each secondary winding. However, because the currents in the windings are in opposite directions, no current is induced in the primary winding. Instead, equal output voltages of magnitude V appear across the loads at ports 1 and 2. It should be noted that with this excitation the output voltages are in phase and the input power is divided equally.

(c)

(d)
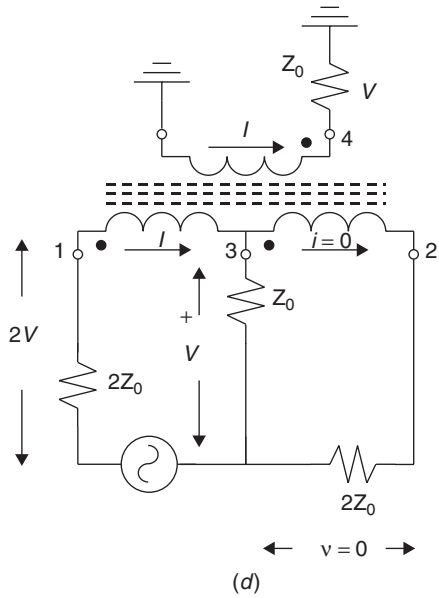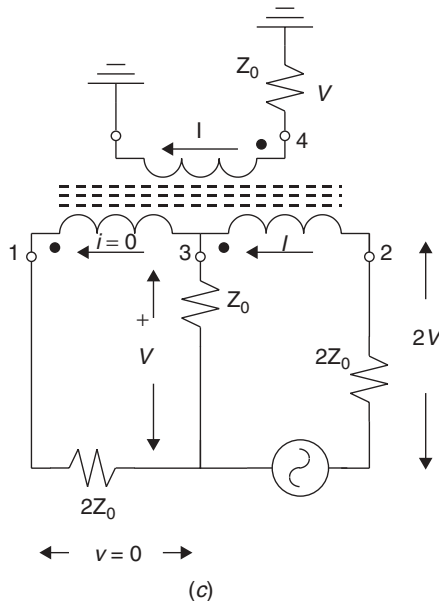
FIGURE 11.40   (*continued*)

When either port 1 or 2 is excited, operation of the hybrid is even more interesting. For example, if port 2 is driven, the current in the secondary winding nearest to the excited node must equal I; thus the voltage induced in that winding must equal V. Since the transformer is ideal, the current in the primary winding must also equal I; hence a voltage V will be present at port 4. Since there is a voltage V across the primary winding, there must also be a voltage V developed in the remaining winding. From Kirchhoff's laws, the voltage at port 1 must be zero.
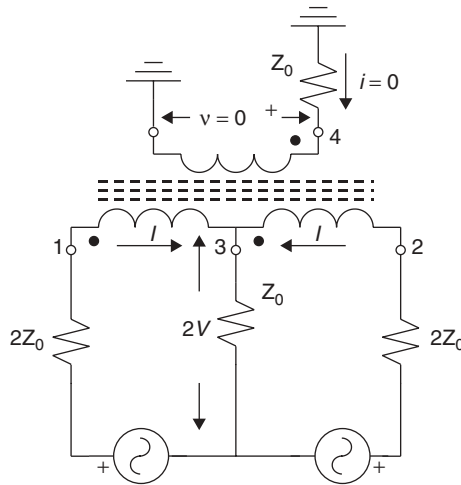
FIGURE 11.41   Voltage and current conditions in a transformer hybrid when ports 1 and 2 are excited in phase.

A fourth excitation mode, shown later to be the key to the operation of balanced mixers employing transformers, occurs when both ports 1 and 2 are driven with equal-amplitude in-phase signals. As shown in Figure 11.41, this mode of operation can be solved by applying the principles of superposition. By employing an analysis similar to that used in Figure 11.40c for the case when port 2 was excited, the current and voltage relationships for the case when port 1 is excited can also be obtained (Fig. 11.40d). Again, as in the earlier example, the opposite port, in this case port 2, exhibits a zero-valued output voltage. A current I is, however, developed in the primary winding but in the opposite direction. Hence, when ports 1 and 2 are both excited, the currents in the primary winding due to each source cancel, and all the power is summed to port 3 with no power delivered to port 4 (Figure 11.41). It should also be noted that if ports 1 and 2 are driven with out-of-phase signals, no power will be delivered to port 3 and all the power will be summed to port 4.

There are also other types of hybrid or balun structures that can be used in the design of single-balanced mixers, but they are typically used in double-balanced designs; therefore, they are described in the next section. Many variations of transformer hybrids involving multiple cores and coaxial windings also exist, but they are typically employed at frequencies below several hundred megahertz and when very low loss or high power-handling capability is desired.

Now that the operation of hybrids is understood, the design philosophy for single-balanced mixers can be described. Regardless of the frequency range involved and the method of construction, single-balanced mixers can be classified as either of two types: (1) designs utilizing 90° hybrids and (2) designs based on 180° hybrids. Which approach is taken depends strongly on the system application, since spurious performance and isolation differ considerably between the two mixer types. Single-balanced mixers have the added advantage of being able to provide some LO noise rejection in the receiving chain. AM noise rejection would be complete if every component in the mixer were perfect, such as diode matching and hybrid balance and isolation; however, rejection values of 20 to 30 dB can be obtained with practical designs [11.16].
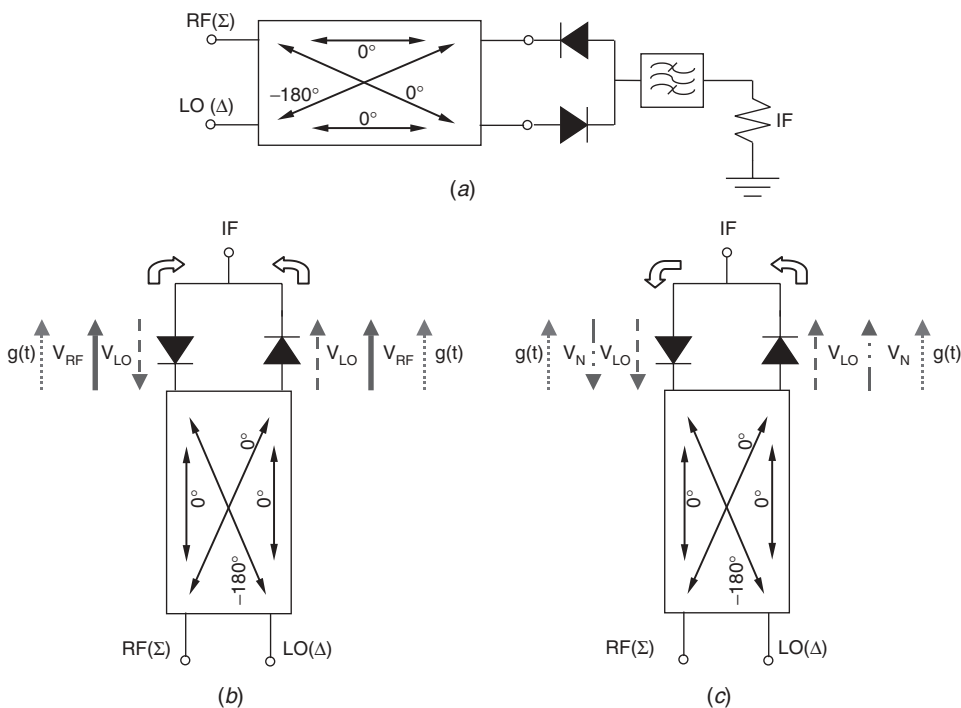
FIGURE 11.42 Phase relationships between LO, RF, IF, and AM noise voltages in single-balanced mixer: (*a*) mixer topology; (*b*) IF current summation; (*c*) AM noise cancellation.

To gain some insight into the performance variations of single-balanced mixers, we will analyze several configurations. The mixer topology illustrated in Figure 11.42*a* employs a 180° hybrid and two series-connected diodes. If the RF signal is applied to the sum port (port 1 of the ring hybrid shown in Fig. 11.33), the signal voltages at the diode ports will be in phase. Similarly, if the LO signal is applied to the delta port (port 2 of the ring hybrid), the pump voltage at the diode ports will be out of phase. In addition, with a perfect hybrid, no LO signal will be present at the RF port (port 1), regardless of whether the diodes are matched to the ring, as long as the diodes are identical. Hence, when matched diodes are employed, the L-to-R isolation of the mixer is essentially that of the hybrid. Thus this configuration usually offers superior L-to-R isolation performance to mixers employing 90° hybrids. However, the VSWR at the LO and RF ports of the ring hybrid will be that of the diode impedance mismatch in the system, which is unlike the case of quadrature coupler designs in that some improvement in port VSWR occurs beyond that obtained with the diode matching network.

Because of the phase relationships involved between LO and RF signals, the correct diode orientation must be selected so that the IF signal does not cancel. Since one of the diodes is reverse connected from the other and the LO signals are 180° out of phase, the diode conductance waveforms are in phase. The resultant IF waveforms from each diode are in phase due to the in-phase application of RF voltage. Thus the IF signal may be extracted at the node between the two diodes (Fig. 11.42*b*).

The situation concerning LO noise is somewhat different. The AM noise voltage present on the pump waveform enters the mixer at the delta port and appears at each diode out of phase. Since the conductance waveforms are in phase, the converted noise-generated products cancel at the mixer's IF port (Fig. 11.42c). In practice, complete cancellation does not occur because of imperfect diode matching and hybrid fabrication.

Determining the spurious performance is a bit more involved, but a qualitative analysis can be used to determine relative spurious characteristics for various topologies. The analysis begins by expressing the diode current, in one of the mixer arms, as an infinite series of the form

$$I_1 = aV_1 + b(V_1)^2 + c(V_1)^3 + d(V_2)^4 + \cdots \tag{11.51}$$

where V_1 is the total diode voltage ($V_{rf} + V_{lo}$). Reversing a diode is equivalent to reversing the applied voltage, which in turn changes the sign of the odd terms in the current expression. Thus the current for the other diode can be expressed as

$$I_2 = -aV_2 + b(V_2)^2 - c(V_2)^3 + d(V_2)^4 - \cdots \tag{11.52}$$

where V_2 is again the total diode voltage. Remembering that the LO signal is applied to the delta port, the voltages V_1 and V_2 can be expressed as

$$V_1 = V_{lo} \cos \omega_p t + V_{rf} \cos \omega_s t \tag{11.53}$$

$$V_2 = V_{lo} \cos \omega_p t + V_{rf} \cos \omega_s t \tag{11.54}$$

Substituting the expressions for diode voltage (11.53) and (11.54) into the expressions for diode current (11.51) and (11.52) and remembering that the current at the IF node is equal to

$$I_{if} = I_1 - I_2 \tag{11.55}$$

because one of the diodes is reversed, a qualitative spurious performance can be obtained. It can be shown that spurious responses arising from products of $mf_{rf} + nf_{lo}$ where m and n are even [(2,2), (4,4), ...] are eliminated and the (2,1) but not the (1,2), where $m = \pm 2$ and $n = \pm 1$, is eliminated. If the roles of the sum and delta ports are reversed, i.e., the LO voltage at the diode ports are in phase and the RF voltage is out of phase, the conversion loss performance, even-order spurious response, and isolation characteristics will not change. However, the (2,1) spurious product will be suppressed but not the (1,2). Hence the system performance must determine which port is used for LO injection. To determine exact spurious levels, a nonlinear mixer analysis must be performed.

The analysis of a single-balanced mixer realized with a quadrature coupler (Fig. 11.43) may be analyzed in a similar manner. As before, the hybrid is used to inject the LO and RF signals into each diode, which can be treated, as in the preceding example, as separate mixers. However, in this case, the RF and LO signals at the diode ports differ by 90°. This phase relationship is best illustrated with the aid of the phasor diagram of Figure 11.44. As can be seen in the diagram, at one arm of the hybrid the LO voltage leads the RF voltage, while at the other diode port, the RF voltage leads. But if one of the diodes is reversed, the phase difference between the diode conductance waveform and the applied RF voltage, at any instant of time, is the same
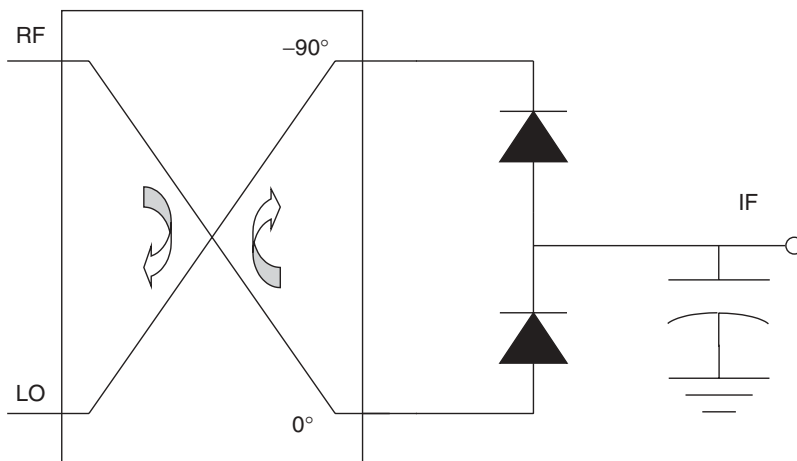
FIGURE 11.43 Single-balanced mixer employing 90° hybrid.
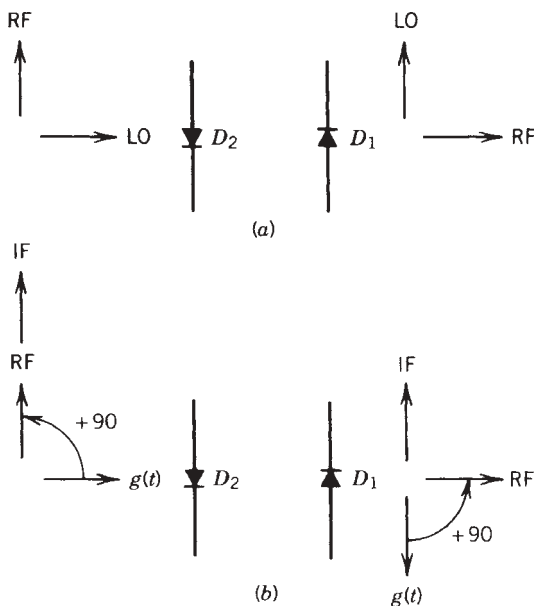
FIGURE 11.44 Phasor diagram illustrating LO, RF, and IF voltages: (*a*) RF and LO phase relationships at each diode; (*b*) phase relationships between RF, IF, and conductance waveform.

for both diodes. Since this phase difference is the same for each diode, the IF currents at the node between both diodes will be summed in phase; thus the IF signal can be extracted at that point in the circuit.

Aside from the differences in isolation and VSWR mentioned previously, the conversion loss characteristics with this approach are identical to those of a mixer realized with a ring hybrid. The even-order spurious performance is also equivalent, but there is no suppression of either the (1,2) or (2,1) spurious products.

11.5   DOUBLE-BALANCED MIXERS

The most commonly used mixer in the microwave portion of the spectrum is the double-balanced mixer. It usually consists of four diodes and two baluns or hybrids, although a double-ring or double-star design requires eight diodes and three hybrids. The double-balanced mixer has better isolation and spurious performance than the single-balanced designs described previously but usually requires greater amounts of LO drive power, are more difficult to assemble, and exhibit higher conversion loss. However, they are usually the mixer of choice because of their spurious performance and isolation characteristics.

A typical single-ring mixer with transformer hybrids is shown in Figure 11.45. With this configuration the LO voltage is applied across the ring at terminals L and L', and the RF voltage is applied across terminals R and R'. As can be seen, if the diodes are identical (matched), nodes R and R' are virtual grounds; thus no LO voltage appears across the secondary of the RF transformer. Similarly, nodes L and L' are virtual grounds for the RF voltage; hence, as before, no RF voltage appears across the secondary of the LO balun. Because of the excellent diode matching that can be obtained with diode rings fabricated on a single chip, the L-to-R isolation of microwave mixers can be quite good, typically 30 to 40 dB.

We can now analyze the performance of the mixer by applying the techniques described in Section 11.4 for a single-balanced mixers. With the LO and RF excitations shown in Figure 11.46a, the IF currents for each diode can be qualitatively determined by analyzing the phase relationships between the conductance waveform for each diode and the applied RF voltage.

To illustrate this concept, we will now analyze the performance of each diode. When the LO and RF voltages are applied as shown, the RF voltage and LO conductance waveform for diode D_1 are in phase; thus we can define an IF current in the direction of the diode symbol. Using the same convention, the RF signal and conductance waveform for diode D_2 are out of phase; hence the IF current is reversed from that of the first diode. Since diodes D_3 and D_4 conduct when the LO voltage polarity is reversed (Fig. 11.46b), their conductance cycles are reversed from that of diodes D_1 and D_2. Hence the IF currents in diodes D_3 and D_4 are reversed from the RF signal. With this LO voltage sense, the IF current can be summed at nodes R and R'. By reversing the LO voltage and applying the same analysis convention, the IF current relationships for
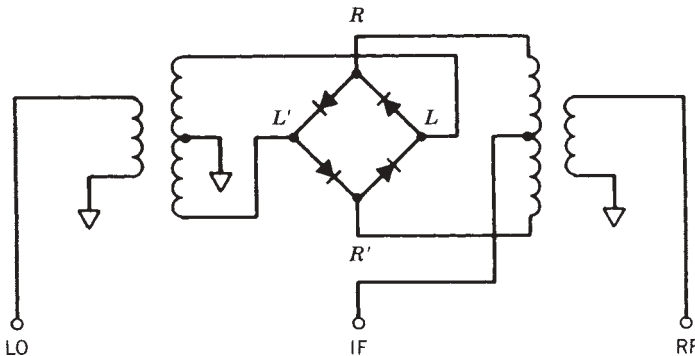
FIGURE 11.45   Circuit diagram of double-balanced mixer with transformer hybrids.
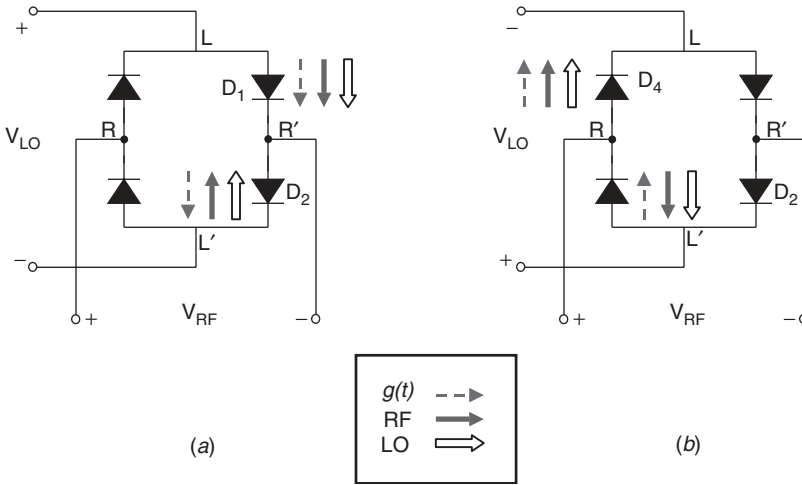
FIGURE 11.46   Phase relationships between LO, conductance waveform, RF, and IF voltages: (*a*) diodes D_1 and D_2 conducting; (*b*) diodes D_3 and D_2 conducting with LO signal reversal.

the diode ring are obtained. This time the IF current can be summed at nodes L and L' or the negative-going current can be summed at nodes R and R'. If the transformer hybrid performs as described in Section 11.4, the IF signal will combine at the center tap of the secondary winding of each balun. The IF signal can be extracted at either tap as long as the opposite tap is used to complete the IF circuit. No IF signal will be present at either the LO or RF port because no current is induced in the primary windings since the IF currents enter the arms of the balun in phase (even mode).

The analysis above is also valid if the balun or hybrids used in the mixer design have no center tap, which is usually the case at microwave frequencies above a few gigahertz; but the IF currents must be externally summed and prevented from being terminated by the RF and LO source impedances. This is commonly done in four-diode broadband double-balanced mixers used in the upper portion of the microwave spectrum.

The mixer circuit above can be analyzed further so that some insight into the spurious performance and embedding impedances for the diodes can be obtained. This analysis is easily accomplished because of the inherent isolation in the circuit, which allows the RF and LO analyses to be conducted separately.

If a transformer hybrid is designed with a $2:1$ turns ratio (Fig. 11.38), as is commonly done, each half of the secondary winding can be modeled as a voltage source V_{lo} with a source impedance of $2Z_{lo}$ (usually 100 Ω) connected across an antiparallel diode pair as shown in Figure 11.47*a*. Thus the LO current in diode D_1 can be expressed as

$$I_1 = a[V_{lo}] + b[V_{lo}]^2 + c[V_{lo}]^3 + d[V_{lo}]^4 + \cdots \qquad (11.56)$$

and the LO current in diode D_2, since it is reversed from diode D_1, can be expressed as

$$I_2 = a[-V_{lo}] + b[-V_{lo}]^2 + c[-V_{lo}]^3 + d[-V_{lo}]^4 + \cdots \qquad (11.57)$$

If we define the total LO current as $I_1 - I_2$, only odd-order terms will be present. However, all harmonics will be present in each diode, but the even harmonic currents
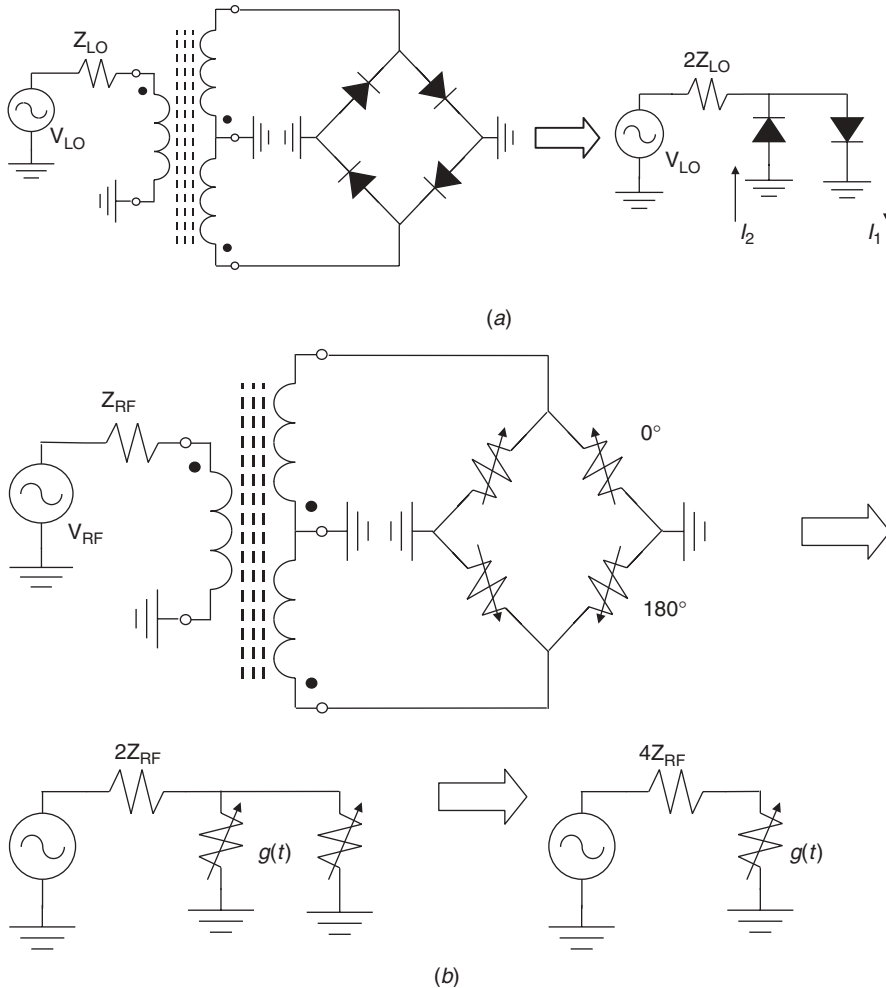
FIGURE 11.47   LO and RF equivalent circuits for single-ring mixer: (*a*) model used for spurious analysis; (*b*) RF embedding impedance circuit model.

will be equal and opposite for each antiparallel diode pair, giving rise to zero-valued embedding impedances for even LO harmonics as well as for the dc component. Of course, the odd harmonic embedding impedances are still determined by the balun. As in the past example of the single-balanced mixer, double-balanced mixers reject spurious responses produced by $mf_{rf} + nf_{lo}$ frequency components when m or n is even, and provide no suppression of odd-ordered products. By employing a similar analysis, the embedding impedances at the RF (Fig. 11.47*b*) for each diode can be shown to be $4Z_{rf}$ (typically, 200 Ω). At the IF, all four diodes are connected in parallel; hence the embedding impedance for each diode is $4Z_{if}$ (typically, 200 Ω).

Another version of the double-balanced diode ring mixer, which is essentially its dual, is the star mixer. A transformer hybrid realization of the star mixer is shown in Figure 11.48. When transformer hybrids are employed in the mixer design, no advantages over conventional approaches are obtained, although some clever mixer
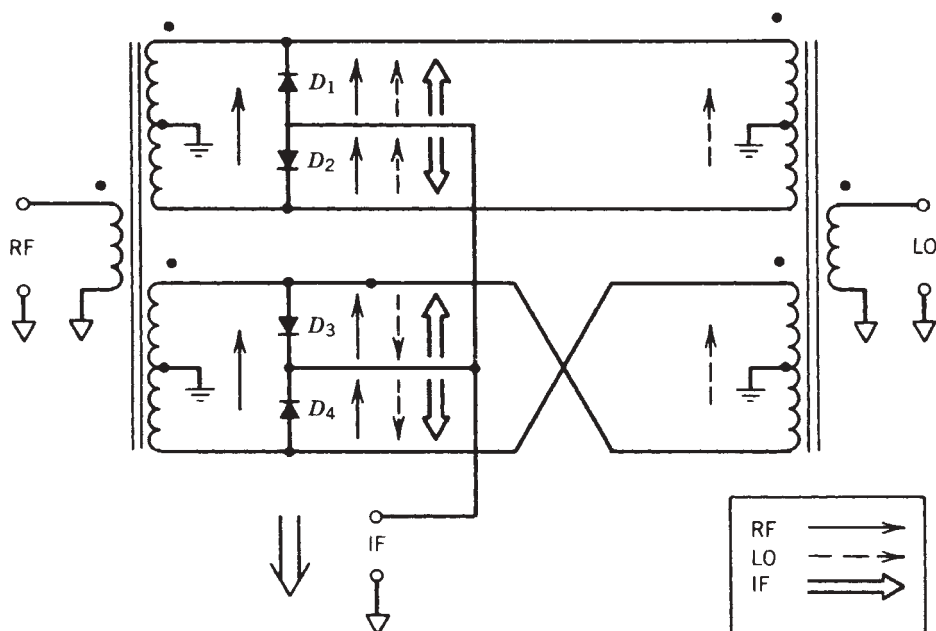
FIGURE 11.48 Circuit diagram of star mixer with multiple secondary transformer hybrids.

circuits have been built with coaxial and microstrip baluns. These microstrip or coaxial mixers are sometimes easier to assemble than conventional realizations.

An extension of the double-balanced ring mixer is the double-ring or double-star double-balanced mixer, referred to occasionally as the double-double-balanced mixer. As can be seen in Figure 11.49, multiple secondary windings are required on the LO and RF baluns, and an additional IF balun is also needed. Because of the four extra diodes, twice as much pump power is required, but since the RF signal is divided eight ways instead of four, the LO-to-RF signal power ratio at each diode is greater, thus extending the mixer's large-signal saturation level. The conversion loss characteristics for a double-ring mixer are approximately equal to that of single-ring designs; hence a true improvement in receiver dynamic range can be obtained, at the expense of LO power, by using this approach. In addition, the IF balun, although adding to the circuit complexity, does allow for completely independent IF extraction regardless of its frequency range provided that the balun still functions. This is another subtle advantage of double-ring and double-star mixers. Occasionally, double-ring mixers are constructed with diode rings that employ multiple series diodes in each leg in order to increase the mixer's compression point. Unfortunately, the extra diodes in the ring(s) do degrade the conversion loss, but at frequencies below 30 mHz, where receiver sensitivity is limited by atmospheric noise, and where signal levels at the antenna terminals can reach several hundred millivolts, the extra dynamic range is usually welcomed.

Up until now, we have described the operation of double-balanced mixers that employ transformer hybrids. As the frequency of mixer operation is extended beyond several gigahertz, transformer hybrids can no longer be fabricated. At these frequencies, transmission line baluns begin to dominate, and by time the operating frequency reaches
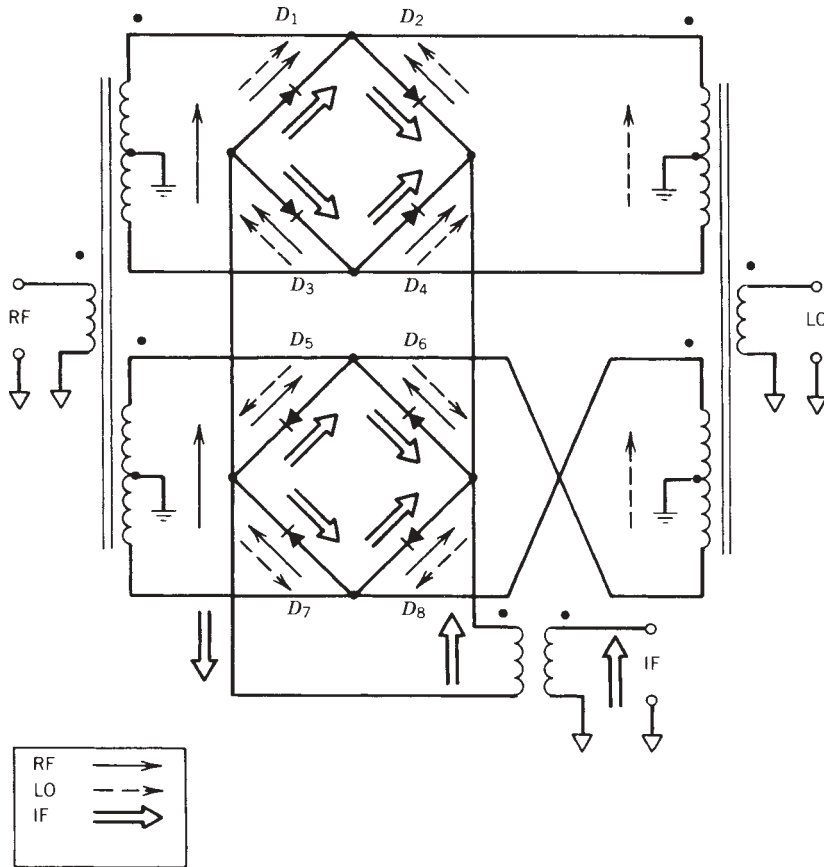
FIGURE 11.49 Low-frequency representation of double-double-balanced mixer.

4 or 5 GHz, a few coupled inductors, fabricated on GaAs substrates, are the only structures resembling transformers that are found.

The simplest of baluns can be realized by employing a length of balanced transmission line 90° in length, connected so that one conductor at the unbalanced end is grounded, with the balanced load (or source) connected across both conductors at the other end (Fig. 11.50*a*). The structure is indeed a balun, since the current in one terminal at the balanced end is equal and opposite to the current in the other terminal. At the center frequency of the structure, the balanced end is also isolated from ground. Baluns of this type can easily be realized, for example, with insulated twisted wire, such as enameled magnet wire, parallel-plate transmission line, or edge-coupled parallel coplanar strips. Another form of quarter-wavelength balun can be constructed with coaxial cable as shown in Figure 11.50*b*. In this case an additional conducting jacket is added around the outside of the cable to form a second transmission line of a noncritical impedance value. If the outer shield is connected to the original coaxial cable's jacket 0.25 wavelength away from the balanced end, a short-circuited transmission line is formed. The resultant quarter-wavelength shorted line effectively chokes any current that may tend to exist on the outside of the original transmission line's shield, thus preventing unbalancing and forcing the currents at the balanced end to be
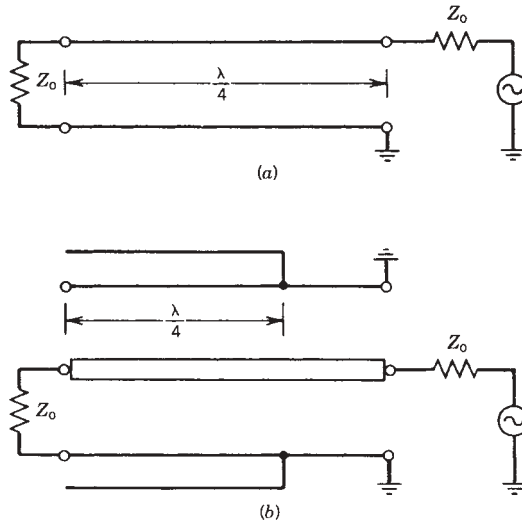
FIGURE 11.50   Simple balun structures: (*a*) balanced-line quarter-wavelength-long balun; (*b*) coaxial balun.

equal and opposite in the center conductor and shield. Although these structures are simple, they exhibit limited bandwidth and are of little use in broadband mixer design.

A clever coaxial balun [11.17], which can be designed to exhibit many decades of bandwidth, is the unbalanced-to-balanced coaxial transition (Fig. 11.51*a*). This structure was first realized by gradually removing the shield along the length of a coaxial cable until only two point connections (terminals) for the center conductor and outer jacket exist at the balanced end. This structure exhibits a very soft low-frequency cutoff point which is reached when the length is approximately 180° at the lowest frequency of operation. However, good performance can be obtained at frequencies several octaves lower. A very popular version of this type of balun is the microstrip-to-parallel-plate line transition [11.18, 11.19] (Fig. 11.51*b*) commonly used in many mixers and antenna feed structures. This structure, which can be built with various impedance contours and ground plane tapering schemes, also exhibits high-pass performance with a very soft low-frequency cutoff characteristic.

Transmission line structures which are naturally balanced, such as slotline and finline, can also be used as balanced feed in mixer design. However, all of the structures above, and the more complex transmission line structures to follow, exhibit one major drawback compared to a transformer hybrid: There is no true RF center tap. As will be seen, this deficiency in transmission line structures extensively complicates the design of microwave balanced mixers.

The lack of a balun center tap does indeed complicate the extraction of IF energy from the structure, but if the IF is low, diplexing can be employed to ease performance degradation. This concept is illustrated in the following design example of a double-balanced 2- to 12-GHz mixer. It will be assumed that because of the soft-substrate transmission line media and frequency range, a packaged diode ring with known impedances will be used. For Si diodes in this frequency range, the typical LO impedance range (magnitude) is on the order of 75 Ω, while the RF impedance is approximately 50 Ω. With these values in mind, microstrip-to-parallel-plate transmission line baluns similar
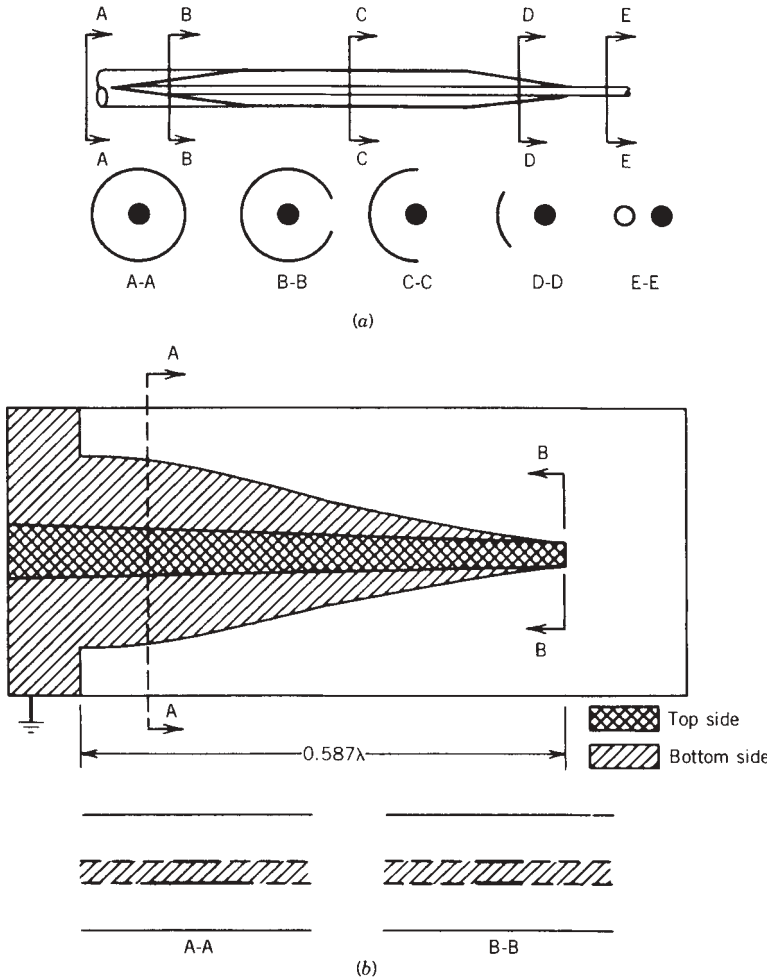
FIGURE 11.51 Broadband high-pass balun structures: (*a*) coax to balanced line; (*b*) microstrip to parallel-plate line.

to the design illustrated in Figure 11.51*b* can be fabricated on soft-substrate material. For baluns of this type that require impedance transforming, a Dolph–Chebyshev contour of impedance values along the balun's length yields excellent broadband performance. These types of tapers can be approximated by dividing the balun into at least 20 segments, with each segment being equally spaced along its length. The cross-sectional dimensions, which can be analyzed as asymmetrical broadside suspended coupled strips, are adjusted so that the desired impedance contour is achieved. It should be noted that the dimensions at each end of the balun are fixed; that is, the balanced end must terminate in a parallel-plate transmission line, and the unbalanced end must terminate as microstrip. However, the ground-plane width at the microstrip end must only be wide enough to simulate microstrip performance, which can usually be accomplished with a width greater than 5 to 10 substrate thicknesses. These boundary conditions constrain the ground-plane side of the structure taper dimensions

but not the taper. The taper from microstrip to balanced line can be linear, exponential, or determined empirically, although a cosine taper seems to yield the best results.

The completed mixer assembly with package diode ring and its equivalent circuit are shown in Figure 11.52. As can be seen, both the RF and LO baluns terminate at the diode ring and provide the proper excitation. But since there is no center tap, the IF must be summed from the top and bottom of either balun. This summing is accomplished with bond wires that have high reactances at microwave frequencies but negligible inductances at the IF. Blocking capacitors form the second element in a high-pass filter, preventing the IF energy to be dissipated externally. An IF return path must also be provided at the terminals of the opposite balun. The top conductor side of the balun is grounded with a bond wire, providing a low-impedance path for the IF return and a sufficiently large impedance in shunt with the RF path. The ground-plane side of the balun provides a sufficiently low impedance for the IF return from the bottom side of the diode ring. The balun inductance and blocking capacitor also form a series resonant circuit shunting the IF output; therefore, this resonant frequency must be kept out of the IF passband.

The upper frequency limit of mixers fabricated using tapered baluns and low parasitic diode packages, along with a lot of care during assembly, can be extended to 20 GHz. Improved "high-end" performance can be obtained by using beam-lead diodes. Although this design technique is very simple, there is little flexibility in obtaining an
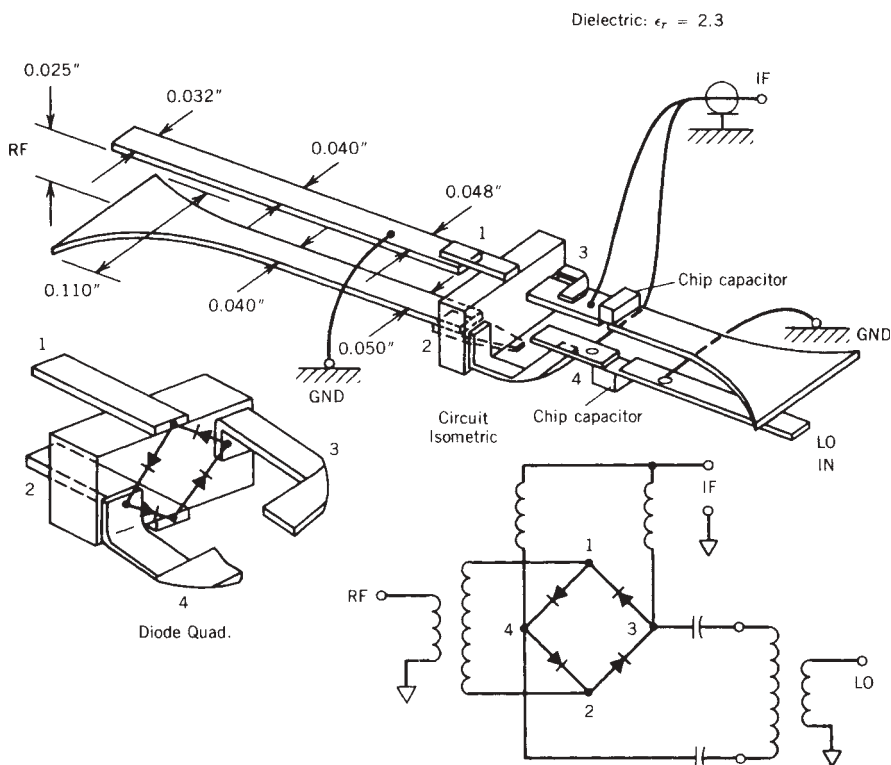
FIGURE 11.52   Double-balanced mixer constructed with microstrip-to-parallel-plate line baluns.

optimum port VSWR since the baluns are designed to match the magnitude of the diode impedance. The IF response of using this approach is also limited, due to the lack of a balun center tap, to a frequency range below the RF and IF ports.

A slightly more complex balun structure can be formed by combining two quarter-wavelength-long coupled line pairs as illustrated in Figure 11.53. Without any compensation, this structure can exhibit greater than an octave of bandwidth and can be realized in a variety of media, such as coaxial cable, microstrip, and parallel-plate transmission line. The structures typically demonstrate excellent phase balance between ports, due to the nature of the coupling mechanism and good amplitude balance. The input VSWR on the unbalanced port is the limiting performance factor.

However, when this structure is realized with coaxial cable, currents existing on the outside of the jacket unbalance the system and are unpredictable. An outer conductor can be added, as was done on the simple coaxial balun illustrated in Figure 11.50b, to eliminate unwanted currents and radiation and to restore balance. The resultant structure, developed by Marchand [11.20] in 1944 and illustrated in Figure 11.54a, with its circuit model shown in Figure 11.54b, is sometimes referred to as the compensated Marchand balun. The structure can be realized with as many as four different impedance transmission lines with different lengths. Hence a considerable amount of flexibility in matching is possible since the balun is a multielement bandpass network. Usually, Z_1 and Z_2 are designed to be of equal value, and Z_{s1} and Z_{s2}, which are effectively in series and then shunted across the balanced load, are made as large as possible. Transmission line Z_b has a characteristic impedance value equal to that of the balanced termination, although it can be used as a matching section. If proper filter synthesis methods are employed in the design of the compensated balun, excellent multioctave performance can be obtained. Coaxial structures are, however, cumbersome to integrate into mixer topologies, but some designs employ simpler versions of the foregoing structure that employ the mixer housing to form the outer balun shield.

An excellent example of this technique, which can be used in the design of octave or multioctave bandwidth mixers, will now be illustrated. The mixers consist of dual RF and LO baluns fabricated with semirigid coaxial cable and four diodes connected in a star, rather than a ring, formation. The length of each half of the dual balun is 180°
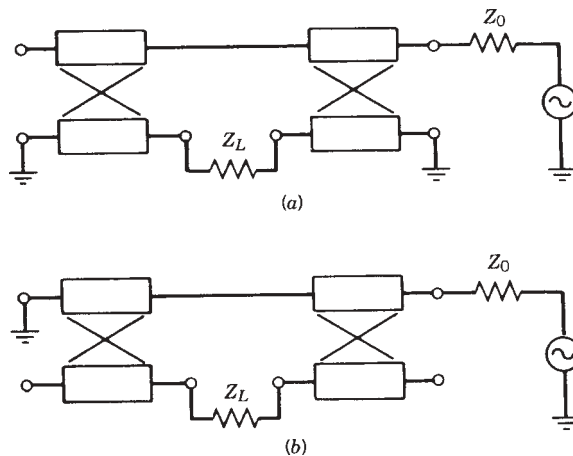
FIGURE 11.53 Planar-coupled line balun structures.
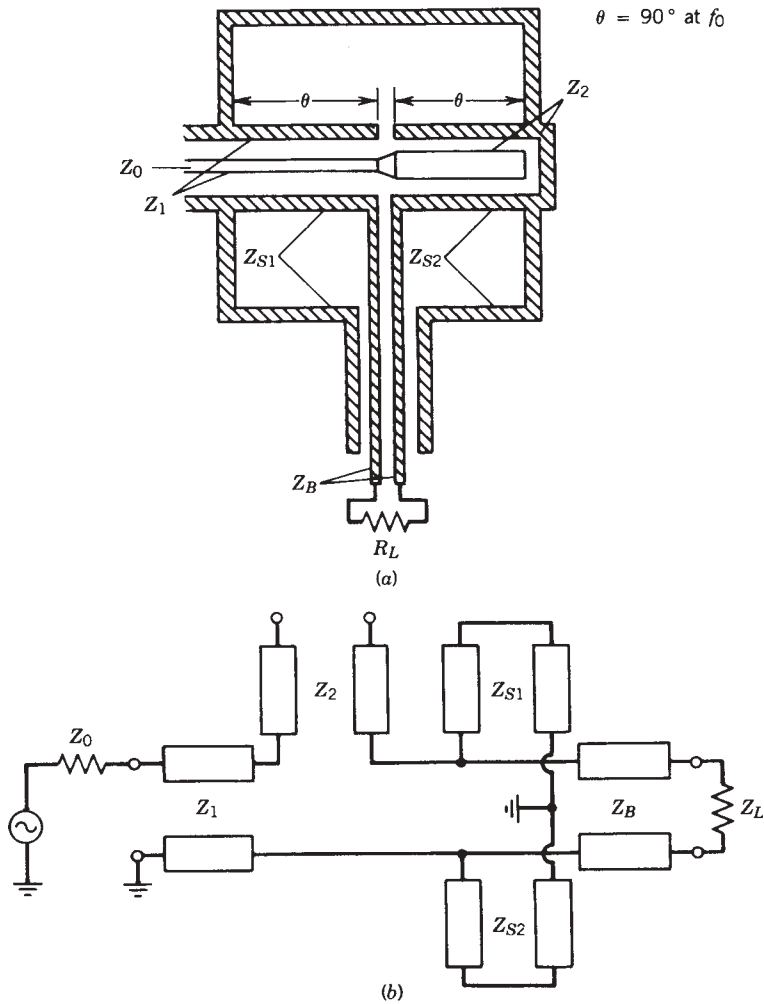
FIGURE 11.54   Marchand compensated balun: (*a*) coaxial cross section; (*b*) equivalent transmission line model.

at the band center frequency, with the outer jacket of the cable cut in the center to form the balun output (Fig. 11.55). The ends of the balun are connected to ground, while the remainder of the structure is suspended. The IF energy is extracted at the center of the diode star, with the IF return path being formed by the balun outer conductor. It should be noted that the upper frequency limit of the mixer occurs when the total length of the balun becomes $360°$. The IF upper limit occurs at the RF band center, that is, when the IF return path is $90°$ in length.

Star structures of this type solve the IF overlapping problem encountered with the previous design approach and exhibit excellent octave bandwidth performance. However, extra care must be employed in selecting the diodes and balun impedances since there is even less flexibility in obtaining an optimum port VSWR.

A suspended substrate version of the compensated balun is easily realized with a parallel-plate transmission line [11.21]. As in the coaxial case, four distinct distributed
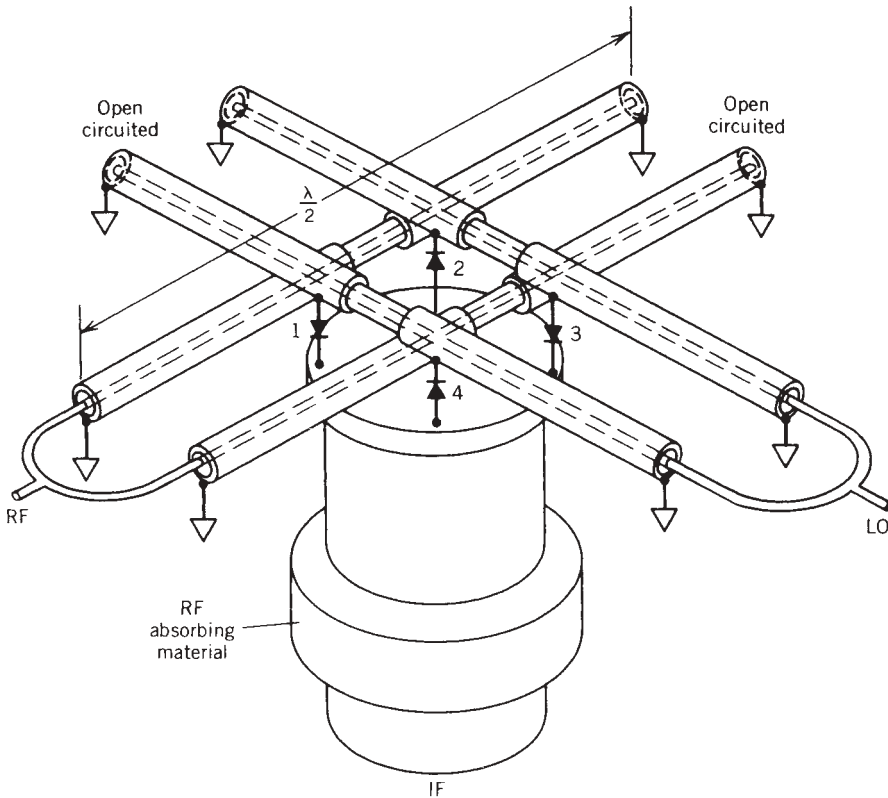
FIGURE 11.55 Octave bandwidth double-balanced mixer using coaxial compensated balun.

elements exist and can be used to the designer's advantage. A typical balun fabricated on a soft-substrate low-dielectric medium (not shown) is illustrated in Figure 11.56*a* and its equivalent circuit is shown in Figure 11.56*b*. It is evident from the illustration that the balun performance is influenced by the packaging since the impedance of several elements, especially Z_{s1} and Z_{s2}, is dependent on the spacing between the substrate and the ground planes. Although a center tap is shown in the equivalent circuit, it is a virtual center tap and is completely valid only at dc, as is the case in all distributed baluns. When the IF is low, Z_{s1} and Z_{s2} form an adequate IF return path for most applications.

A dual version of the balun above can easily be constructed by adding a second conducting strip parallel to Z_{s1} and Z_{s2} (Fig. 11.57). Dual baluns [11.22] of this type have many applications, such as providing the power-dividing function on a common LO port for a phase-tracking mixer pair or providing the equivalent of two secondary windings which are required when realizing double-ring or double-star mixers. Little to no degradation in performance occurs by adding a second strip, and when the dual balun is used to feed two mixers, a small amount of isolation is obtained. There is also a subtle advantage with planar baluns of this type in that the balanced output is in the plane of the substrate rather than normal to the substrate, as is the case with the microstrip-to-parallel-plate balun. A space quadrature relationship of this type can be useful in eliminating crossover connections which are common in multidiode designs.
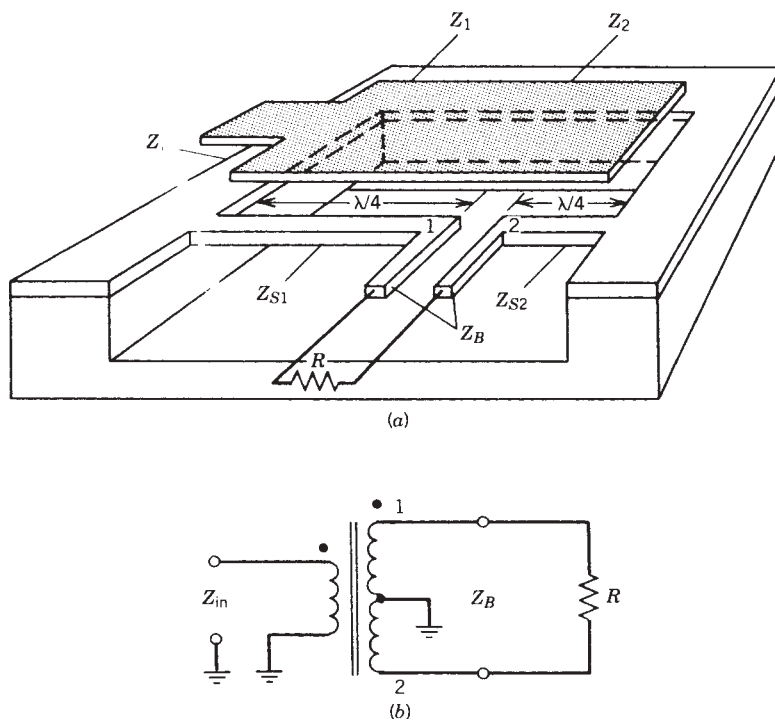
FIGURE 11.56   Planar compensated balun fabricated on a low-dielectric substrate: (*a*) metallization pattern and package floor; (*b*) low-frequency equivalent circuit model.

When hard substrates such as quartz and alumina are used in mixer construction, the added mechanical advantage relative to soft substrates allows the designer to eliminate package parasitics by employing beam-lead or chip diodes. The reduction in parasitics, in conjunction with the elimination of excess diode lead lengths and crossover connections, dramatically extends the upper frequency limit of the typical mixer structure. For example, the interconnections between diodes and baluns can be virtually eliminated by selecting an LO and RF balun structure with orthogonal orientations of the balanced signal, because the diodes can be mounted directly to the conductor surfaces. A typical diode and balun interconnect arrangement is shown in Figure 11.58. With this arrangement a diode pair is bonded to the top surface of the substrate, while a second pair is bonded to the bottom surface. Plated-through holes are used to connect the two pairs into a conventional ring. As can be seen, there is less than 0.3 mm of excess length in the structure.

This design technique has been applied to the realization of a 20- to 40-GHz double-balanced mixer [11.23, 11.24]. The mixer, which is shown in Figure 11.59, consists of a microstrip-to-parallel-plate line balun (Fig. 11.51*b*) and a compensated planar balun similar to the design illustrated in Figure 11.56, except that both baluns are fabricated on a quartz substrate. Interdigitated capacitors were also used in the IF diplexer circuit to eliminate loss and parasitics. The circuit model for the mixer is shown in Figure 11.60 and is similar to the models described previously. The conversion loss and isolation performance are shown in Figure 11.61. As can be seen, the performance is comparable to that of the best low-frequency designs.
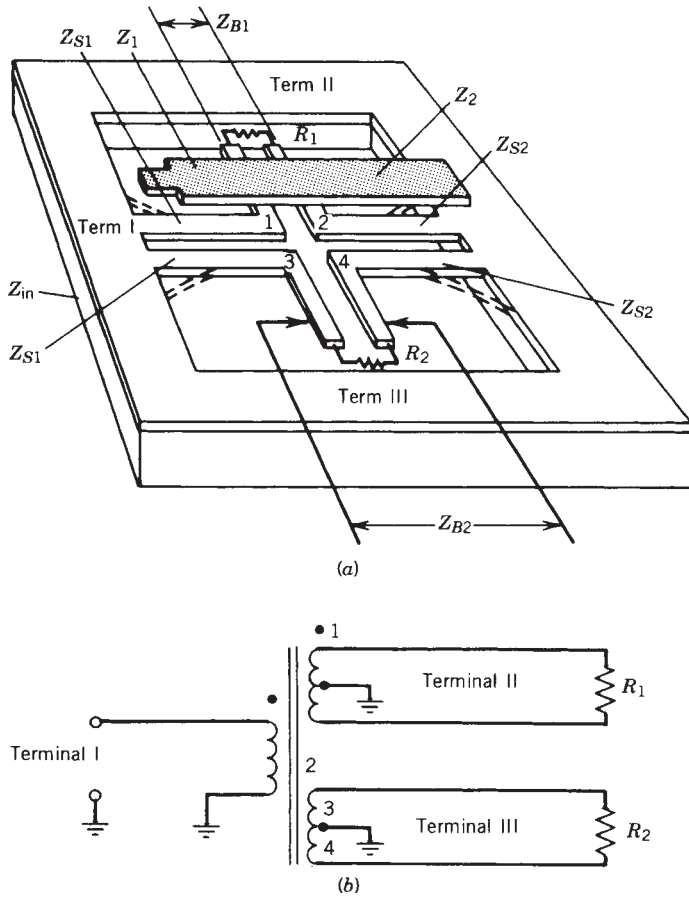
FIGURE 11.57 Dual planar compensated balun: (*a*) metallization pattern; (*b*) low-frequency equivalent circuit model.
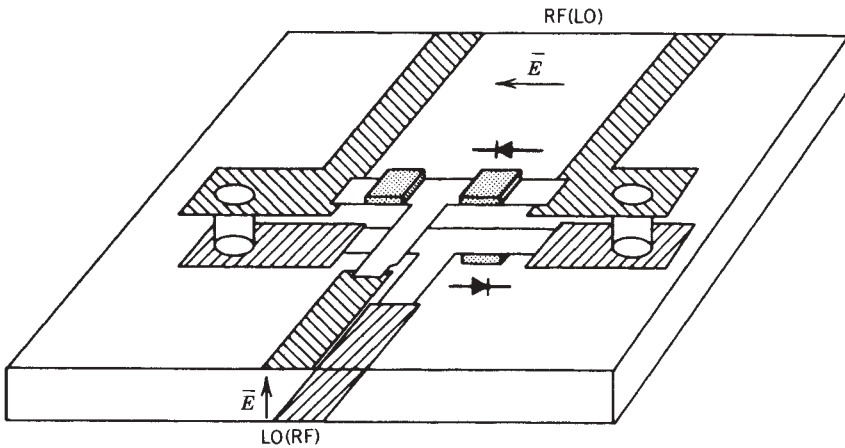
FIGURE 11.58 Interconnect configuration for planar orthogonal baluns and diode ring.
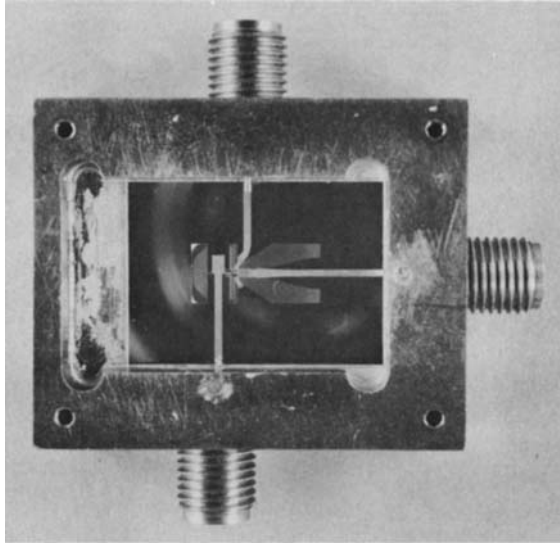
FIGURE 11.59 Double-balanced mixer for 20- to 40-GHz operation fabricated on a 0.25-mm-thick quartz substrate. (Courtesy of Texas Instruments.)
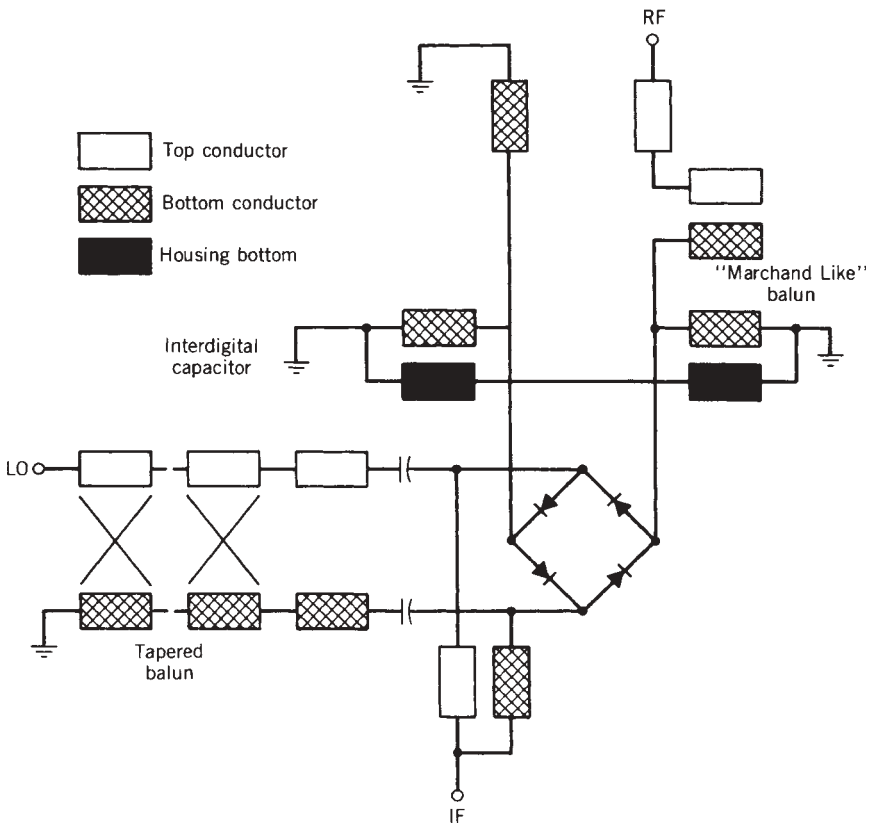
FIGURE 11.60 Circuit model for 20- to 40-GHz mixer.
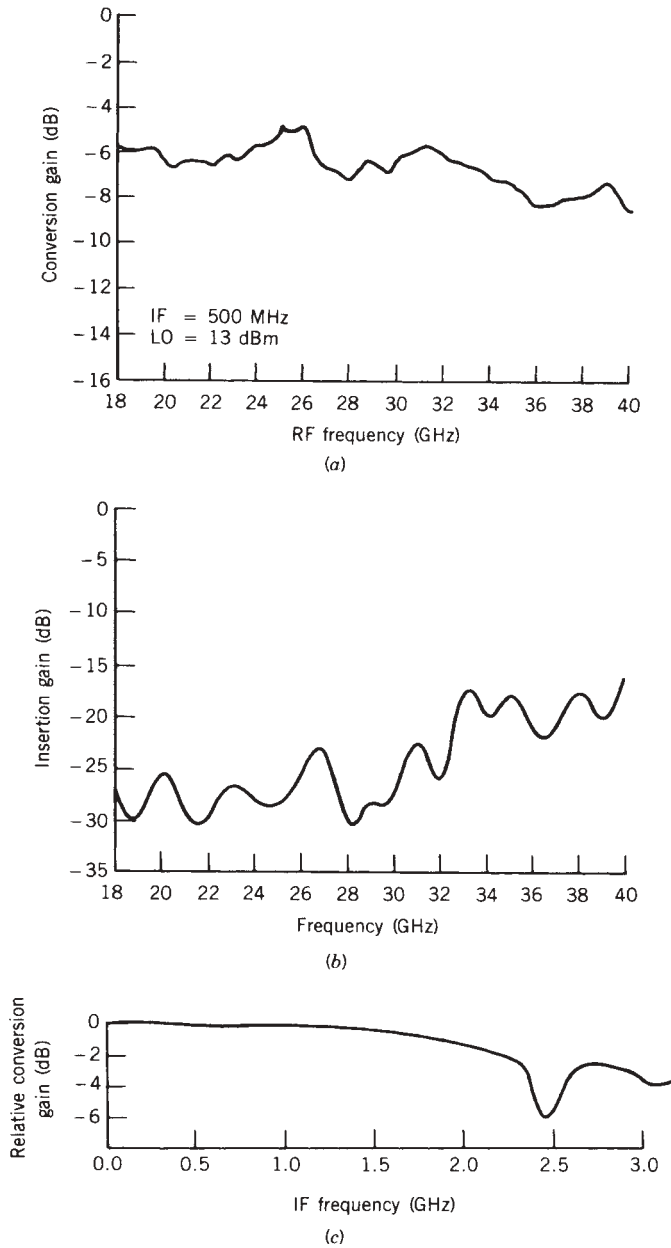
FIGURE 11.61   The 20- to 40-GHz mixer performance: (*a*) conversion loss; (*b*) isolation; (*c*) IF response.

Planar-compensated baluns can also be used in the design of star mixers, provided that dual secondary windings or their equivalent are available from the balun structure. Dual secondary performance can be obtained, as described above, by adding a second coupled conductor set to the balun feed (Fig. 11.57). If two such structures are orthogonally connected within the plane of the substrate, as depicted in Figure 11.62,
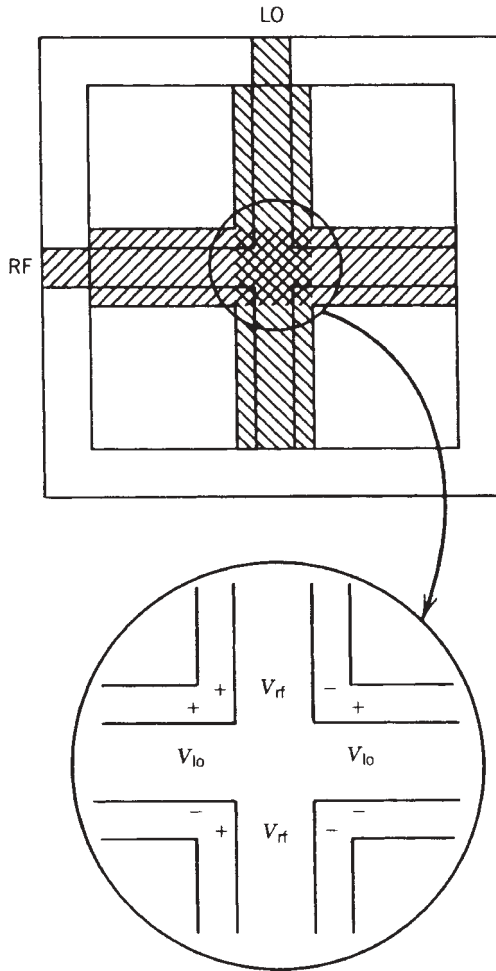
FIGURE 11.62   Dual-balun circuit arrangement for star mixer.

and the feed structures are bridged, the resulting four-node junction will have the proper voltage excitation and phasing for a star mixer. A star mixer employing this technique with glass-packaged diodes is shown in Figure 11.63. The IF response of mixers fabricated in this manner is quite broadband, exhibiting a gentle slope as a function of frequency until cutoff is reached (f_0 of balun).

By properly selecting the balun dimensions, an unbalanced source impedance of 50 Ω can be conveniently transformed anywhere within a 50- to 150-Ω impedance range. The circuit bandwidth is almost always greater than an octave and is strongly influenced by the impedance of the open-circuit transmission line in the feed structure (Z_2).

Typically, the lower this impedance can be made, the greater the bandwidth; hence the selection of a thin dielectric will tend to prevent the line widths from becoming unreasonably large when striving for the lowest possible impedance. Typical VSWR
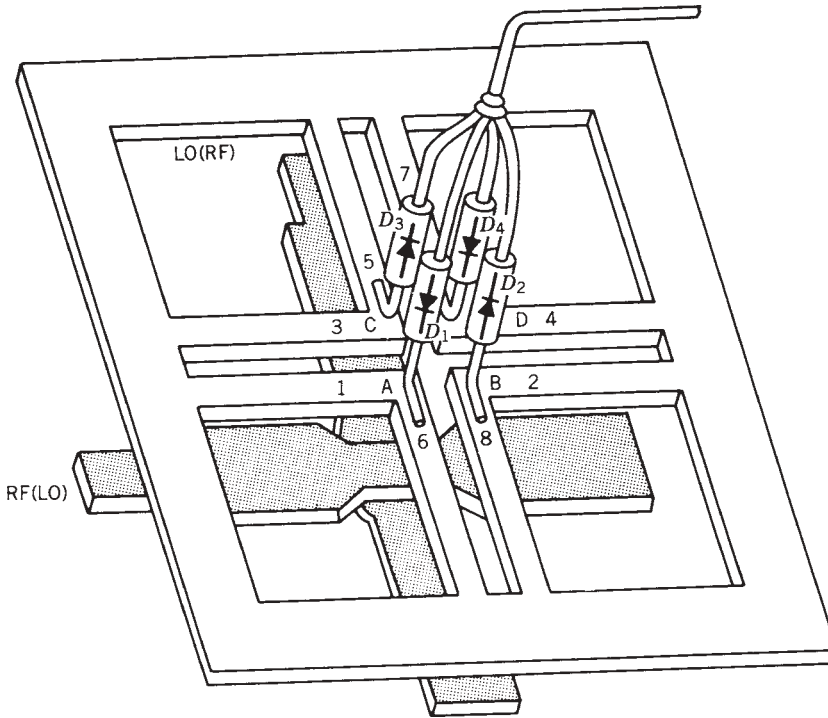
FIGURE 11.63   Star mixer employing glass packaged diodes.

(unbalanced port) performance and a transmission line model for the dual balun are shown in Figure 11.64.

Double-double-balanced or dual-ring mixers also require balun structures that simulate multiple secondary windings. Microstrip-to-parallel-plate transmission line baluns, similar to the configuration illustrated in Figure 11.51*b*, if connected in parallel at the unbalanced end, produce the equivalent of the dual planar-compensated balun, with the exception of the balanced output voltage orientation. As in the single-balun case, the balance output of this type of balun is normal to the plane of the substrate. A typical circuit configuration for the balun type above is illustrated in Figure 11.65. A phase reversal can also be placed in one arm of the dual balun (Fig. 11.65*b*) so that the arm-to-arm voltage orientation is odd. This arrangement can be advantageous, as will be shown later for some mixer topologies.

The mixers described previously, although capable of considerable bandwidth performance, in general exhibit two main drawbacks: (1) IF bandwidth and extraction difficulties and (2) dynamic range. As we remember from the mixer descriptions above, multiple-ring structures, due to the fact that the IF can be independently extracted at the junction of the two rings, can have overlapping RF, IF, and LO frequency ranges. The extra diode ring, which implies that the mixer will require 3 dB more pump power than will a conventional single-ring design, will also exhibit 3 dB greater compression and distortion characteristics. The major drawback to multiple-ring designs is their added complexity.
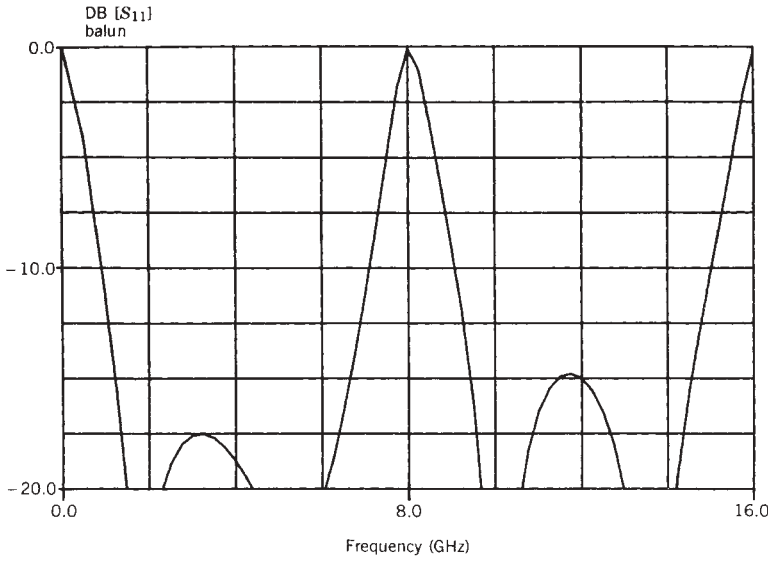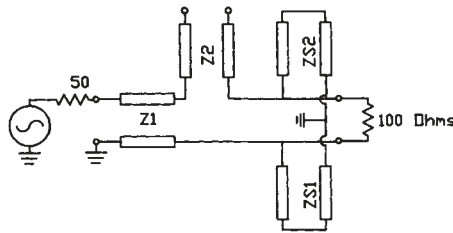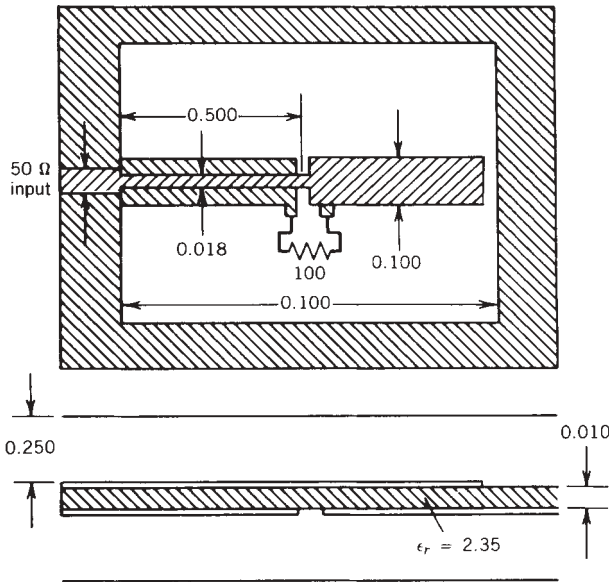
FIGURE 11.64 Typical dual planar-compensated balun: (*a*) unbalanced port VSWR; (*b*) transmission line model; (*c*) element values.
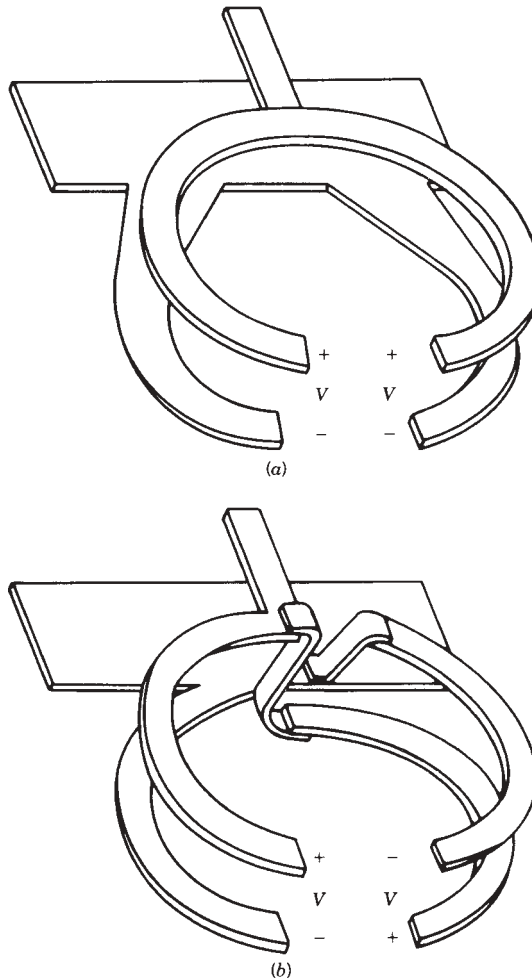
FIGURE 11.65 Dual microstrip-to-parallel-plate line baluns: (*a*) even excitation; (*b*) odd excitation.

When one examines the low-frequency model of a multiple-ring mixer such as the one depicted in Figure 11.49, the actual microwave construction and assembly problems are somewhat elusive. However, when Figure 11.66 is examined, which illustrates a typical broadband double-ring design employing a variation of the microstrip-to-parallel-plate line balun, the complexity becomes apparent. It should be noted that the substrate is not a single piece of material, but two separate circuits assembled orthogonally within the housing. This orientation of the substrates is not a problem when the mixer is assembled in a housing by itself, but a miserable integration results when trying to combine the mixer with other planar components.

The problem is eased somewhat by employing the approach depicted in Figure 11.67. This structure also uses a modified version of the microstrip-to-parallel-plate line balun described previously, with the addition of a phase reversal at the feed of one of the dual baluns. This reversal allows the substrate to be continuous, although it still needs to be suspended to preserve performance.
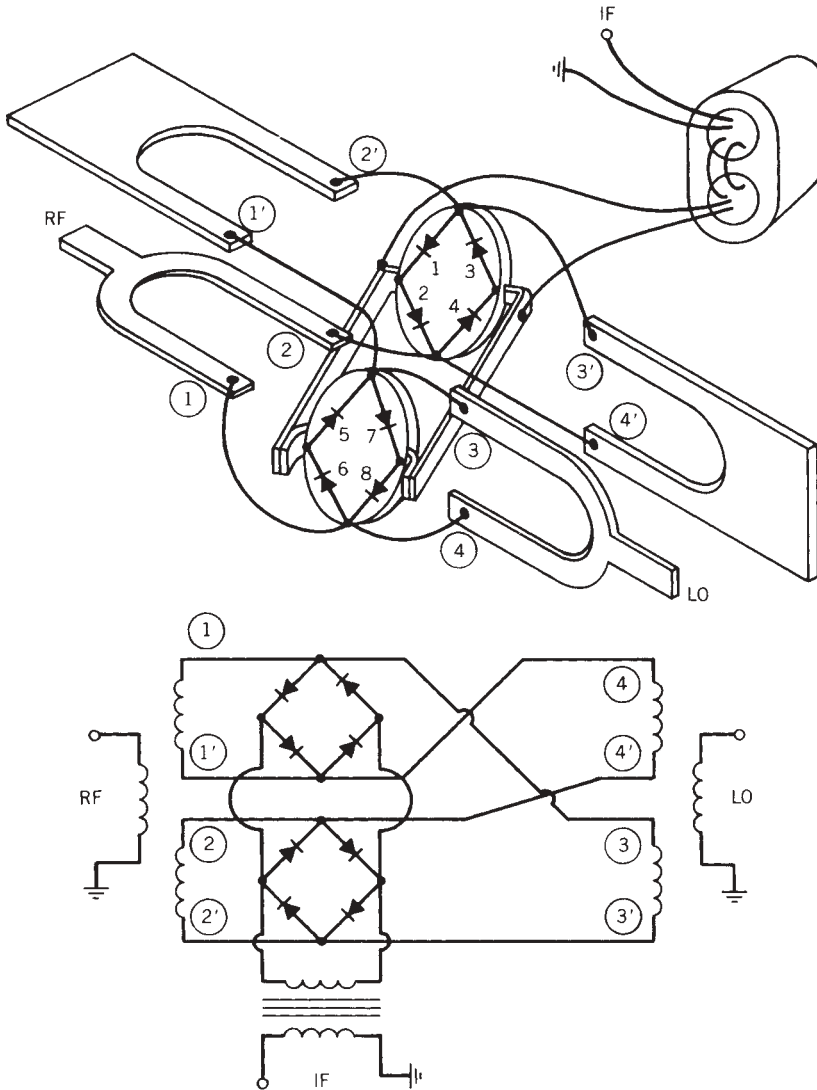
FIGURE 11.66   Double-ring mixer using orthogonal microstrip-to-parallel-plate line baluns.

Both of the double-ring designs above exhibit conversion loss characteristics similar to those of single-ring designs (6 to 10 dB) when more pump power is available, with the added advantage of overlapping frequency ports and higher dynamic range. These designs also exhibit the same RF and LO bandwidth capabilities as those of single-ring designs, with several decades of performance not uncommon. However, as one would expect, the IF bandwidth is limited by the IF balun performance. The ferrite baluns shown can be made to operate up to several gigahertz, provided that the total wire length is less than a half-wavelength. If greater bandwidth is desired, a microstrip-to-parallel line balun can be used for microwave IF operation, since its low-frequency cutoff must still be preserved, but unfortunately, the substrate orientation will, again, in all likelihood need to be orthogonal to the main substrate.
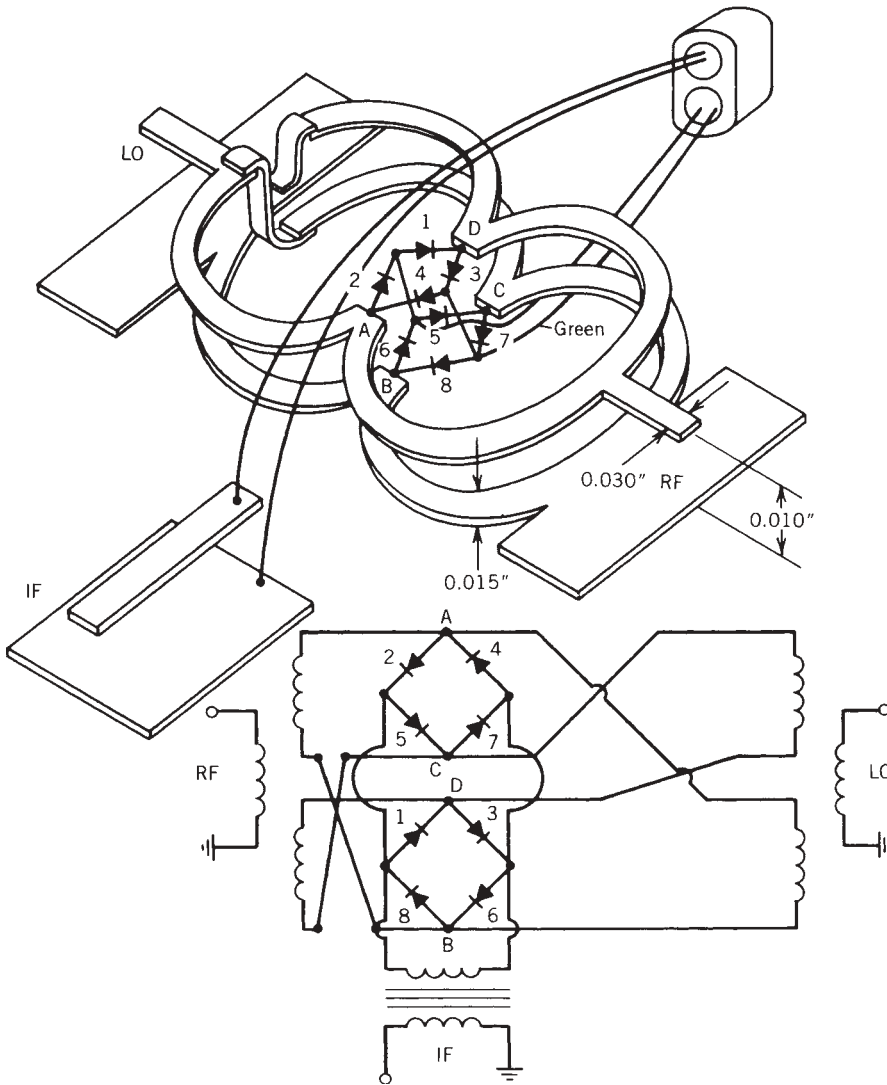
FIGURE 11.67 Planar double-ring mixer with microstrip-to-parallel-plate line baluns.

The potential for improved dynamic range is the other main advantage of double-ring structures. However, dynamic range is also a strong function of the diode characteristics as well as circuit topology. The high-level performance of any mixer topology can be improved by increasing the diode junction potential. There are a variety of high-barrier diodes available commercially which have junction potentials greater than 0.6 V. Since most balanced mixer designs employ low-barrier diodes with junction potentials on the order of 0.3 V, an improvement in compression characteristics of 6 dB is feasible, provided that an additional 6 dB of pump power is available.

For example, a typical double-ring design employing conventional high-barrier diodes would require approximately 20 dBm of LO drive; hence the maximum input signal level would be approximately +15 dBm before entering the region of heavy

saturation. As the pump power is increased, the compression level of the mixer would also increase until full LO saturation of the diode(s) is reached, which is usually on the order of 23 to 27 dBm. A further increase in LO power would result in performance degradation, due partially to the effective increase in diode R_s.

Multiple diode combinations, such as series-connected junctions, can be used to further raise the compression characteristics of a mixer because the effective junction potential of the pair is increased. Various combinations of high- and low-barrier diodes can be used to optimize the mixer's performance for a particular set of signal and low-power levels. As in the case of single high-barrier devices, multiple diodes require as much or more LO drive, but the compression point is also raised.

An interesting high-level diode available from MACOM [11.25] is uniquely fabricated with three junctions. The diode consists of three junctions, two $p-n$ junctions and a conventional Schottky barrier. A diode cross section depicting its construction and a simplified circuit model are shown in Figures 11.68a and b. The $I-V$ characteristics for junction J_2 and the series combination J_2 and J_3 are compared in Figure 11.68c. The effective turn-on potential for the J_2/J_3 combination is considerably higher than for the main junction J_1; hence at low bias voltages it is essentially off. A comparison between the $I-V$ characteristics of a typical Schottky high-barrier diode (type B) and the $I-V$ characteristics of the composite triple-junction high-barrier diode (type A) is shown in Figure 11.69. It is evident from the data that under large-signal conditions the conventional high-barrier diode (type B) begins to saturate severely at a forward voltage of about 0.5 V, while the triple-junction device is still unsaturated well above a forward voltage of 0.8 V. Hence as LO power is increased, the effective R_s of the type B diode rapidly increases, causing a severe degradation in performance.

A star mixer of the type illustrated in Figure 11.63, employing othogonally connected planar-compensated baluns, was fabricated and evaluated as a high-level up converter by Hallford [11.26]. To compare their performance, conventional high-barrier and triple-junction diodes were evaluated in the same mixer structure. Although the mixer was capable of octave-band performance, it was used as a high-level up converter in the frequency range 70 MHz to 1500 to 2000 MHz. With conventional high-barrier diodes, a single-sideband output power of 15 dBm was obtained with 28 dBm of LO power and an IF signal level of 22.5 dBm. When triple-junction diodes were used (type A), the performance of the mixer improved dramatically. The compression characteristics of the up converter are shown in Figure 11.70 for a LO power of 25 dBm. By increasing the LO power to 27 dBm, the performance was further enhanced. The two-tone distortion characteristics at this LO drive level are shown in Figure 11.71.

Although the 35-dBm third-order intercept point is impressive, a careful examination of the measured results reveals a more interesting phenomenon. Note that with an IF signal input level of 22.5 dBm and a LO power level of 27 dBm a single-sideband output power of 21 dBm was measured. These levels correspond to a double-sideband (DSB) conversion gain of 1.5 dB in a passive mixer. Although this result is unusual, it should be remembered that the total power output (DSB) of 250 mW is still substantially less than the total input power (LO + signal) of 680 mW.

It is apparent that some process other than resistive mixing is occurring to account for the conversion performance. Considering that the diode is quite large ($C_{j0} = 1.5$ pF and $R_s = 1.4$) and pumped quite heavily, perhaps some parametric conversion mechanism can account for the added performance. High-level mixers in general exhibit
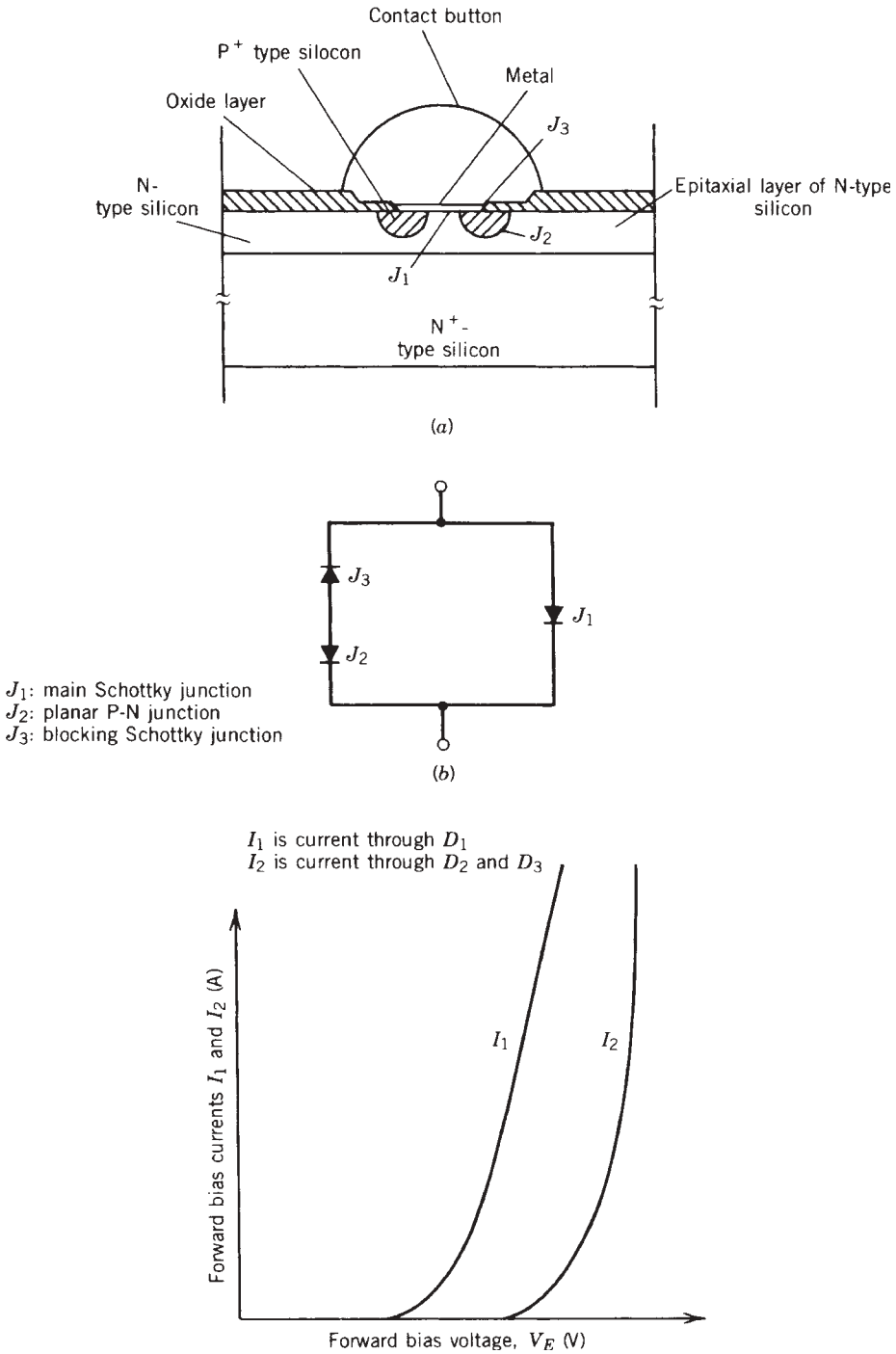
FIGURE 11.68   Triple-junction diode: (a) diode cross section; (b) simplified circuit model; (c) relative $I-V$ characteristics of junctions J_1 and J_2/J_3. (Courtesy of M/A-COM [11.25].)
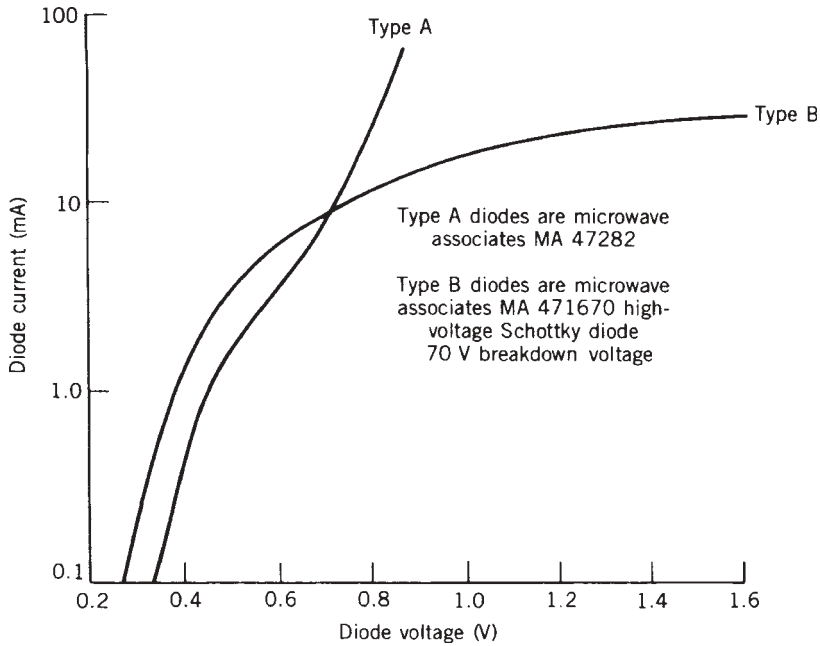
FIGURE 11.69 Typical diode $I-V$ characteristics: type A, conventional high-barrier diode; type B, triple-junction diode. (Courtesy of M/A-COM [11.25].)
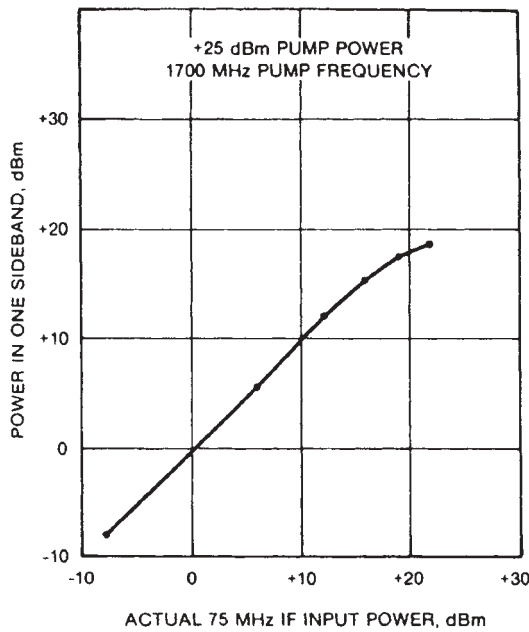
FIGURE 11.70 Compression characteristics of high-level up converter.
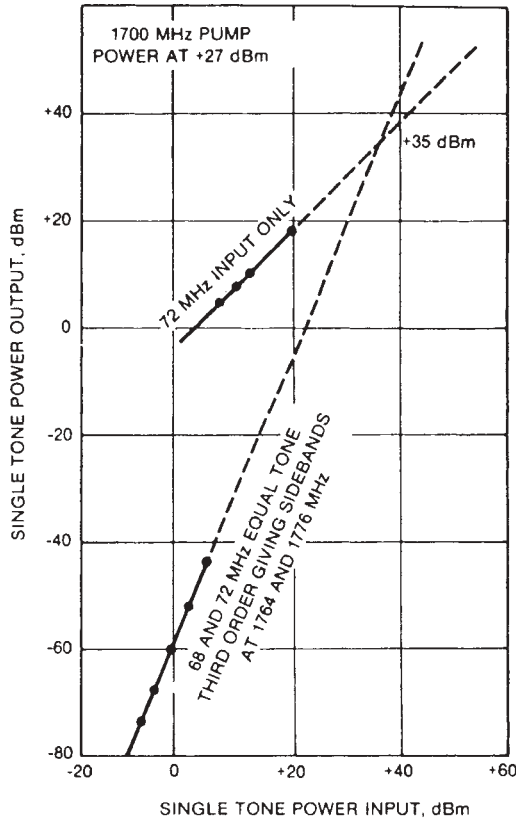
FIGURE 11.71 Two-tone distortion performance of high-level up converter.

better spurious performance than that of conventional small-signal designs. Unfortunately, calculating or determining the absolute spurious performance is difficult. In fact, the only sure method is to measure the mixer in question embedded in the actual system. Approximate tables and formulas are available throughout the literature, but they assume that the mixer baluns are indeed baluns at harmonics of the LO and RF signals and that broadband resistive terminations are present on all ports. When broadband mixers are used in the lower portion of their operating range, the conditions above may be approximated. But at frequencies above 18 GHz, diode balance, balun performance, and terminations are surely in question, even when a low-order spurious response such as the (2, 2) is involved.

All the broadband mixer designs that employ suspended substrate techniques exhibit strong interactions with their packages. It is for this reason that it is very common to find the housings of commercially available mixers loaded with lossy ferrite materials. The loading materials not only dampen resonances but also de-Q the circuit transmission lines. By lowering the circuit Q, the mixer will operate closer to the transmission zeros of the circuit, thus increasing the bandwidth but degrading the overall conversion loss characteristics. However, if suspended broadband structures are constructed without loading materials, sharp resonances will usually occur somewhere within the mixer passband.

11.6 FET MIXER THEORY

Interest in JFET mixers has been very strong due to their excellent conversion gain and intermodulation characteristics. Numerous commercial products employ JFET mixers, but as the frequency of operation approaches 1 GHz, they begin to disappear. At these frequencies and above, the MESFET can easily accomplish the conversion functions that the JFET performs at low frequencies. However, the performance of active FET mixers reported to date by numerous authors has been somewhat disappointing. In short, they have not lived up to expectations, especially concerning noise figure performance, conversion gain, and circuit-to-circuit repeatability. Hence, in the hybrid circuit world, most mixer applications are left to the diode.

Recently, growing interest in GaAs monolithic circuits is again beginning to heighten interest in active MESFET mixers. This is indeed fortunate, since properly designed FET mixers offer distinct advantages over their passive counterparts. This is especially true in the case of the dual-gate FET mixer; since the additional port allows for some inherent LO-to-RF isolation, it can at times replace single-balanced passive approaches. The possibility of conversion gain rather than loss is also an advantage, since the added gain may eliminate the need for excess amplification, thus reducing system complexity.

Unfortunately, there are some drawbacks when designing active mixers. With diode mixers, the design engineer can make excellent first-order performance approximations with linear analysis; also, there is the practical reality that a diode always mixes reasonably well almost independent of the circuit. In active mixer design, these two conditions do not hold. Simulating performance, especially with a dual-gate device, requires some form of nonlinear analysis tool if any circuit information other than small-signal impedance is desired. An analysis of the noise performance is even more difficult.

In the following section(s), a theory that describes the operation of single- and dual-gate mixers is developed. Emphasis is on the practical implementation of FET mixers for microwave frequency ranges, but techniques for VHF and UHF applications are also described. Special circuit design approaches involving active and passive techniques are stressed, particularly for monolithic circuit applications. Analysis and simulation constraints using commercially available nonlinear solvers are also discussed.

The nonlinear FET modeling described in Chapter 5, combined with the mixer analysis developed for diodes in Section 11.2, can be extended to describe the operation of FET mixers. As we have learned, the dominant nonlinearity of the FET is its transconductance, which is typically (especially with JFETs) a square-law function. Hence it makes a very efficient multiplier with products of reasonably low spuriousness.

The small-signal circuit [11.27] shown in Figure 11.72 denotes the principal elements of the FET that must be considered in the model. The parasitic resistances R_g, R_d, and R_s are small compared to R_{ds} and can be considered constant, but they are important in determining the noise performance of the circuit. The mixing products produced by parametric pumping of the capacitances C_{gs}, C_{dg}, and C_{ds} are typically small and add only second-order effects to the total circuit performance. Time-averaged values of these capacitances can be used in circuit simulation with good results.

The leaves the FET transconductance g_m, which exhibits an extremely strong non-linear dependence as a function of gate bias. A typical transconductance versus gate bias for a 150-μm low-noise FET is shown in Figure 11.73. It is evident from the illustration that the greatest change in transconductance occurs near pinchoff, with the most linear change with respect to gate voltage occurring in the center of the bias
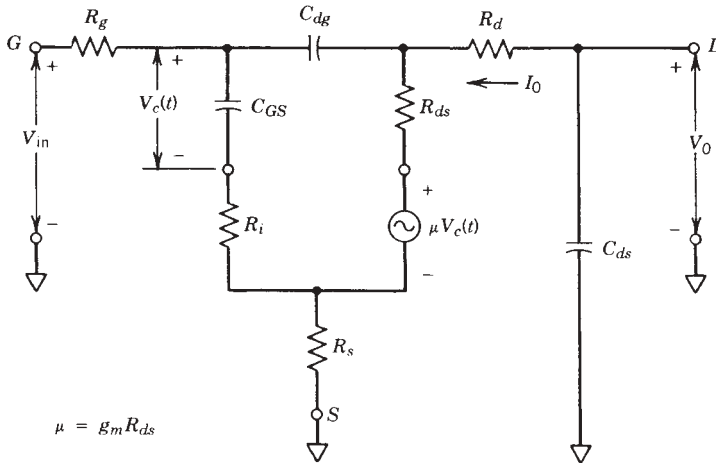
FIGURE 11.72   Small-signal GaAs FET equivalent circuit with voltage source representation.
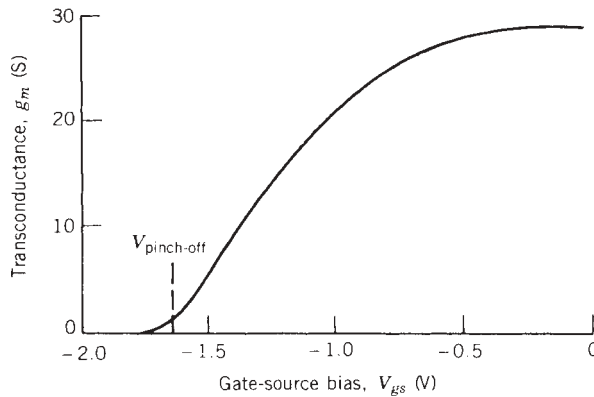
FIGURE 11.73   Transconductance as a function of gate bias for a typical 150-μm gate-width FET.

range. As the FET is biased toward I_{dss}, the transconductance function again becomes nonlinear. It is in these most nonlinear regions that the FET is most efficient as a mixer.

When a fixed bias is applied to the gate of an FET and a large pump signal is applied, the transconductance of the FET will be periodically modulated. If the pump frequency is defined as ω_p, the transconductance can be expressed as

$$g_m(t) = \sum_{k=-\infty}^{\infty} g_k e^{j\omega_p t} \tag{11.58}$$

where

$$g_k = \frac{1}{2\pi} \int_0^{2\pi} g(t) e^{-j\omega_p t} \, d\omega_p t \tag{11.59}$$

If we use the time-averaged value of R_{ds}, the amplification factor $\mu(t)$ can be approximately written as

$$\mu(t) = R_p(g_m(t)) \tag{11.60}$$

where R_p is the time-averaged value of R_{ds} at the pump frequency.

If we now introduce a second signal, V_c, such that it is substantially smaller than the pump, across the gate-to-source capacitance C_{gs}, the nonlinear action of the transconductance will cause mixing action within the FET. The conventional current source in the FET can be replaced by a voltage source $V_c(t)$ which has mixing product frequencies $|n\omega_p \pm \omega_1|$, where n can be any positive or negative integer. Since V_c is small, only mixing products that are a function of ω_1 and not its harmonics need to be considered.

Any practical analysis must include mixing products at both the gate and drain terminal and at a minimum allow frequency components in the signal, image, LO, and IF to exist. For ease of conception, the analysis will focus on the FET used as a down converter where the IF is defined as $|\omega_p - \omega_1|$ and is usually substantially lower in frequency than either the signal or the pump. The image frequency is defined as $|2\omega_p - \omega_1|$ and, as mentioned above, must be included in the analysis. The voltage sources and circulating currents for the single-gate FET mixer are shown in Figure 11.74.

The network above can be analyzed using conventional circuit theory. If we define I_p, I_1, I_2, I_3 and V_p, V_1, V_2, V_3 to be the complex amplitudes of the currents and voltages for the pump, signal, image, and IF components on the gate side of the FET and define I_p, I_4, I_5, I_6 and V_p, V_4, V_5, V_6 as the corresponding complex amplitudes of the current and voltage components at the drain side of the FET, the problem can be solved by applying the boundary conditions imposed by the external sources. These sources can be defined as E_1 with internal impedance Z_1 for the signal (ω_1) and as E_p with internal impedance Z_p for the pump (ω_p), with all other mixing products appearing on both sides of the FET being terminated by complex impedances. Thus the
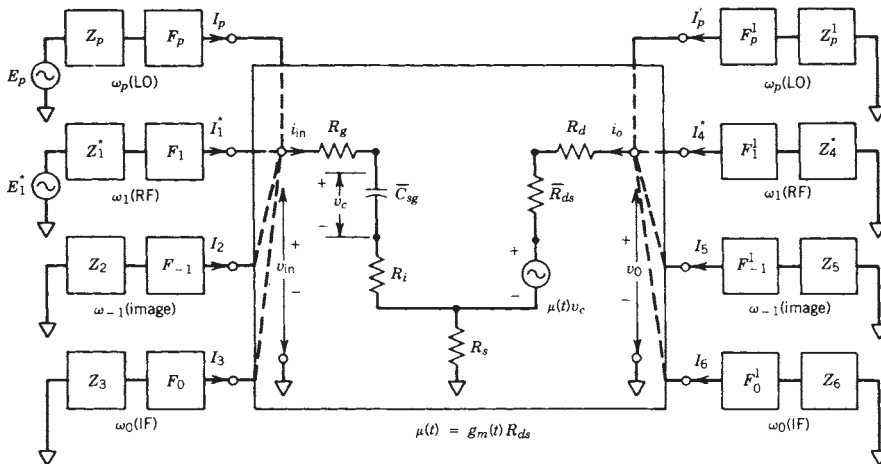
FIGURE 11.74   Circuit diagram of single-gate FET mixer showing signal, image, and IF circuits. (© IEEE 1976, [11.27].)

voltage and currents at the gate–source and drain–source terminals can be related as

$$V_k = E_k - I_k Z_k \tag{11.61}$$

where $k = 1, 2, \ldots, 6$ and $E_k = 0$ for k not equal to unity. For convenience, a lower sideband relationship between the signal and pump was chosen; therefore, I_1 must be replaced by I_1^*. Similarly, I_4 must also be replaced by I_4^*.

Although the filters shown in Figure 11.74 are assumed to be ideal, that is, they only losslessly pass their respective frequency and reject all others, in practice this assumption can be approximated only when the IF is sufficiently spectrally separated form the RF and LO frequencies. In general, the mixer is most efficient when all mixing products except the IF (ω_p) are short circuited at the drain terminal. It is also desirable to short circuit the IF at the gate in order to reduce mixer noise. Separating the pump and signal components at the gate terminal is also difficult and is usually accomplished with the aid of a directional coupler rather than by employing filters.

An equivalent small-signal analysis of the circuit in Figure 11.74 can be conducted since time-averaged values of the nonlinear elements will be employed. Hence, by applying loop analysis and neglecting any harmonics of the pump frequency, the circuit performance can be represented as

$$[E] = [V] = +[Z_t][I]$$
$$= [Z_m[I] + [Z_t[I] \tag{11.62}$$

where

$$[E] = \begin{bmatrix} E_1^* \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{11.63}$$

$$(V) = \begin{bmatrix} V_1^* \\ V_2 \\ V_3 \\ V_4^* \\ V_5 \\ V_6 \end{bmatrix} \tag{11.64}$$

$$[I] = \begin{bmatrix} I_1^* \\ I_2 \\ I_3 \\ I_4^* \\ I_5 \\ I_6 \end{bmatrix} \tag{11.65}$$

The quantities $[Z_m]$ and $[Z_t]$ are the multiport equivalent matrix representations of the mixer proper and the terminating network, which are given by

$$[Z_m] = \begin{bmatrix} Z_{11}^* & 0 & 0 & Z_{14}^* & 0 & 0 \\ 0 & Z_{22} & 0 & 0 & Z_{25} & 0 \\ 0 & 0 & Z_{33} & 0 & 0 & Z_{35} \\ Z_{41}^* & 0 & Z_{43} & Z_{44}^* & 0 & 0 \\ 0 & Z_{52} & Z_{53} & 0 & Z_{55} & 0 \\ Z_{61}^* & Z_{62} & Z_{63} & 0 & 0 & Z_{66} \end{bmatrix} \tag{11.66}$$

and

$$[Z_t] = \begin{bmatrix} Z_1^* & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & Z_3 & 0 & 0 & 0 \\ 0 & 0 & 0 & Z_4^* & 0 & 0 \\ 0 & 0 & 0 & 0 & Z_5 & 0 \\ 0 & 0 & 0 & 0 & 0 & Z_6 \end{bmatrix} \tag{11.67}$$

The elements of the matrix $[Z_m]$ are given by

$$Z_{11} = R_g + R_i + R_s + \frac{1}{j\omega_1 C} \tag{11.68}$$

$$Z_{22} = R_g + R_i + R_s + \frac{1}{j\omega_{-1} C} \tag{11.69}$$

$$Z_{33} = R_g + R_i + R_s + \frac{1}{j\omega_0 C} \tag{11.70}$$

$$Z_{44} = R_d + R_{ds} + R_s \tag{11.71}$$

$$Z_{55} = R_d + R_{ds} + R_s \tag{11.72}$$

$$Z_{66} = R_d + R_{ds} + R_s \tag{11.73}$$

$$Z_{14} = Z_{25} = Z_{36} = R_s \tag{11.74}$$

$$Z_{41}^* = \text{conj}\left(R_s + -\frac{g_p R_{ds}}{j\omega_1 C} \right) \tag{11.75}$$

$$Z_{61} = R_s + -\frac{g_1 R_{ds}}{j\omega_1 C} \tag{11.76}$$

$$Z_{52} = R_s + -\frac{g_p R_{ds}}{j\omega_2 C} \tag{11.77}$$

$$Z_{62} = -\frac{g_1 R_{ds}}{j\omega_2 C} \tag{11.78}$$

$$Z_{63} = R_s + -\frac{g_p R_{ds}}{j\omega_3 C} \tag{11.79}$$

$$Z_{43} = Z_{53} = -\frac{g_1 R_{ds}}{j\omega_3 C} \tag{11.80}$$

In the equation set above the quantity C represents the time-averaged value of C_{gs} at the frequencies of ω_k, where k can be -1, 0, or 1. Similarly, the quantity R_{ds} is the time-averaged value of the drain-to-source resistance at its respective frequency. The value of R_{ds}, from frequency to frequency, can be quite different, especially if the IF is very low.

The available conversion gain G_{av} [11.27, 11.28], which is of course the quantity of most interest, can be expressed as the ratio of power delivered to the load at port 6 to the power available from the source. Thus

$$G_{\mathrm{av}} = \frac{|I_6|^2 \mathrm{Re}[Z_6]}{|E_1|^2/\mathrm{Re}[Z_1]} \tag{11.81}$$

$$= 4R_g R_L \left|\frac{I_6}{E_1}\right|^2 \tag{11.82}$$

where Z_1 is defined as $R_g + jX_g$ and Z_6 is defined as $R_L + jX_L$. The quantity I_6/E_1 can be obtained by solving (11.62) [11.27]. If the IF is substantially lower than the RF or LO frequencies, the conversion gain expression can be simplified. Thus

$$G_{\mathrm{av}} = \frac{2g_1 R_{ds}}{\omega_1 C} \frac{R_g}{(R_g + R_{\mathrm{in}}) + (X_g - 1/\omega_1 C)^2} \frac{R_L}{(R_{ds} + R_L)^2 + X_L^2} \tag{11.83}$$

where $R_{\mathrm{in}} = R_g + R_i + R_s$. When the source and load impedances are conjugately matched, the conversion gain is a maximum and can be defined as

$$G_c = \frac{(g_1)^2 R_{ds}}{4(\omega_1)^2 C^2 R_{\mathrm{in}}} \tag{11.84}$$

It is interesting to note that the expression for conversion gain is similar to the expression for amplifier gain. The ratio of these two gains for the same signal frequency is expressed as

$$G_r = \left(\frac{g_1}{g_m}\right)^2 \left(\frac{C_{ds}}{C}\right)^2 \frac{\tilde{R}_{ds}}{R_{ds}} \tag{11.85}$$

When the IF is low compared to the signal frequency, the gain ratio in (11.85) can be greater than unity even if $g_1 < g_m$. That is because the ratios C_{ds}/C and $\tilde{R}_{ds}/R_{ds}$ are greater than unity when the FET is biased near pinchoff for maximum conversion gain.

The variation on mixer performance as a function of LO drive is also of prime importance. If we assume that the total gate-to-source voltage is the sum of the LO voltage and dc bias, such that

$$V_{gs} = V_{g\mathrm{dc}} + V_p \cos \omega_p t \tag{11.86}$$

then the conversion transconductance as a function of dc gate bias and peak LO voltage may be calculated. A plot conversion transconductance versus gate bias for a typical

150-μm FET is shown in Figure 11.75. The values for g_1 were obtained from a SPICE analysis, but they could have also been obtained by Fourier analysis of $g_m(t)$. As the gate bias was varied, the amplitude of the LO signal V_p was adjusted so that the peak gate voltage was at the onset of forward gate current. Hence, as the gate bias became more negative, the magnitude of V_p must be increased to the point of gate conduction. As can be seen in the illustration, a maximum in conversion gain occurs near pinchoff and a second local maxima occurs near forward conduction. It should be noted that the shape and magnitude of the curve are very dependent on the g_m characteristic of the FET. The dependence of LO drive voltage on conversion gain can be found in a similar manner and is illustrated in Figure 11.76. The shape of the curve is very similar to that obtained with conventional diode mixers except that the conversion gain saturation is less abrupt.
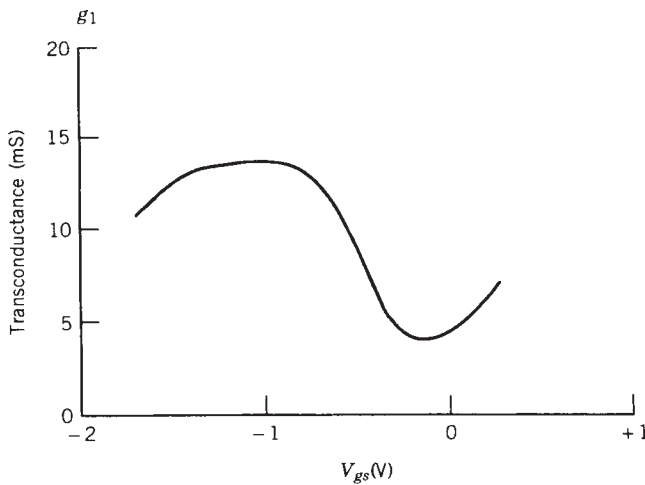
FIGURE 11.75   Conversion transconductance for a typical 150-μm FET.
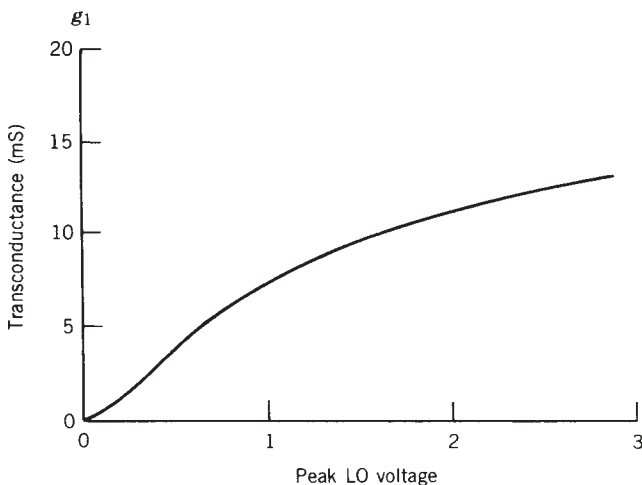
FIGURE 11.76   Conversion gain as a function of LO drive voltage.
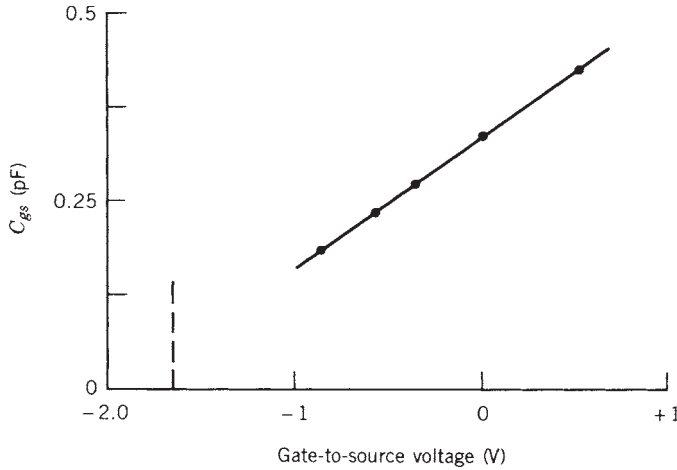
FIGURE 11.77 Gate-to-source capacitance as a function of bias.

The dependence of gate capacitance as a function of gate-to-source voltage is much less severe. This dependence can be linearly approximated as illustrated in Figure 11.77. It is evident from the capacitance function above that the values for C_{gs} (static value), C (time-averaged value at ω_1), and C_p (time-averaged value at ω_p) can be substantially different.

Unfortunately, the best mixer conversion loss is obtained for large values of LO voltage. With this in mind, and knowing the FET parasitic element values, which can be obtained from small-signal S-parameter measurements, an estimate of the required LO can be made. From conventional circuit theory, the power dissipated in the gate circuit is

$$P_{\text{LO}} = \frac{1}{2}(\omega_p \tilde{C}_p V_p)^2 R_{\text{in}} \tag{11.87}$$

where R_{in} is the input resistance, as defined earlier. When the total gate periphery of the FET is small, the optimum LO power will be modest (3 to 6 dBm), but as the FET becomes larger, the term C_p in (11.87) begins to dominate. It is not uncommon for a large FET to require 20 dBm of LO drive power. The amount of LO power required for maximum conversion loss at a particular FET size can also be reduced by selecting or designing the FET for the lowest possible value of pinchoff voltage. Since, for a given gate periphery, the values of R_{in} and C_p change little compared to the change in pinchoff voltage obtained when changing the FET doping profile, a dramatic improvement in LO efficiency is obtained when using low-noise FETs with pinchoff voltages in the 1.5-V range as compared to power FETs that exhibit pinchoff voltages in the range 4 to 5 V.

Experimental results for both single- and multiple-FET mixers verify the predictions above for optimum conversion loss, bias, and LO requirements. For example, a single-gate X-band mixer [11.27] using a 500×2.5-μm FET with a pinchoff of 3.3 V was constructed on a 0.5-mm-thick alumina substrate and evaluated. The circuit model for the mixer is shown in Figure 11.78. The conversion gain performance as a function of LO drive power at a signal frequency of 7.8 GHz and an IF of 30 mHz for the mixer is shown in Figure 11.79. The calculated performance shown is from the theory
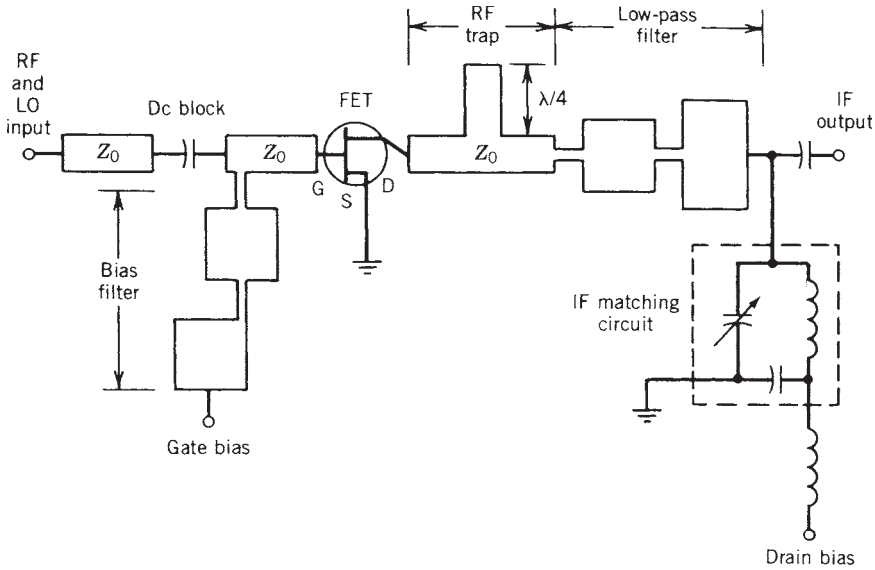
FIGURE 11.78   X-band single-gate FET mixer reported by Pucel. (© IEEE 1976, [11.27].)
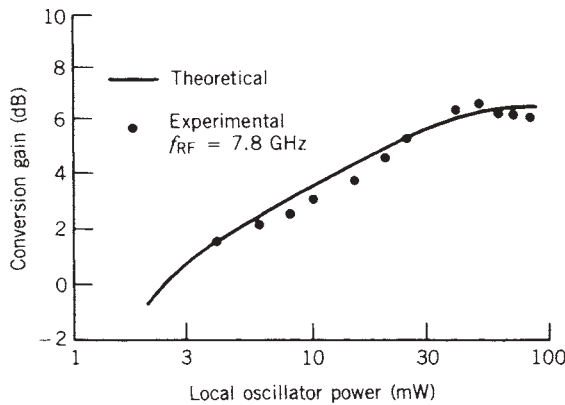
FIGURE 11.79   Conversion gain of X-band mixer as a function of LO driver power. (© IEEE 1976, [11.27].)

above, and the measured data were obtained with the FET biased near pinchoff. It is interesting to note that the conversion gain obtained of 6.4 dB is greater than the 4.7 dB of gain that can be obtained when the same device is used as an amplifier. As can be seen, the calculated results agree quite well with measured performance.

Computer simulation of any proposed mixer circuit can be conducted as long as the FET characteristics are completely known. The computed and measured conversion loss performance results versus LO power for a similar X-band mixer are shown in Figure 11.80, and the mixer circuit topology is shown in Figure 11.81. As can be seen in the illustration above, the computed nonlinear circuit simulation performed using Microwave Harmonica also agrees quite well with the measured results. Computer
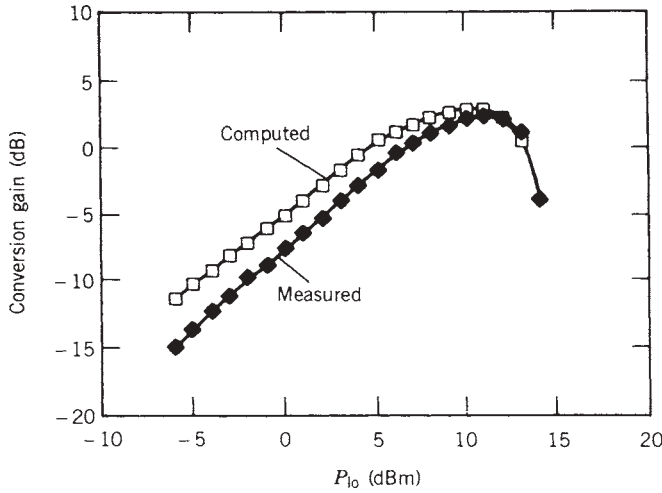
FIGURE 11.80 Measure versus computed performance of X-band mixer.

simulators of this type enable the design engineer, as in this case, to optimize the circuit parameters for best performance. In addition, nonlinear simulators allow the designer to examine circuit voltage waveforms and spectral performance. A sample voltage waveform and the spectral response of the circuit above are shown in Figures 11.82 and 11.83.

The noise performance of a GaAs FET mixer is much less well understood than its companion amplifier. However, the noise figure performance is related to the intrinsic noise sources of the FET (R_g, R_s, and R_d) as well as to shot noise and noise due to traps in the semiconductor material. The $1/f$ noise spectra of the GaAs FET mixer can extend to several hundred megahertz but usually, with a well-designed FET, extends to less than 50 mHz. A variety of single-gate mixers, with operating frequencies extending through the X band, have been reported to have exhibited noise figures less than 5 dB and an associated gain of several decibels. This performance, although not easy to realize, is quite comparable to conventional diode mixers, except that a small amount of gain, not loss, is obtained.

However, a good first-order approximation to the noise figure performance of a single-gate FET mixer can be determined by applying the accepted noise parameters of MESFETs [11.29]. The noise equivalent circuit of an FET is shown in Figure 11.84, where the noise sources e_g, e_s, and e_d, due to the parasitic resistances R_g, R_s, and R_d, and the noise sources i_d and I_g, due to channel current and induced gate current, are included. The mean-square value of the current sources and their correlation coefficient are given by

$$I_d^{\overline{2}} = 4kTBg_m P \tag{11.88}$$

$$I_g^{\overline{2}} = 4kTB \frac{(\omega C_{gs})^2}{g_m} R \tag{11.89}$$

$$C_r = \frac{I_g^* I_d}{(I_g^2 I_d^2)^{1/2}} \tag{11.90}$$
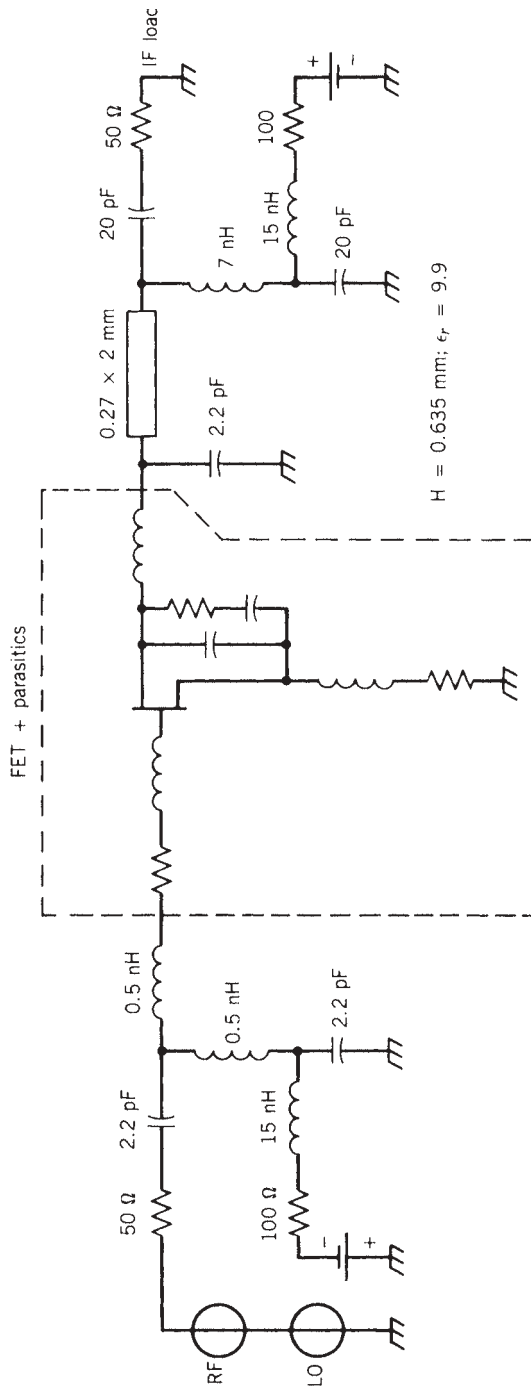
FIGURE 11.81 Single-gate FET mixer used in harmonic balance analysis.
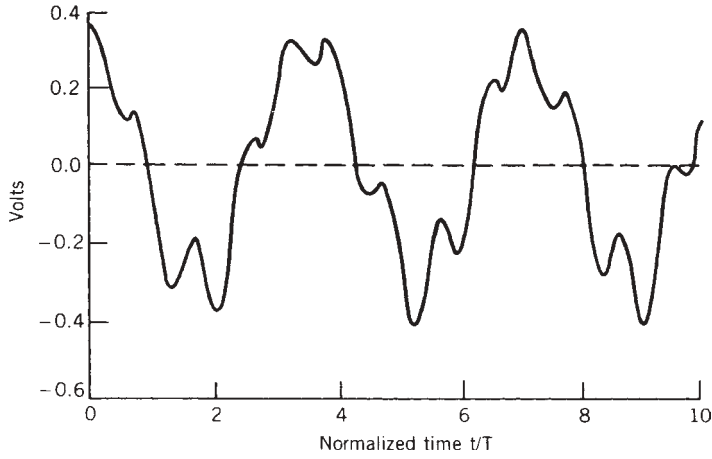
FIGURE 11.82   IF output voltage obtained from nonlinear analysis.
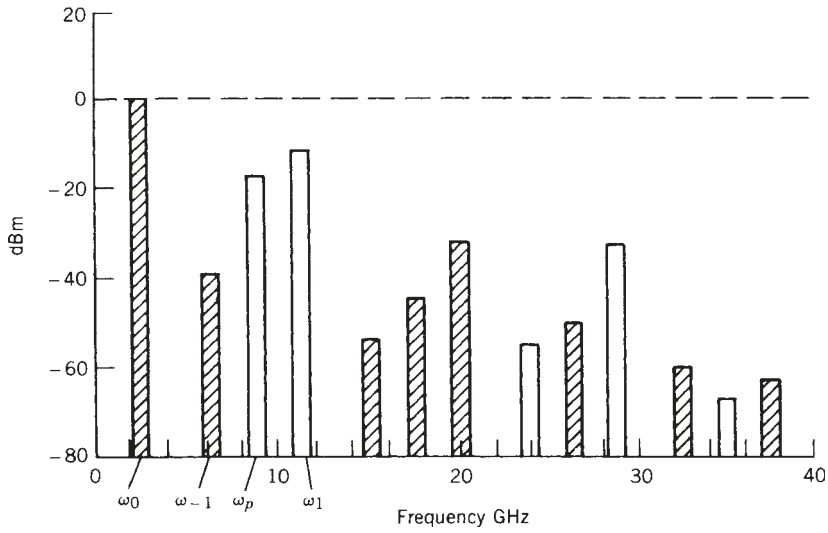
FIGURE 11.83   Computed mixer spectral performance.
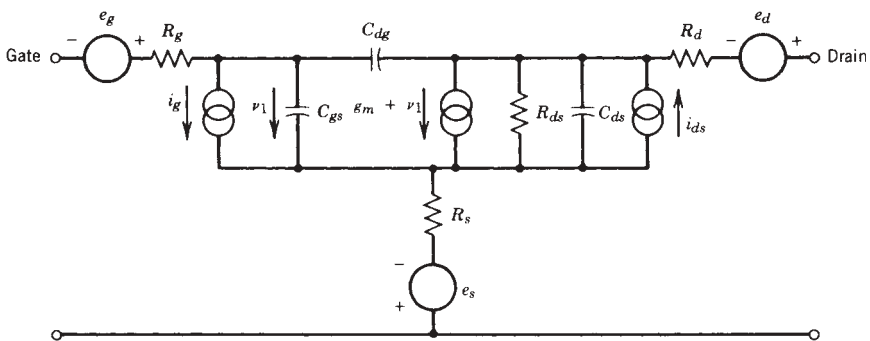
FIGURE 11.84   Noise equivalent circuit of an FET.

where $k =$ Boltzmann's constant

$T =$ temperature

$B =$ bandwidth

$R, P =$ dimensionless noise parameters of FET

If we replace the FET model in the mixer model shown in Figure 11.72 with the noise model of the FET, the mixer noise model shown in Figure 11.85 results. The noise sources i_{gn1} and i_{gn0} in the mixer's input gate circuit are functions of the induced gate noise source at the RF and IF, while i_{dn1} and i_{dn0} are noise sources in the mixer's output circuit that are functions of the drain noise current i_d. The noise voltage sources can also be defined from the general relationship

$$\overline{e^2} = 4kTB\,(\text{Re}[Z]) \tag{11.91}$$

The noise figure of the mixer can then be determined by summing all the noise currents within the mixer circuit arriving at the IF output port. This is accomplished with the aid of a formula developed by Friis in 1944 [11.30]. Thus the noise figure can be expressed as

$$F = \frac{\overline{|I_{no1} + I_{no0} + I_{no3} + I_{dn0} + (4kTB/R_d)^{1/2}|^2}}{|I_{no}^2|} \tag{11.92}$$

where I_{no1}, I_{no0}, and I_{no3} are the noise components at the IF output circuit due to the RF and IF noise sources at the FET input and the RF noise source at the FET output. The sources I_{dn0} and $(4kTB/R_d)^{1/2}$ are noise current components generated within the IF drain circuit, and the source I_{no} is the noise at the IF port due to the matching network at the FET gate.

If we now let Y_1, Y_0, and Y_3 be the transfer admittances and G_1, G_0, and G_3 the current gains from the RF and IF input and the RF output ports to the IF output port, respectively, the mixer noise figure can be expressed as

$$F = 1 + \frac{R_g + R_s}{R_1} + \frac{|Y_0|^2}{|Y_1|^2}\frac{R_g + R_s + \text{Re}[Z_0]}{R_1} + \frac{|Y_3|^2}{|Y_1|^2}\frac{R_d + \text{Re}[Z_3]}{R_1}$$

$$+ \frac{1}{|Y_1|^2 R_1 R_d} + \frac{|G_1|^2}{|Y_1|^2}\frac{\overline{|i_{ng1}^*|^2}}{4kTBR_1} + \frac{|G_3|^2}{|Y_1|^2}\frac{\overline{|i_{nd1}^*|^2}}{4kTBR_1}$$

$$+ \frac{|G_0|^2}{|Y_1|^2}\frac{\overline{|i_{ng0}|^2}}{4kTBR_1} + \frac{\overline{|i_{nd0}|^2}}{|Y_1|^2\ 4kTBR_1} + \frac{2\{\overline{|i_{ng1}^*|^2}\ \overline{|i_{nd1}^*|^2}\}^{1/2}}{|Y_1|^2\ 4kTBR_1}$$

$$\times \text{Re}\{G_1^* G_3 \tilde{C}_{r1}\} + \frac{2\{\overline{|i_{ng0}^*|^2}\ \overline{|i_{nd0}^*|^2}\}^{1/2}}{|Y_1|^2\ 4kTBR_1}\text{Re}\{G_0^* \tilde{C}_{r0}\} \tag{11.93}$$

where $\tilde{C}_{r1}$ and $\tilde{C}_{r0}$ are the time-averaged values of the correlation coefficients between i_{ng1}^* and i_{nd1}^* and i_{ng0} and i_{nd0}, respectively. The conversion loss is calculated as described previously.

To verify the noise theory, three mixers were constructed with various combinations of RF and IF terminations. Mixer 1 was constructed with an IF short circuit on the gate side of the FET and an RF short at the drain. Mixer 2 was constructed with an IF
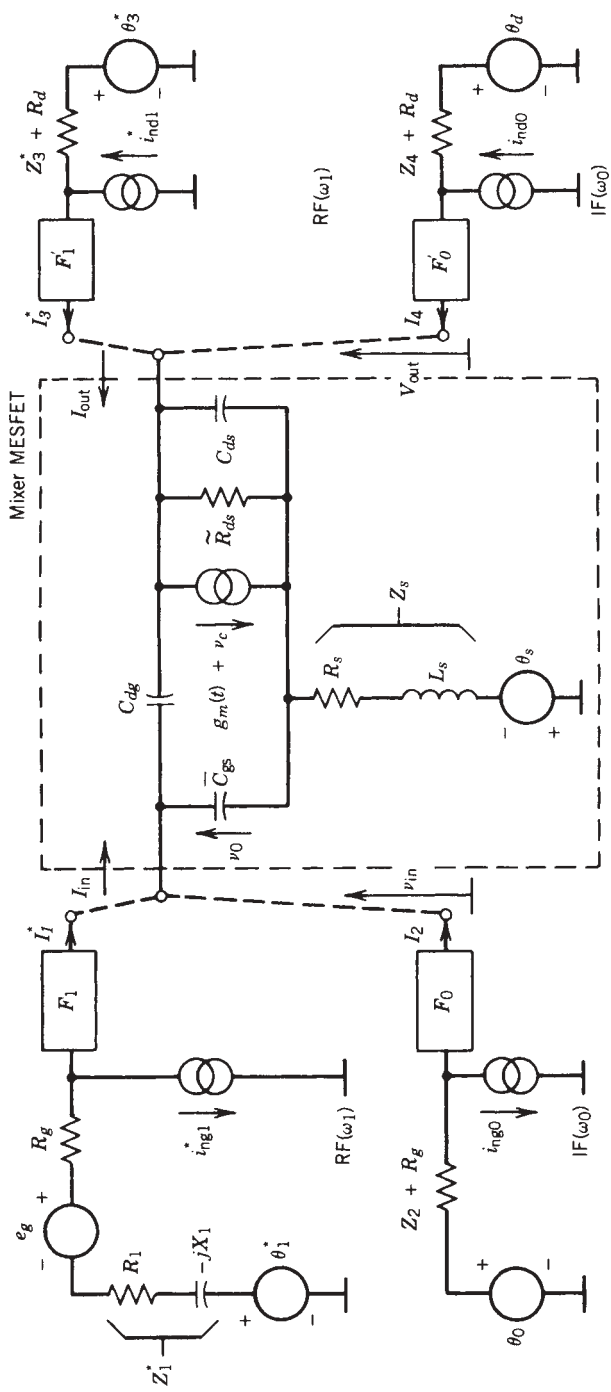
FIGURE 11.85 Equivalent circuit of single-gate FET mixer used for noise analysis. (© IEEE 1983, [11.29].)

open circuit at the gate and an RF short at the drain, while mixer 3 used open-circuit terminations at both the gate and drain for the IF and RF, respectively. A comparison between the measured and predicted conversion loss and noise figure performance for the mixers are shown in Figures 11.86–11.88. The measured and predicted conversion gain performance agree quite well, but the noise figure performance as a function of LO is in error. However, the noise figure values themselves are quite accurate and do predict the minimum noise figure obtainable. The error may be due to errors in the values of P, R, and C_r. It is interesting to note that the noise figure was essentially unaffected by the reactive terminations and may be limited by the current gains acting on the noise current components at the signal, image, pump, and IF frequencies.

The analysis above was formulated for gate injection of the LO, but the pump may be applied to either the source or drain terminals. These two injection methods may be preferable when no convenient method of RF and LO separation is possible, such as in applications where no directional coupler is available or when the LO and RF signals are too close together in frequency to be separated by filtering. The performance obtainable when pumping either the drain or source is comparable to gate pumping. However, there are slight differences in conversion gain and noise figure when pumping either the gate or drain.

Since the LO injection, with drain-pumped designs, is at the drain terminal of the FET, there is some inherent isolation between the RF and LO ports in the mixer. IF extraction, however, is somewhat more complex, but since the LO and IF are usually
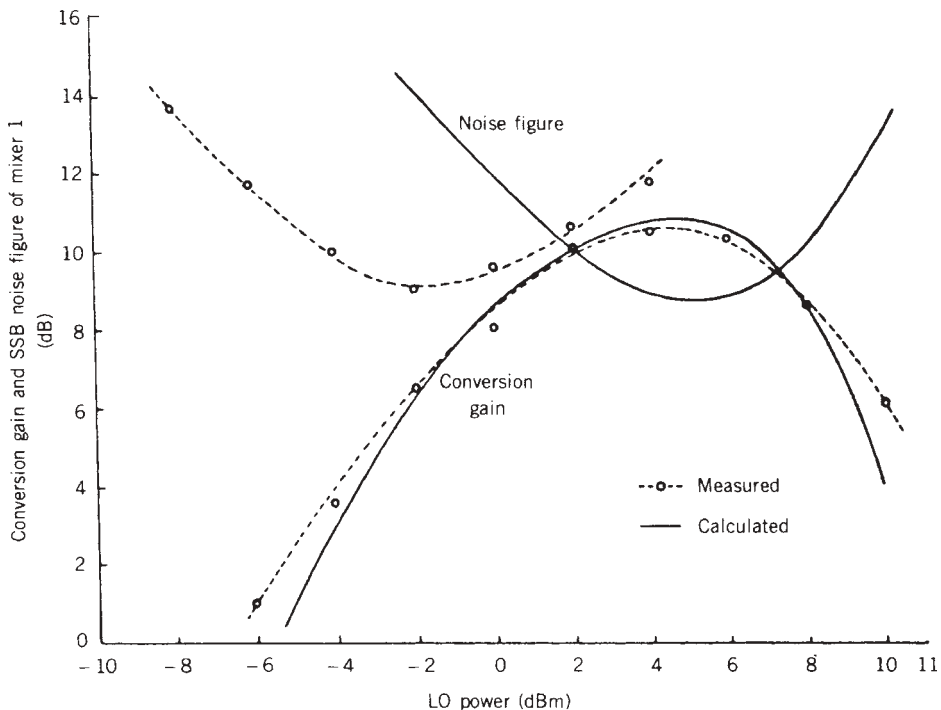
FIGURE 11.86   Measured and calculated noise figure and conversion gain of mixer 1, in which the IF input and RF output loads are short circuits. (© IEEE 1983, [11.29].)
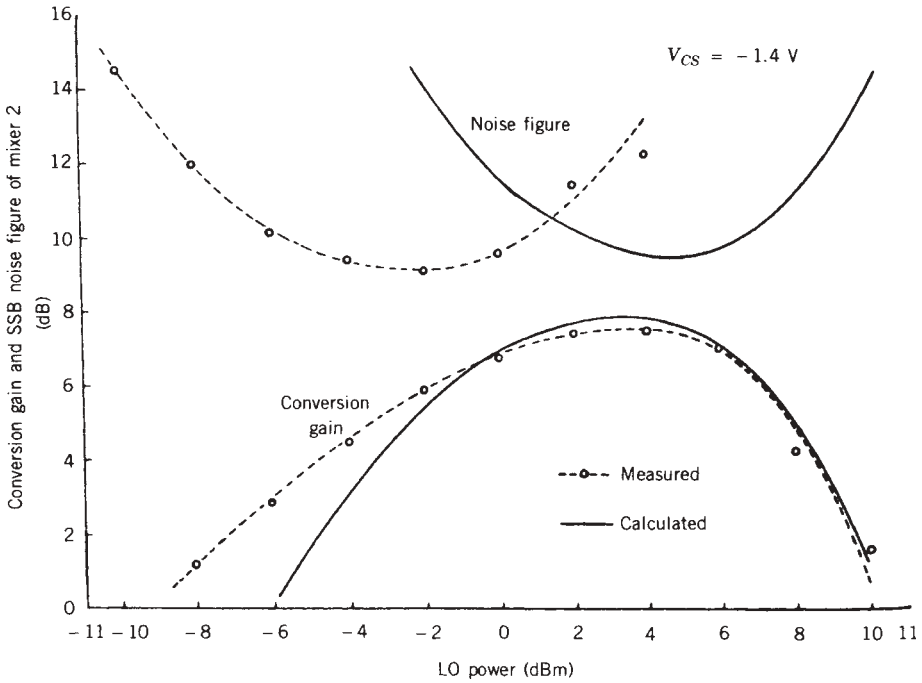
FIGURE 11.87 Measured and calculated noise figure and conversion gain of mixer 2. The IF input load = high impedance, RF output load = short circuit. (© IEEE 1983, [11.29].)
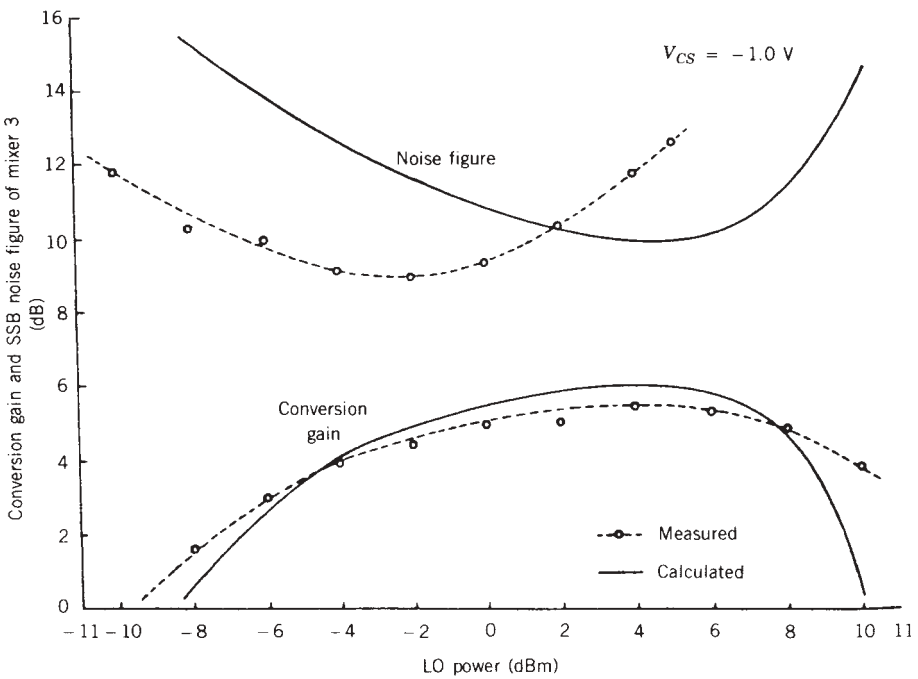
FIGURE 11.88 Measured and calculated noise figure and conversion gain of mixer 3. The mixer's IF input and RF output loads are high impedances. (© IEEE 1983, [11.29].)

FIGURE 11.89 Circuit diagram of drain-pumped single-gate FET mixer showing signal, image, and IF circuits.

separated significantly in frequency, the diplexing task should be easier than diplexing the RF and LO signals as in the gate-pumped case.

Analyzing the drain-pumped configuration is almost identical to the gate-pumped configuration and can be formulated using the circuit model illustrated in Figure 11.89. The circuit is analyzed as before by writing the loop equations for each mixer product current and treating each frequency component as a separate port in the network. Thus, neglecting the harmonics of the pump as before, the circuit performance can be described as

$$[E] = [V] = +[Z_t][I]$$
$$= [Z_m][I] + [Z_t][I] \tag{11.94}$$

where the quantities $[Z_m]$ and $[Z_t]$ are the multiport equivalent matrix representations of the mixer proper and the terminating network. With the source and load impedances conjugately matched, the conversion gain can be expressed as

$$G_c = \frac{|g_1 R_{ds1}|^2}{4(\omega_1)^2 C^2 (R_{in})(R_s + R_d + R_{dsp})} \tag{11.95}$$

where R_{ds1} and R_{dsp} are the time-averaged values of R_{ds} at the signal and pump frequencies. A more detailed discussion of the analysis above was presented by Begemann and Jacob [11.31].

Using the expression above for conversion gain, the performance of an NEC24483 with a signal frequency of 4.1 GHz and an IF of 100 MHz was calculated. Figure 11.90 illustrates the conversion performance as a function of gate bias and drain-to-source voltage. The value of the LO amplitude V_p was equal to V_{ds}.

An interesting comparison between the performance of drain- and gate-pumped mixers was shown by Bura and Dikshit [11.32]. Both mixers employed an NEC24483 FET and were pumped at 6 GHz. The RF input range was 5.9 to 6.4 GHz, and the IF band

FIGURE 11.90 Maximum available conversion gain of drain-pumped mixer as a function of V_{gs} and V_{ds}. (© IEEE 1979, [11.31].)

was 3.7 to 4.2 GHz. The conversion gain for both mixers is shown in Figure 11.91*a* and the noise figure performance is shown in Figure 11.91*b*. As can be seen, the drain-pumped mixer requires substantially more LO power for optimum conversion loss but is only slightly lower gain at equivalent pump levels. However, the noise figure performance for the drain-pumped design is substantially lower and is not too far from the noise figure of a comparable amplifier designed for the same frequency range using the same device type.

Single-ended mixers can also be designed using dual-gate FETs. Dual-gate devices offer several advantages over conventional devices, such as ease of LO injection, improved isolation, and added gain. They are, however, considerably less stable; hence added care must be used when designing non-self-oscillating mixers.

The operation of a dual-gate FET can easily be understood if the FET is considered as a cascode-connected FET pair, as was described in Chapter 5. Using this concept for the FET, the drain characteristics for the pair can be approximated by combining the characteristics of each intrinsic FET. This concept is illustrated in Figure 11.92*a*. A slightly more convenient representation of the drain characteristics is shown in Figure 11.92*b*. With this representation the operating point for FET 1 can be found as a function of gate 1 and 2 bias as well as its drain-to-source voltage.

The operating point path can vary significantly depending on how the FET is biased. Typically, gate 1 is used for signal injection with gate 2 biased ($V_{gs2} < 0$) for FET operation in the low-noise mode (shaded area in Fig. 11.92*b*). Gate 2 is also used for LO injection. Applying the LO at gate 2 is in effect drain pumping the first FET; hence FET 1 is the primary mixing element, while FET 2 acts as a common-gate amplifier. The operation is reversed if a sufficiently high bias voltage ($V_{gs2} > 2$) is applied to
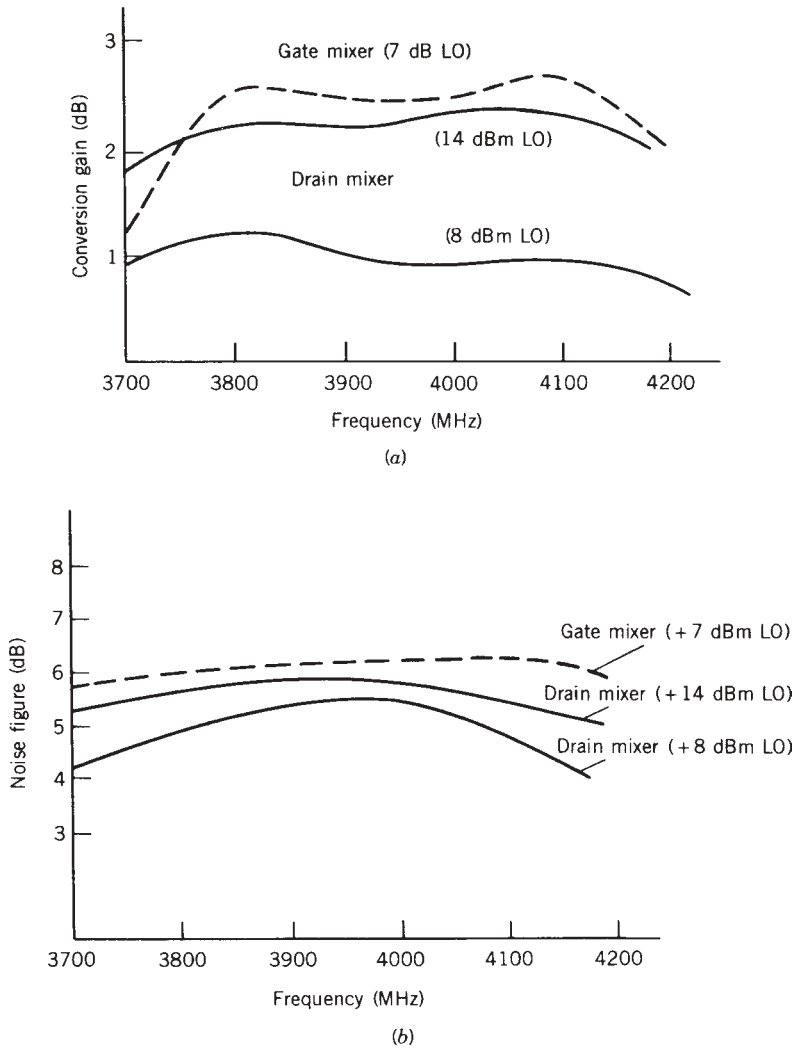
FIGURE 11.91 Comparison between drain- and gate-pumped mixers: (*a*) conversion gain performance as a function of LO power; (*b*) single-sideband noise figure performance as a function of LO power. (© IEEE 1976, [11.32].)

gate 2. With these bias conditions, FET 1 acts as an RF preamplifier, while FET 2 becomes the primary mixing element.

Slightly more insight into the operation of a dual-gate FET mixer can be had by examining the drain current dependence due to gate 1 and 2 bias voltage (Fig. 11.93) and the conversion gain characteristics as a function of LO drive voltage as reported by Tsironis et al. [11.33, 11.34] (Fig. 11.94). The shape and characteristics of the curves in the illustration are almost identical to the data obtained from a typical MOSFET (Fig. 11.95). As can be seen, a large percentage change in drain current as a function of gate bias occurs in both of the operating regions described above; hence maximum conversion gain should also correspond to the same operating points. Also, as in the
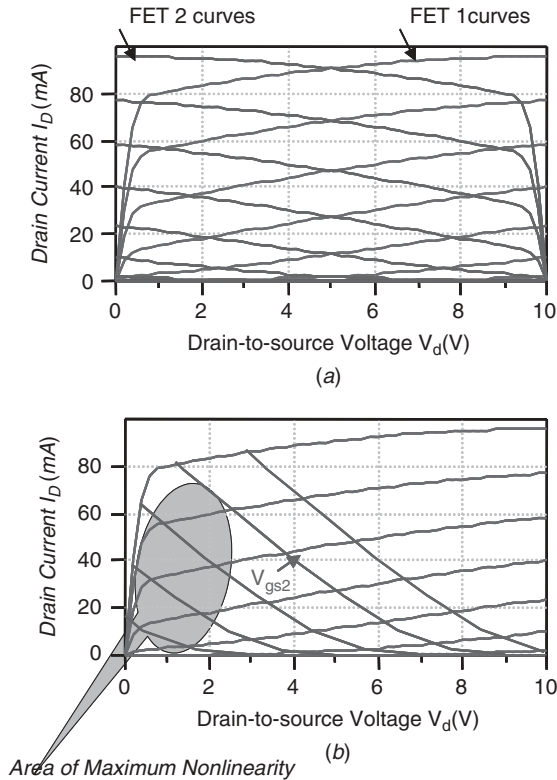
FIGURE 11.92   Dual-gate FET $I-V$ characteristics: (*a*) intrinsic FET $I-V$ characteristics connected "back to back" to simulate a dual-gate FET; (*b*) dual-gate FET $I-V$ characteristics as a function of V_{gs1} and V_{gs2}.
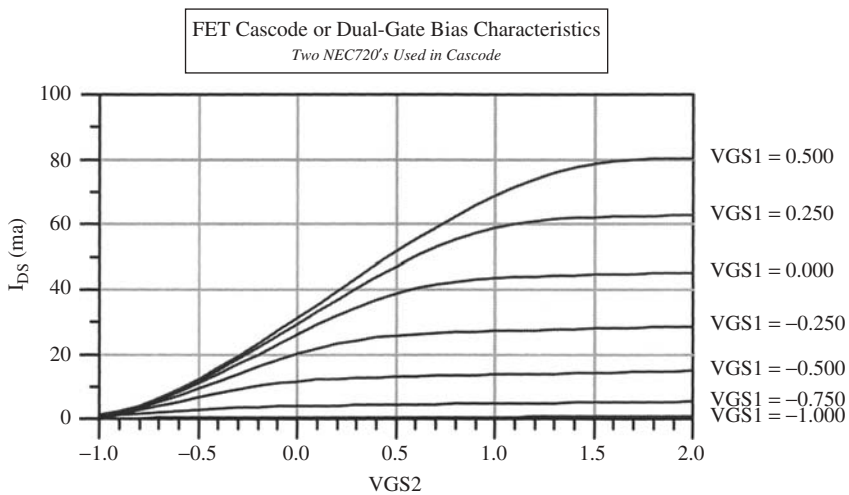
FIGURE 11.93   Dual-gate FET drain current as a function of V_{gs1} and V_{gs2}.
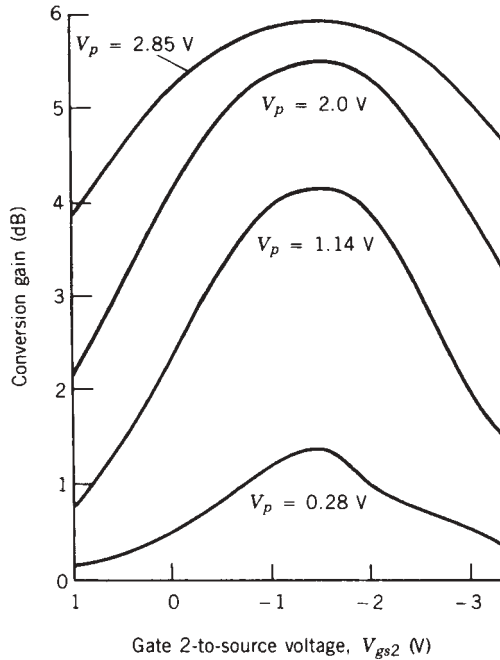
FIGURE 11.94   Conversion gain characteristics of dual-gate FET as a function of LO peak voltage. (© IEEE 1983, [11.29].)
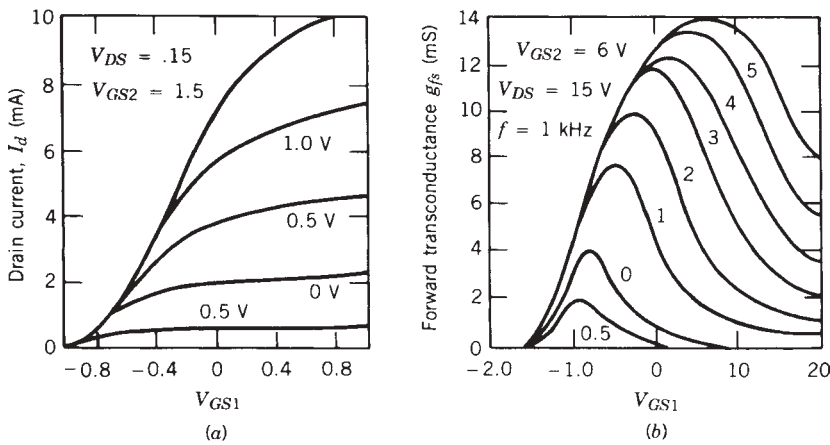
FIGURE 11.95   Drain current and conversion gain performance of a typical MOSFET: (a) drain current as a function of V_{gs1} and V_{gs2}; (b) transconductance versus V_{gs1} and V_{gs2}.

case of the single-gate mixer, the conversion gain increases as the LO drive voltage is increased, until the point of LO saturation.

Dual-gate FET mixers can be analyzed as described above or designed with the aid of a nonlinear simulator such as Microwave Harmonica or Microwave SPICE. Conversion gain performance obtainable with dual-gate mixers is comparable to that

obtained with conventional devices, with the exception of slightly degraded noise figure and possibly more gain. There is also some suspicion that the intermodulation performance for dual-gate MESFET devices may be better than single-gate FETs, but this idea has not yet been proven.

The distributed amplifier concepts developed in Chapter 9, combined with FET mixer theory, can be applied to the syntheses of distributed mixer structures [11.35, 11.36]. The distributed mixer employs the input capacitance of the FET gates and high-impedance series transmission lines to realize a lumped-element transmission line section of impedance Z_0. Several FETs can be cascaded in this manner to form very broadband structures for both the LO and RF mixer ports (Fig. 11.96). Thus low VSWR on both ports and good LO-to-RF isolation can be achieved.

These transmission lines must have equal phase shifts as a function of frequency between the FET stages when the mixer is operating as a down converter with a low IF. Using equal phase shifts between LO and RF signals at each FET yields a constant phase offset at the IF, which allows the IF power to be summed in phase by connecting the drain nodes of the dual-gate FETs together. Higher IF or use of this mixer as an up converter would require that the drains of the FETs also be connected with a traveling-wave structure.

A variety of design considerations affect the bandwidth and conversion gain of the mixer, such as the number of FETs, gate periphery, gate resistance, LO power requirements, and gate length. These design trades can be determined by applying standard distributed amplifier theory and the FET mixer theory discussed above.

The reported mixer circuit was designed using both linear and nonlinear analysis programs. Linear analysis can be used to determine element values for port matching, but conversion analysis can only be performed with a nonlinear solver. Nonlinear analysis allows the design engineer to optimize FET characteristics as well as drive levels and bias conditions.

The monolithic mixer shown in Figure 11.97 was fabricated on a 0.1-mm-thick semi-insulating GaAs substrate, with the active layers being formed by ion implantation. Since the output impedance at the common-drain node of the mixer is on the
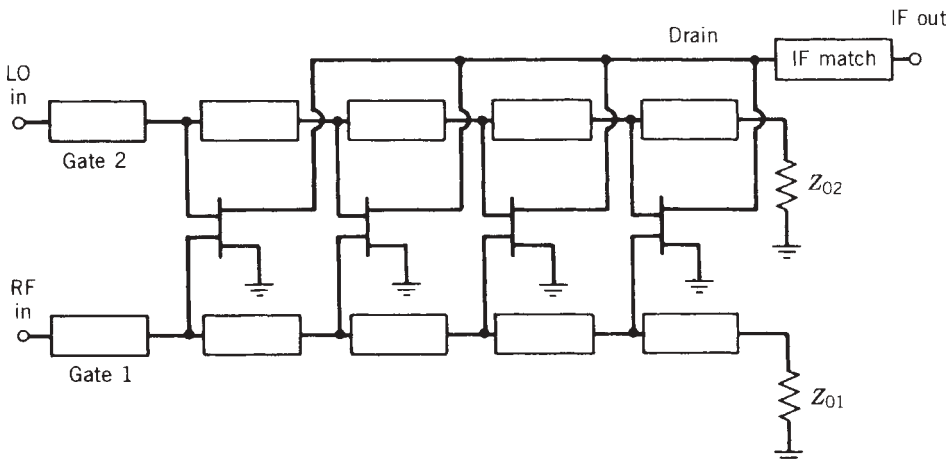
FIGURE 11.96 Schematic diagram of distributed dual-gate FET mixer.
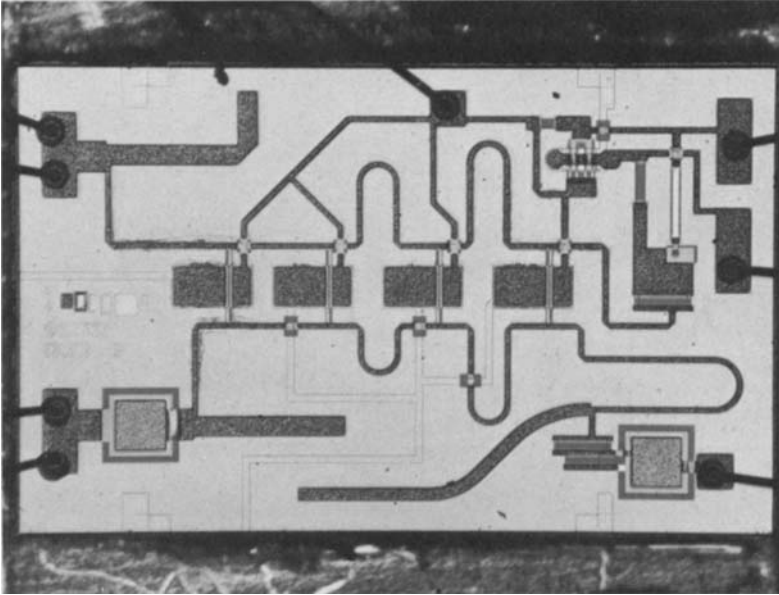
FIGURE 11.97   Monolithic distributed mixer chip photograph. (Courtesy of Texas Instruments.)
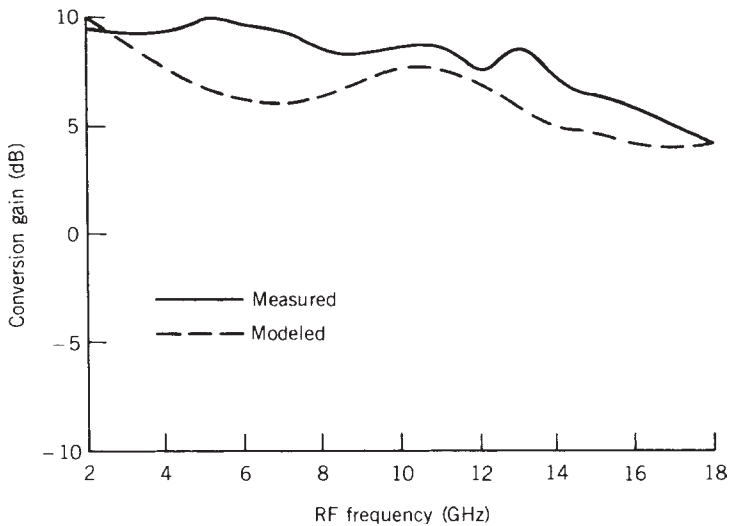
FIGURE 11.98   Measured versus modeled conversion loss characteristics of distributed mixer.

order of 400 Ω, a source-follower single-gate FET IF amplifier was used for impedance matching. A comparison between the measured and modeled (Microwave SPICE) conversion loss (gain) performance for the mixer is shown in Figure 11.98. The conversion gain versus LO power and the conversion gain versus dc bias performances, measured and modeled, are shown in Figure 11.99 and 11.100. As can be seen, the distributed
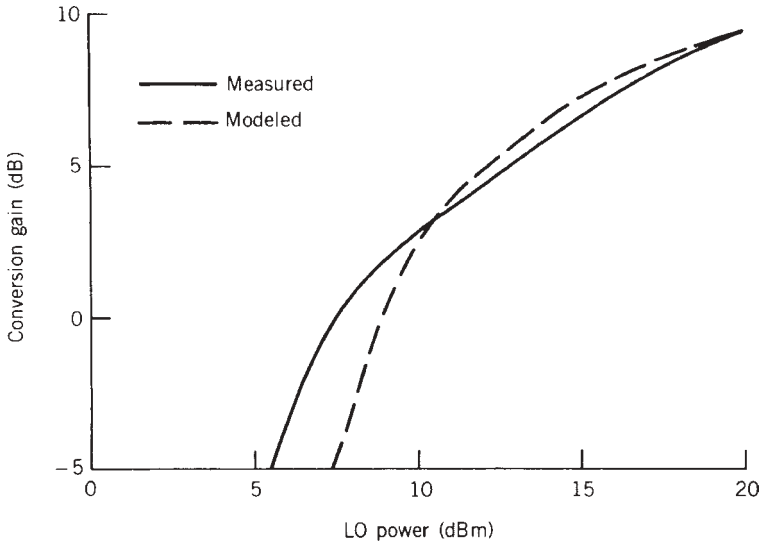
FIGURE 11.99 Measured and modeled performance of LO saturation characteristics of distributed mixer.
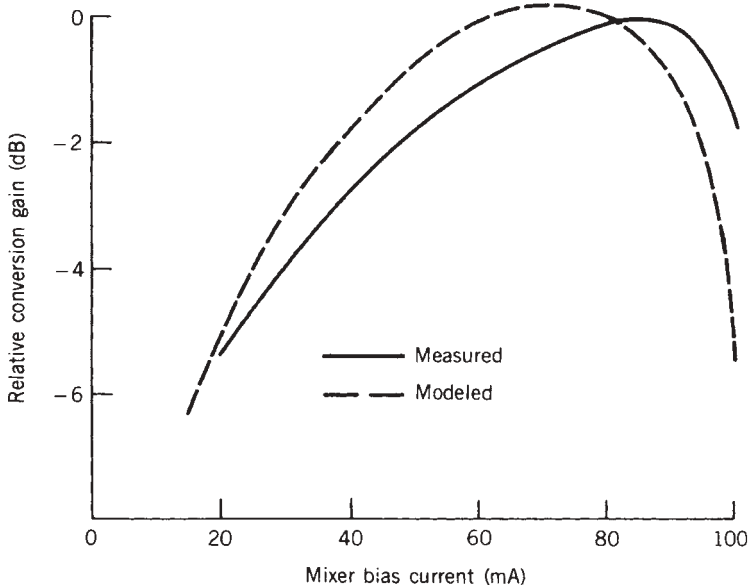
FIGURE 11.100 Measured versus modeled performance of mixer bias sensitivity.

mixer exhibits similar LO compression characteristics as single-FET designs. Although multiple FETs are employed, the mixer is still single ended and offers no spurious product rejection or AM noise suppression; however, it does offer excellent broadband performance, small size, low port VSWR, and compression characteristics similar to those of multidiode mixers.

11.7   BALANCED FET MIXERS

In the previous section we have developed the mixer theory for single-ended FET mixers. The process of combining FETs to form balanced mixer structures and applying the single-ended FET mixer analysis is very straightforward and is easily accomplished by incorporating baluns or hybrids as in the realization of diode mixers. There are, however, some differences and limitations, especially when GaAs monolithic realizations are desired.

In the low-frequency realm, where transformer hybrids are possible, the differences are minor, with the main problem being dc bias decoupling. A single-balanced VMOSFET mixer, which illustrates the added decoupling and bias circuitry and can be designed for HF through UHF operation, is shown in Figure 11.101. The input signal is applied differentially to the FET gates via the RF balun while the LO is injected in each gate in phase. Thus, the IF signals which are developed at each FET drain node, are "out of phase" and must be summed with an additional balun or hybrid. The extra hybrid is required since we cannot "flip" the FET, as we can a diode in a conventional signal-balanced mixer. Since the LO is injected in phase, it cancels in the IF balun, but the RF signal, which enters with the proper phase relationship, is summed at the IF port. Hence, the mixer exhibits LO-to-RF isolation and LO-to-IF isolation but no RF-to-IF isolation. Typically a low-pass filter structure is added at the drain to suppress
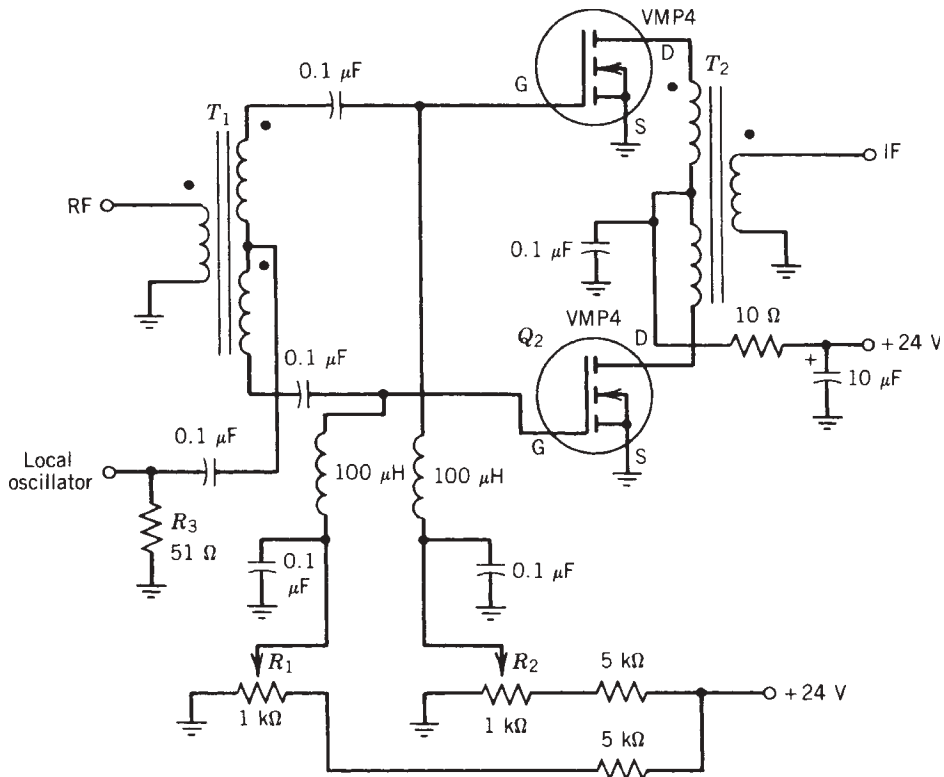
FIGURE 11.101   Single-balanced VMOSFET mixer. (© McGraw-Hill 1988, [11.53].)

the RF signal. If dual-gate FETs were used in place of the single-gate devices, the LO would be injected (in phase) at gate 2 of each FET by simply paralleling both gates at the LO port.

Double-balanced FET mixers can also be designed using transformer hybrids [11.37]. Figure 11.102 shows a typical balanced JFET mixer which can be designed to operate from HF to UHF. An additional balun is again required because of the phase relationships of the IF signals. This structure is completely balanced and exhibits spurious rejection performance similar to diode mixers constructed for the same frequency range. However, the intermodulation and noise figure performance of such structures are superior to simple four-diode designs. For example, third-order intercept points in excess of 33 dBm, with an associated gain of 6 dB, are common in such structures. High-level multiple-diode ring mixers that would require substantially more LO power would exhibit comparable intermodulation characteristics but would never exhibit any gain. At frequencies above several gigahertz, the active balanced mixer problem becomes more complex. At these frequencies, center-tapped baluns are not possible, and it is difficult, because of thermal and other considerations, to integrate suspended structures with GaAs FETs. Single-balanced FET mixers can, however, be constructed with conventional hybrids and phasing networks. An X-band single-balanced mixer employing single-gate FETs was reported by Pucel et al. [11.27], but since then numerous such mixers have been reported. The mixer consisted of two single-gate FETs combined with a quadrature hybrid at the LO and RF ports and a phasing network to properly sum the 30 MHz IF signal. A representative circuit is shown in Figure 11.103. The mixer conversion and noise figure performance as a function of LO power are shown in Figure 11.104. The intermodulation characteristics of the mixer are shown in Figure 11.105.

The third order intermodulation performance of the mixer is shown in Figure 11.105. As can be seen in the above illustrations, the noise figure and third-order intercept point performance compare favorably to those of well designed diode mixers. Designing GaAs FET double-balanced mixers becomes more difficult because of the balun realization. Diode double-balanced mixers, as we recall, typically employ large transmission line baluns, realized with three-dimensional structures, although completely planar 2–18 GHz double balanced mixers have been demonstrated [11.38]. Conventional mixer designs such as these are not feasible for monolithic implementation since their passive elements require excessive GaAs wafer area. Hence, a completely new design concept must be used to develop double-balanced monolithic GaAs FET
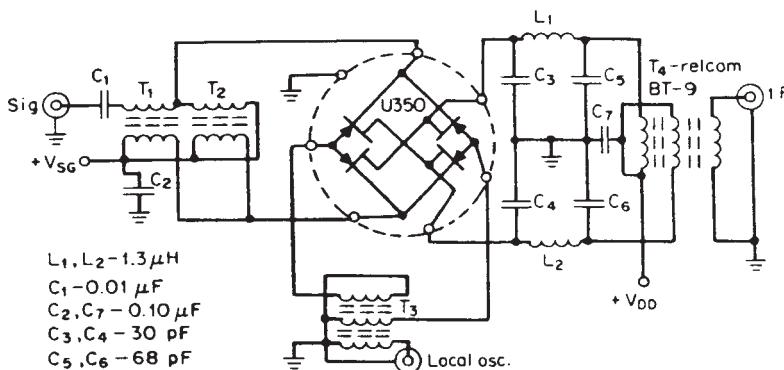
FIGURE 11.102   Double-balanced JFET mixer employing broadband transformers.
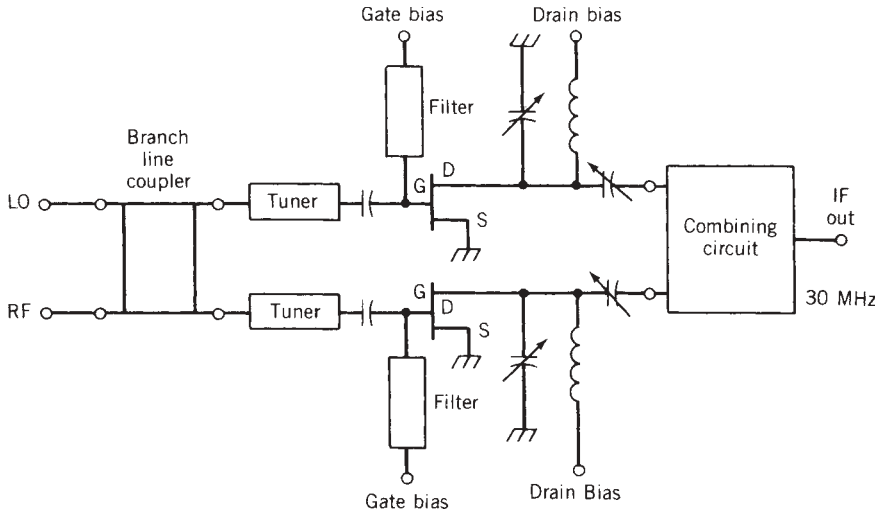
FIGURE 11.103   Single-balanced MESFET mixer. (© IEEE 1976, [11.32].)
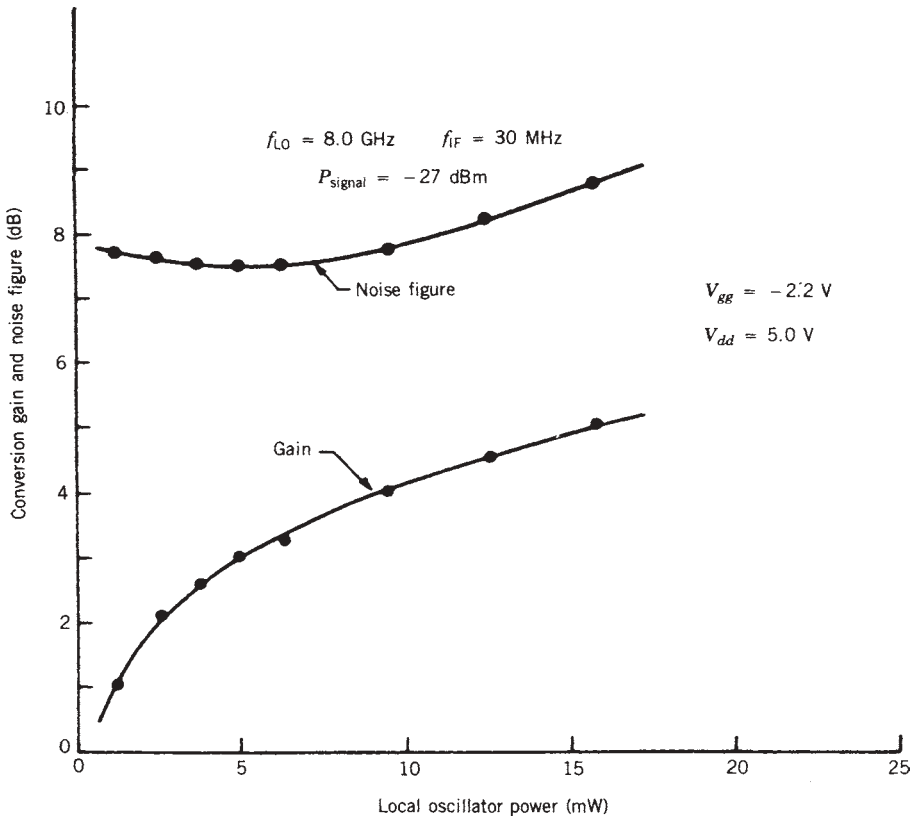
FIGURE 11.104   Measured conversion gain and double-channel noise figure of a balanced GaAs MESFET mixer at X band as a function of LO drive. (© IEEE 1976, [11.32].)
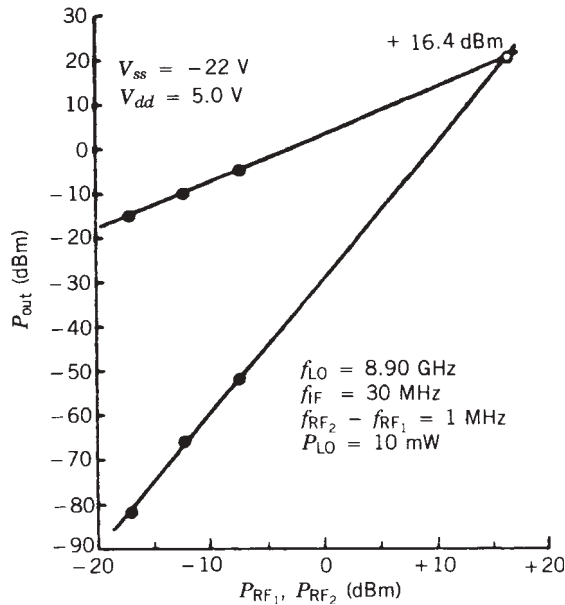
FIGURE 11.105   Third-order two-tone modulation curves obtained with balanced GaAs MES-FET mixer at X band. (© IEEE 1976, [11.32].)

mixers. In the monolithic realm, the balun problem is further constrained by chip area and backside processing requirements. If conventional passive mixer baluns were used, they would be approximately 2 cm. in length, which is an order of magnitude too large for a monolithic circuit realization. Thus, active baluns or lumped-element transformers are the only viable options. A new balun topology that can be readily implemented using monolithic circuit technology has been devised which eliminates the above problems and provides a virtual center tap. Since the balun uses common-gate and common-source circuit techniques, an ideal 180° phase shift occurs for the signals present between the upper and lower halves of the circuit (Fig. 11.106). Typical broadband amplitude performance for a balun designed with no center tap and resistive terminations at the reverse end of the drain transmission line is shown in Figure 11.107. As can be seen, the balun exhibits excellent balance through the design band of 2 to 18 GHz. The performance of a center-tapped balun designed for the same frequency range is shown in Figure 11.108.

Hence, if two such baluns are used in conjunction with a diode or FET ring to form a double-balanced mixer, the IF signal appearing at the ring terminal propagates (in phase) down both arms of the balun and can be summed at a common node, thus forming a virtual center tap. This center tap can be used for IF extraction or grounded to complete the IF return path. Since active baluns are not reciprocal, a combining or dividing structure will be needed on the RF port depending on whether the mixer is used as an up or down converter (Fig. 11.109). The frequency limitations of the RF and LO ports are determined by the distributed amplifier–like sections which can be designed to operate over extremely large bandwidths. The IF frequency response can also be designed to exhibit broadband performance. This mixer concept can also be extended to include double-ring mixer topologies (Fig. 11.110). Double-ring approaches have
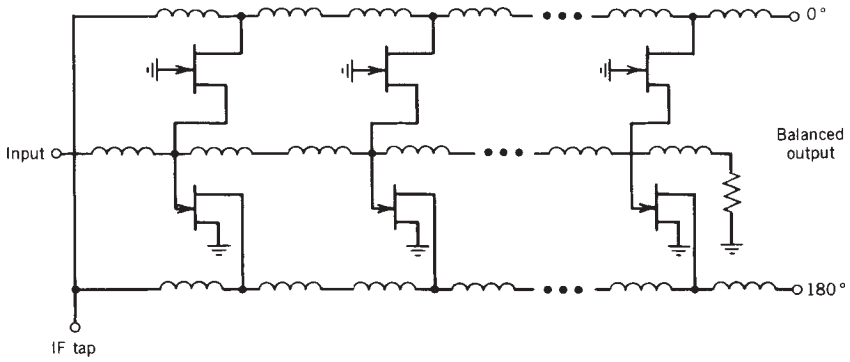
FIGURE 11.106   Lumped-element equivalent circuit of center-tapped balun.
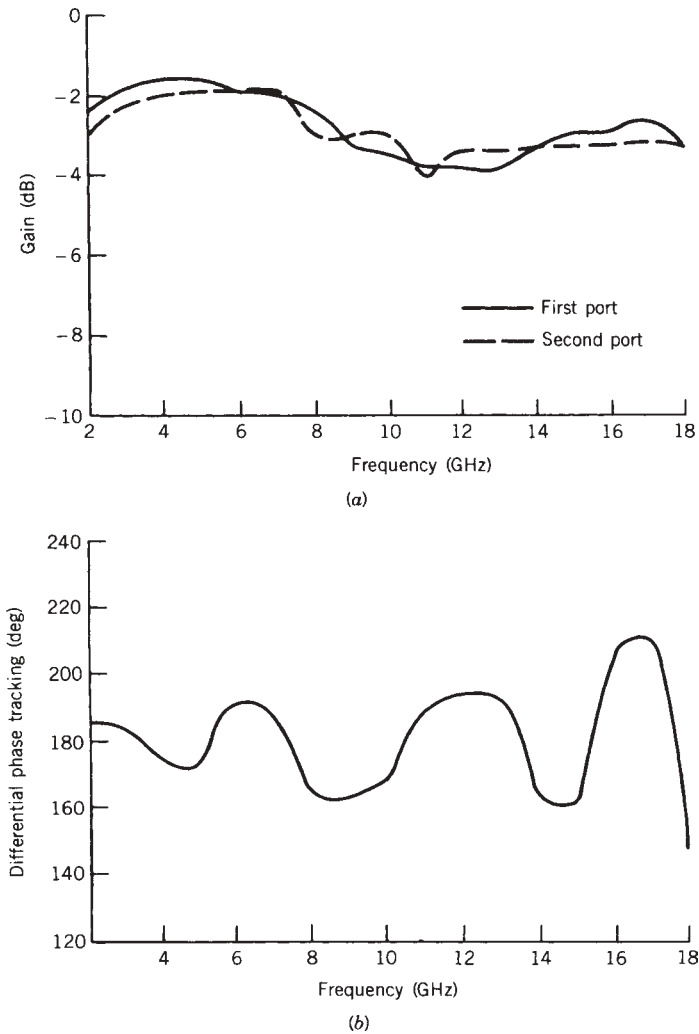
FIGURE 11.107   (*a*) Frequency response and amplitude balance of monolithic balun; (*b*) differential phase performance of monolithic distributed splitting balun.
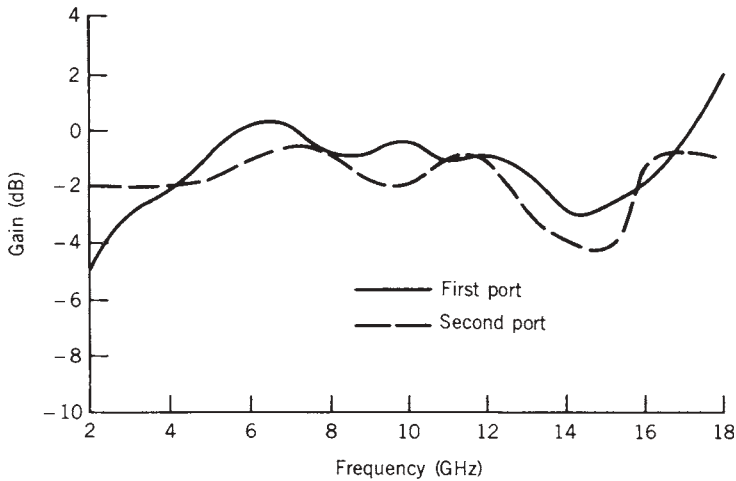
FIGURE 11.108 Center-tapped balun performance (distributed splitting balun with IF tap).

the added advantage of allowing the IF response to overlap the RF and LO frequency bands, thus making IF extraction even easier.

A slightly different topology [11.39] that can be readily implemented using monolithic technology employs active baluns in conjunction with a unique distributed dual-gate FET mixer structure. The proposed circuit topology employs a single balun, which can be either active or the passive lumped-element type (transformer, differential line, etc.), and distributed dual-gate FET mixer sections. Transmission line models for the balun and mixer are shown in Figure 11.111. The number of distributed sections employed is somewhat arbitrary and depends on the bandwidth, conversion gain, and impedance matching requirements. In the above design only two sections were required to achieve adequate distributed performance; however, greater conversion gain could probably have been obtained if more sections were employed at the expense of chip complexity.

As can be seen in the circuit diagram, one mixer section employs a common source topology while the other uses common gate techniques. Thus, an ideal 180 degree phase shift occurs for the signals present between the upper half and lower half of the circuit; hence, eliminating the requirement for a second balun. Both the LO and RF voltages, which are present at the FET drains of each mixer section, are also out of phase by 180 degrees while the IF voltages are in phase. By summing the output of both mixer sections, an independent IF port is obtained and the RF and LO signals are cancelled. Thus, the mixer structure is a completely double balanced.

The frequency limitations of the mixing portion of the circuit are determined by the distributed amplifier–like sections, which can be designed to operate over extremely large bandwidths. With the addition of an IF amplifier (active matching) or bandpass matching network, the IF response could also be further broadened. Because of the large number of active nonlinear elements, the dynamic range can be made as good as or better than the best conventional diode mixers. The RF balun can also be designed with sufficient gain, thus reducing or eliminating the need for an RF preamplifier in the final receiver. These types of structures are not limited to just monolithic circuit
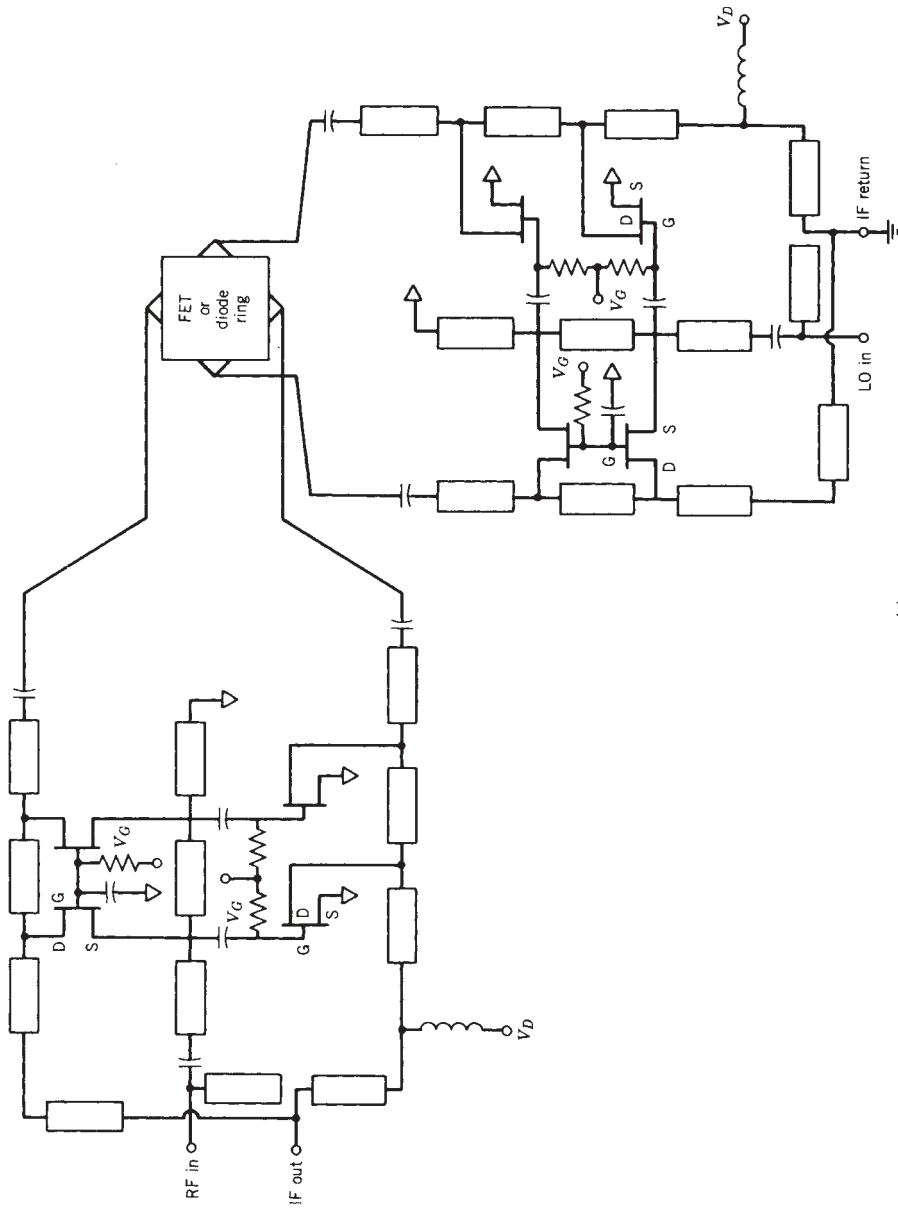
FIGURE 11.109 (*a*) Down-converter mixer circuit diagram; (*b*) up-converter mixer circuit diagram.

(*a*)
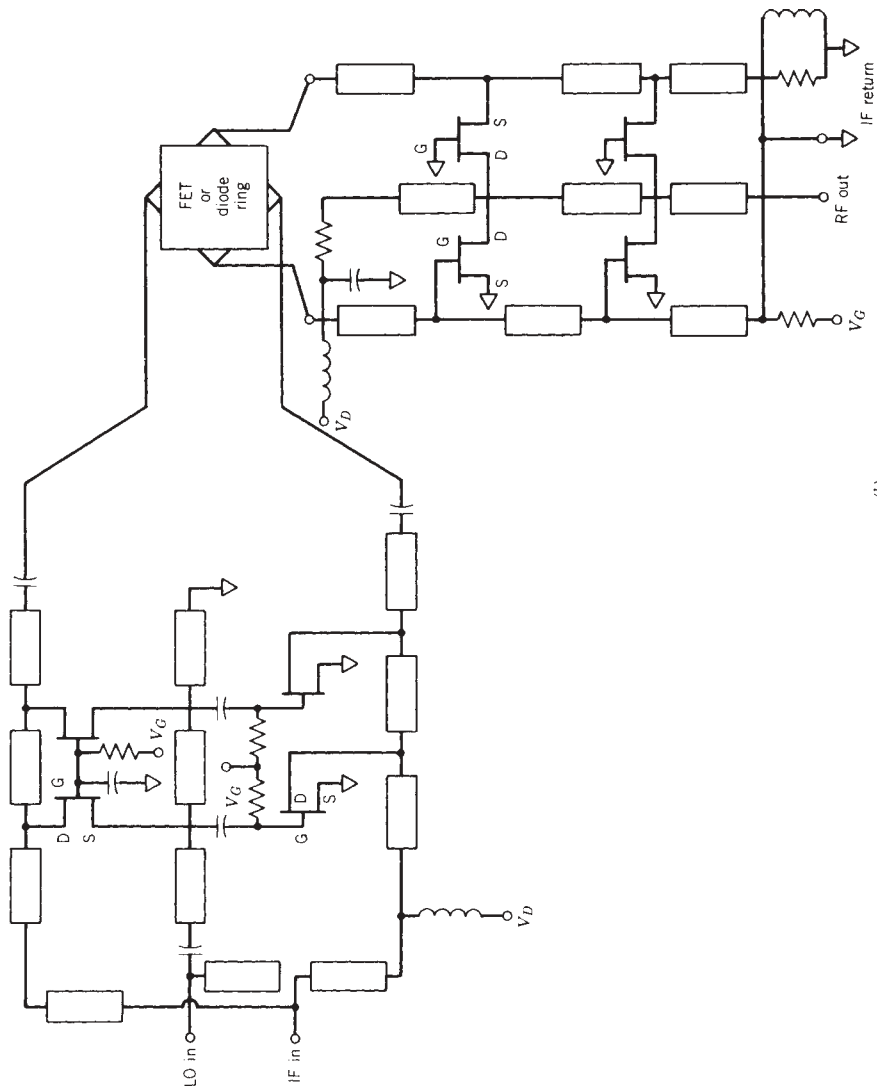
FIGURE 11.109 (continued)
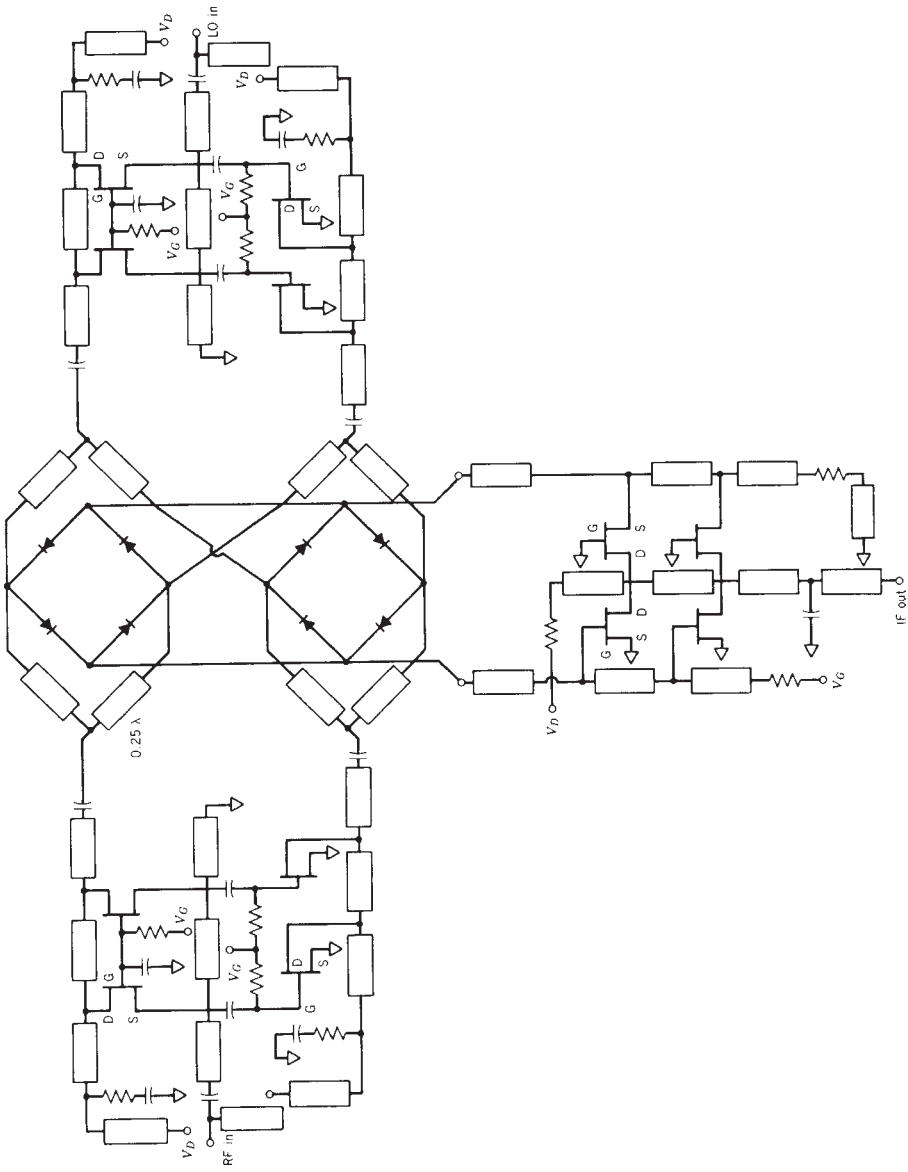
FIGURE 11.110 Circuit diagram of double-ring mixer.

RF out /0°

V_D

V_G

RF in

V_G

V_D

RF out /180°

(a)

RF in /0°

G_2 D
G_1 S

V_{G2}

IF out

V_{G1}

G_1 S
G_2 D

RF in /180°

LO in

V_{G2}

V_D

(b)
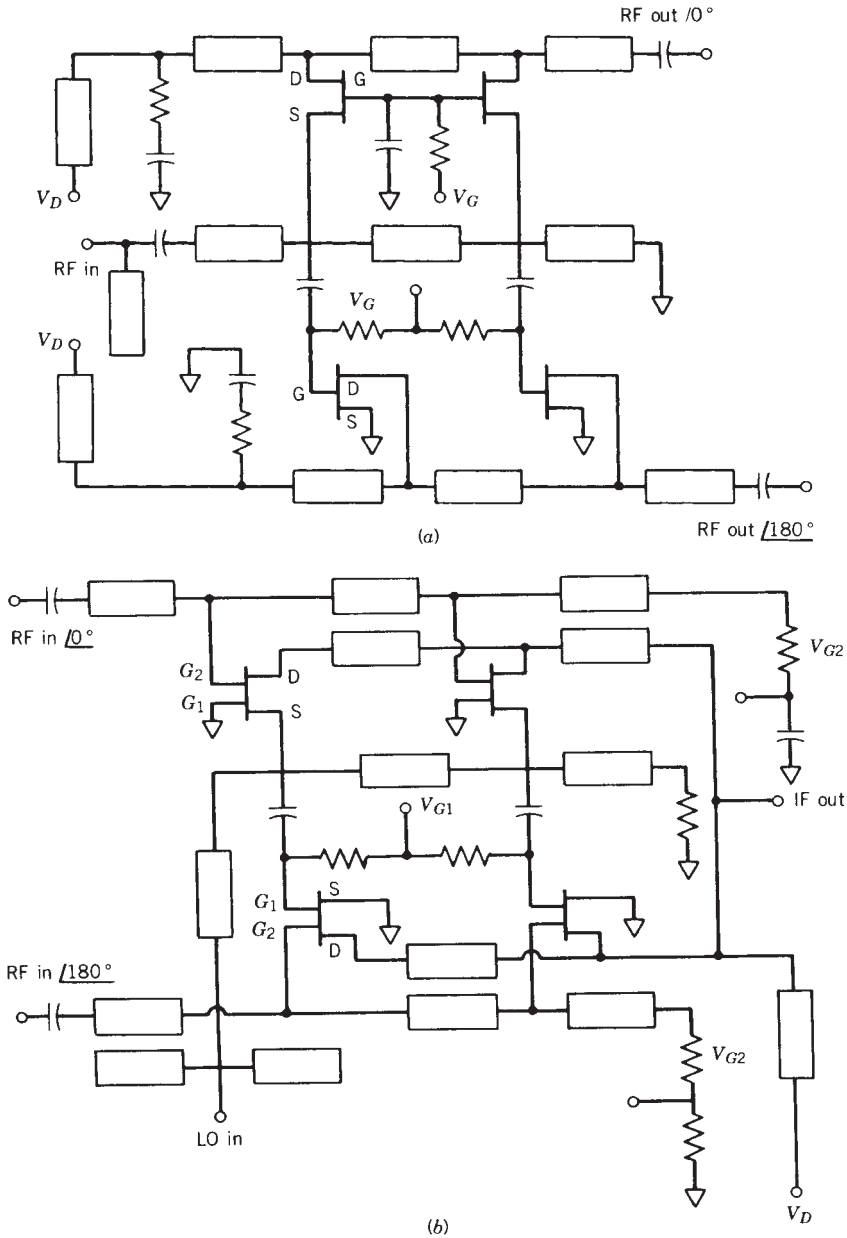
FIGURE 11.111 (*a*) Transmission line model of distributed active balun; (*b*) transmission line model of monolithic double-balanced mixer.

implementation; they can easily be built in other media such as low-temperature cofired multilayer ceramic (LTCC), where resistors, inductors, and capacitors can be integrated.

The distributed monolithic balun and mixer shown in Figure 11.112 were designed using 0.5-μm × 150-μm dual-gate FETs fabricated on a 0.15-mm-thick GaAs substrate. The FETs were modeled as cascode-connected, single-gate FETs with the linear model
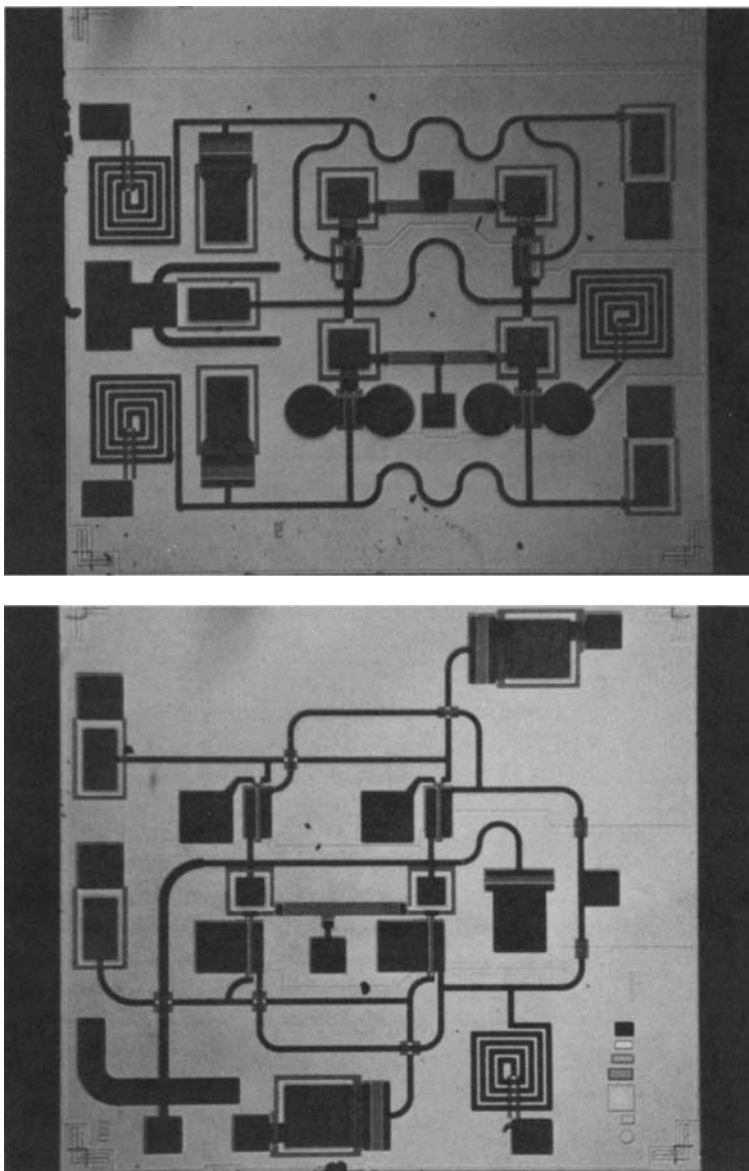
FIGURE 11.112   Monolithic double-balanced mixer and active balun ICs. (Courtesy of Texas Instruments.)

elements determined from S-parameter measurements. The nonlinear drain current and transconductance characteristics were obtained from $I-V$ curve data obtained at 1 MHz. (*Note*: Technique is described in Chapter 9.) Short-pulse-width ($<$300-μs) pulsed $I-V$ systems with dc offset would yield better nonlinear data. The active balun used with the mixer also employed both distributed common-source and common-gate amplifier sections in order to obtain a broadband differential phase output with good amplitude balance.

The mixer–balun combination was evaluated as a conventional double-balanced mixer with the LO drive applied to the first gate through the first gate 1 circuit. The RF signal was applied to the active balun, which in turn drives the second gates. The dc bias on both gates was adjusted for optimum conversion loss; however, since the mixer performance was very insensitive to bias, the second gate voltage was set to zero while the first gate was biased for a drain current of $I_{dss}/2$. Using the above bias conditions, the conversion loss characteristic shown in Figure 11.113 was obtained. The RF-to-IF and LO-to-IF isolations, which demonstrate the excellent balance obtained in the design, are shown in Figure 11.114. Conversion loss performance as a function of LO
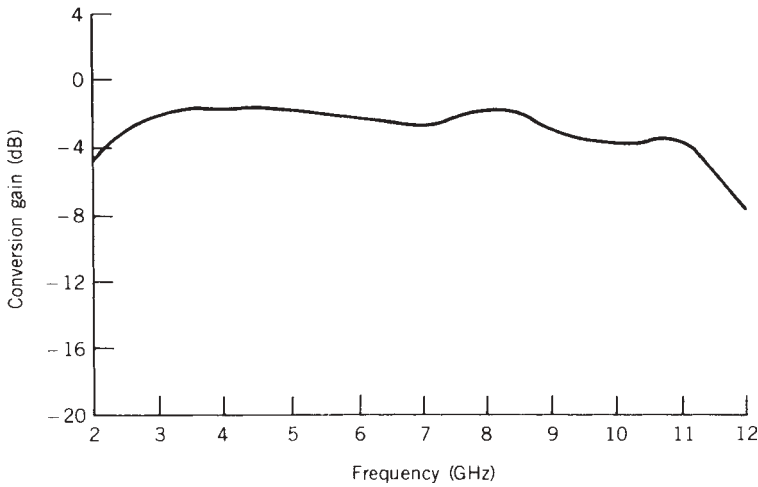
FIGURE 11.113   Monolithic double-balanced mixer conversion loss performance as a function of frequency.
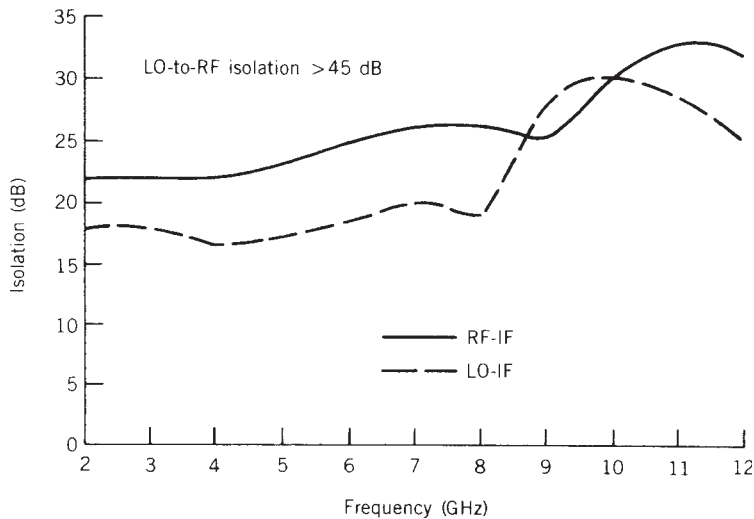
FIGURE 11.114   Isolation performance of double-balanced mixer.
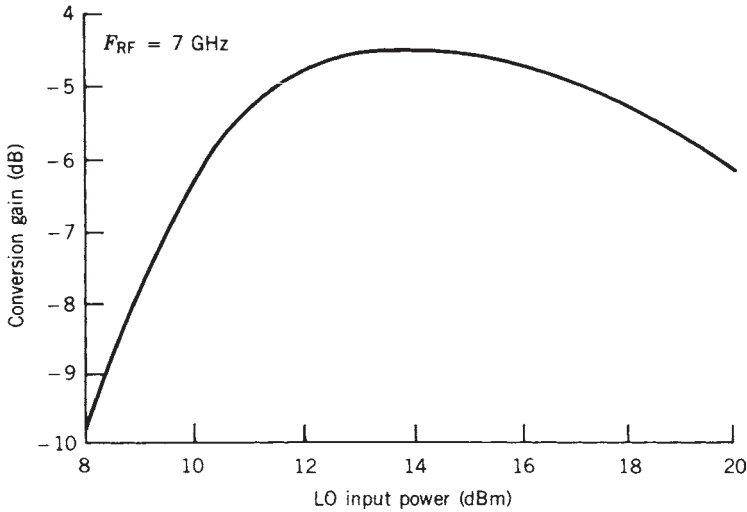
FIGURE 11.115   Conversion loss as a function of LO power.
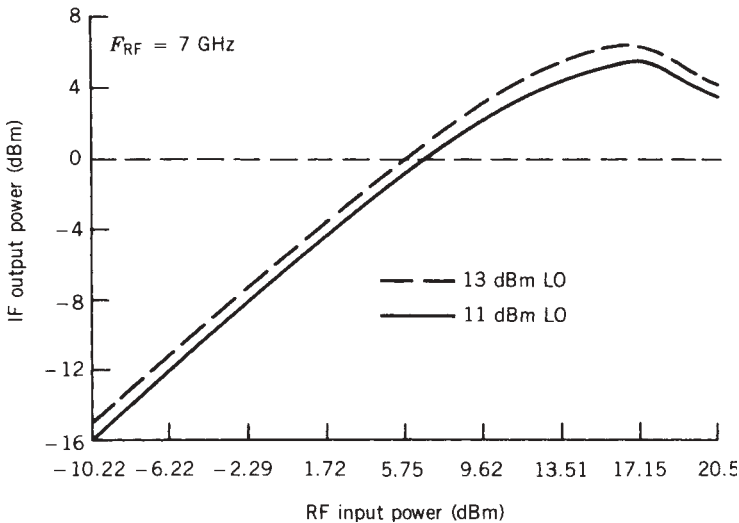
FIGURE 11.116   RF compression characteristics.

power and the RF compression characteristics are shown in Figures 11.115 and 11.116. As can be seen, the mixer's performance is comparable to hybrid diode designs.

This type of structure, with its unique balanced characteristics, can be used as a broadband up converter as well as a conventional mixer in a variety of receiver applications. In addition, since the mixer is completely balanced, the IF response can overlap both the LO and RF responses which usually can only be accomplished with a double-double-balanced structures.

As mentioned previously, distributed active baluns can be used in conjunction with diode rings to form active/passive double-balanced mixers. Although this approach is

not, strictly speaking, a balanced FET mixer, it is an interesting approach and will be presented briefly. As noted, two distributed baluns can be used in conjunction with a diode ring to form a double-balanced mixer, and a double-double-balanced design can be accomplished by adding a third balun. By using the above-mentioned technology, both single- and double-ring designs of the types depicted in Figures 11.109a and 11.110 were fabricated. The single-ring design exhibited a conversion loss performance on the order of −8 dB at an associated IF of 4 GHz. The operating bandwidth for both the LO and RF ports of the mixer was 4 to 18 GHz. The mixer LO-to-RF and LO-to-IF isolation are shown in Figure 11.117. The conversion performance as a function of frequency, which was measured at an IF of 500 MHz, for the double-double-balanced design (two four-diode rings) is shown in Figure 11.118. Although the mixers employ diodes as the nonlinear element, the conversion loss (gain) of the double-ring design is somewhat greater than a conventional structure because of the gain associated with the baluns. The isolation characteristics, which are comparable to a hybrid designs, are shown in Figure 11.119.

By using this dual-mode characteristic of distributed broadband baluns in diode mixer topologies, a very compact monolithic circuit, which is very process tolerant, can be designed to operate over a frequency range several octaves wide with performance comparable with conventional passive diode mixers. These types of structures are very process tolerant because the mixing action is performed by diodes, which exhibit consistent mixing action almost independent of the fabrication process, which is not the case for FETs. In addition, distributed structures are the most forgiving active
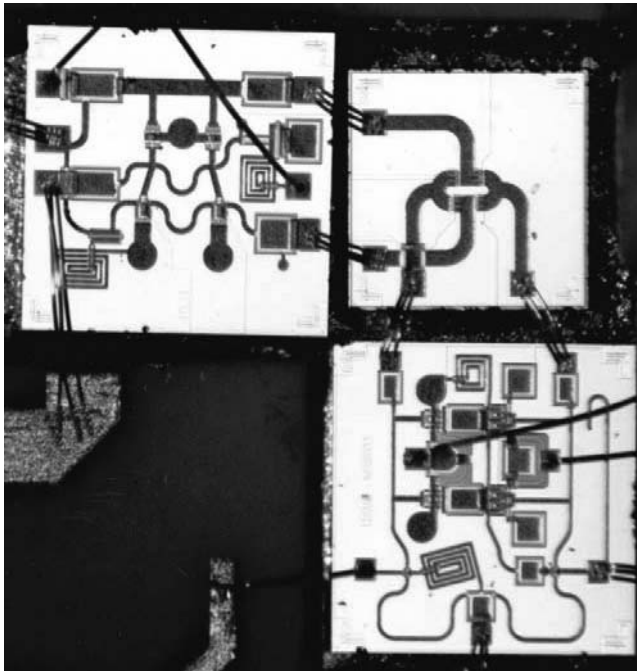
(a)

FIGURE 11.117 (a) Monolithic active/passive double-balanced mixer. (Courtesy of Texas Instruments.) (b) Isolation performance. (c) Compression characteristics.
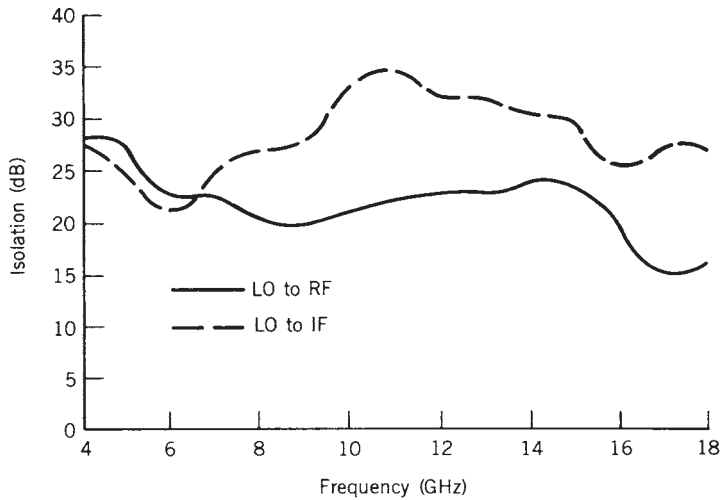
(b)
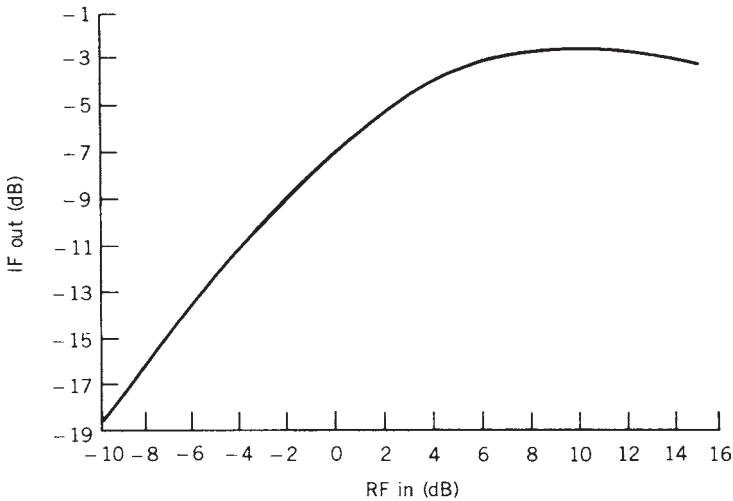
(c)

FIGURE 11.117   (*continued*)

circuit topologies, since active circuits have gain and reverse isolation, they effectively isolating diode and circuit mismatch variations.

11.8 SPECIAL MIXER CIRCUITS

There are a variety of interesting mixer topologies in widespread use that perform vital system functions which cannot be simply classified as balanced mixers. Probably the most popular configuration is the image rejection or single-sideband mixer. However, a variety of subharmonically pumped and self-oscillating mixers are in limited use [11.40].
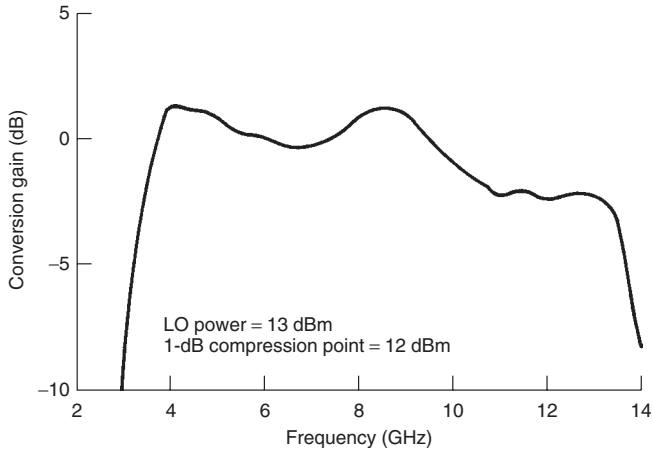
FIGURE 11.118 Conversion loss performance of monolithic double-ring mixer.
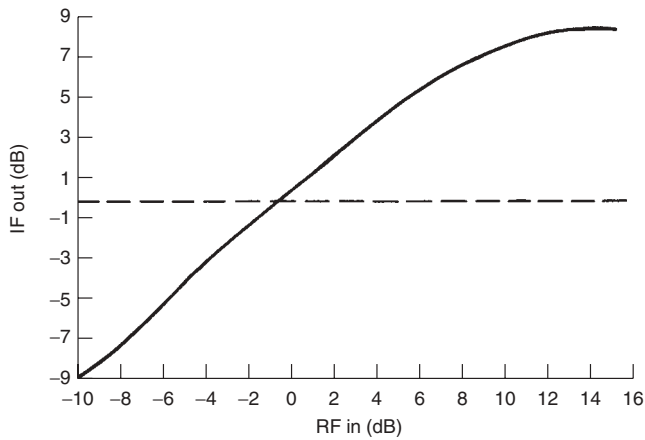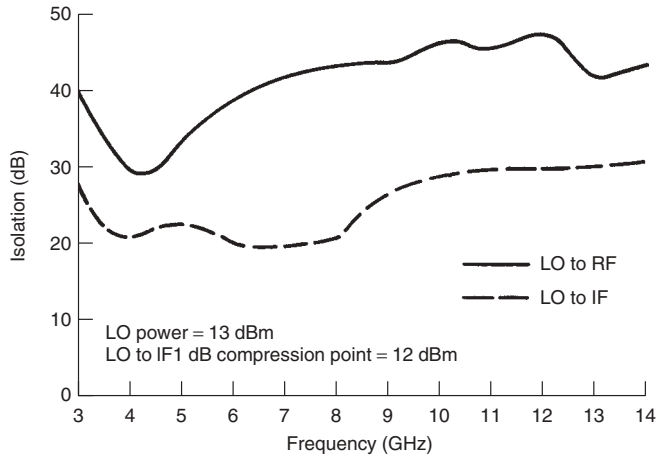
FIGURE 11.119 (*a*) Isolation and (*b*) compression performance of monolithic double-ring mixer.

In many systems it is very advantageous to eliminate or substantially reduce the additional noise power due to the mixer's image response, which is converted to the IF passband. When the IF is low or the operating bandwidth sufficiently large, image filtering cannot be implemented effectively; hence the mixer must be designed with inherent suppression of the unwanted mixing product. This suppression can be obtained by the use of a different type of balanced structure, not unlike a conventional balanced mixer. Unfortunately, no performance enhancement is obtained other than image suppression, as in the case of image-enhanced mixers, since the image energy is not recycled but rather is directed to an unwanted circuit port and dissipated. This is usually not a problem, since many systems may even sacrifice conversion loss or mixer noise figure performance to obtain an image-fee response characteristic, since the system noise figure can be restored with additional RF amplification. Also, the image-suppressed response will enable the system to exhibit up to 3 dB of sensitivity improvement beyond what could have been obtained with a conventional broadband mixer regardless of the amount of additional RF amplification.

The classic image rejection mixer (Fig. 11.120*a*) or single-sideband modulator (Fig. 11.120*b*) topology consists of two mixers with at least one signal applied in quadrature (depending on the application) while the other signal is either combined at the IF output or applied to the IF input in quadrature. Usually, double-balanced mixers are employed in the circuit to suppress the carrier, but single-balanced designs are sometimes used.

The operation of an image rejection mixer is easy to understand, but at first glance it may resemble a conventional hybrid combined (balanced) amplifier. The differences lie in the way the upper sideband (USB) and lower sideband (LSB) components for both positive and negative frequency are processed by the circuit. For example, when the positive LSB is down converted, it becomes a negative IF signal. Similarly, when
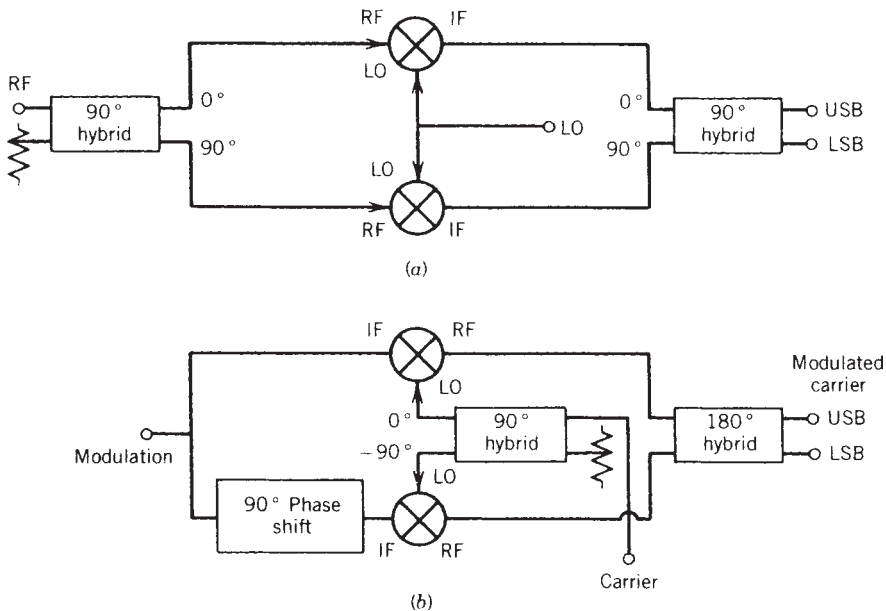
FIGURE 11.120   (*a*) Image rejection and (*b*) single-sideband mixer topology.
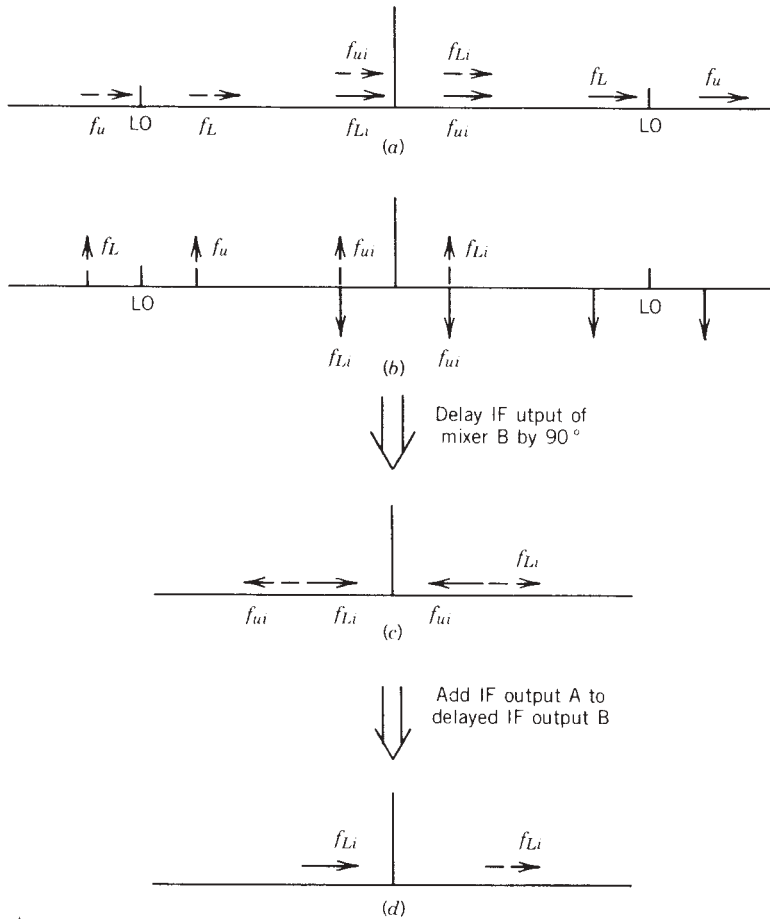
FIGURE 11.121 Frequency spectra at various points within the image rejection mixer: (*a*) spectra of mixer A; (*b*) spectra of mixer B; (*c*) IF output of mixer B delayed by 90°; (*d*) composite spectra at LSB IF output.

the negative USB is down converted, it becomes positive. Hence the positive and negative components are processed differently by the RF and IF couplers. Figure 11.121 illustrates this concept.

With the phase relationships depicted in Figure 11.120, the IF components due to the positive and negative RF upper and lower sidebands are all down converted with zero phase shift by mixer A. But if the positive RF signals (USB and LSB) are delayed by 90°, which is equivalent to advancing the negative RF components by 90°, the IF spectra depicted in Figure 11.121*b* result. Note that the positive and negative IF components from mixer B due to the upper and lower RF sidebands are 180° out of phase. If we further delay the IF output of mixer B by 90° (IF hybrid), the spectra shown in Figure 11.121*c* result. Thus when the IF outputs of mixers A and B are summed in the IF hybrid, the USB components of the IF signal will cancel, leaving only the positive and negative IF LSB components. If the IF outputs of mixers A and B are subtracted, only the USB will be present.

When all the components in the circuit are perfectly matched, image cancellation is complete. Unfortunately, perfection is difficult to obtain, although sometimes demanded; hence the rejection of the image will be finite. This rejection [11.41], which is a measure of the circuit performance, can be expressed as a function of the total circuit amplitude and phase imbalance. We then can define the image rejection as

$$R_i = \frac{1 - 2(A)^{1/2} \cos \Delta\theta + A}{1 + 2(A)^{1/2} \cos \Delta\theta + A} \tag{11.96}$$

where $\Delta\theta$ is the phase imbalance and A is the amplitude imbalance. Typically, well-designed broadband mixers can achieve image rejections of approximately 20 dB, and narrowband designs can sometimes achieve as much as 30 dB. A suppression of 20 dB corresponds to an amplitude imbalance of 1 dB and phase errors of less than 10°. A convenient graph for determining image rejection based on circuit amplitude and phase errors is shown in Figure 11.122.

A typical broadband image rejection mixer (Fig. 11.123) which was fabricated on a 0.5-mm-thick quartz substrate was configured as shown in Figure 11.124. The image rejection achieved for the 2- to 10-GHz frequency range is shown in Figure 11.125*a* and the carrier suppression performance is shown in Figure 11.125*b*. The RF quadrature coupler, which is visible in the photograph, was realized with a velocity-compensated multisection coupler [11.42] employing an eight-strip Lange center section. The IF hybrid was external to the mixer.
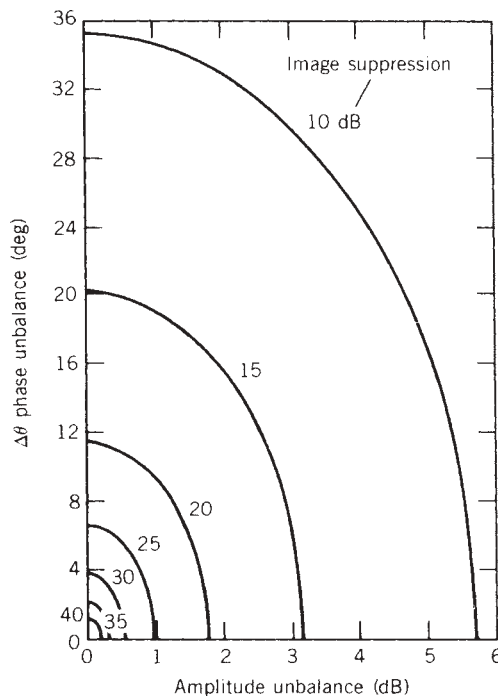
FIGURE 11.122   Image rejection as a function of circuit amplitude and phase errors.
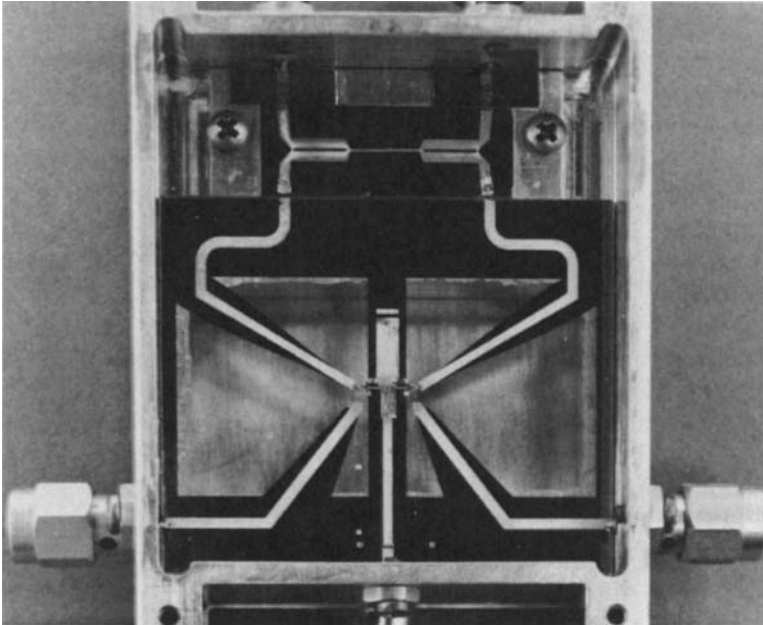
FIGURE 11.123   Typical image rejection mixer consisting of a dual double-balanced mixer and multisection coupler. (Courtesy of Texas Instruments.)
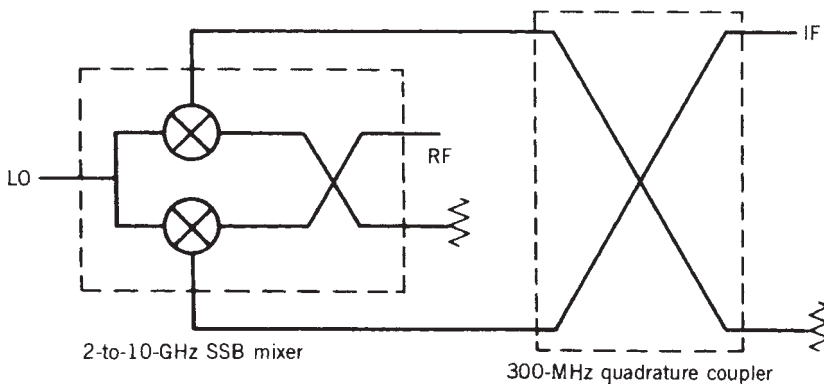
FIGURE 11.124   Image rejection mixer circuit configuration.

A similar dual double-balanced mixer and multisection coupler (Fig. 11.126), configured as shown in Figure 11.127, was evaluated as a broadband SSB modulator. The sideband suppression and carrier suppression for the modulator are shown in Figure 11.128. The mixers and coupler were fabricated on a quartz substrate and the modulation signal was supplied with the proper sin/cos relationship.

Active devices can also be used as nonlinear elements in SSB modulators and image rejection mixers. A convenient monolithic GaAs FET double-balanced mixer structure, reported by Thompson and Pavio [11.43], is shown in Figure 11.129. The circuit (Fig. 11.130) consists of two differential pairs with their associated current
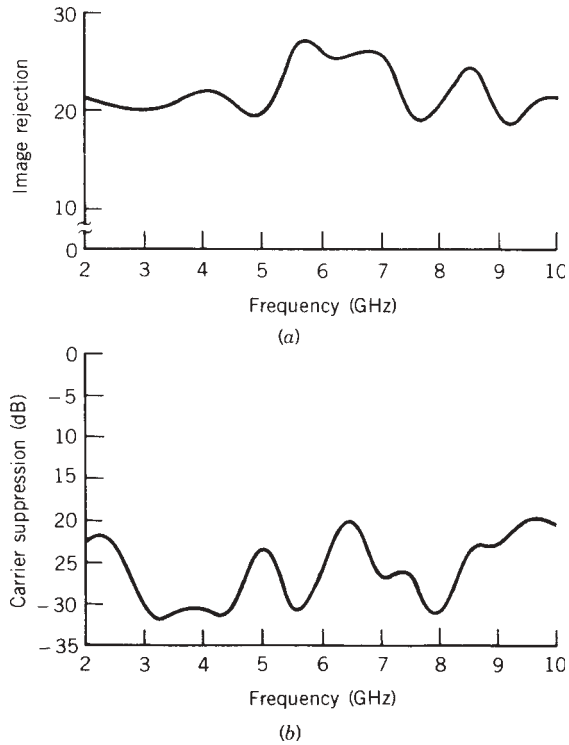
FIGURE 11.125 Performance of 2- to 10-GHz image rejection mixer: (*a*) image rejection; (*b*) carrier suppression performance.
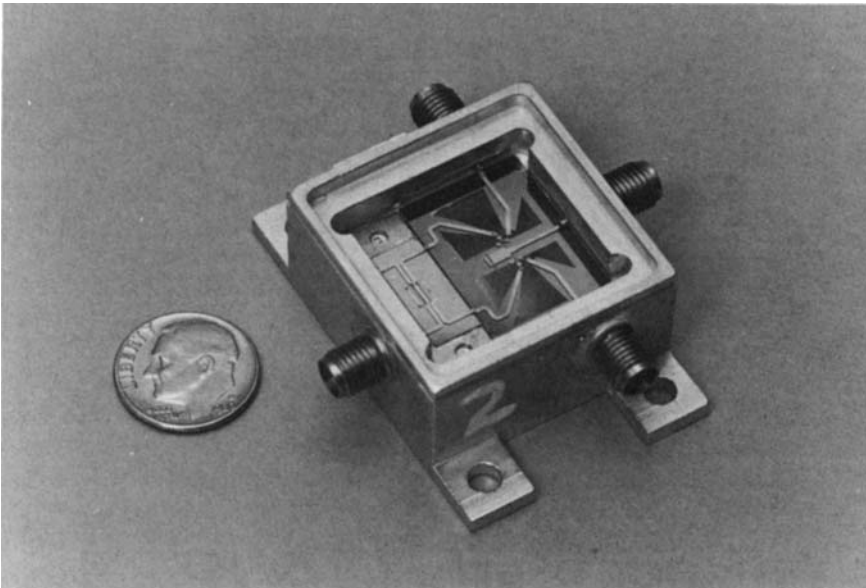
FIGURE 11.126 Single-sideband 8- to 18-GHz modulator fabricated on a quartz substrate. (Courtesy of Texas Instruments.)
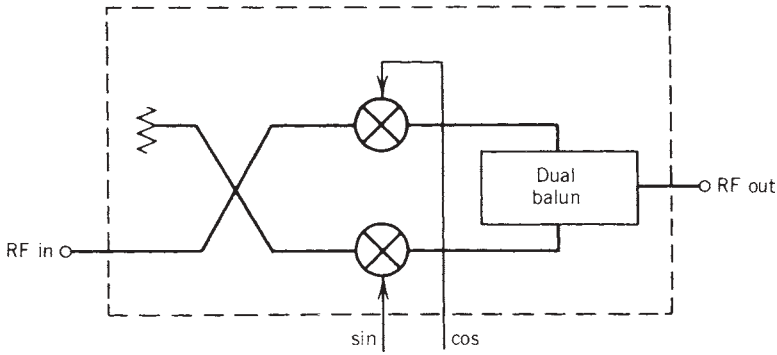
FIGURE 11.127   Single-sideband modulator circuit configuration.
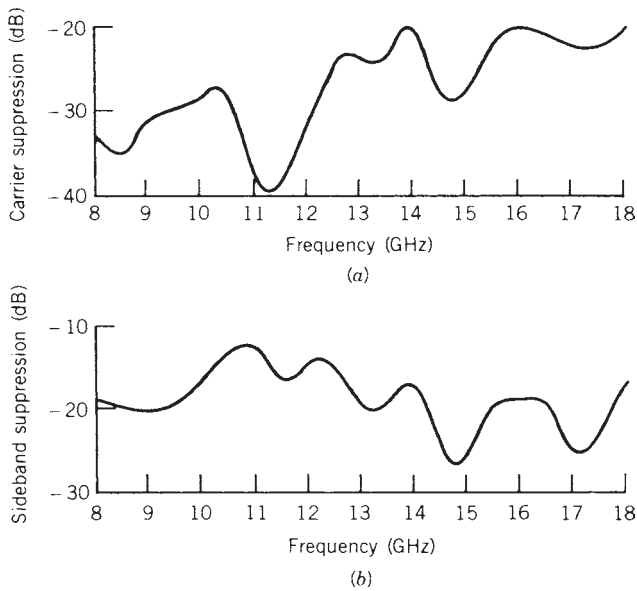
FIGURE 11.128   Single-sideband modulator performance: (*a*) carrier suppression; (*b*) sideband suppression.

sources and an external quadrature coupler. The modulation input signal was also supplied from an external source with the proper sin/cos phase relationship.

When the RF (carrier) signal is applied to one gate of a differential pair, currents equal in magnitude and opposite in phase are produced in each FET. Since the drains of each FET are connected together, the carrier is canceled. However, since the modulation is applied to each FET differentially, the phase difference between the carrier and modulation in each FET is the same; thus the IF currents developed are summed at the drain terminals of each FET pair. The carrier and modulation are then applied to each pair in quadrature so that only one sideband of the modulator waveform appears at the circuit output. Sideband selection can be accomplished by reversing the phase relationship between the modulation signals (sin/cos to sin/−cos).
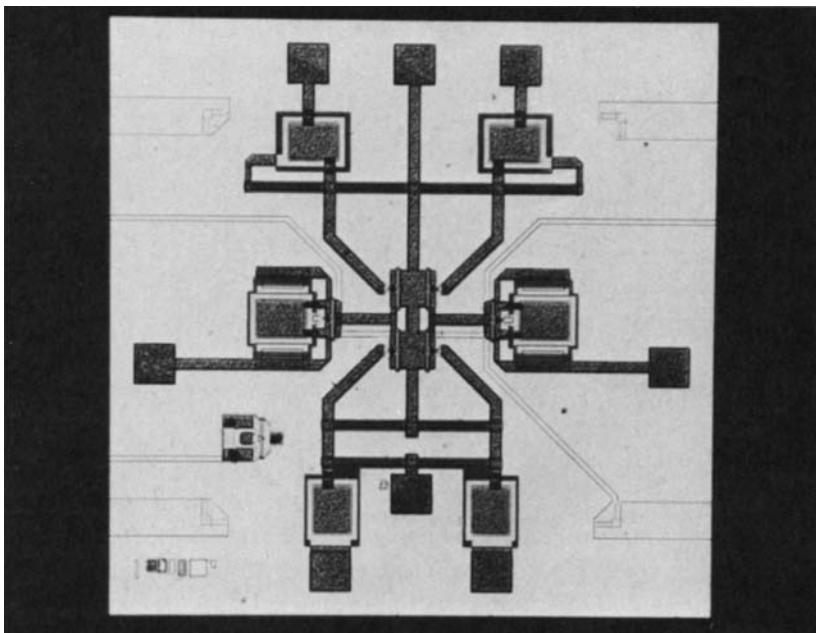
FIGURE 11.129   Monolithic GaAs FET single-sideband modulator. (Courtesy of Texas Instruments.)
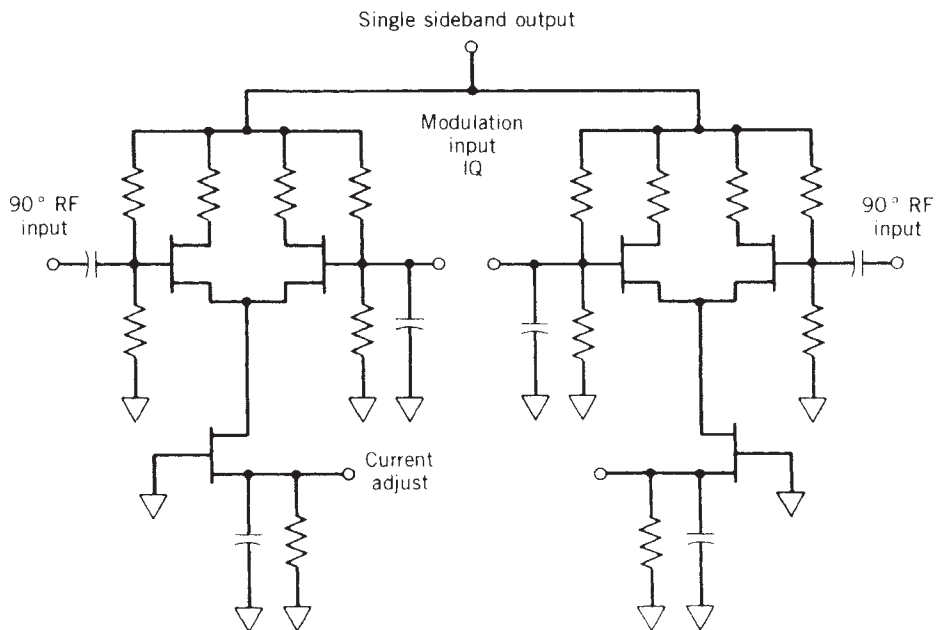
FIGURE 11.130   FET modulator circuit configuration.
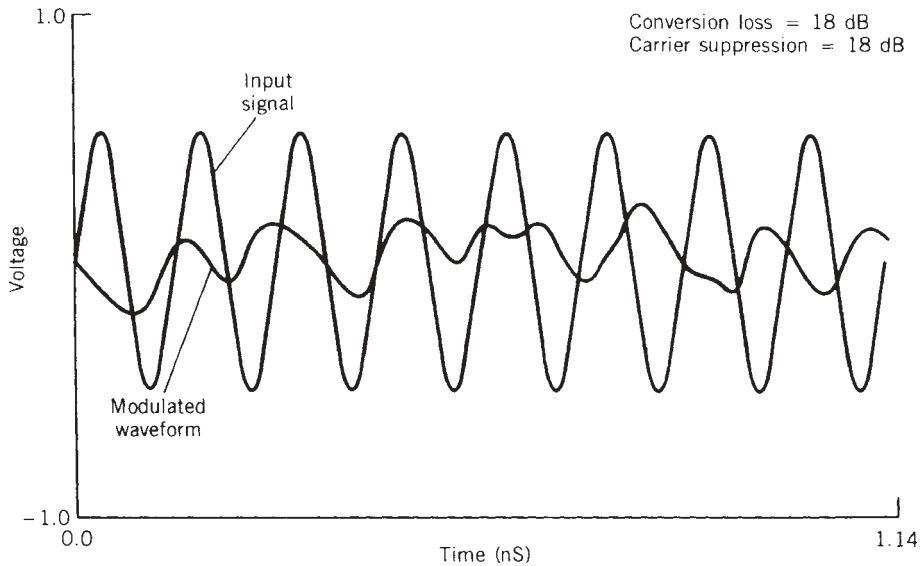
FIGURE 11.131   Input and output voltage waveforms for SSB modulator.

A typical output waveform which was calculated using Microwave SPICE is shown in Figure 11.131. It is interesting to note that the number of cycles plotted for the input waveform is one more than the number of cycles of the output waveform for the same time span. Hence the analysis clearly demonstrates LSB performance. Although the analysis was conducted at a carrier frequency of 7 GHz, the output voltage waveform of the circuit was verified using a traveling-wave oscilloscope at a carrier frequency of 1 GHz. The measured versus computed spectral performance of the circuit is shown in Figure 11.132.

Another important structure is the subharmonically pumped mixer. Subharmonic pumping is usually employed when fundamental LO injection is not feasible due to oscillator frequency limitation, noise performance, or economics. These techniques are common in the millimeter frequency range but are sometimes employed in low-cost commercial products.

Any mixer structure can be operated at a subharmonic of the LO, but the conversion efficiency is usually poor unless the mixer is specifically designed to enhance a particular $1 \times m$ product. Most structures employ antiparallel diode pairs, although single-diode mixers can be used. The basic circuit concept is shown in Figure 11.133, where the LO and RF signals are applied through bandpass filter structures and the IF signal is similarly extracted by means of a bandpass network.

When the diodes are matched (identical), the 1×1 (1, 1) response is canceled. This phenomenon can easily be explained if one considers the conductance waveform of each diode and its composite. If the circuit had only a single diode, the diode would conduct during the positive-going half of the LO waveform and be nonconductive throughout the rest of the cycle; thus one conductance peak would occur per LO cycle. When a second diode is introduced, but with a reverse polarity, it too conducts only once per LO cycle. However, its conductance waveform is produced during the opposite half cycle from that of the first diode.
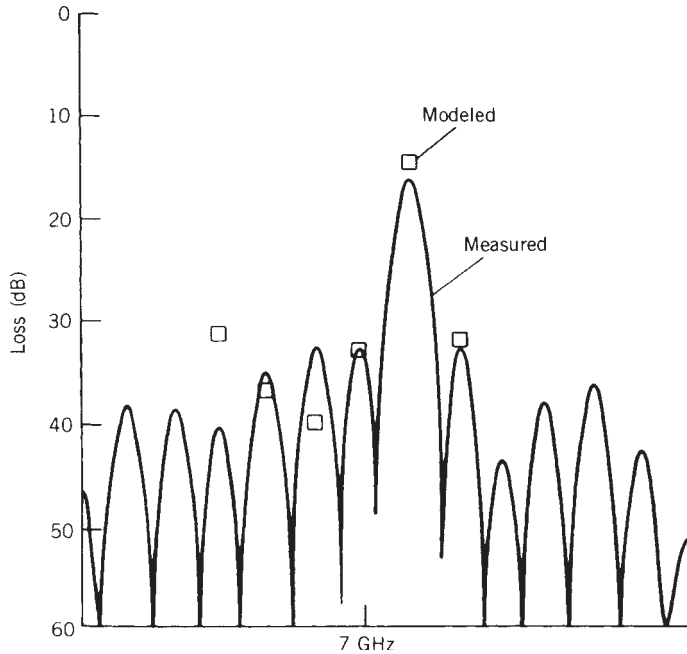
FIGURE 11.132 Measured versus computed spectral performance of SSB modulator.
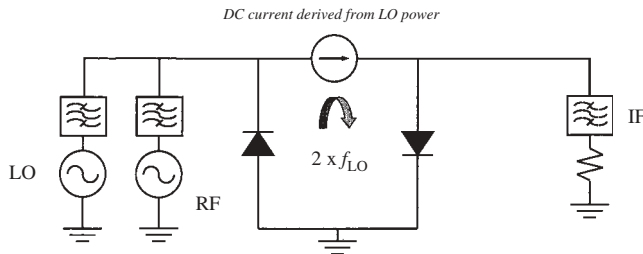
FIGURE 11.133 Simplified circuit configuration of subharmonically pumped diode mixer.

The IF signal generated in each diode by the LO (f_p) and RF inputs must then be 180° out of phase. Since the diodes are paralleled, the fundamental response cancels. The composite conductance waveform exhibits two conductance peaks per LO cycle, which is equivalent to one conductance peak per LO cycle at twice the LO frequency ($2F_p$). This is essentially the same 1×2 (1,2) mixing response that would be obtained with a single diode, except for differences due to the diode's junction capacitance waveform. Relatively efficient mixer performance can also be obtained using the fourth harmonic of the LO, which yields conversion losses in the range 15 to 20 dB.

Subharmonically pumped mixers are very popular at millimeter-wave frequencies where obtaining high-frequency local oscillators at reasonable power levels is complex, difficult, and expensive. Popular commercial applications for this type of circuit are mixers for 77-GHz radar and police traffic radar applications. A simple monolithic circuit mixer which illustrates all the necessary circuit functions is shown
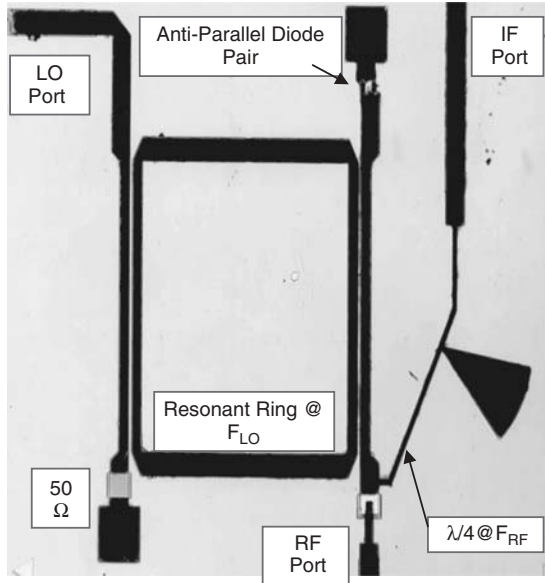
FIGURE 11.134   Typical single-ended subharmonically pumped MMIC mixer.

in Figure 11.134. The directional ring resonator filter effectively isolates the RF and LO signals, and since the IF band is typically much lower in frequency than either the LO or RF signals, the blocking capacitor at the RF port and IF low-pass filter ($L–C–L$) form an excellent signal diplexer. The IF current return path is through the grounded end of the diode pair and the IF load.

The previous discussion presented just a few of the special or unique mixer structures that are currently in use. As GaAs FET and bipolar technology matures, many new structures and some old friends from the linear IC world will start to find their way into the microwave region. However, it will still be difficult to surpass the performance of a well-designed diode and diode mixer.

11.9   USING MODERN CAD TOOLS

In the previous sections of this chapter, various analytical methods which can be used to design both active and passive mixers were illustrated. Whether the method employs Voltera series analysis, conventional harmonic balance, or time-domain techniques or design by linear equivalent networks, it is important that one fully understand the basis of these techniques before unleashing a nonlinear simulator. Modern CAD tools have become so powerful that any type of mixer can easily be simulated with excellent results. The passive portions of even the most complex double-double-balanced mixers are straightforward to analyze using an electromagnetic simulator such as Sonnet Software's EM. In the past, some of the mixers illustrated in Section 11.4 that could only be designed using "cut-and-try" techniques now can be completely simulated and optimized.

To help illustrate the power of modern nonlinear simulators, two types of mixer topologies will be investigated. The first mixer, conceived by Barrie Gilbert in
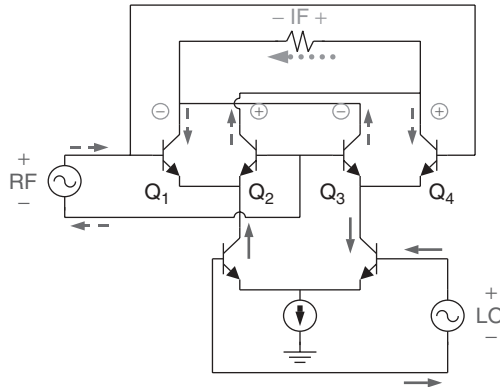
FIGURE 11.135 Ideal Gilbert cell mixer.

1968 [11.44], is the basis for most balanced active mixers used in wireless products today. Figure 11.135 shows a simplified version of a Gilbert cell mixer implementation showing the phase relationships between the LO, RF, and IF signals.

If we first consider the first differential pair formed by transistors Q_1 and Q_2, the RF signal is applied equally to both devices; hence RF currents are equal but opposite at the collector terminals (note the direction of the arrows). Similarly, the RF currents are equal and opposite at the collectors of Q_3 and Q_4, and since the two pairs are cross connected, the RF current in the output load is "balanced" to zero. In addition, the LO current is also zero in the output load due to circuit balance. Although the RF currents at the collectors of Q_1 and Q_4 have the same phase relationship, the IF signal generated is out of phase by $180°$ since the LO currents that modulate the differential pairs are out of phase by $180°$. The same condition occurs at the collectors of transistors Q_1 and Q_2. Hence, the IF signal is combined at the output load. It can be shown that the output IF current of a Gilbert cell mixer is [11.45]

$$I_{IF} \sim K(I_{EE}, V_T)[\tanh(V_{RF}) \tanh(V_{LO})]. \tag{11.97}$$

For small-signal levels the mixer is linear since

$$\tanh(x) = x \tag{11.98}$$

at the zero crossing point. In addition, emitter degeneration and other forms of negative feedback can improve linearity [11.46]. Although these mixers do not offer stellar performance when it comes to intercept point and noise figure performance, they do offer some advantages. This circuit is attractive because it can be monolithically integrated with other signal-processing circuitry, provides conversion gain, requires very low power to drive the LO port, and provides excellent balance (reduced even-order products) and isolation between signal ports.

The performance characteristics of a typical Gilbert cell mixer can be easily illustrated with the aid of a nonlinear circuit simulator such as ADS 2003C [11.47]. A typical silicon bipolar Gilbert cell mixer circuit, supplied with the circuit simulator less device parameters, is shown in Figure 11.136. The most basic parameter of interest is the mixer's conversion gain, which is shown in Figure 11.137. As can be seen
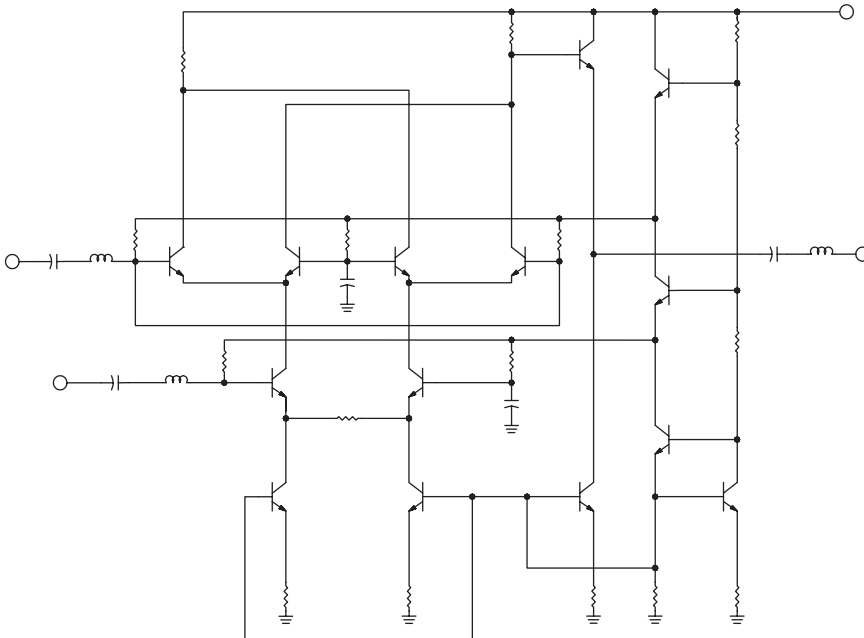
FIGURE 11.136   Typical Gilbert cell mixer using bipolar technology.
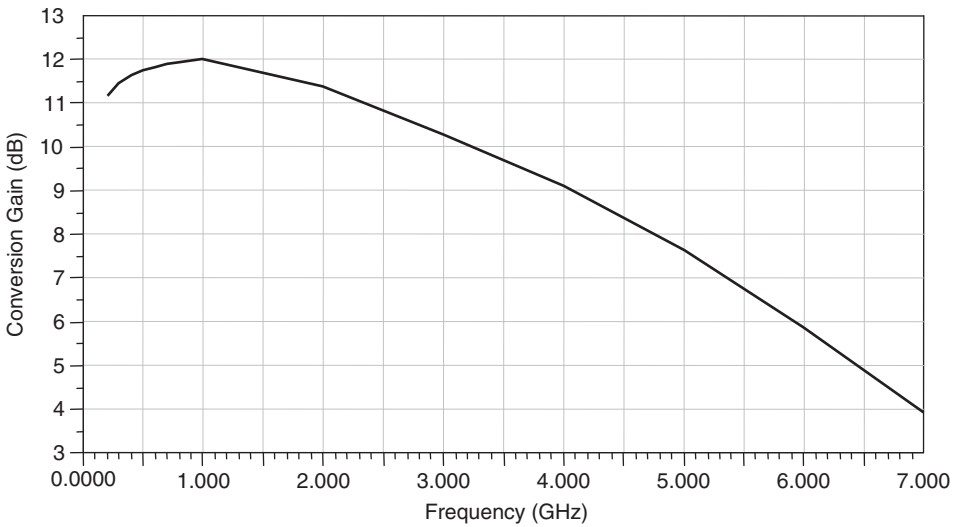
FIGURE 11.137   Gilbert cell mixer conversion gain as a function of frequency.

in the performance data, a key advantage to this type of mixer is conversion gain and balanced performance, a condition that is not the case for a passive diode mixer. Another interesting characteristic of active mixers is noise figure performance. Mixers synthesized with current sources in series with the active mixing element exhibit high noise figures. This situation varies with device technology and frequency, but typically

noise figure values range from 10 to 20 dB. The simulated noise figure performance for the above Gilbert cell mixer also falls within this range (Figure 11.138). If noise figure performance is of premiere importance, the lowest noise figure could be obtained with a drain-pumped GaAs FET mixer. A mixer of this type can be designed to exhibit gain but gets complicated to build in other than single-ended configurations. Although Gilbert cell mixers tend to be marginal in the area of linearity, they require very little LO power. Other mixer topologies are better suited for high-dynamic-range applications. Mixers constructed with passive switching elements (JFET, GaAs FET, diode, etc.) and either transmission line or ferrite baluns can exhibit outstanding dynamic range performance but usually require a lot of LO power. The simulated distortion characteristics for the above Gilbert cell mixer are shown in Figure 11.139. It should be noted that linearity characteristics are about equivalent to a single-balance diode mixer with 6 to 10 dBm of LO drive.

Passive mixer circuits are also much easier to design using modern CAD techniques. A single-balanced diode mixer realized using LTCC technology can be used to illustrate nonlinear and electromagnetic circuit analysis methods. We begin the design by developing a nonlinear mixer diode model based on a commercially available component. The first step is to fit the dc $I-V$ data with the diode circuit element available in the simulator. At this point, RF parasitic circuit elements can be ignored. The model
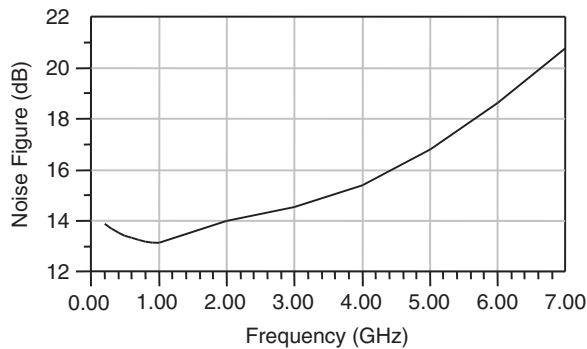
FIGURE 11.138   Simulated noise figure performance for Gilbert cell mixer.
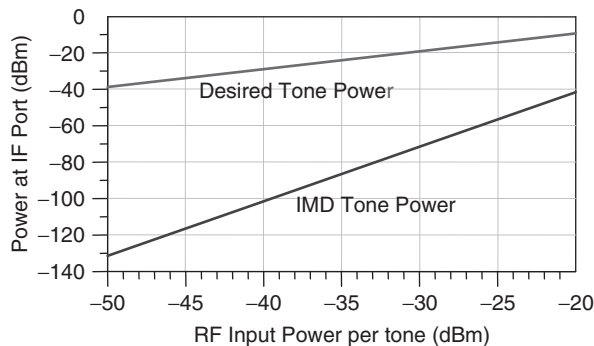
FIGURE 11.139   Simulated two-tone distortion performance for Gilbert cell mixer.
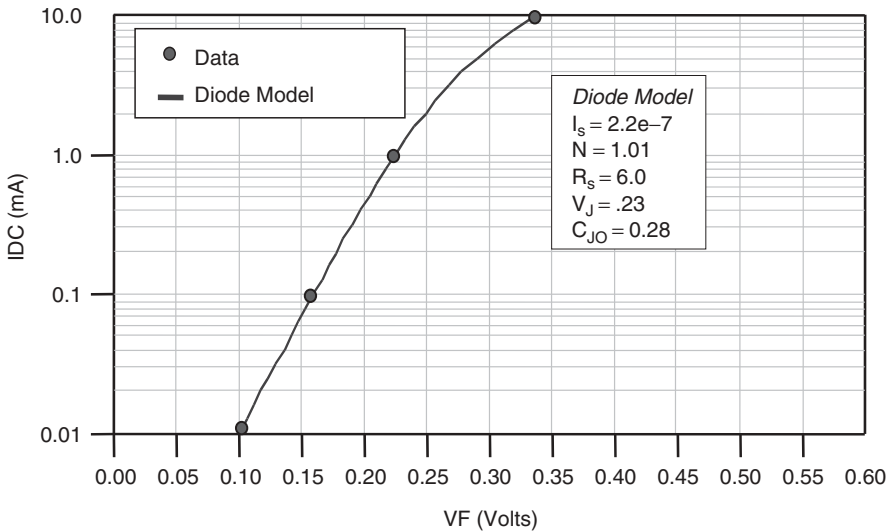
FIGURE 11.140   A dc $I-V$ diode model with measured dc data and model parameters.

parameters, data sheet parameters, and model performance are shown in Figure 11.140. As can be seen from the above illustration, the $I-V$ characteristics obtained from the data sheet are easily be captured by a simple diode model. The next step is to incorporate the RF package elements to the diode model. Since most manufactures supply diode S-parameter data as a function of bias current, package element values can be obtained by fitting the complete diode model at the appropriate bias current to the supplied RF data. For moderate levels of LO power (6 to 10 dBm), a diode bias current of 1 mA. is a reasonable representation of the time-averaged current developed in the mixer diode from the LO source power. By combining the package parasitic elements C_P and L_P with the dc $I-V$ model, the composite nonlinear RF diode model is obtained. It should be noted that the values of R_S and C_{J0} obtained from the dc $I-V$ model were allowed to vary slightly during final optimization so that the diode model would best represent the measured RF data. The model element values obtained are still physically consistent with the measured RF and dc data. The complete diode nonlinear model is shown in Figure 11.141.

We now must decide on the mixer topology that best suits the system requirements. Since it is desired to design a mixer to operate in the 5- to 6-GHz frequency band, a transmission line realization of the circuit will be required. In addition, most systems usually require very low LO leakage power; hence, obtaining good LO-to-RF isolation must be a consideration. A low-cost mixer could be designed using LTCC technology. This multilayer construction method allows for the easy realization of any type of balun. With these constraints in mind, a single balanced mixer using a broadband 180° hybrid, similar to the one shown in Figure 11.92(a), as the mixer balun will be employed. By injecting the LO signal in the Δ port of the hybrid, LO energy will be minimized at the RF port, hence reducing the LO leakage at the antenna input of the system.

We begin the design by determining the dimensions of the "flipped" coupled-line section of the hybrid using an electromagnetic solver such as Sonnet Software EM.
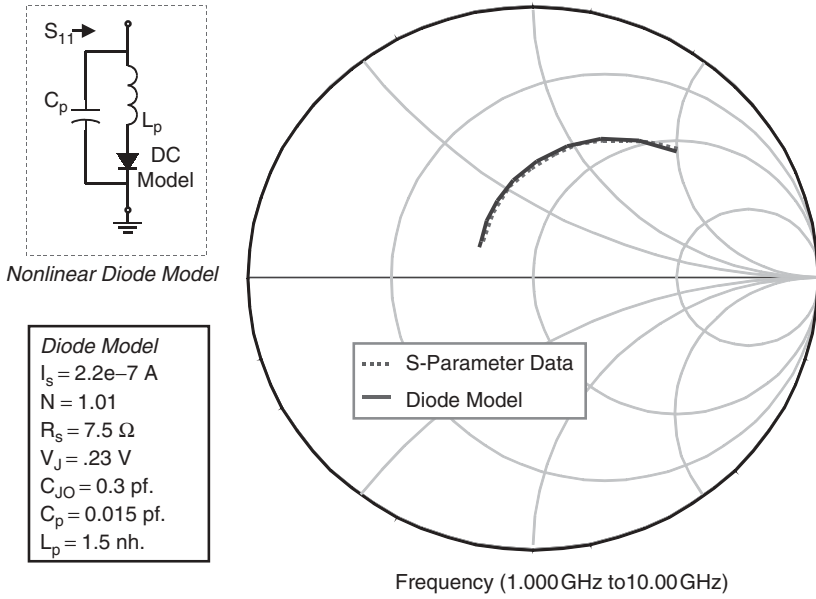
FIGURE 11.141 Nonlinear mixer diode model and model parameters with measured RF data.
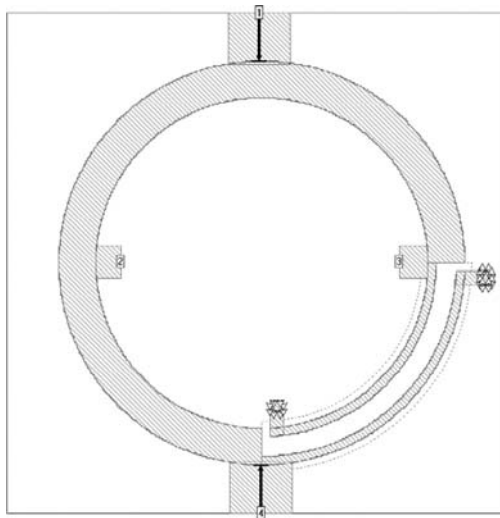
FIGURE 11.142 Broadband hybrid ring used in electromagnetic analysis.

Although the coupled-line section can be realized in a variety of ways, a reentrant mode coupler [11.48] is easily realized in the multilayer ceramic media. The quickest approach to the hybrid design is to model the simple elements using standard microstrip models combined with the coupler analysis. The final hybrid can then be analyzed using an electromagnetic solver. The layout for the hybrid is shown in Figure 11.142.
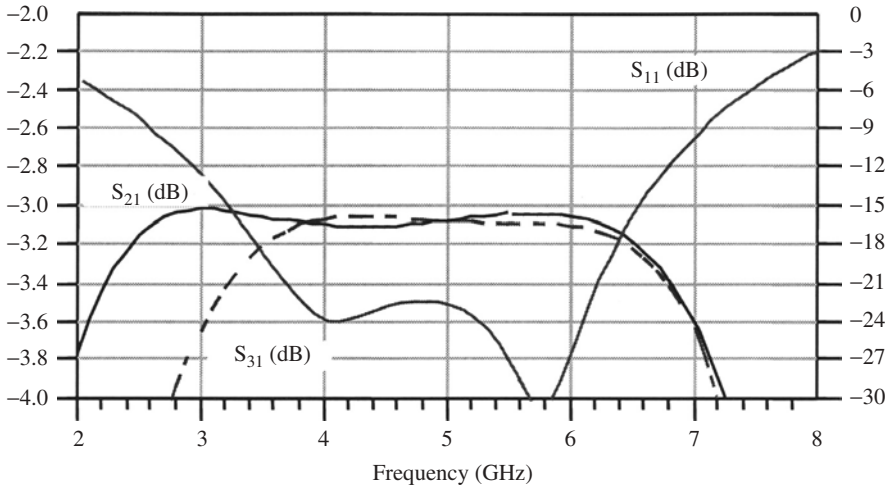
FIGURE 11.143   Frequency response of broadband hybrid.
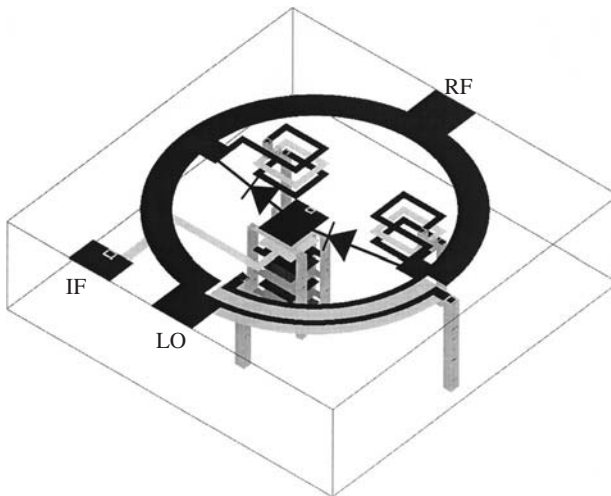
FIGURE 11.144   Single-balanced LTCC broadband diode mixer.

The computed frequency response for the hybrid is shown in Figure 11.143, which is a complete analysis for the total structure. The hybrid is then combined with the nonlinear diode model and IF filter/diplexer to form the mixer. The resulting circuit realization is depicted in Figure 11.144. This circuit layout shows the hybrid ring with IF return "chokes" realized with multiturn inductors and a multi-layer capacitor used as an IF filter and RF/LO return path for the diodes. The computed mixer conversion loss is shown in Figure 11.145. As in the previous example, noise figure, intermodulation distortion, and VSWR, as well as other parameters of interest, can also be easily simulated with the aid of a nonlinear circuit simulator.
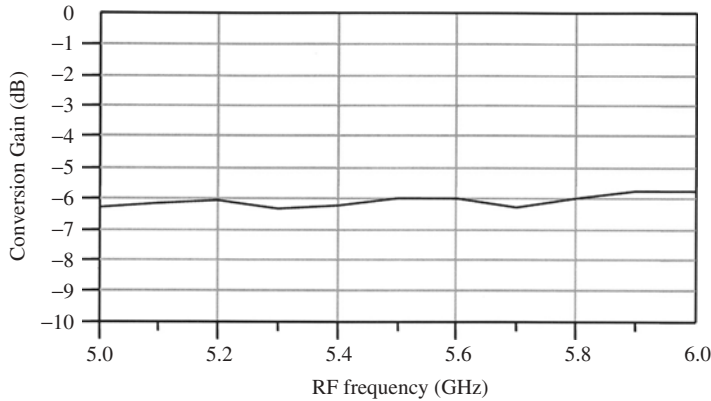
FIGURE 11.145   Computed single-balanced mixer conversion gain performance.

11.10   MIXER NOISE

Mixer noise analysis is mystifying and so far has been dealt with in the literature using either exhaustive analyses or specially developed simulation tools. Nonlinear CAD techniques for microwave mixer analysis and optimization are well established. Conversion matrix methods and full nonlinear approaches based on the harmonic balance concept have been in use for years. An important shortcoming of existing mathematical models for mixer noise analysis is that the noise model is not addressed systematically. In fact, even from a theoretical viewpoint, there is a considerable lack of information concerning the noise analysis problem for FET mixers.

Recent publication [11.49] has shown a new approach to mixer noise analysis and demystifies mixer noise analysis to a great extent. An active mixer comprises of the input transconductance, switches, and an output load, and noise is present in all the transistors making up theses functions. Simple analytical equations are derived to estimate the low-frequency noise (flicker) and high-frequency (white) noise at the output of a switching mixer. Total mixer noise is the contribution from the (11.99) low-frequency noise $(1/f)$ and (11.100) high-frequency (white) noise. The noise model described here is for the FET and holds for similar devices (MOSFET/GaAsFET). The goal of noise analysis is to find the total mixer output noise delivered to the IF.

Figure 11.146 shows the small-signal intrinsic model for the MOSFET. The mean-square values of the noise sources in the narrow frequency range Δf are given as

$$\overline{i_{dn}^2} = (4kT g_m \gamma)\ \Delta f \tag{11.99}$$

$$\overline{i_{gn}^2} = \left[4kT \frac{(wC_{gs})^2}{g_m} \delta\zeta \right]\ \Delta f \tag{11.100}$$

$$\overline{i_f^2} = KF \left(\frac{|I_d|^{\mathrm{AF}}}{f^{\mathrm{FCP}}} \right)\ \Delta f \tag{11.101}$$

$$\overline{i_{gn} i_{dn}^{\bullet}} = j \left(\sqrt{\overline{i_d^2 i_g^2}} \right) C \tag{11.102}$$

where AF = flicker noise exponent and FCP = flicker noise frequency shaping factor.

where g_m = drain output conductance

γ = bias-dependent factors (for long channel given as $1 \geq \gamma \geq \frac{2}{3}$)

ζ = bias-dependent factors (for long channel given as 0.2)

δ = bias-dependent factors (for long channel given as $\frac{4}{3}$)

C = $j0.395$ (for long channel)

Figure 11.146b shows the equivalent circuit representation of the noise model of the intrinsic MOSFET as shown in the Figure 11.146a.

The noise contributions from R_g (gate ohmic resistance), R_d (drain ohmic resistance), R_s (source ohmic resistance), and R_b (bulk ohmic resistance) are shown in the Figure 11.146b. The contribution of flicker ($1/f$) noise is incorporated by connecting the noise current source in parallel with the intrinsic drain port and is given by $\overline{i_f^2} = KF(|I_d|^{\mathrm{AF}}/f^{\mathrm{FCP}}) \, \Delta f$, and the modified value of i_{dn}^2 is given as $(4kTg_m\gamma) \, \Delta f + F(|I_d|^{\mathrm{AF}}/f^{\mathrm{FCP}}) \, \Delta f$.

Figure 11.146b shows the noise generators (i_{dn}, i_{Rgn}, i_{Rdn}, i_{Rsn}, and i_{Rbn}) and its mean-square value in the narrow frequency range. Let Δf be the bandwidth (normalized to 1 Hz). The noise generators introduced in the intrinsic device are shown below,
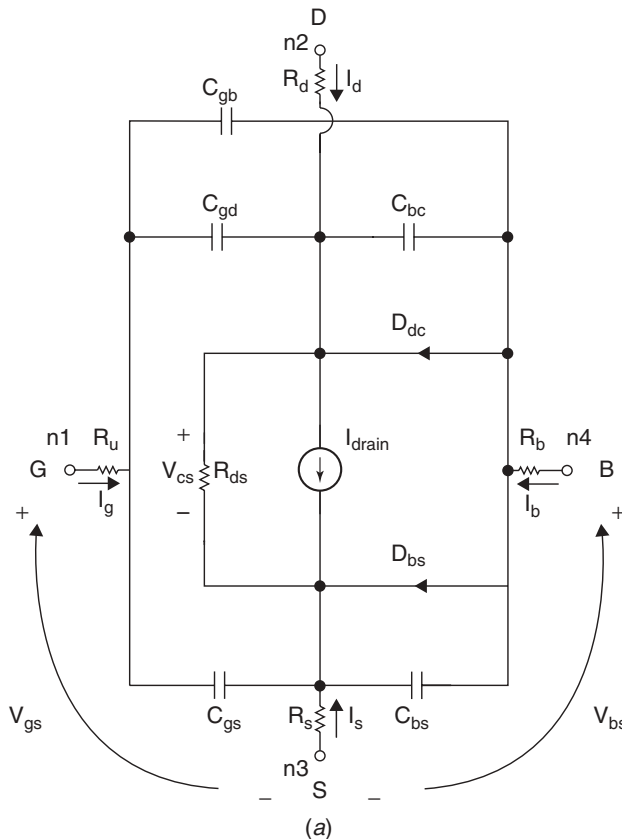
FIGURE 11.146 (*a*) Intrinsic model for N-MOSFET. (*b*) Noise model of intrinsic MOSFET transistor.
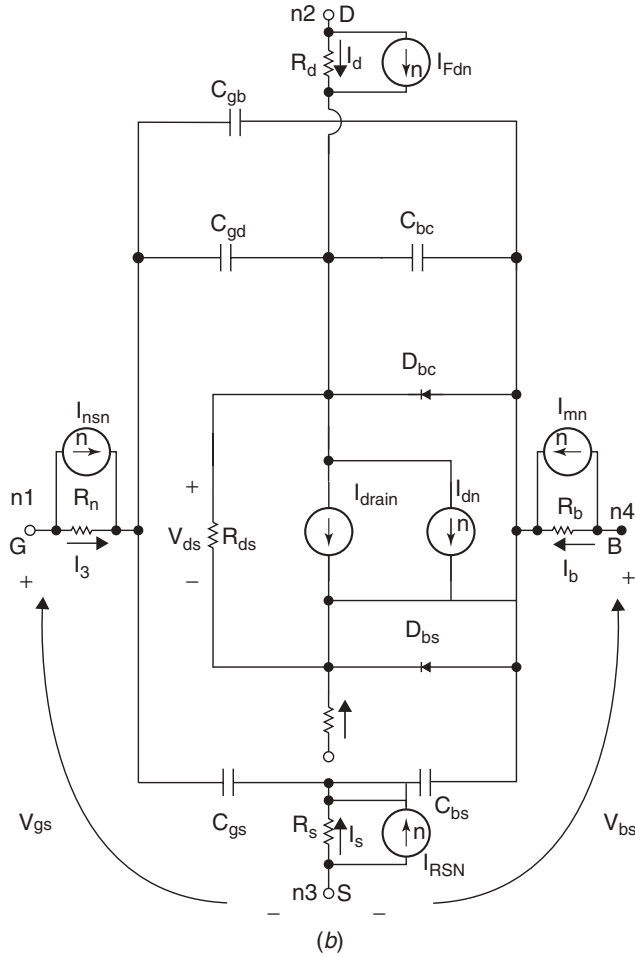
FIGURE 11.146   (*continued*)

and have mean-square values of

$$\langle i_{dn}^2 \rangle = \frac{8kT g_m}{3} \Delta f + KF \frac{I_D^{\mathrm{AF}}}{f^{\mathrm{FCP}}} \Delta f$$

$$\langle i_{Rgn}^2 \rangle = 4\frac{kT}{R_g} \Delta f$$

$$\langle i_{Rdn}^2 \rangle = 4\frac{kT}{R_d} \Delta f$$

$$\langle i_{Rsn}^2 \rangle = 4\frac{kT}{R_s} \Delta f$$

$$\langle i_{Rbn}^2 \rangle = 4\frac{kT}{R_b} \Delta f$$

Mixer Noise Analysis (MOSFET)

1. Low-frequency noise associated with the mixer is due to the following:

(a) Transconductance noise
(b) Load noise
(c) Switch noise (direct switch noise and indirect switch noise)

(a) *Transconductance noise*: Figure 11.147 shows the typical switching active mixer with the noise source at the transconductor input. As shown in Figure 11.147, noise in the lower transconductance FETs accompanies the RF input signal and is translated in frequency just like the signal. Therefore, flicker noise in theses FETs is up converted to ω_{LO} and to its odd harmonics while white noise at ω_{LO} (and to its odd harmonics) is translated to dc. If the output of interest lies at the low frequency or zero IF, then the transconductance FETs only contribute white noise after frequency translation, since the flicker corner frequency of theses devices is usually much lower than the LO frequency.

(b) *Load noise*: In a zero- or low-IF receiver, flicker noise in the loads of the down-conversion mixer competes with the signal. PMOSFETs show lower flicker noise as compared to NMOSFET's of the same dimensions; therefore PMOS loads are preferred over NMOS ones.

The noise due to load resistance R_L is given by

$$[\hat{V}_{0n}^2]_{\text{noise load}} = 4kTR_L + 4kTR_L = 8kTR_L \qquad (11.103)$$

(c) *Switch noise*: Mixer noise due to the switching mechanism is characterized as direct switch noise and indirect switch noise.

Direct switch noise: Figure 11.148 shows the single-balanced mixer with switch noise modeled at the gate. As shown in Figure 11.148, the bias current in the switch FETs M1 and M2 is periodic at a frequency ω_{LO}. Flicker noise arises from traps with much longer time constants than the typical period of oscillation at RF, and it may be assumed that the time-averaged inversion layer charge in the channel determines the root-mean-square (rms) flicker fluctuations. These charge fluctuations are referred as a
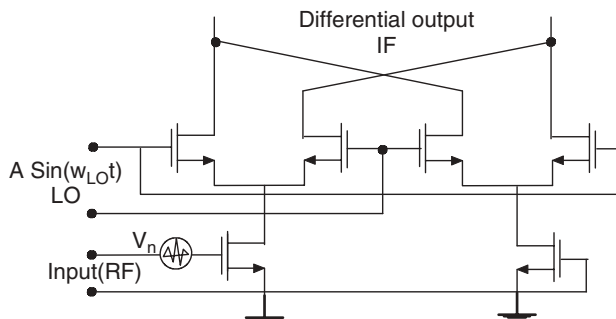
FIGURE 11.147 Typical switching active mixer with noise source shown at the transconductor input.
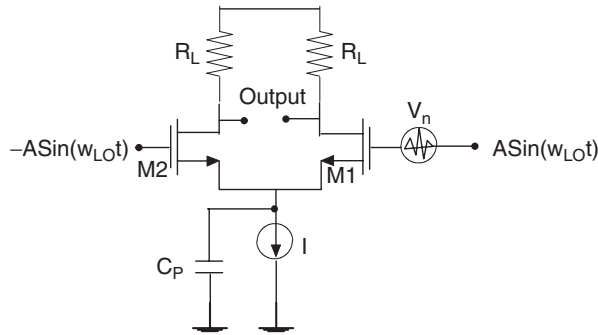
FIGURE 11.148   Single-balanced mixer with switch noise modeled at gate.

voltage to the gate of one of the MOSFETs in the differential pair with a constant rms value and a noise spectral density proportional to $1/f$, as shown in Figure 11.148, and this equivalent noise voltage (V_n) is a slow-varying offset voltage associated with the differential pair. The input-referred flicker noise (based on the carrier density fluctuation model) of MOSFETs is independent of V_{GS}, and this phenomenon is experimentally verified [11.50, 11.51].

For ease in analysis, it is assumed that the circuit switches sharply and a small differential voltage excursion causes the current to completely switch from one side of the differential pair to the other side. The switch noise is characterized as direct and indirect switch noise. Considering the direct effect of the switch noise at the mixer output, the transconductance RF input stage is replaced by a current source I at the tail, as shown in Figure 11.148. In the absence of noise, for positive values of LO voltage M1 switches on and M2 switches off, and a current equal to I appears at the right branch and again in the next half period the current switches to the left branch, thereby generating output as a square wave at frequency ω_{LO} with zero dc value. In the presence of the noise, the slowly-varying noise voltage V_n modulates the time at which the pair M1, M2 switches and at every switching instant the skew in switching instant modulates the differential current waveform at the mixer output. The height of the square-wave signal at the output remains constant; however, noise advances or retards the time of zero crossing by $\Delta t = V_n(t)/S$, where S is the slope of the LO voltage at the switching time. The waveform at the mixer output consists of a square wave of frequency ω_{LO} and amplitude I, representing the LO feed-through, superposed with a pulse train of random widths Δt and amplitude of $2I$ at a frequency of $2\omega_{LO}$, representing noise.

The average output current over one period is given by

$$i_{0,n}(t) = \frac{2}{T}2I \ \Delta t = \frac{2}{T}2I\frac{V_n}{S} = 4I\left(\frac{V_n}{ST}\right) \tag{11.104}$$

and the frequency spectrum of the baseband noise current at the output is given by

$$i_{0,n}(f) = 4I\left[\frac{V_{n(f)}}{ST}\right] = \left(\frac{1}{\pi}\right)\left(\frac{I}{A}\right)V_n(f) \tag{11.105}$$

where T is the period of LO and S is the slope of the LO voltage at the switching time. Sampled images of this spectrum appear at integer multiples of $2\omega_{LO}$. The low-frequency noise V_n at the gate switch appears at the output without frequency translation and corrupts a signal down converted to zero IF. The zero-crossing modulation Δt depends on the low-frequency noise V_n and the LO voltage slope (S) at zero crossing normalized to LO frequency ST. For a sine wave LO, $ST = 4\pi A$, where A is the amplitude and a factor of 2 accounts for the fact that V_n is compared to a differential LO signal with an amplitude of $2A$. If the mixer is used for up conversion, the switches contribute no flicker noise to the output at ω_{LO}, although flicker noise in the transconductance stage is up converted to this frequency.

The signal-to-noise ratio of the mixer is given by

$$\text{SNR} = \left(\frac{S \times T}{2\pi (V_{GS} - V_t)} \right) \left(\frac{V_{\text{in}}}{V_n} \right) = \left(\frac{2A}{V_{GS} - V_t} \right) \left(\frac{V_{\text{in}}}{V_n} \right) \tag{11.106}$$

where $V_{GS} - V_T$ is the transistor gate overdrive voltage is the period of the LO and S is the slope of the LO voltage at the switching time.

From the above expression the SNR improves by raising the product of the slope of the LO waveform at the zero crossing and its period, by increasing the gate area of the switch FETs to lower flicker noise V_n, and by lowering the transconductance FET overdrive. However, increasing the switch gate area or lowering the transistor gate overdrive voltage will degrade the mixer bandwidth.

The above expression also holds good for a double-balanced mixer, the main difference being that there is no LO feedthrough, and V_n represents the equivalent noise of four switches in the mixer, as shown in Figure 11.147.

Indirect switch noise: The analysis so far suggests that flicker noise at the mixer output may be eliminated if the slope at the zero crossing is increased infinitely; however, as the LO slope rises, output flicker noise appears via another mechanism that depends on LO frequency and circuit capacitance, called the "indirect" mechanism.

The output noise current is given by [11.49]

$$i_{0,n} = \frac{2}{T} \int_0^{T/2} i_{Cp}(t)dt = \left(\frac{2}{T} C_p \right) V_n \tag{11.107}$$

where i_{Cp}, the capacitive current, has frequency equal to the LO frequency, with zero dc value.

The conversion gain (CG) to flicker noise in V_n due to the indirect process is given as

$$[\text{CG}]_{\text{indirect}} = \frac{2}{T} C_p \tag{11.108}$$

Conversion gain due to the indirect mechanism $[\text{CG}]_{\text{indirect}}$ grows with LO frequency but is usually smaller than the gain $[\text{CG}]_{\text{direct}}$ due to the direct mechanism.

In most practical cases, flicker noise due to a sine wave LO is attributable to the direct mechanism, which is frequency independent. However, even a LO waveform

with infinitely fast rise time and fall time does not eliminate flicker noise but pushes it down to a level determined by the tail capacitance. In general, LO waveforms with a large *ST* product, which is a low-frequency LO with sharp transitions, will have lower flicker noise.

2. High-frequency noise associated with the mixer is due to the following:

(a) White noise in mixer switches
(b) Transconductor noise

(a) *White noise in mixer switches*: The high-frequency mixer output noise is white and cyclostationary and can be expressed as the product of a periodic and deterministic sampling function and white and stationary switch input-referred noise [11.52].

The mixer output noise and sampling function are given by [11.49]

$$i_{0,n} = p(\omega_{LO}t)V_n(t) \tag{11.109}$$

$$p(\omega_{LO}t) = \sum_n G_m\left(t - \frac{nT}{2}\right) \tag{11.110}$$

where $p(\omega_{LO}t)$ is a periodic and deterministic sampling function, $V_n(t)$ is the white and stationary input-referred noise, and G_m is periodic at twice the LO frequency (since there are two zero crossings over every cycle of the LO).

The switch noise V_n is transferred to the output only at the zero crossing. Switches contribute noise to the mixer output when they are both on, and if one switch is off, it obviously contributes no noise, and neither does the other switch that is on because it acts as a cascade transistor whose tail current is fixed to I by the RF input transconductance stage. Starting with the direct mechanism, the noise current at the mixer output consists of a train of pulses with a rate of twice the LO frequency, a height equal to $2I/S$, and a width which is randomly modulated by noise.

The autocorrelation of the output noise is given by

$$R_{i0,n}(t + \tau, t) = p(t)p(t + \tau)R_{vn}(\tau) \tag{11.111}$$

The autocorrelation of the white noise $R_{vn}(\tau)$ is a delta function and the autocorrelation of the output noise is a function of both t and τ, which indicates that the output noise is not stationary but periodic, white, and cyclostationary. The input noise is white and stationary and its power spectral density is given by

$$[\hat{V}_n^2]_{\text{noise transconductance}} = \frac{4kT\gamma}{g_m} \tag{11.112}$$

$$[g_m]_{\text{zero crossing}} = \frac{2I}{\Delta V} \tag{11.113}$$

where the value of γ, is the channel noise factor, is normally $\frac{2}{3}$ for long MOSFET channels and g_m is the switch transconductance at the zero crossing.

The power spectral density of the output noise current is given by

$$[\hat{i}_{0n}^2]_{\text{output noise}} = \int_0^T p^2(t)\,dt[\hat{V}_n^2] = \left(\frac{2}{T}\right)\left(\frac{2I}{S}\right)^2\left(\frac{1}{T_s}\right)[\hat{V}_n^2] \quad (11.114)$$

$$[\hat{i}_{0n}^2]_{\text{output noise}} = 4kT\gamma\left(\frac{4I}{ST}\right) \quad\quad\quad\quad (11.115)$$

$$[\hat{i}_{0n}^2]_{\text{output noise}} = 4kT\gamma\left(\frac{4I}{\pi A}\right) \quad\quad\quad\quad (11.116)$$

where S is the slope of the LO waveform and, for sine wave, $S = 2A\omega_{\text{LO}}$.

From above it shows that the output noise power spectral density depends on LO magnitude (A) and bias current (I) and not on transistor size!

(b) *Transconductor noise*: White noise originated in the transconductor is indistinguishable from the RF input signal; therefore mixer commutation is assumed as square-wave-like and the LO frequency and its odd harmonics down convert the respective components of the white noise to the IF and is given by

$$[\hat{V}_{0n}^2]_{\text{noise transconductance}} = n\left(\frac{4kT\gamma}{g_m}\right)\left(\frac{2g_m R_L}{\pi}\right)^2 \quad (11.117)$$

Any periodic LO waveform, sine wave or otherwise, which switches the mixer results in square-wave commutation of the transconductance stage output current and the factor n is given as

$$n = 2\left[1 + \frac{1}{3^2} + \frac{1}{5^2} + \cdots\right] = \frac{\pi^2}{4} \quad\quad (11.118)$$

Total Mixer Output Noise (MOSFET)   The total mixer noise is the contribution from (1) the low-frequency noise ($1/f$) and (2) the high-frequency (white) noise and can be given by

$$[\hat{V}_{0n}^2]_{\text{total mixer noise}} = [\hat{V}_{0n}^2]_{\text{low frequency}(1/f)} + [\hat{V}_{0n}^2]_{\text{high frequency (white)}} \quad (11.119)$$

$$[\hat{V}_{0n}^2]_{\text{total mixer noise}} = 8kTR_L + 8kT\gamma\left(\frac{R_L^2 I}{\pi A}\right) + n\left(\frac{4kT\gamma}{g_m}\right)\left(\frac{2g_m R_L}{\pi}\right) \quad (11.120)$$

where $k = 1.38 \times 10^{-23}$ J/K
$\quad R_L$ = load resistor
$\quad g_m$ = transconductance
$\quad \gamma$ = channel noise factor
$\quad I$ = dc bias current
$\quad A$ = amplitude of LO signal
$\quad n = \pi^2/4$

The simplified expression of total mixer noise is given by

$$[\hat{V}_{0n}^2]_{\text{total mixer noise}} = 8kTR_L\left(1 + \gamma\frac{R_L I}{\pi A} + \frac{\gamma\ g_m R_L}{2}\right) \quad (11.121)$$

where the first term is due to the two-load resistor R_L, the second term is the output noise due to the two switches, and the third term is the noise of the transconductance stage transferred to the mixer output.

In the double-balanced mixer there are twice as many FETs in the transconductance stage and the switches, so the output noise is given as

$$[\hat{V}_{0n}^2]_{\text{total mixer noise}} = 8kTR_L \left(1 + \gamma \frac{2R_L I}{\pi A} + \gamma\ g_m R_L \right) \tag{11.122}$$

where I is the bias current in each side of the mixer.

From the above expressions, mixer noise varies with different circuit parameters, such as LO amplitude (A), mixer dc bias current (I), load resistance (R_L), and transconductance g_m and allows the designer to design and optimize the mixer noise as per the desired specifications.

Comparing a scaled double-balanced mixer with the same total current as a single-balanced mixer (i.e., the former is biased at half the current per branch but the same $V_{GS} - V_t$ as the later), the output noise for double-balanced and single-balanced mixers is the same. However, since the gain of the double-balanced mixer from the differential input is half, the input referred noise voltage is twice as large. Referred to a differential 100-Ω source, its noise figure is 3 dB larger than that of a single-balanced mixer referred to a single-ended 50 Ω source resistance. The main advantage of the double-balanced mixer is that it suppresses LO feed-through as well as noise or interferes and superimposed on the LO waveform applied to the mixer but it cannot suppress the uncorrelated noise in the switches. The noise treatment of double balanced mixer is found in [11.53].

Mixer Noise Optimization   The expression for total mixer output noise is expressed in terms of bias quantities by replacing transconductance g_m for a short-channel **MOSFET** by $I/(V_{GS} - V_t)$ as

$$[\hat{V}_{0n}^2]_{\text{mixer noise}} = 8kTR_L \left(1 + \gamma \frac{R_L I}{\pi A} + \gamma \frac{R_L I}{2(V_{GS} - V_t)} \right) \tag{11.123}$$

Equation (11.123) shows that the relative noise contribution of the switches to the transconductance FET is $2(V_{GS} - V_t)/\pi A$. As the gate overdrive bias on the transconductance FET approaches the sine wave LO amplitude, the switches and transconductance stage contribute comparable noise at the mixer output. This is the fundamental trade-off between noise and linearity in active mixers.

Linear mixers may bias the transconductance FET at a large overdrive to enhance the linearity, accompanied by modest LO swings to keep the switch transistors operating at saturation. These conditions boost the relative noise contribution of the switches, and as the dc voltage drop across the load resistor approaches the gate overdrive of the transconductance FET, the noise contribution of the load becomes more important. Simple estimates of mixer noise sometimes neglect the contribution of the switches and load resistors, which underestimates noise figure by 2 to 4 dB.

GaAs FET Noise Model   The small-signal noise model of the GaAs FET is given in Figures 11.149a and 11.149b.
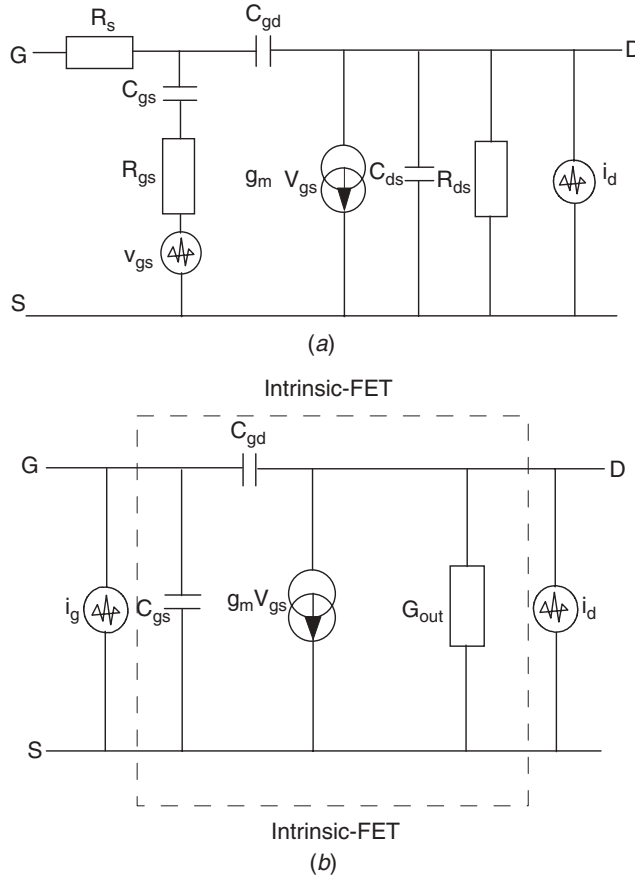
FIGURE 11.149 Small-signal noise model of GaAs FET with (*a*) voltage noise source at input and current noise source at output and (*b*) current noise sources at input and output.

The mean-square value of the noise sources and their correlation coefficient in the narrow frequency range Δf are given by

$$\overline{i_d^2} = 4kTg_m P \; \Delta f \tag{11.124}$$

$$\overline{i_g^2} = \frac{4kT(wC_{gs})^2 R}{g_m}\Delta f \tag{11.125}$$

$$\overline{i_g i_d^\bullet} = jwC_{gs} 4kTC\sqrt{PR} \; \Delta f \tag{11.126}$$

where the noise sources i_d is due to channel current and i_g is due to induced gate current.

The noise spectral densities are given by

$$S(i_d) = \frac{\overline{i_d^2}}{\Delta f} = \left\langle |\overline{i_d^2}| \right\rangle = 4kTg_m P \tag{11.127}$$

$$S(i_g) = \frac{\overline{i_g^2}}{\Delta f} = \left\langle |\overline{i_g^2}| \right\rangle = \frac{4kT(wC_{gs})^2 R}{g_m} \tag{11.128}$$

$$S(i_g i_d^{\bullet}) = \left\langle |\overline{i_g i_d^{\bullet}}| \right\rangle = -jwC_{gs} 4kTC\sqrt{PR} \tag{11.129}$$

where k is Boltzmann's constant and T is temperature in degrees kelvin.

The spot correlation matrices of the gate and drain noise current sources are given as

$$[C_Y(w)] = [N]_{\text{noise-matrix}} = \begin{bmatrix} \overline{i_g i_g^{\bullet}} & \overline{i_g i_d^{\bullet}} \\ \overline{i_d i_g^{\bullet}} & \overline{i_d i_d^{\bullet}} \end{bmatrix} \tag{11.130}$$

$$[C_Y(w)]_{\text{GaAs FET}} = 4kT \begin{bmatrix} \dfrac{w^2 c_{gs}^2 R}{g_m} & -jwc_{gs} C\sqrt{PR} \\ jwc_{gs} C\sqrt{PR} & g_m P \end{bmatrix} \tag{11.131}$$

where P, the drain noise parameter, is a function of the device structure/channel and bias condition given by

$$P = \left(\frac{1}{4kTg_m}\right)\overline{i_d^2} = 1.2 \text{ Hz}^{-1} \text{ for GaAs FETs} \tag{11.132}$$

R, the gate noise parameter, is a function of the device structure/channel and bias condition given by

$$R = \left(\frac{g_m}{4kTw^2 C_{gs}^2}\right)\overline{i_g^2} = 0.4 \text{ Hz}^{-1} \text{ for GaAsFETs} \tag{11.133}$$

and C is a correlation coefficient given as

$$C = -j\left(\frac{\overline{i_g i_d^{\bullet}}}{\sqrt{[\overline{i_d^2 i_g^2}]}}\right) = 0.6\text{–}0.9 \text{ for GaAsFETs} \tag{11.134}$$

The contribution of the flicker $(1/f)$ noise can be incorporated by means of a noise current source connected in parallel with the intrinsic drain port and given by

$$\overline{i_f^2} = Q\left(\frac{|I_d|^{\text{AF}}}{f^{\text{FCP}}}\right)\Delta f \tag{11.135}$$

where I_d is the instantaneous value of the channel current, and Q, AF, and FCP are empirical parameters. In most practical cases, AF and FCP are directly obtained from measurements (typically for GaAsFET, AF = 2, FCP = 1), while Q (power law parameter) is not.

The expression of Q is given by

$$Q\left(\frac{|I_d|^{AF}}{f^{FCP}}\right) = g_m P \tag{11.136}$$

Total Mixer (GaAs FET) Output Noise   The total mixer noise is the contribution from (1) the low-frequency noise (1/f) and (2) the high-frequency (white) noise and can be given by

$$[\hat{V}_{0n}^2]_{\text{total mixer noise}} = [\hat{V}_{0n}^2]_{\text{low frequency}(1/f)} + [\hat{V}_{0n}^2]_{\text{high frequency (white)}} \tag{11.137}$$

$$[\hat{V}_{0n}^2]_{\text{total mixer noise}} = 8kTR_L\left(1 + P\frac{R_L I}{\pi A} + P\frac{g_m R_L}{2}\right) \tag{11.138}$$

where the first term is due to the two-load resistor R_L, the second term is the output noise due to the two switches, and the third term is the noise of the transconductance stage transferred to the mixer output.

In the double-balanced mixer there are twice as many GaAs FETs in the transconductance stage and the switches, so the output noise is given as

$$[\hat{V}_{0n}^2]_{\text{total mixer noise}} = 8kTR_L\left(1 + P\frac{2R_L I}{\pi A} + P\ g_m R_L\right) \tag{11.139}$$

where $K = 1.3 \times 10^{-23}$ J/K

R_L = load resistor

g_m = transconductance

P = channel noise factor

I = dc bias current

A = amplitude of LO signal

In the double-balanced mixer there are twice as many FETs in the transconductance stage and the switches, so the output noise is given as

$$[\hat{V}_{0n}^2]_{\text{mixer noise}} = 8kTR_L\left(1 + P\frac{2R_L I}{\pi A} + P\ g_m R_L\right) \tag{11.140}$$

where I is the bias current in each side of the mixer.

Self-Oscillating Mixer   The self-oscillating mixer was already introduced in the oscillator Chapter 10. Here we look at the frequency response and noise figure as a function of the circuit. The circuit was modified to a different, higher frequency range. Figure 11.150 shows the circuit diagram of this additive mixer. Additive means that both signals are applied to the same input. The frequency range and resonant frequency are determined by the inductance and transmission line. Figure 11.151 shows the frequency response indicating a gain of 5 dB at the operating frequency of 11.03 GHz. The frequency response also shows a notch at 10.005 GHz. The load line of the mixer now is different than the load line for the oscillator and is shown in Figure 11.152. It can be
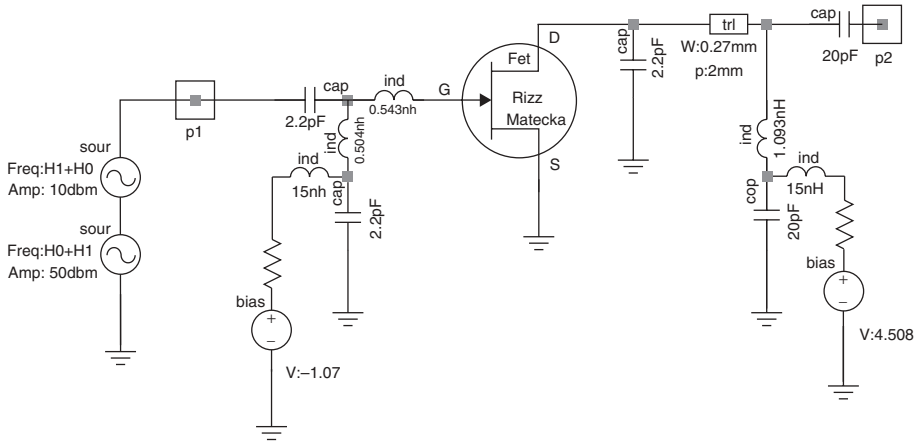
FIGURE 11.150   Schematic of the self-oscillating mixer operating at approximately 12 GHz.
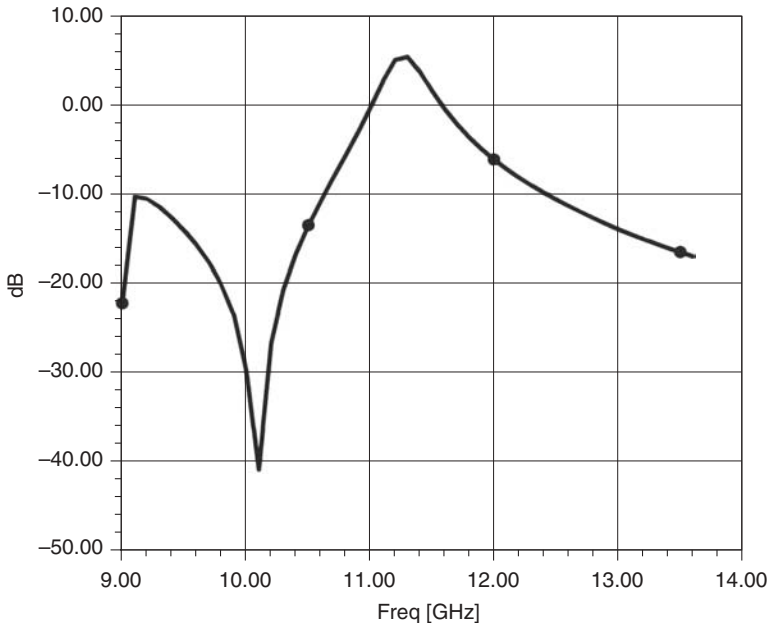
FIGURE 11.151   Frequency response (S_{21}) of self-oscillating mixer.

seen that the load line is incorrect in its impedance. The self-oscillating frequency with a level of 10 dBm is generated by the circuit itself but is represented by an external source. Question to the reader: What is the actual impedance and what should it be? Finally, Figure 11.153 shows the simulated noise figure of the self-oscillating mixer. It is quite an achievement for the harmonic balance simulator, the model Designer from Ansoft, to be able to calculate both the phase noise and the noise figure of this circuit. In the range from approximately 11 to 11.8 GHz, the noise figure is approximately 9 dB. This is an excellent number for an active mixer, a mixer that has gain.
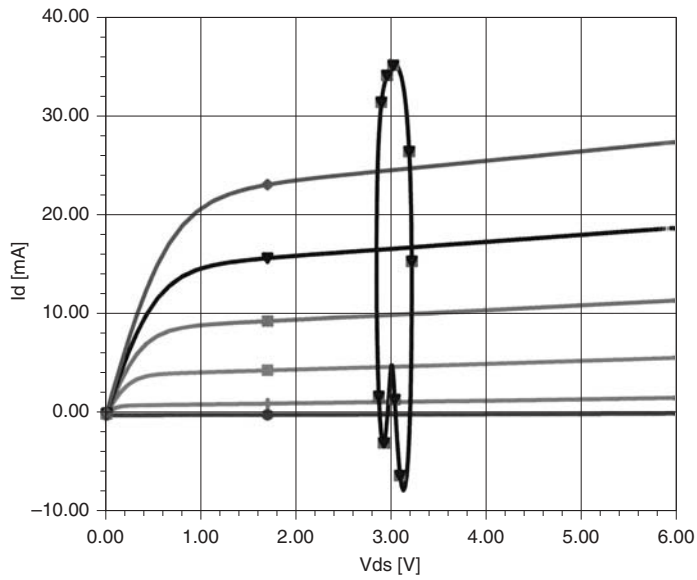
FIGURE 11.152   Output load line in mixer mode of self-oscillating mixer.
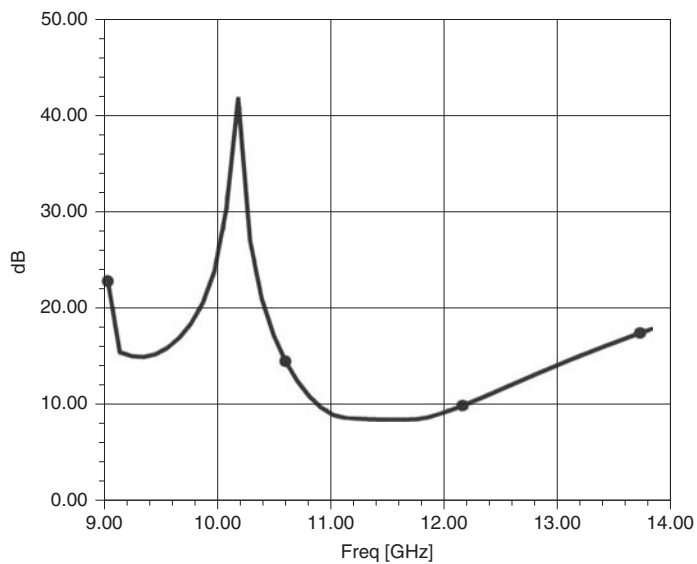
FIGURE 11.153   Simulated noise figure of self-oscillating mixer.

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PROBLEMS

11.1 Using the HP 5082-2800 Schottky barrier diode, design a single-ended mixer with the following specifications

$$F_{LO} = 2.2 \text{ GHz} \qquad V_{LO} = 5.0 \text{ V (peak)} \qquad R_{GEN} = 50 \text{ }\Omega$$

$$F_{RF} = 2.0 \text{ GHz} \qquad V_{RF} = 0.1 \text{ V (peak)} \qquad R_{GEN} = 50 \text{ }\Omega$$

$$F_{IF} = 200 \text{ MHz} \qquad R_{LOAD} = 50 \text{ }\Omega$$

The goal is 6 to 8 dB conversion loss. Investigate the effect of $R_S = 5\text{--}25 \text{ }\Omega$.

Diode Parameters	Package Parameters
$I_S = 2.2 \text{ e}^{-9}$	$L_p = 2$ nH
$R_S = 25$	$C_p = 0.2$ pF
$N = 1.08$	
$BV = 75$	
$I_{BV} = 10 \text{ e}^{-6}$	
$C_{J0} = 1.6 \text{ e}^{-12}$ (Note $\dfrac{1}{\omega C_{J0}} \cong 50 \ \Omega$)	
$V_J = 0.6$	
$E_G = 0.69$	
$XTI = 2$	
$M = 0.5$	

The suggested circuit is a high-pass input filter and a low-pass output filter:
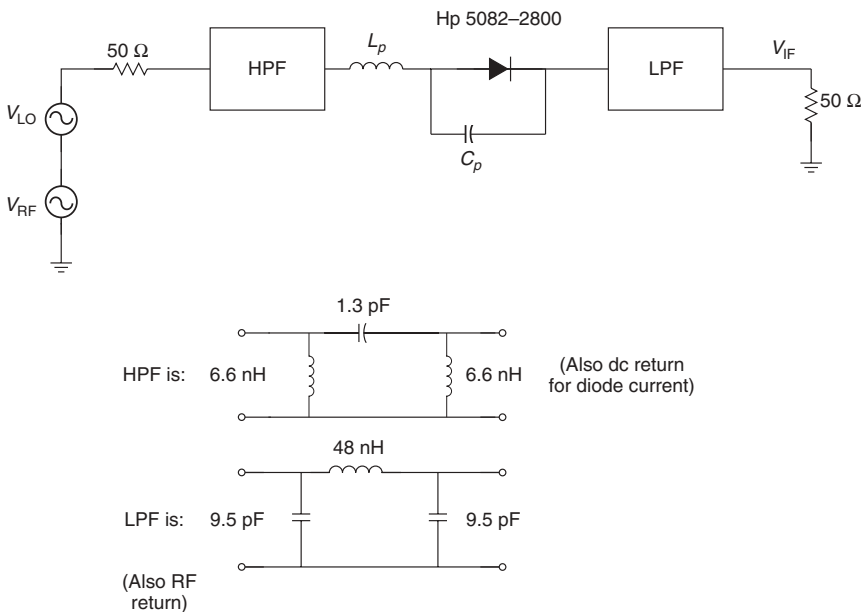
Calculate $P_1 \text{dBc}$ at the load for F_{IF}.

11.2 Repeat problem 11.1 for a singly balanced mixer with two diodes. Increase V_{LO} by 3 dB ($V_{LO} = 7.07$ V). Calculate $P_1 \text{dBc}$ at the load.

11.3 Using ideal baluns, repeat problem 11.1 for a doubly balanced mixer with four diodes. Increase V_{LO} by 6 dB ($V_{LO} = 10$ V). Calculate $P_1 \text{dBc}$ at the load.

11.4 Examine the time-domain waveforms through the diode, that is, diode current and diode voltage, for the above problems near $P_1 \text{dBc}$.

CHAPTER 12

RF SWITCHES AND ATTENUATORS

One of the most basic elements of any modern RF system is the RF switch. Traditionally switching functions were performed by mechanical means, but with the advent of microwave semiconductors, most RF switching can be performed using solid-state devices. The power-handling capability of solid-state devices is also impressive, since it is not uncommon to find *pin* diode transmit/receive (T/R) switches operating well into the multikilowatt range, with some power limiters operating in peak power environments above a megawatt [12.1]. Most low-power switching functions have been performed by *pin* diodes; however, since the world is now blessed with "cheap" GaAs, FET switches are becoming very popular, particularly in hand-held and portable devices, where power consumption is an important consideration.

12.1 *pin* DIODES

The pin diode was previously covered in Ch. 3 (pp. 65–78). For many years, the *pin* diode was king of the solid-sate microwave and RF switch realm, due to its superior diode switching characteristics, such a low "off" capacitance and very low "on" resistance. However, *pin* diodes have one major flaw, as with any diode they are only two-terminal devices. As with any two-terminal device, dc bias must be separated from the RF path with external decoupling elements. In contrast, when GaAs FET switches are used, the gate, which is very high impedance and draws no current, effectively isolates the switching voltage from the RF path. One should not be misled by this benefit, since the *pin* diode offers superior intermodulation characteristics and power-handling ability when compared to GaAs FETs [12.2].

Traditionally *pin* diodes have been fabricated using silicon (Si) technology, but at millimeter-wave frequency GaAs *pin* diodes are also popular due to their excellent

high-frequency performance [12.3]. Regardless of the technology employed, *pin* diodes function as variable resistors at RF frequencies. The typical *pin* diode consists of an intrinsic high-resistivity layer (*i*), ideally with no doping, sandwiched between positively doped (*p*) and negatively doped (*n*) layers. In reality, the *i* layer is very lightly doped and becomes conductive during forward-bias conditions. In addition, the *i* layer's length separates the highly doped *p* and *n* layers, thus reducing the diode's capacitance when reversed biased (off state).

If we depict the typical *pin* structure and doping profile of that shown in Figure 12.1, the characteristics of the diode when biased can be understood. At zero bias, diffusion of both holes and electrons cause space charge regions to form in the *p* and *n* layers, where these layers interface with the *i* layer. The thickness of these space charge regions is inversely proportional to the impurity concentration or doping level. This results in fixed negative charge in the *p* layer and bound positive charge in the *n* layer, with the *i* layer depleted of charge carries. As reverse bias is applied, the space charge regions become thicker, with the electric field appearing across the *i* region, thus assuring that all charge carries are swept out of the *i* layer. Regardless of the value of reverse bias applied, the distance between the conducting *p* and *n* layers is set by the *i*-layer thickness; hence, the reverse-bias diode capacitance is essentially constant and linear, unlike other types of diodes. In addition, for a given diode area, this capacitance is also much smaller than other types of diodes. This capacitance C_j is shunted by the *i*-layer resistivity R_j, which at RF frequencies is many orders of magnitude greater than the reactance of the junction capacitance. The small-signal equivalent circuit of the reverse-bias *pin* diode is essentially C_j in series with a small-value resistor R_s, which is approximately equal to the series resistance under forward-bias conditions. When the diode is reversed biased and the applied RF voltage swing is small, the diode is essentially a high-Q capacitor. If the RF voltage swing is sufficiently large, carriers will be injected into the *i* region, causing the diode to conduct current during part of the RF cycle, thus appearing resistive to large signals. This is illustrated in Figure 12.2.

When the diode is forward biased, carrier injection into the *i* region becomes significant, and the diode resistance drops. If the carrier lifetime τ is long enough
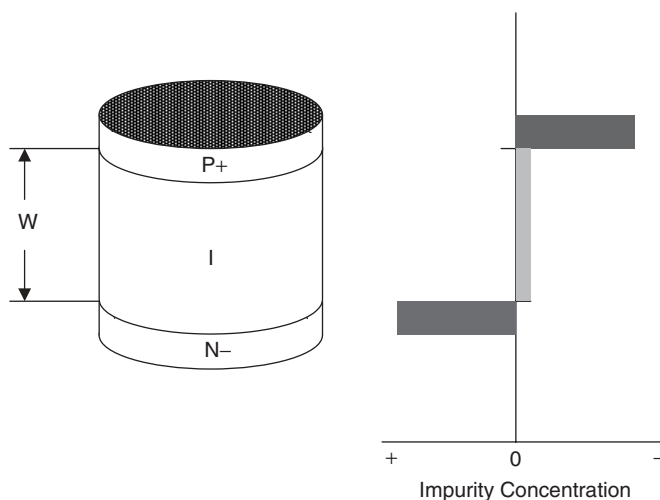
FIGURE 12.1   A *pin* diode mesa with relative doping profile.
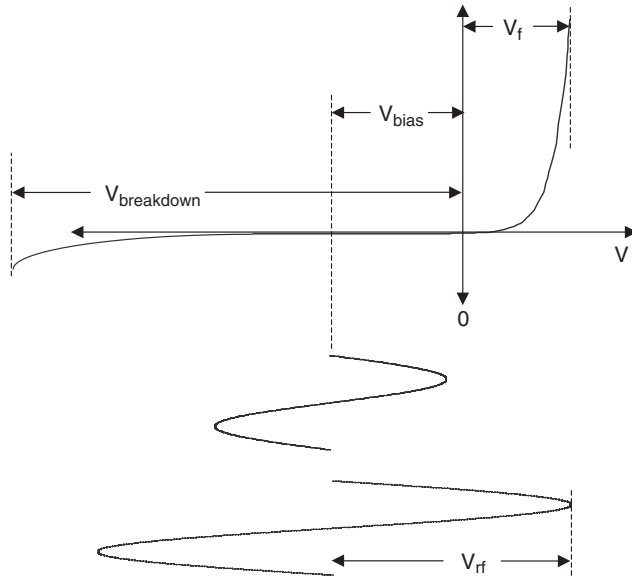
FIGURE 12.2   Diode current as a function of applied RF voltage.

and the thickness or length of the *i* region *W* is thin enough, the *i* region becomes flooded with charge carriers, thus drastically lowering the diode's resistance to a virtual short. Since there is so much stored charge in the diode, even for large RF signals, there is not sufficient time during the reverse portion of the RF cycle to eliminate conduction. In essence, the stored charge *Q* is substantially greater than the charge that the RF waveform can add or remove during any half cycle of operation. Both the carrier lifetime τ and thickness *W* of the *i* region, which relates to the transit time frequency of the diode, are factors in determining the low-frequency limit of the diode. Below this low-frequency limit, the *pin* diode functions as a poor *p–n* junction rectifying the RF waveform.

It now becomes obvious that one of the most important parameters of *pin* diodes is the switching time, since most applications are switch applications. However, it should be noted that the switching time not only is a function of the diode characteristics but also is very dependent on the dc bias driver circuitry. When the diode is reversed biased, there are no carriers in the *i* region; however, if a forward voltage is suddenly applied, the depletion region collapses almost immediately. During this charge storage interval, the *i* region uniformly fills with charge assuming that the transit time in the region is short and the carrier lifetime τ is long. The charging of the *i* layer relates to the turn-on time of the diode. The turn-off time, however, is not the same because the carriers in the *i* layer behave differently in this case. As we apply reverse voltage, current flow begins immediately, limited by the dc driver circuitry and the contact resistance of the diode. Hence, designing the driver to spike this current improves switching time. As the charge is swept out of the *i* region, depletion layers form at the boundaries of the *p* and *n* layers, thus forming a series capacitance with the charge still present, which forms a low series resistance in the center of the *i* layer. The applied reverse voltage or electric field eventually sweeps out all the charge carriers in the *i* layer, returning the diode to the steady-state off condition.

12.2 *pin* DIODE SWITCHES

The *pin* diode switches are very popular throughout the industry and are used in a variety of applications and frequency bands ranging from HF radio receivers and multikilowatt transmitters to millimeter radar and communications systems [12.4, 12.5]. Regardless of application or frequency range, the diodes are still used as current controllable resistors. To help illustrate the design concepts, we will first examine the principles of simple series or shunt switches. Before any switch design can begin, one must at least have an idea of how to represent a *pin* diode with an equivalent circuit model.

Since the frequency range between 900 and 2500 MHz has become popular, the circuit model for a surface-mountable plastic packaged device will be used. Parameters for a typical diode can be obtained from a variety of manufacturer data sheets. Assuming small signal to moderate power levels (<6 W), the steady-state models for the on state and the off state are shown in Figure 12.3. Typically, the junction resistance R_j can be ignored during reverse-bias conditions, since $R_j \ll 1/\omega C_j$, thus dominating the reverse isolation characteristic of the diode. Similarly, the on state model can be simplified by combining R_j, which is a very small quantity during forward-bias conditions, with R_s (contact resistance) to form a new value for R_s. The element values for a typical plastic packaged *pin* diode are shown in Table 12.1.

Using the above diode parameters, a simple series single-pole single-throw (SPST) switch can be analyzed. A single diode series switch with no resonant elements provides
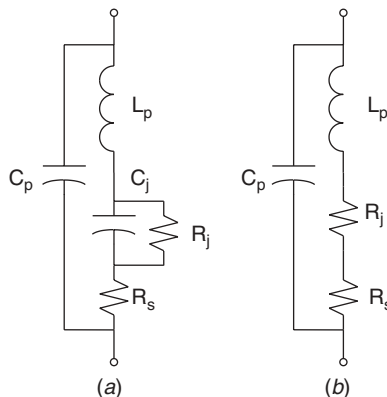
FIGURE 12.3   Packaged *pin* diode model: (*a*) off state; (*b*) on state.

TABLE 12.1   Plastic Surface-Mount *pin* Diode Model Parameters for Forward- and Reverse-Bias Conditions

	On State	Off State
R_s or R_j	1.47 Ω	45 kΩ
C_j		0.21 pf
C_p	0.05 pf	0.05 pf
L_p	1.23 nH.	1.23 nH.
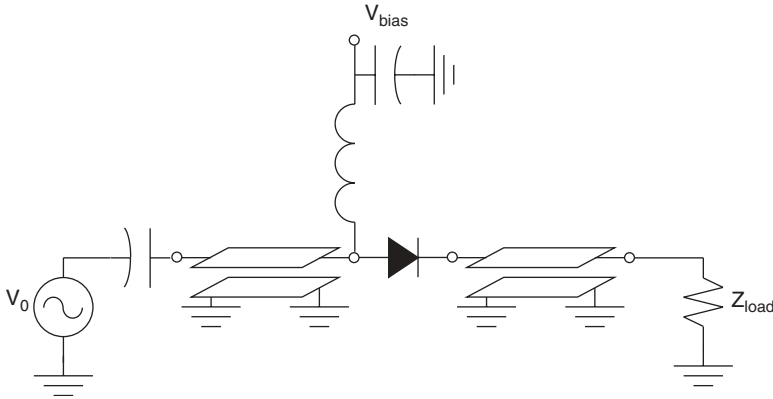
FIGURE 12.4   Simple single-pole single-throw *pin* switch model.

broad frequency response with a minimum of insertion loss. The minimum insertion is due to the fact that there is only one diode; however, that also means that the isolation is also limited. A simple realization for the switch is shown in Figure 12.4. To help illustrate the design concept, we may simplify the forward and reverse diode models to just a single element, R_s and C_j, respectively. This approximation will yield a reasonably good value for insertion loss and isolation. A simple series switch is easy to realize using microstrip technology since all circuit components can be surfaced mounted. However, for high-power applications, shunt-mounted diodes are easier to heat sink and thus can dissipate more power but must be mounted through the substrate.

Simple SPST RF switches are not very common in industry today, so the performance of a simple single-pole double-throw (SPDT) switch (Fig. 12.5) will be illustrated. If one assumes that one diode is reversed biased and the other diode is forward biased, the switched performance can easily be analyzed using a modern CAD tool such as ADS 1.5. Using the parameters form Table 12.1, the isolation and transmission loss of the above switch are shown in Figure 12.6. It should be noted that
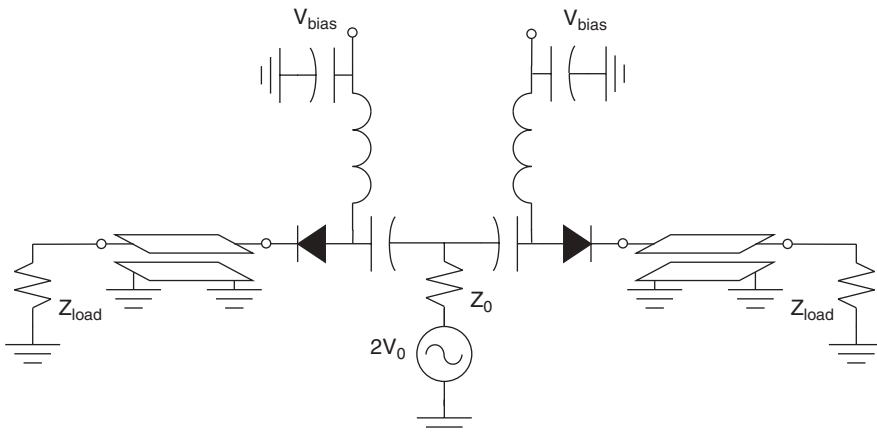
FIGURE 12.5   Simple single-pole double-throw *pin* switch model.
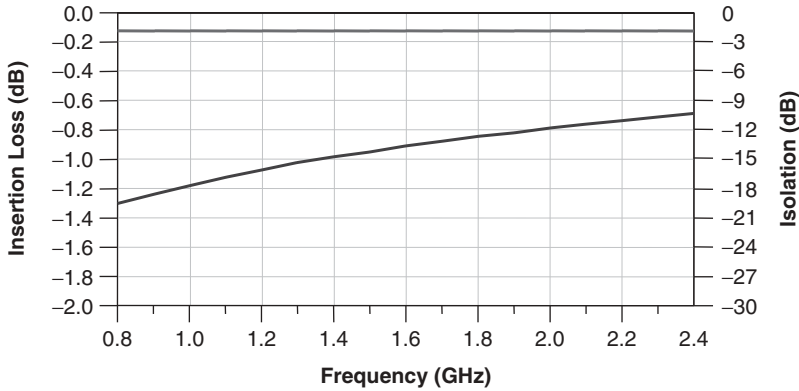
FIGURE 12.6 Insertion loss and Isolation of simple SPDT *pin* diode switch.

the forward-bias diode was modeled as a series resistor R_s, and the reactance of the off diode was assumed to be $1/j\omega C_j$. The insertion loss of this simple switch can be approximated as

$$\text{IL (dB)} = 20 \, \log\left(1 + \frac{R_s}{2Z_{\text{load}}}\right) \tag{12.1}$$

and the isolation can be defined as, disregarding parasitics,

$$\text{Isolation (dB)} = 10 \, \log[1 + (4\pi f_0 C_j Z_{\text{load}})^{-2}] \tag{12.2}$$

It is also convenient to note that the power dissipated by the diode can be approximated by

$$P_d \sim \frac{(R_s/Z_{\text{load}})V_0^2}{2Z_0} \tag{12.3}$$

provided the load is matched to the source.

Using the same principles, a multithrough switch can also be designed limited only by the parasitics of the common node to ground. Improved isolation for series switches can be obtained by adding shunt diode elements on the load side of the series diodes. For narrow-band designs, $\lambda/4$ transmission line sections can be added with various combinations of multiple series and shunt diodes. The addition of the tuned transmission line sections greatly improves switch isolation at the expense of bandwidth. Typically, in practice, it is difficult to achieve switch isolations greater than about 30 dB by a single *pin* diode when used in either a shunt or series configuration, regardless of operating frequency. The causes of this limitation are finite values of diode off capacitance and series resistance as well as circuit radiation effects in the transmission medium employed and inadequate shielding. That is why switches composed of combinations of series and shunt diodes (compound switches), usually with resonant structures (tuned switches), are used to improve isolation performance. The most common compound switch configurations employ *pin* diodes mounted in either the series-shunt, or PI, or tee designs. In the low-insertion-loss or on state for a compound switch, the series diode is forward biased while the shunt diode is reversed or zero biased. The converse
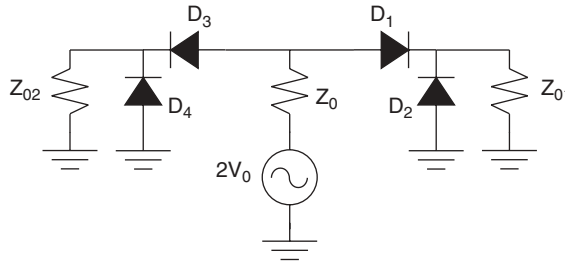
FIGURE 12.7   Simple circuit model of compound SPDT *pin* diode switch.

is true for the isolation (high-insertion-loss) or off state. However, the addition of multiple diodes with different bias conditions does complicate the switch because of the need for various dc decoupling elements.

As an example, let us consider a SPDT series–shunt switch with no resonant elements. The switch is shown in Figure 12.7. To simplify the example, all the bias elements have been removed from the circuit model and, as before, a simple diode model will be used during circuit analysis. However, we will add one more element to the off-state diode model, the reversed-bias junction resistance R_j. Thus the off-state diode model will consist of the parallel combination C_j and R_j. The diodes are biased such that the low-insertion-loss path is from the source to Z_{01}. To achieve this condition, diodes D_1 and D_4 will be forward biased while diodes D_2 and D_3 will need to be reversed biased. Conversely, the isolated path will be from the source to Z_{02}. As before, the switch can be analyzed using a linear CAD simulator. The switch isolation, insertion loss, and input return loss are shown in Figure 12.8. As illustrated in Figure 12.8, the addition of the second diode greatly improves isolation. The improved isolation performance does have its price. In addition to the added complexity, the insertion loss and return loss performance are slightly degraded when compared to the single diode switch in the previous example.
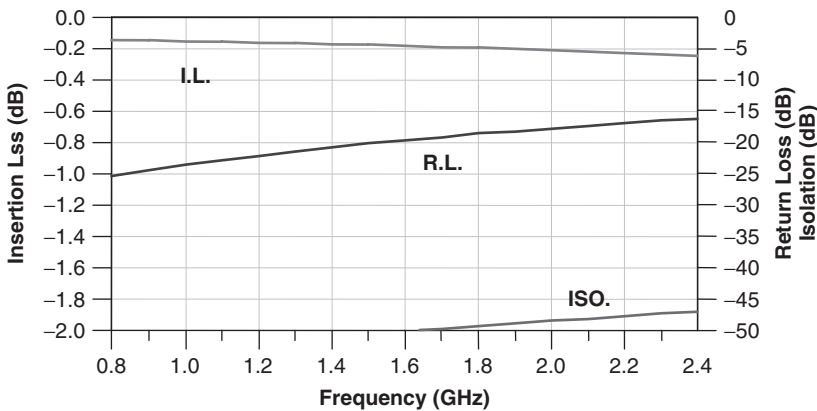
FIGURE 12.8   Insertion loss, return loss, and isolation of simple SPDT compound *pin* diode switch.
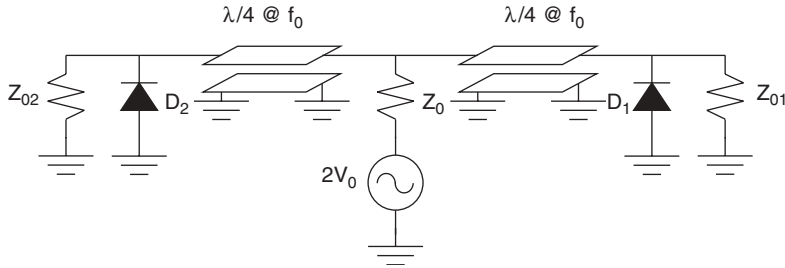
FIGURE 12.9 Simple circuit model of shunt SPDT *pin* diode switch.

In applications where narrow-band frequency response is adequate, tuned elements combined with fewer diodes may produce reasonable switch performance. This concept can be illustrated by again analyzing the SPDT shunt switch, depicted in Figure 12.9. As before, bias elements are not included. It should be noted, contrary to series-diode-only switch designs, the shunt switch performance characteristics are dependent on the opposite diode parameters. The insertion loss of a shunt switch is primarily a function of the junction capacitance and reversed-bias junction resistance (C_j and R_j), while the isolation is primarily a function of the forward-bias series resistance R_s. Another advantage of shunt-only configurations is the ability to easily heat sink the diodes for high-power applications. The operation of the shunt switch operates slightly differently from that of the previous switch examples, which did not have any tuned elements. When diode D_2 is biased on its near-short-circuit impedance is transformed to a near-open circuit by the $\lambda/4$ transmission line between the common node and Z_{02}. This transformation prevents the low impedance of the diode from loading the common node of the switch. Since Z_{01} is biased off, it does not affect Z_{01}, and since Z_0 and Z_{01} are typically equal (50 Ω), the $\lambda/4$ transmission line between the common node and Z_{01} provides no transformation. The switch simulation, which uses the same diode element values as the previous example, is shown in Figure 12.10. As can be seen in the performance simulation, the isolation, which is still broadband in nature, is quite reasonable since it is primarily determined by R_s. The return loss and insertion loss performances are also good, but only for a much narrower frequency range, which is a function of the resonant transmission lines and the diode characteristics.

To help illustrate all the above concepts in a single switch configuration, we will now analyze a typical *pin* T/R switch (Fig. 12.11). The basics circuit for the T/R switch consists of a *pin* diode connected in series with the transmitter and a shunt diode connected a quarter wavelength ($\lambda/4$) away from the antenna port, directly across the receiver port. When the handset is placed in the "transmit" mode, the series diode on the transmitter side is forward biased, appearing as a very low impedance, thus providing a low loss path to the antenna. Since both the series and shunt diodes are dc connected together, they are also forward biased at the same time. The shunt diode, because it is forward biased when the system is transmitting, effectively shorts the receiver port, preventing the transmitter power from damaging the receiver circuitry. As in the previous example, the shunt diode's near-short-circuit impedance is transformed by the $\lambda/4$ transmission line to become near open circuit at the antenna port. As in all switch designs, isolation and insertion losses are a function of the diode parameters. When the switch is in the "receive" position, the diodes are reversed or at least zero biased,
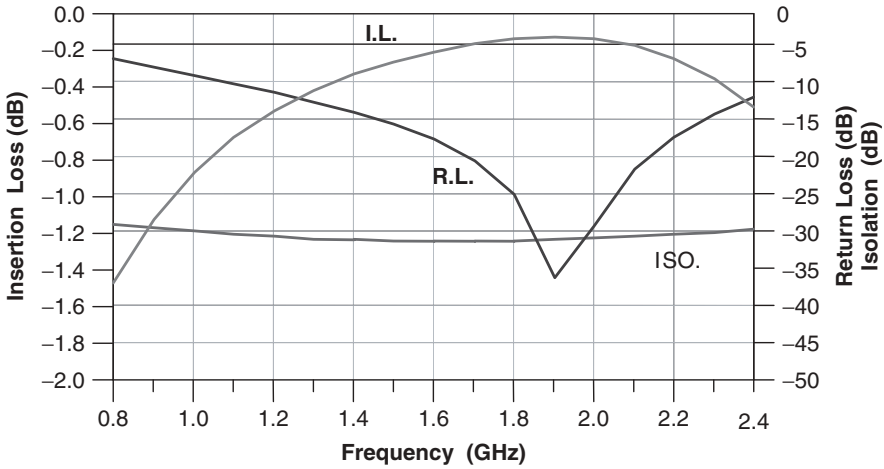
FIGURE 12.10   Insertion loss, return loss, and isolation of tuned element SPDT shunt *pin* diode switch.
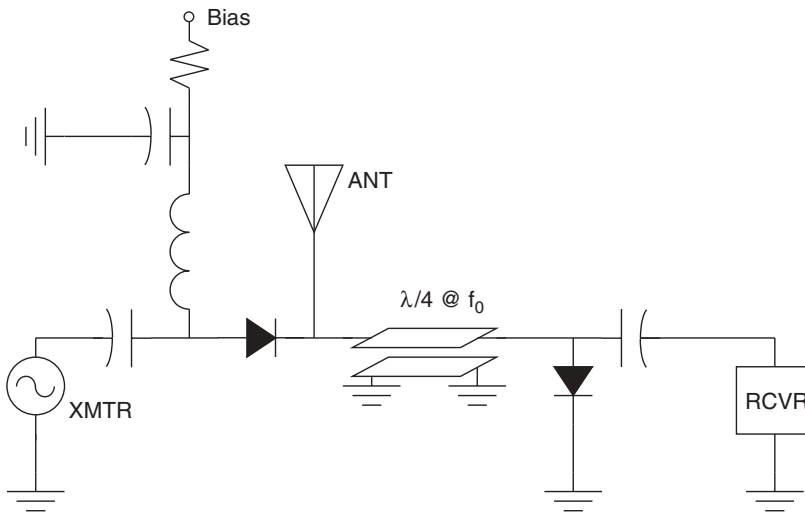
FIGURE 12.11   Simplified circuit model of series/shunt *pin* diode T/R switch.

thus appearing as small-value, high-Q capacitors. In this condition, the transmitter is essentially disconnected from the common or antenna port while the shunt diode at the receiver port appears as a near open circuit. Hence the loss between the antenna and receiver is very low. There is also a subtle advantage to this switch configuration. When the handset is in the receive, or "standby," mode, no dc is consumed. It should be noted that the shunt diode has the ability to dissipate as much or more power than the series diode due to the fact that the quarter-wavelength transmission line transforms the common node (antenna) impedance to a very low value. Since this impedance is low, it implies that the RF current is high. The situation rapidly worsens

if the antenna becomes mismatched, creating a high VSWR in the system. The amount of incident power that this switch can handle depends on the power rating of the *pin* diode, the diode's series resistance, and the maximum VSWR in the system. The diode breakdown voltage is not an issue with this type of switch because when RF power is applied both diodes are forward biased—a condition that is not always present with other switch topologies. Since modern CAD tools, with nonlinear analysis capability, (Advanced Design System 2002 by Agilent [12.6]) are readily available, the maximum RF currents or voltages in any switch circuit can be determined as a function of system VSWR and applied RF power. It is then very easy to have the simulator compute the required diode power dissipation. Rather than try to calculate maximum RF current or power dissipation with simple approximations, this method is preferable because circuit Q and VSWR strongly influence the results. In addition, it should be noted that this type of switch, with a single forward low current bias supply ($\sim$10 mA), is really only adequate for low-power applications on the order of 5 W. However, with more forward-bias current, substantially more incident RF power can be accommodated.

Up to this point we have made the assumption that there is sufficient charge in the *i* region of the diode during forward-bias conditions, that the RF current during the reverse half of the cycle cannot alter the diode series resistance. To a first-order approximation this is correct; however, the applied RF current does modulate the forward resistance to some extent, thus causing distortion [12.7 and 12.14]. The junction resistance and junction capacitance (R_s and C_j) as well as the low-frequency $I-V$ characteristic of the diode can also cause distortion. Distortion can even be a problem in receiver applications requiring wide dynamic range, where *pin* diodes are used in attenuator circuits for gain control. The *pin* diodes are always more linear than its common diode counterpart.

In applications that employ both forward- and reversed-bias diodes when RF power is applied, the distortion from the reversed-bias diode, provided the peak RF voltage is less than the dc bias, will usually be smaller than the forward-bias diode. As in a variety of circuit applications, back-to-back connected diodes can be used to reduce distortion. The reduction in distortion is due to the fact that the distortions generated in each diode are equal and opposite, provided the diodes are matched, thus canceling the distortion currents in the circuit branch. In practice, about 20 to 30 dB of distortion improvement can be obtained with not quite perfectly matched diodes or perfectly balanced circuits. Back-to-back connected diodes can greatly complicate circuit implementation and degrade other switch performance criteria such as insertion loss or isolation.

The distortion generated by a single forward-bias *pin* diode used in a typical microwave switch has been analyzed [12.7 and 12.14]. Diode distortion performance has been shown to be related to the ratio of stored charge to forward resistance and the desired frequency of operation. The distortion effects related to carrier lifetime are a function of the amount of dc charge stored in the diode to the incremental amount of charge added or removed during the applied RF cycle. The second-order intermodulation distortion or intercept point (IP2) and the third-order intermodulation distortion or intercept point (IP3) can be approximated as

$$\text{IP2} = 34 + 20\log\left(\frac{f_0 \tau I_f}{R_s}\right) \tag{12.4}$$

$$\text{IP3} = 21 + 15\log\left(\frac{f_0 \tau I_f}{R_s}\right) \tag{12.5}$$

where f_0 is the operating frequency in megahertz, τ is the carrier lifetime in seconds, I_f is the forward-bias current in amperes, and R_s is the diode series resistance in ohms.

The analysis for the series/shunt switch will now become considerably more complicated. A T/R switch of this type can be realized in a variety of transmission line media such as microstrip fabricated on Teflon–fiberglass substrate or in a multilayer low-temperature cofired ceramic (LTCC) substrate. Multilayer ceramics offer high circuit density, small size, and high circuit Q and are cost effective. It should also be noted, to save space on the substrate, the $\lambda/4$ transmission line will be replaced by a lumped-element equivalent consisting of inductors and capacitors. The LTCC switch model is shown in Figure 12.12 and was optimized for a center frequency of 860 MHz. An illustration of the LTCC substrate depicting its layer structure is shown in Figure 12.13. The T/R switch is fabricated on a LTCC substrate composed of 12 layers with a layer thickness of 0.0037 in. The dielectric constant of the material is 7.8 (ε_r) and both the conductor metalization and via metal are silver. The two plastic packaged *pin* diodes are surface mounted to the substrate. Because of the multilayer nature of the design, an electromagnetic simulator, such as Sonnet Software's EM, must be used in the design of the circuit elements. As in the previous example, when the diodes are forward biased, the antenna is connected to the transmitter. Conversely, when the diodes are reverse biased, the receiver is connected to the antenna. Bias for the diodes is provided through the series 100-Ω resistor, with the dc return through the transmitter port. The computer performance simulation and the switch photograph are shown in Figure 12.14.

In applications where performance is a premium GaAs *pin* diodes are used for switching elements. The *pin* diodes fabricated on GaAs offer superior high-frequency performance because for a given diode area the reverse-bias impedance is high and the forward loss resistance is low due to the high mobility of the material. Because of the excellent high-frequency performance, a somewhat more complex circuit model may become useful (Fig. 12.15).

The values shown in Table 12.2 are for a monolithic GaAs *pin* diode with a diameter of 25 μm [12.8]. It is interesting to note the impedance range of the diode as a function of bias current. This can be calculated by grounding one end of the diode and evaluating S_{11} at the particular frequency of interest. The input reflection coefficient (S_{11}) for the grounded diode evaluated at several bias currents is shown in Figure 12.16.
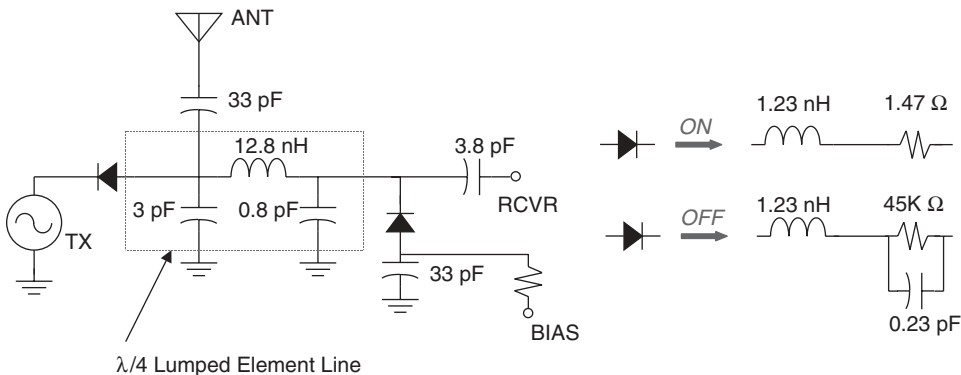
FIGURE 12.12   Model of series/shunt *pin* diode T/R LTCC Switch.
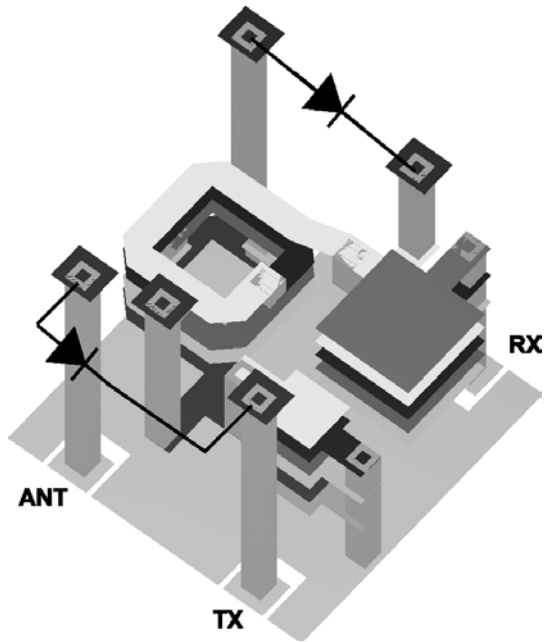
FIGURE 12.13 Layer structure of the LTCC *pin* diode T/R switch.
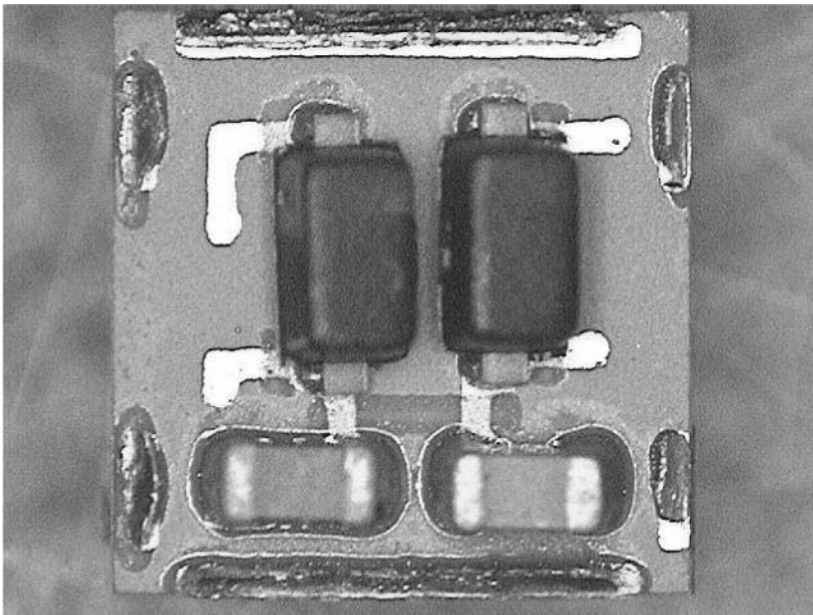
(*a*)

FIGURE 12.14 LTCC *pin* diode T/R switch: (*a*) photograph; (*b*) simulated performance.
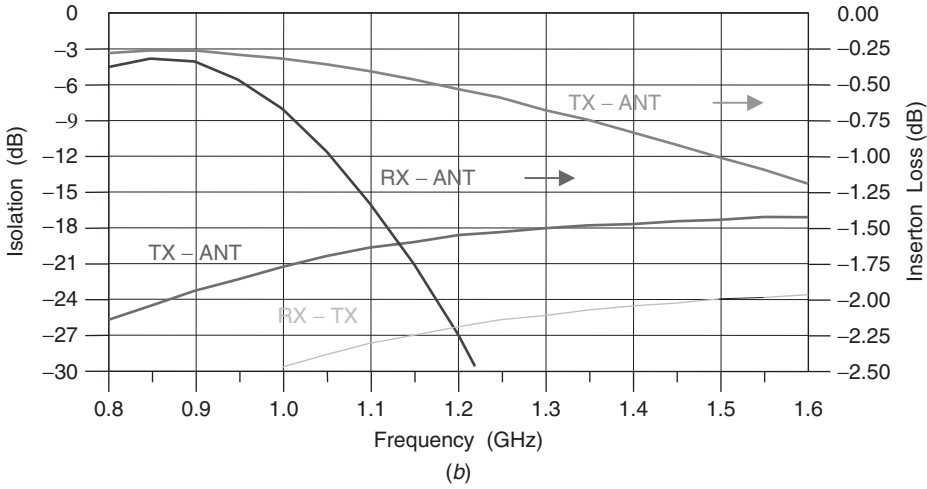
FIGURE 12.14   (*continued*)
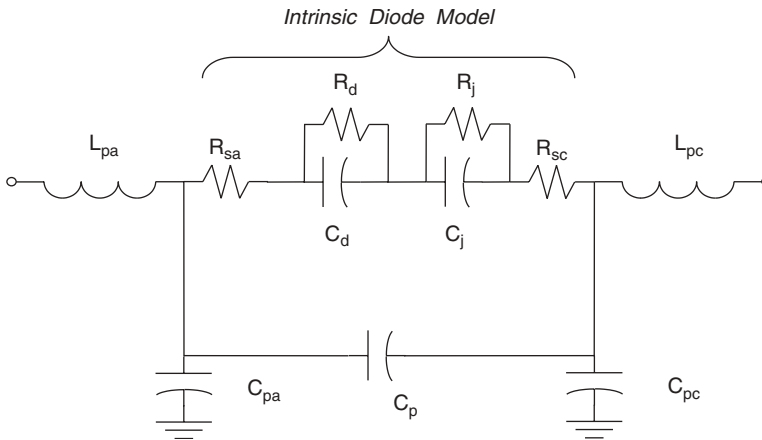
FIGURE 12.15   GaAs *pin* diode small-signal model.

12.3   *pin* DIODE ATTENUATORS

The variable series resistance characteristic of a *pin* diode can also be used as the controlling element in attenuator circuits. This resistance can vary from a very high value (at zero bias) to a very low value, as we saw in our previous switch examples. As discussed earlier in the chapter, the forward resistance of the diode is a function of the semiconductor characteristics of the *pin* junction as well as being, throughout most of the operating range, inversely proportional to the bias current ($R_s \sim 1/I_f$). For example, the thicker the *i*-region length W, the higher the series resistance R_s. Also the higher the charge carrier mobility, the lower R_s can ultimately become. Typically, for a change of four orders of magnitude in bias current (0.01 to 100 mA), the series resistance varies by about four orders of magnitude (Fig. 12.17) [12.9].

TABLE 12.2   GaAs *pin* Diode Small-Signal Model Parameter Values

Parameter		Value
	Bias-Dependent (Intrinsic) Values (0–100 mA)	
C_d:	junction capacitance	2.86–30.2 pF
R_d:	junction resistance	0.79–36 Ω
R_j:	*i*-region resistance	0–49,000 Ω
C_j:	*i*-region capacitance	0.02–0.13 pF
	Static Model Values	
L_{pc}:	cathode series inductance	0.03 nH
L_{pa}:	anode series inductance	0.04 nH
C_p:	cathode-to-anode fringing capacitance	0.075 pF
C_{pc}:	Cathode pad capacitance	0.068 pF
C_{pa}:	Anode pad capacitance	0.035 pF
R_{sc}:	Cathode bulk resistance	0.27 Ω
R_{sa}:	Anode bulk resistance	0.06 Ω
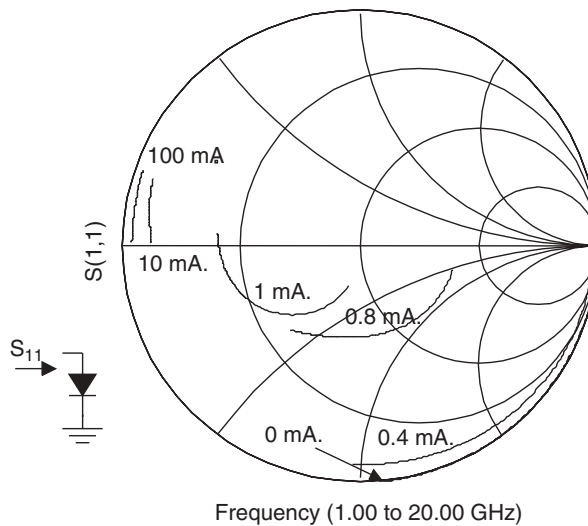
FIGURE 12.16   GaAs *pin* diode small-signal S_{11} as a function of bias current.

Unlike switches, in which the diodes are biased well in the forward-bias region, the stored charge is substantial, or the diodes are reverse biased where there is no conduction, variable attenuator circuits can employ diodes biased anywhere in the forward-current regime. The designer must carefully consider the range of diode resistance required in an attenuator for any particular circuit, since the amount of stored charge in the diode decreases as the bias current is reduced. For very high values of series resistance, very little bias current is required; hence, very little stored charge is present in the *i* region of the diode. When there is little charge in this region, it takes very little applied RF power to cause distortion. This condition limits the useful
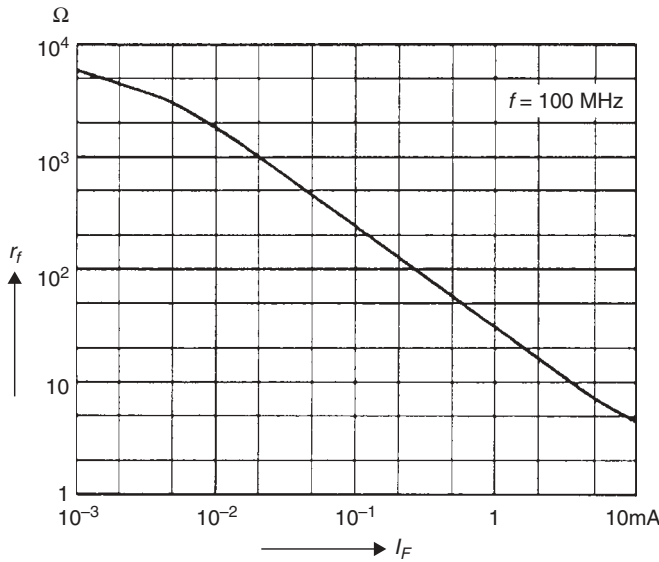
FIGURE 12.17   The *pin* diode small-signal series resistance as a function of bias current.

variable resistance range of the diode for wide-dynamic-range applications. Because of distortion considerations, it is sometimes necessary to cascade attenuator sections to obtain the required performance. In general, *pin* diode attenuators used for gain control applications (AGC, power-leveling circuits, etc.) provide better overall performance than other types of attenuators employing different device technology. In particular, much better system linearity is achieved when compared to varying the bias on a transistor, since its linearity degrades rapidly as one moves away from the optimum bias point.

As mentioned previously, another application of *pin* diodes is the high-frequency (HF) realm. In the HF range, due to the long carrier lifetime of the junction, the *pin* diode still behaves like a real resistance, the magnitude of which is a function of forward diode current. In view of this behavior, the *pin* diode can be used as a switch or a variable resistor for HF signals. An important application of *pin* diodes that has found favor in recent times is their application to dc-operated attenuators in TV tuners and antenna distribution amplifiers. As evidence of their excellent HF and VHF linearity characteristics, the second-order intermodulation distortion (IMD) and the cross-modulation performance of a typical 10-dB attenuator are shown in Figure 12.18 [12.9].

There are many kinds of attenuator configurations used in the industry today, ranging from reflective circuits to PI or bridged-tee matched attenuators, as in the above HF example. Such devices exhibit useful performance characteristics for frequencies ranging from HF radio to millimeter waves. Due to space limitations, only the balanced reflective attenuator, which can be extrapolated into a balanced reflective phase shifter by replacing the terminations with a shorted length of line (ϕ), and the matched bridged-tee attenuator will be illustrated [12.10].

The balanced reflective attenuator, shown in Figure 12.19, consists of a balanced hybrid, 90° coupler, two shunt or series diodes, two matched terminations, and
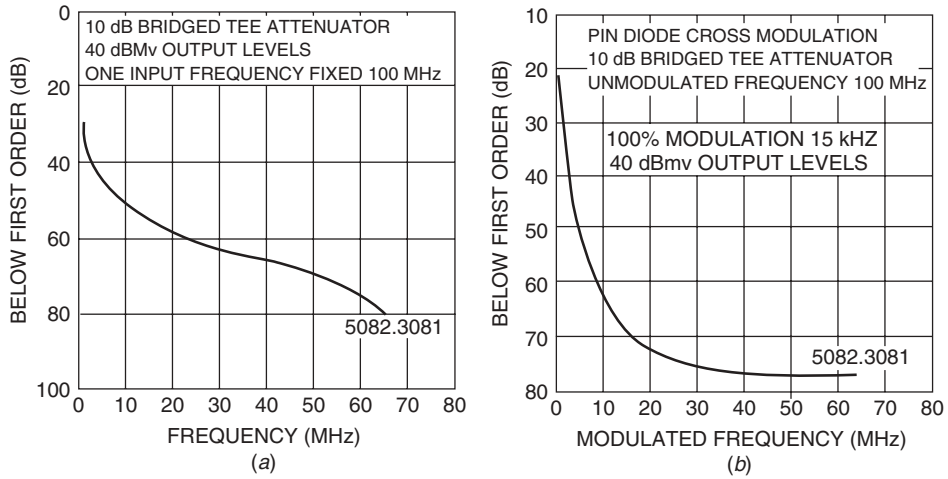
FIGURE 12.18 Intermodulation performance in a *pin* diode: (*a*) second-order IMD; (*b*) cross-modulation.
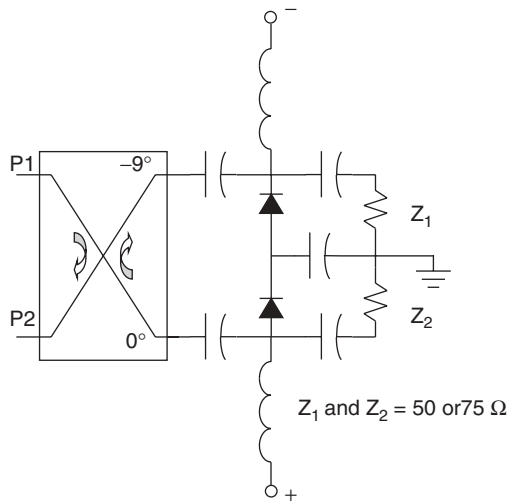
FIGURE 12.19   A *pin* diode balanced reflective attenuator.

associated bias-decoupling elements. For the moment, let us assume that only the matched terminations are connected to the hybrid. If a RF signal source is placed at port 1 (P1) of the hybrid, the signal power is divided equally between the two matched terminations with the divided voltage phases being different by 90°. Assuming the loads are perfectly matched and the hybrid is perfectly balanced, the reflected signal is zero; hence, no power is present at port 2 (P2). Conversely, if both output arms of the hybrid are either short or open circuited, the input signal is again equally divided, but it is completely reflected by the perfectly mismatched loads. The reflected signals are

then combined at the output of the hybrid at P2. Since the diodes can be forward biased anywhere from essentially the open-circuit position to the short-circuit case, the power at P2 can be varied from zero to full power. In practice, this is of course not the case since there are fine values of coupler isolation and loss to contend with. In addition, the diodes will not be exactly matched, and the loads will not be exactly 50 Ω or matched to each other; this will also affect the ultimate useful range of the attenuator. However, with proper component selection 20 to 30 dB of useful range is attainable. One of the subtle features of this type of attenuator is the fact that if the load at P2 is matched, the source will see a matched termination through all values of attenuation. It should also be noted that the terminations Z_1 and Z_2 must be capable of dissipating at least one half of the input power applied to the attenuator since, during the operating condition of full attenuation, all the source power is present at these loads Z_1 and Z_2. This type of attenuator can also be constructed without the terminations Z_1 and Z_2 if the diodes are biased from the 50-Ω point to full conduction. This will improve the distortion characteristics because of the increased minimum value of stored charge present in the *i* region but might make the circuit a little more sensitive to diode variations as well as requiring higher values of diode power dissipation.

The bridged-tee attenuator, which is very common at HF and UHF, has some very useful features. The circuit that we will discuss is shown in Figure 12.20. For clarity, all bias elements have been ignored. Although the attenuator is single ended, if the diodes are biased correctly, the input and output return loss of the network can be reasonably good. To maintain an impedance match, the diodes must be biased in such a way as to satisfy the following relationship:

$$Z_0 = (R_{s1} R_{s2})^{1/2} \tag{12.6}$$

where R_{s1} and R_{s2} are the series resistances of diodes D_1 and D_2, respectively. Minimum attenuation occurs when diode D_1 is biased to its maximum value of R_{s1} and D_2 is biased for minimum series resistance (R_{s2} at maximum I_f). The attenuation and return loss of this ideal attenuator are shown in Figure 12.21. It should be noted that the return loss was calculated assuming that the diode forward-current tracking, which determines the values of R_{s1} and R_{s2}, has a 10% error and the resistors (Z_0) have a 5% tolerance. With these assumptions, the return loss of the attenuator is always less than −30 dB and the attenuation range is greater than 30 dB.
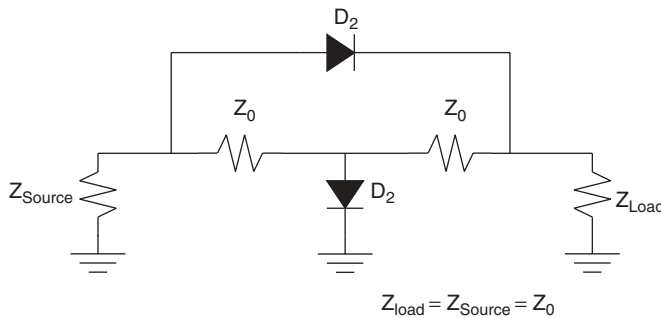
FIGURE 12.20   A *pin* diode bridged-tee attenuator.
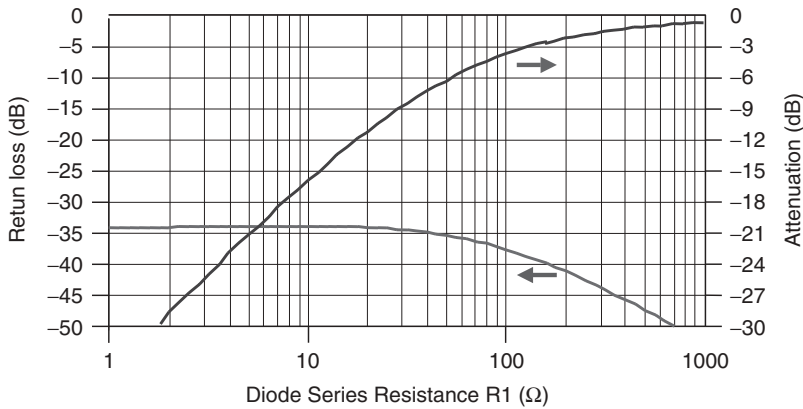
FIGURE 12.21   The *pin* diode bridged-tee attenuator performance.

12.4   FET SWITCHES

Field-effect transistors, whether they are Si junction devices or GaAs MESFETs, have been used as switching devices for a long time. As we have learned in the mixer Chapter 11, the FET makes excellent switches, since the ratio between the on and off resistances of the channel is quite high.

At practical RF and microwave frequencies, the off resistance is shunted by the drain-to-source capacitance and is primarily the dominant parameter in the off state. If the FET is sized correctly for the application, the on resistance can be comparable to that of a *pin* diode, that is, on the order of 1 Ω. It is sometimes convenient to define the figure of merit of a switch as a hypothetical cutoff frequency:

$$\omega_c = \frac{1}{R_{on}C_{off}} \tag{12.7}$$

where R_{on} is the total series resistance of the device at full conduction (zero bias) and C_{off} is the drain-to-source capacitance in the off state ($V_{gs} = V_{pinchoff}$). This relationship is essentially independent of device size since these parameters scale relatively well. For example, if we make the FET three times larger, the on resistance will be three times smaller but the off capacitance will be three times larger; hence ω_c is unchanged. However, there are additional device parameters that must be considered when selecting a device for use in switch applications. The pinchoff and drain-to-gate breakdown voltages determine key switch performance characteristics such as operating supply voltage, power-handling capability, and distortion. Although a control voltage on the FET gate is required to control switching, the gate of a FET, whether it is a Si JFET, GaAs FET, or MOSFET, requires no current. Since FET switches require no power, biasing the circuits is relatively simple. This feature is a distinct advantage when designing multithrough switches realized with monolithic circuit technology.

As we have learned previously, FET switches can be constructed in a variety of circuit configurations [12.11]. The simplest configuration would employ a FET as a switching element in series with the transmission path or as a shunt element in

parallel with the path. Shunt-only switch configurations tend to be used only in modulator or attenuator applications where there are no multithrow requirements. Isolation improvement, compared to a single device, can be obtained when compound circuits with series and shunt devices are implemented. Since the series resistance and the drain-to-source capacitance of the FET are similar to that of *pin* diodes, basic switch performances are similar. The differences will be in the dc power consumption and distortion performance.

Let us first consider the simple SPDT series switch configuration of Figure 12.22. If one assumes that the hypothetical FET, with 1 mm of gate periphery, exhibits a series resistance of 2 Ω and a drain-to-source capacitance of .17 pF when biased at cutoff, the isolation and insertion loss of the circuit can easily be calculated using a linear circuit simulator (ADS 2002 [12.6]). It should be noted that the bias elements are included in the performance simulation and that the bandwidth is quite wide. The limitation in the useful operating bandwidth is the value of the bypass and dc-blocking capacitors. Broadband performance can easily be achieved since the bias networks are simple high-value resistors. This is in sharp contrast to *pin* diode switches where the bias networks must actually carry current. This usually requires inductors as decoupling elements, unless the bias current is small and the $I-R$ drop of a resistor can be tolerated. Assuming the simple FET model presented above, with one device biased on and the other biased off, the broadband performance of the SPDT switch is shown in Figure 12.23.

In the above example, it should be noted that the FET was sized for operation in the lower portion of the microwave frequency range. As the frequency is increased, the drain-to-gate capacitive reactance of the FET becomes substantial; hence, switch isolation degrades. Microwave applications [12.12–12.14] which require broadband multithrow switches, for the 2- to 18-GHz frequency range, would probably be realized using a series/shunt configuration with small-periphery FETs. As an example, we can now investigate the design of a single-pole four-throw (SP4T) decade bandwidth switch.

The design of the SP4T switch is based on a series–shunt–shunt configuration. In this configuration, each switch arm is composed of a series FET (75 μm) and two shunt devices (75 μm, 200 μm). The desired path is determined by correctly
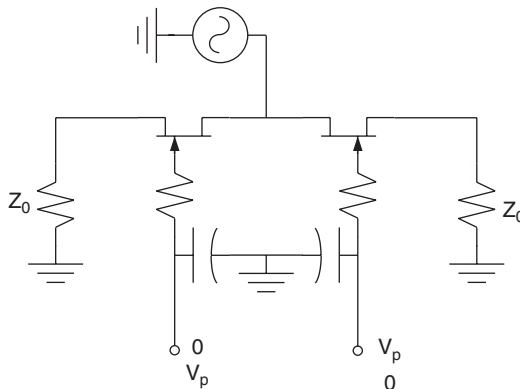
FIGURE 12.22   SPDT series FET switch.
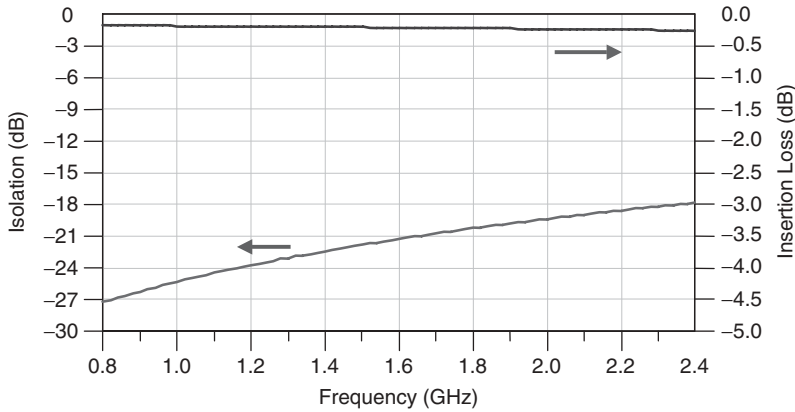
FIGURE 12.23   Broadband SPDT FET switch performance.

biasing the FETs in all switch arms. The arm with minimum through loss would have the series FET biased as a short ($V_{gs} = 0$ V dc), with both shunt devices biased at pinchoff ($V_{gs} < -5$ V dc). The devices in the other arms would be biased conversely. The schematic of the switch is shown in Figure 12.24.

The complete switch topology is designed using low-pass filter synthesis techniques. In the low-attenuation state, the shunt FET's drain characteristics provide the shunt capacitance for the filter, while the series inductors for the filters are realized using high-impedance transmission lines (Fig. 12.25). It should also be noted that the three series devices that are biased at "pinchoff" appear at the common node as a shunt capacitive reactance and must be accounted for in the final switch design. The off capacitance, as with all series switch elements, also impacts switch isolation and VSWR. For optimum isolation, the series FETs are chosen to be small. However, the smaller the series switching element is made, the higher the insertion loss will become. Unfortunately similar compromises must be made when selecting the size of the shunt devices. With careful selection of device size and matching element values, a broadband switch (2 to 20 GHz) can be realized that exhibits an insertion loss less than 2 dB with a corresponding isolation greater than 40 dB [12.12, 12.13].

Although the above examples assume that the FET switch elements are biased with either a zero or negative gate bias with respect to ground, many modern applications
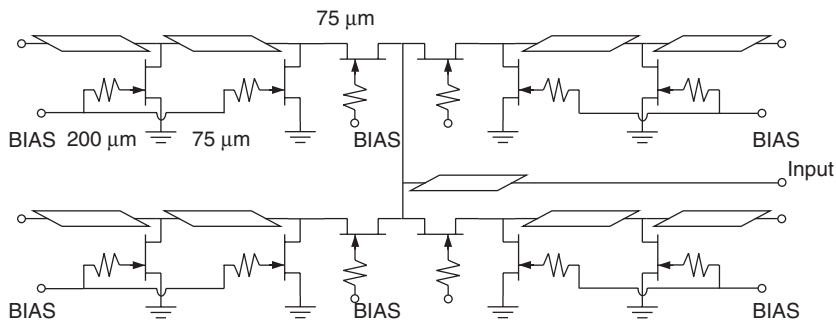
FIGURE 12.24   Broadband SP4T FET switch schematic.
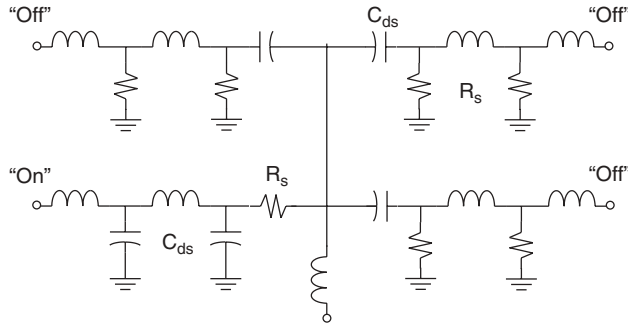
FIGURE 12.25   Broadband SP4T FET switch equivalent circuit model.

have only positive dc power supplies. This is not an issue, since it is the polarity of the gate voltage with respect to the source that is important. Proper FET operation can be easily obtained by biasing the source positive with respect to ground. The high-impedance-bias state can be obtained by bringing the gate potential to ground, while the low-impedance-bias state can be had by biasing the gate at the same potential as the source. Single positive supply operation sometimes may require an extra dc blocking or RF bypassing capacitor.

As mentioned previously in the chapter, FET switches do not have the power-handling capability of *pin* diode switches. Power handling is typically defined as the amount of input power that causes the insertion loss of the switch to increase by 1 dB ($P_{-1 \text{ dB}}$), which is the single-tone measurement corresponding to the two-tone intermodulation intercept point ($\text{IM}_{3\text{rd}}$). The amount of power in a switch is primarily determined by the amount of current that the channel can sustain in the on state, the magnitude of the reverse voltage applied to the gate, and the ratio of this voltage to the pinchoff voltage of the device. In addition, the breakdown voltages of the device are also important, since a device biased in the off state (near pinchoff) can sustain damaging gate currents caused by avalanche breakdown. When the switching FET is biased in the on state, the applied RF voltage swing can tend to reverse bias the device, thus increasing insertion loss. A small amount of forward gate bias can help alleviate this problem. The switching device can also be optimized during fabrication by increasing the carrier concentration in the channel, improving $I_{d\text{sat}}$. Decreasing the channel depth, which reduces the pinchoff voltage, is also beneficial. Increasing the gate-to-drain spacing increases the breakdown voltage but increases R_{on}. Switches used in handset applications typically employ series devices, with a gate periphery on the order of 1000 µm; hence, these switches are linear with several watts of applied RF power. The typical FET T/R switch used in GSM handset applications exhibit second- and third-order distortion products that are 65 dB below the 35-dBm carrier power level. For a given topology and operating frequency, the user must consider these requirements carefully. It may also be helpful to simulate the nonlinear behavior of the composite switch with a harmonic balance circuit simulator.

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CHAPTER 13

MICROWAVE COMPUTER-AIDED WORKSTATIONS FOR MMIC REQUIREMENTS

13.1   INTRODUCTION

Recent changes in technology have led to designs at operating frequencies in the millimeter-wave range: above 26 GHz almost to 100 GHz and beyond. These designs have been made possible by GaAs foundry services, and there are at least 11 foundries in the United States that provide such services. Many of the microwave/millimeter-wave monolithic integrated circuit (MMIC) requirements come from particular high-volume/low-cost designs for military applications. This fact is highlighted by the recent broad agency announcement (BAA) Phase 0. This interest in affordable MMIC activities, together with a reduction in cost of computer-aided design (CAD) work-stations and personal computers, has provided tools for a MMIC computer-aided design/manufacturing/test. Table 13.1 lists required synthesis/analysis capabilities to accommodate the need for MMIC requirements and to provide an integrated microwave computer-aided engineering, manufacturing, and test (CAE/CAM/CAT) workstation.

   In this chapter we show the Compact/Ansoft Software approach to an integrated CAE/CAM/CAT workstation for general microwave design use, including specific examples and in response to the MMIC goals. The ability to do tolerance analysis or yield optimization is probably most significant in light of the fact that the purpose of the exercise is to be able to provide reliable and cost-effective production. This has not been possible before. There are a variety of new software tools available, and the reader should carefully evaluate the choice of tools against his/her needs.

13.1.1   Integrated Microwave Workstation Approach

Figure 13.1 shows a 1989 CAD software workstation approach. This follows the flow of a practical CAD approach for microwave processes or MMIC design, as shown

TABLE 13.1   Lists Required for Synthesis/Analysis Capabilities for MMIC Requirement to Provide CAE/CAM/CAT Work Station

1. Linear and nonlinear synthesis programs
    A. Matching networks for single-frequency and wide-frequency bands (e.g., a 4:1 for complex loads and termination).
    B. Narrow-band/wide-band lumped and distributed filter synthesis.
    C. Oscillator synthesis from small- or large-signal S parameters. Parallel–series design, determination of all components, determination of efficiency, output power, phase noise, and other relevant data.
    D. Open and closed loop, PLL design, phase noise determination, nonlinear switching, frequency lock phase lock.
    E. Systems analysis and optimization for noise figure IMD performance.
2. Linear and nonlinear analysis program
    A. Analysis of lumped and distributed elements.
    B. Optimization of lumped elements against measured S parameters.
    C. Analysis of linear bipolar and field-effect transistors with provision for temperature and bias (new concept for noise tuning).
    D. Optimization of bipolar and FET models (and HEMT and dual-gate FETs) against measured S parameters.
    E. Analyze and optimize performance of circuits with arbitrary combinations of active and passive devices. These calculations must be available from either electrical or physical parameters.
    F. All proximity effects caused by electrical or magnetic fields must be predictable. Special effects such as multiple coupled lines, cover effects, and multilayer dielectric substances must be included. Arbitrary layouts should be handled using spectral domain techniques. To reduce computational speeds, look-up-table generators should be considered.
    G. A nonlinear analysis of high-frequency circuits can be within limitations using SPICE-like programs. A better way is to use a modified harmonic-balanced method that splits the FET and bipolar model into a linear and nonlinear time-domain/frequency-domain analysis. This technique allows interfacing with a linear program such as Super-Compact, has the advantage of providing an optimizer, and will distribute elements that are lacking in SPICE programs. In addition, the slow execution speed of SPICE is overcome in this approach.
    H. For accurate device modeling and determination of equivalent circuits special test equipment and modeling software are required that cover both dc and low-frequency analysis. Simulation and verification are part of the CAT portion.
    I. To provide reliable and low-cost designs, yield optimization and sensitivity analysis must be provided in addition to the familiar performance optimization. Traditional software approaches looked only at performance optimization.

in Figure 13.2. Starting with system definition and specification, the design is broken up into a variety of subsystems and then further into circuit blocks. Inside the circuit blocks, active and passive devices must be separated. Today this has been carried even further, so that Ansoft Designer has three major capabilities: Em simulation of the layout, nonlinear simulation of the active and passive components, and finally complete system analysis.

A first approach should be to simulate the active devices to get direction for the type of semiconductor that should be used. This has been covered in Chapter 3. This can be approached by using either a library of discrete transistors or GaAs foundry information. Device selection is based on the requirements with respect to low noise,
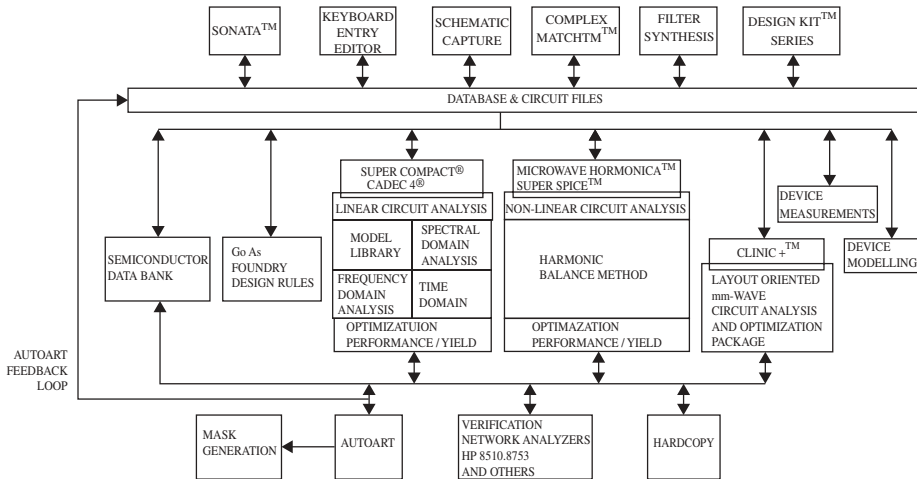
FIGURE 13.1   Designer Suite Workstation.

high gain, and/or high output power. The active devices will then be incorporated in a circuit. If synthesis programs are available, a circuit synthesis should be performed, which would be the most cost-effective way. In many cases, unfortunately, designers try to optimize existing circuits for new semiconductors. Most designs do not operate between pure 50-Ω terminations; therefore, an overall simulation of the system is essential.

At the systems level, we make a decision whether to accept or reject. If the circuit does not have to be redone, a more detailed analysis, including linear and nonlinear simulation and a first try at layout, including proximity effects, is carried out. If this is acceptable, we look at tests and tolerances and move to the final layout. There we have to check design rules, perform another simulation of the subsystem, and finally, begin fabrication. This is followed by an RF wafer test and total circuit analysis. Unless modifications are required, fabrication can be completed.

Looking again at Figure 13.1, the first row of programs are essentially synthesis programs. Here we enter electrical specifications for the circuits and obtain circuit element values. The Sonata program is a nonlinear synthesis program for oscillators. The schematic capture program helps to translate a design into a circuit file. Figure 13.3 is a screen picture taken from an Apollo computer showing the schematic capture. The schematic capture program has a library of approximately 145 elements and tracks the program as it is developed. It also contains the synthesis programs shown. These programs write to the data base and output of circuit files, which will then be analyzed. The main block of simulators are for linear circuits and nonlinear circuits. The analysis tools for linear circuits, such as Designer Suite, are based on frequency-domain analysis and provide either performance or yield optimization. Next we introduce the concept of MMIC design and foundry consideration.

13.1.2 Nonlinear Tools

The first approach to nonlinear CAD goes back to the development of SPICE (Simulation Program with Integrated Circuit Emphasis) at the University of
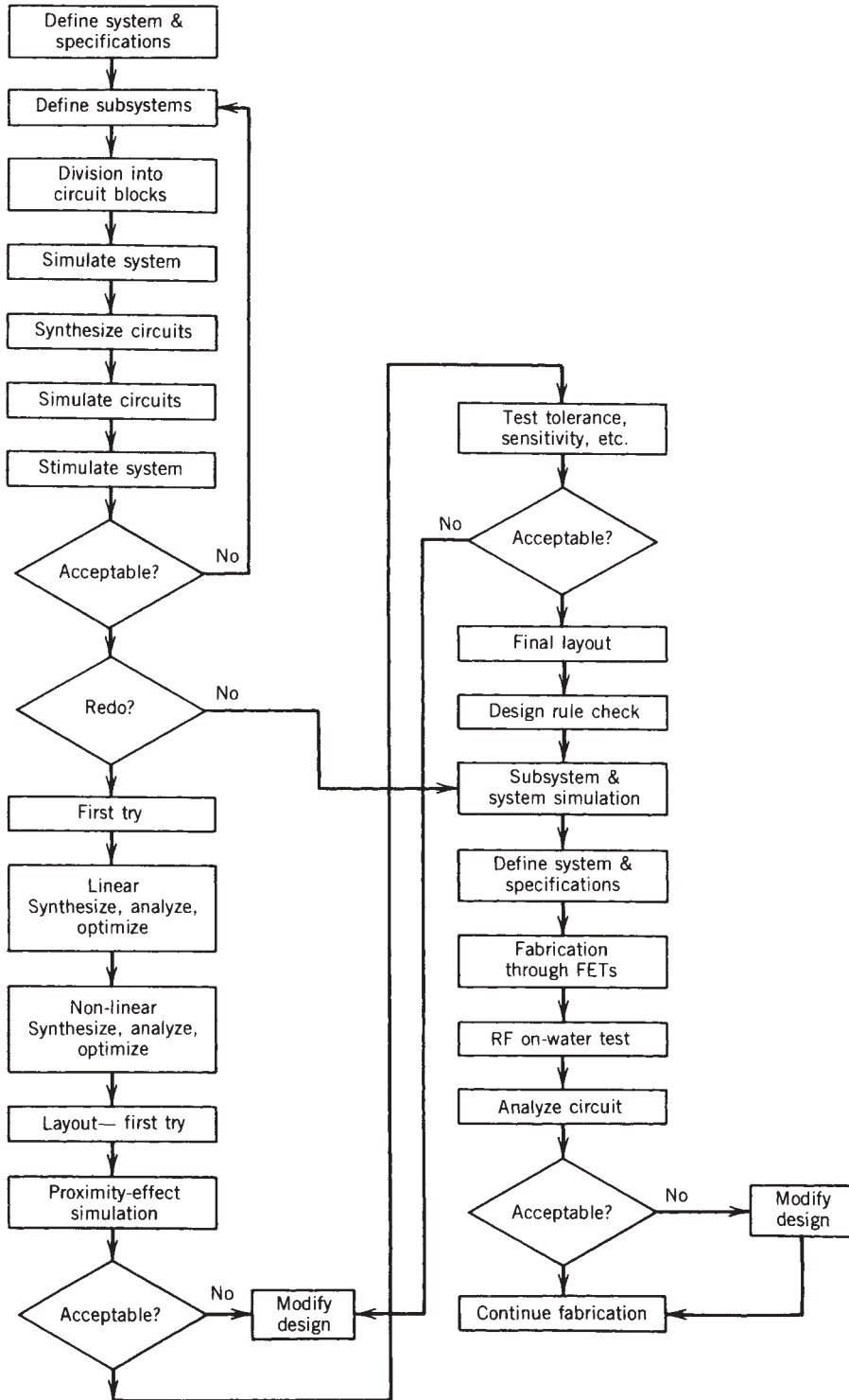
FIGURE 13.2   MMIC design flowchart.
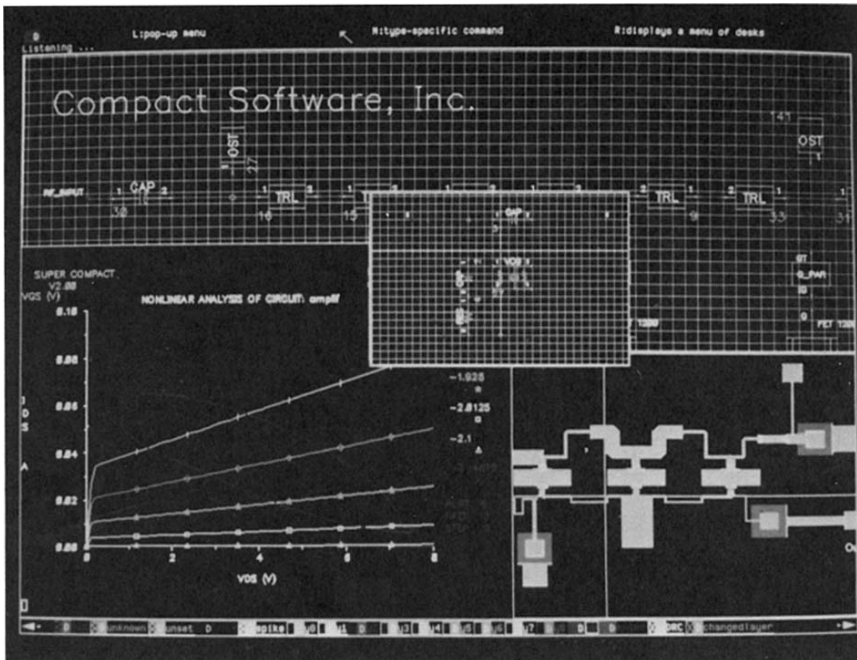
FIGURE 13.3   Screen dump of Designer Suite schematic capture interface.

California—Berkeley. Most commercial SPICE programs are based on version 2G5 or 2G6 or later, which are in the public domain. Although many readers will be aware of this approach, following is a short summary of its capabilities.

Circuit behavior can be simulated with respect to time, frequency, and voltage variation. Three different analyses can be performed:

1. Nonlinear dc
2. Nonlinear transient
3. Linear ac small-signal analysis

Any of these analyses can be conducted at various user-specified temperatures.

The following element types are found:

Resistors
Capacitors
Inductors
Transformers
Independent voltage sources
Transmission lines
Diodes
BJTs
Junction FETs
MOSFETS

TABLE 13.2   Nonlinear Model of AT41435 BJT

```
* <41435_S.CIR>
* AT41435 MODEL
*
. options acct node abstol-10n nopage
. width out-80
. temp 27
. ac lin  6 .5ghz 3ghz
*
* packaged chip used in circuit + sources
*
vin 520  sin (0) 100mv 1ghz     ac 1
r_rs     52 51               50
c_cs     51 50               1000p f
1_li     50 53               1 e4nh
vbb      53 0                0.814
xr       50 54    at         1000p f
c_cout   54 55               50
r_rl     55 0                1e4nh
1_lo     54 56               8
vcc      56 0
 probe
*
*   model for packaged chip - ux (35)
*
.subckt at    40 49
l_linp   40 41               0.05nh
t_tip    41 0 42  0          zo-66  f-1ghz n1-
l_lbp    42 43               0.3nh   0.178
c_cbep   42 44               0.03p f
c_cbcp   42 47               0.04p f
x_qip    43 47 45 q1
t_t3p    44 0  46 0          zo-25
c_cecp   44 47               0.03p f f-1ghz nl-
1_lep    45 44               0.2nh   2.175
l_lgp    46 0                0.02nh
t_t2p    47 0  48 0          zo-65
l_lop    48 49               0.05nh
.ends                                f-1ghz nl-
                                     0.023
*
*   equivalent circuit for die
*
.subckt ql    10 14  17
r_riq1   10 11               r1     1.21
r_r2q2   11 12               r2     3.12
r_r3q1   12 13               r3     2.68
d_d1q1   10 15               dmod   782
d_d2q2   11 15               dmod   629
d_d3q1   12 15               dmod   366
r_rcq1   14 15               rq     10
r_req1   16 17               rq     0.24
c_ceq1   15 17                      0.03p f
c_cbq1   10 15                      0.03p f
q_1      13 15          16  qmod    420
.ends
```

TABLE 13.2   (*continued*)

```
*
* include all resistor models and active SPICE parameter files
*
. inc res.mod
. inc m414.mod
*
.end
```

Compared to a linear program such as Ansoft Designer Suite there are some restrictions:

1. There is no optimizer.
2. As the program is a time-domain-only simulator, it is much slower than the frequency-domain approach, and the execution speed depends on the value of the components.
3. Most needed passive microwave elements are missing.

Table 13.2 shows a typical input form for a SPICE program. Note the data required for describing the bipolar transistor and the FET. To overcome these disadvantages, the harmonic balance method was created. An introduction to this that combines the best of the time- and frequency-domain techniques is given later.

The rest of the chapter is broken down into a series of sections that introduce new CAD-related techniques:

13.2 Introduction to foundry services and CAD
13.3 Introduction to field optimization
13.4 Introduction to the harmonic balance method
13.5 Load-pull technique using programmable microwave tuners
13.6 Introduction to MIMIC considering layout effects
13.7 Introduction to layout-related problems
13.8 Practical design examples and examples for CAD software

13.2   GALLIUM ARSENIDE MMIC FOUNDRIES: ROLE OF CAD

A GaAs MMIC foundry produces circuits to customer designs. MMICs are microwave circuits, such as switches, amplifiers, and receivers, which are integrated within one die. This requires the technology to supply low-noise and power FETs, resistors, capacitors, inductors, transmission lines, diodes, and so on. Not only must these components be available to the designer, but they must be highly reproducible and have accurate dc and microwave models. The FET technology, in particular, is critical to the high-frequency performance that can be achieved. Today, foundries typically produce FETs that operate to well over 20 GHz and feature minimum sizes of 0.3 μm, requiring the use of deep ultraviolet or electron-beam lithography.

To design MMICs successfully, a number of important items must be supplied by the foundry:

1. Well-controlled (fixed) IC process(es)
2. Extensive MMIC component characterizations
3. A design manual
4. A standard components library with data and layout tape
5. Wafer qualification procedures
6. Recommended CAD software and hardware configurations
7. Support engineering during the customer design cycle

For a foundry to be successful, its MMIC process must be well controlled, reproducible, documented, and of high quality. To do this, the foundry must have characterized the dc and RF performance of a large number of standard components and their variations with voltage, temperature, and so on. Also, statistical data are needed in the form of means and standard deviations for the component parameters. These data are important, as MMIC designers need to be able to predict circuit performance spreads since, unlike conventional hybrid circuits, MMICs are not easy to adjust in performance after they have been processed.

Figures 13.4 and 13.5 illustrate the standard layouts of a 0.3-μm FET and square spiral inductor, respectively. Figure 13.6 is a scanning electron micrograph (SEM) of the inductor. By using data from a design manual and the standard components or derivatives of them, circuits can be designed to meet particular specifications. During this process the foundry usually provides support engineering, since technical questions that may be unique to particular requirements and not covered by the design manual need to be answered. Support engineering continues until circuit layouts have been
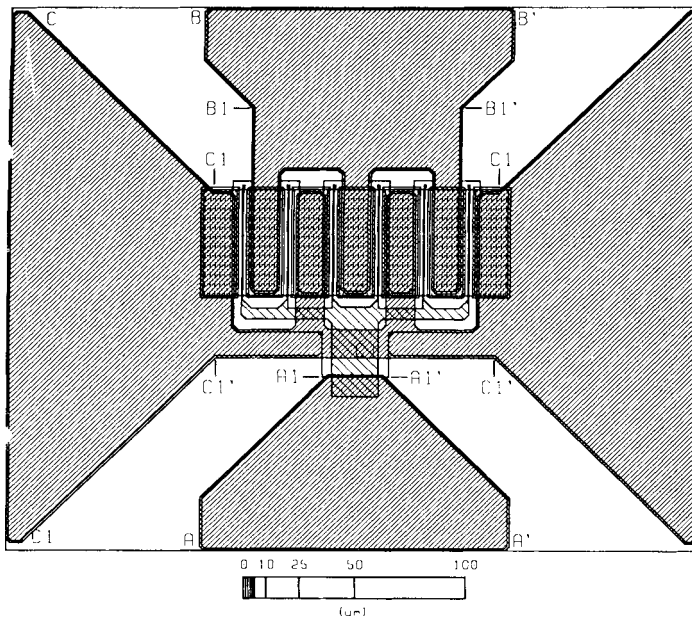
FIGURE 13.4   Standard 0.3-μm gate length FET layout.
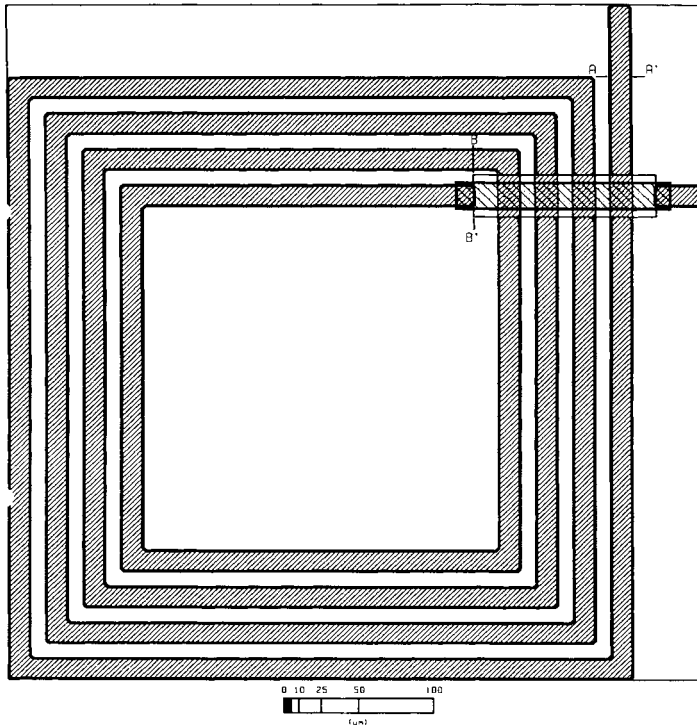
FIGURE 13.5   Standard four-turn spiral inductor layout.
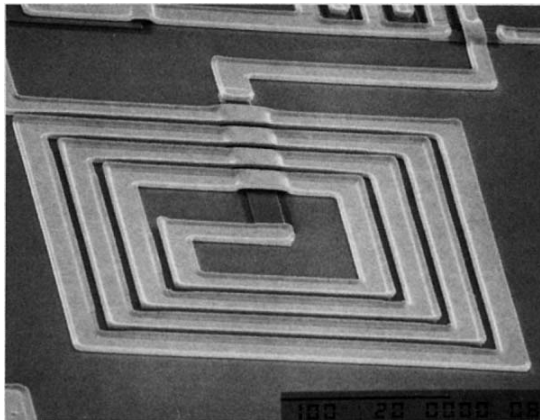
FIGURE 13.6   Scanning electron micrograph of a four-turn inductor.

completed. Prior to design release, the foundry will check the layout for layer design rule errors and may even check the microwave CAD data files. After design release the masks are procured, the MMIC fabrication completed, and a number of qualification tests made on the wafer lot.

The role of CAD in the design cycle is vitally important. Without modern analysis and optimization tools, MMIC design would be very nearly impossible and, at best,
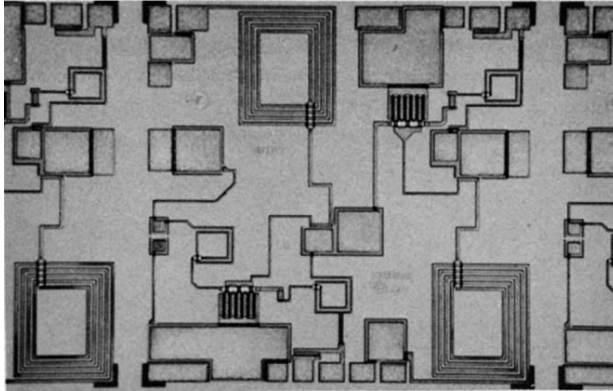
FIGURE 13.7   Microphotograph of a 2- to 8-GHz MMIC amplifier.

very time consuming! As an example, consider the circuit in Figure 13.7. This is a microphotograph of a 1×1.5-mm 2- to 8-GHz amplifier having 15 dB of gain and 100 mW of output power. It is a simple circuit but typical of today's MMIC foundry circuit complexity. The circuit contains 2 FETs, 11 capacitors, 6 resistors, 5 spiral inductors, 16 transmission lines, and 15 bond pads. The analysis data file for this IC, however, contains 125 data lines, with a typical analysis time on a standard IBM AT PC computer with math coprocessor of 4 minutes. The analysis file is complex because it includes a number of models for monolithic components such as thin-film resistors, inductors, and so on. Analysis and optimization programs are only just starting to put MMIC component models into their routines.

A foundry can use a mixture of their own models and some standard ones. Sometimes these standard models are not sufficient because they do not relate directly to the particular foundry process. One way around this is for the foundry to work with a software developer to produce models and data-bank information that will allow analysis to be more efficient and accurate.

Circuit analysis and optimization such as described above can be achieved more efficiently by "pulling" models from a data bank and saving the foundry user the time needed to generate them initially and the computer the time taken to analyze them. To avoid limitations in this approach during optimization, closed-form equations are needed to allow automatic calculation of full component parameters.

Software such as Linmic+ is available to model more accurately such components as inductors and transformers, and any coupling effects between them can be accounted for. This allows the packing density of MMICs to be increased, which directly affects die costs. This would also allow the generation of the closed-form equations mentioned above without forcing the foundry to go through the time-consuming, tedious, and expensive tasks of component fabrication, test, and modeling.

Of increasing importance to users of foundry services is the need to be able to investigate circuit response as a function of temperature and FET or diode bias currents and voltages. Traditionally, this has been achievable on a computer only by using SPICE, where the accuracy of the simulation is limited by the active component models. However, by introducing bias- and temperature-dependent S parameters into a modern linear analysis program, the designer can quantify these important effects. To be usable,

however, this needs to be done in a complete way. It is necessary, for example, to have temperature coefficients for all components. Many of these effects are technology dependent and therefore need to form part of the foundry data bank.

Many foundry users need to develop nonlinear circuits, such as oscillators, multipliers, and mixers for receivers and power amplifiers for transmitters. Traditionally, the characterization of large-signal models for FETs, diodes, and so on, has been very time consuming and, until recently, only approximate. Equally, the CAD base to the general microwave community for nonlinear analysis has been poor. The need for foundries to supply accurate large-signal bias-dependent models is as important as the need for an efficient, general-purpose nonlinear analysis and optimization program. By introducing the concept of a load-pull tuner for characterization of large-signal performance of active devices (see Section 13.3) and using the Microwave Harmonica program, a program based on the harmonic balance method (Compact Software, Inc.), both needs are now being met and improved MMIC designs are effected.

13.3   YIELD-DRIVEN DESIGN

The ability to produce low-cost MMICs in large quantities will be significantly enhanced by the microwave and millimeter-wave integrated circuit (MIMIC) program, sponsored by the Department of Defense. Not only has it provided manufacturers with the incentive to speed research and development, but it has created a need for a higher level of computer-aided design, with all operations from design to fabrication integrated into a single interactive package.

A missing link has been the ability to design circuits for maximum yield when element tolerances are considered. A major step toward realization of that goal was taken by Compact Software in its role as a member of the Raytheon/Texas Instruments MIMIC team. It performed tolerance analysis (yield optimization) and accurate assessments of the yield of MMICs across a wafer.

The technique is a significant departure from the traditional manner in which MMICs are designed or, for that matter, the way microwave circuits in general are designed and constructed. It incorporates a range of tolerances rather than using rigid values for circuit elements. Think of it as fine versus coarse tuning.

The current manner in which circuits are designed using microwave CAE strives for optimum performance at the expense of yield. The new approach strives for performance within an acceptable range that is compatible with optimum yield; that is, performance criteria are met while keeping cost down. It is this "real-world" approach that is demanded by the requirements of the MIMIC program: high-volume low-cost circuits, with acceptable performance.

13.3.1   No Simple Task

Yield optimization is a complex task and was previously unavailable to the MMIC designed. It is actually an old concept, having been proposed by John Bandler more than 10 years ago. It bears close scrutiny. The concept was first proposed for MMIC design by Robert A. Pucel at the 1984 GaAs IC Symposium.

Pucel concluded that since the optimization routines used in all commercial CAE software do not include the variability of commercial passive and active components in

their analysis, the process is better suited to the research and development environment rather than to commercial production, where manufacturing yield is important.

The present method of CAE cannot guarantee that the optimized design will yield the lowest spread in performance for the given range of tolerance. It is inadequate for MMIC design and will not readily lead to circuit designs or topologies with the highest design yield.

The variations in performance inherent in any device used in a microwave circuit generally require that "tweaking" take place after the circuit is fabricated. Tweaking is not convenient for MMICs, but even if it were, it would not be desirable. Ideally, to achieve the goal of acceptable performance as well as optimum yield, the customer should allow the manufacturer a range of performance to which the delivered part can conform and still meet system requirements.

Manufacturers must have in their CAE program a database of reliable information on the components used in the MMICs. This is especially critical for active devices, which are always the components with the highest degree of uncertainty. The database must include tolerance data, accompanying statistics, and probability distribution.

13.3.2 Rethinking Design

Yield optimization requires a change in the design process. Rather than optimizing a circuit for best performance using one set of device values, the tolerance data are used for optimization, in a process called "design centering," a phrase attributable to Bandler.

We can illustrate this process using a graph. For the sake of simplicity, assume that the range of acceptable performance (Fig. 13.8) allows only two element values (P_1 and P_2) to be varied. In the current CAE design process, only a fixed set of values can be used to optimize the circuit for maximum performance, with no regard for element tolerances.

It is more likely that more than one set of element values will be permissible if a "window" of acceptable performance is specified rather than a best-possible performance, thus allowing element tolerances. These sets of element values can be represented on a graph by defining the entire region of possibility (Fig. 13.9). This "element constraint region" consists of all possible element combinations that will yield performance within the acceptable range.
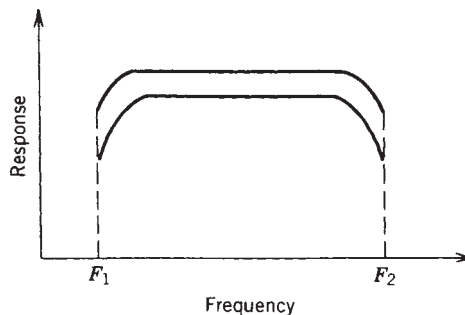
FIGURE 13.8   This range of acceptable performance represents a "window" whose limits represent acceptable performance from the customer's standpoint.
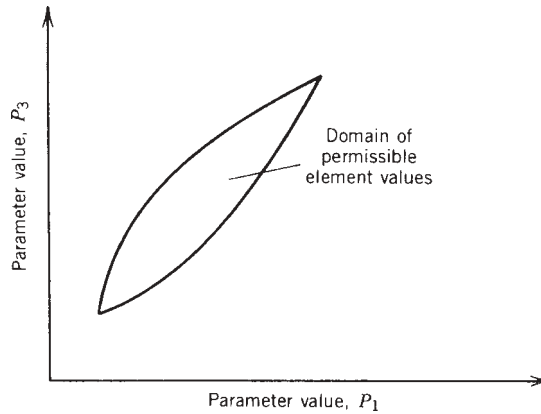
FIGURE 13.9   The permissible element values will provide performance defined as acceptable in Figure 13.8.
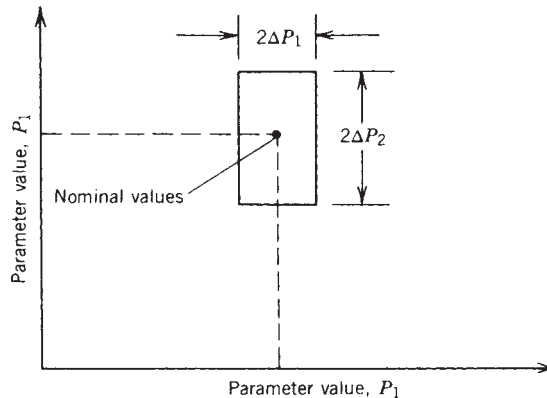
FIGURE 13.10   The rectangular area is the tolerances of circuit elements distributed around a nominal value.

Taking this one step further, we add tolerances to elements P_1 and P_2 and assume that they are distributed about some nominal value for each pair. This tolerance condition can be depicted by a rectangle (Fig. 13.10), within which is the tolerance of any pair of element values. The probability that any combination of elements values is in the area of the rectangle is inversely proportional to the area of the rectangle. By superimposing the tolerance rectangle over the element constraint region (Fig. 13.11) for some arbitrary choice of nominal values of P_1 and P_2, the number of circuits that will satisfy the performance window will be proportional to the fraction of the rectangle area that falls within the element constraint region.

13.3.3   Hitting the Mark

Thus, if the element values are chosen correctly, the design yield can be optimized more accurately. In the example shown (Fig. 13.12), the overlap in the tolerance rectangle
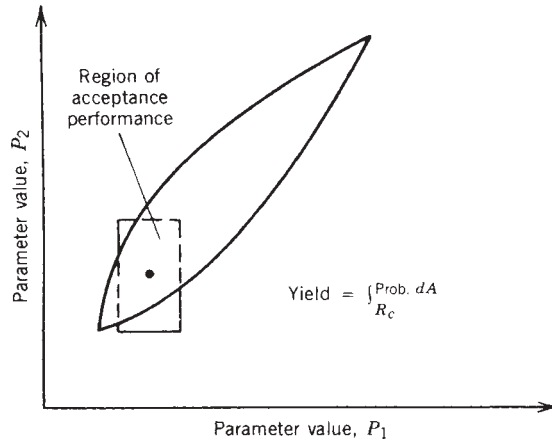
FIGURE 13.11 Yield is determined by superimposing the tolerance rectangle of Figure 13.10 over the area of acceptable element values. The yield is proportional to the amount of rectangle that falls within the acceptable element value region.
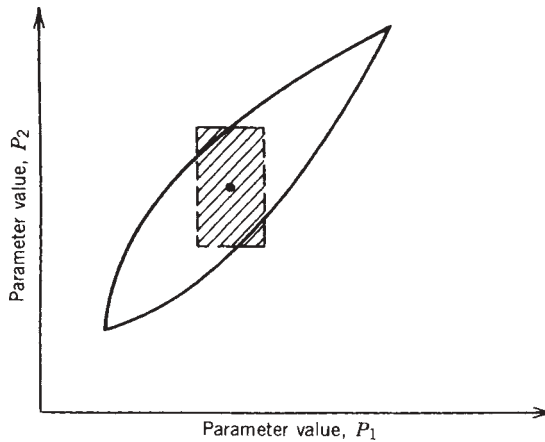
FIGURE 13.12 If element values are chosen carefully, yield can be maximized. This illustration represents that condition.

and element constraint region is maximum. Of course, by loosening the performance window or reducing tolerances, 100% yield can be achieved (Fig. 13.13).

This method, which could be called the "cost-driven" approach, is much more realistic than the "performance-driven" approach. It is intrinsically attuned to what the MMIC manufacturer will encounter in the real world, that is, assuming variability in device performance.

It is important to remember that design yield has been determined in advance of production. No wafers have been fabricated. With the cost of one pass through the foundry at approximately $50,000, this is an extraordinary saving in time, material, and processing costs. It is also possible to determine at this early stage that the circuit topology chosen is inappropriate for production, which reaps additional benefits.
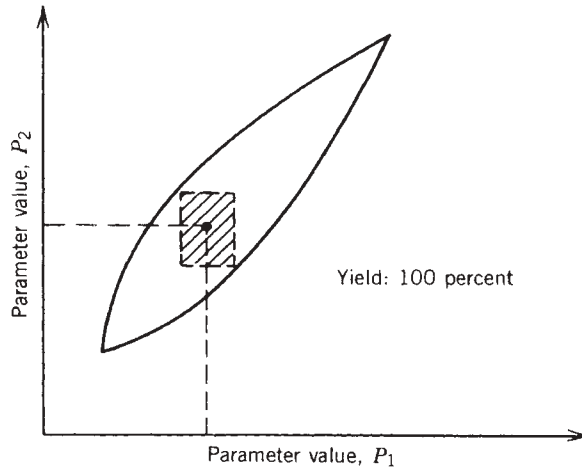
FIGURE 13.13 By relaxing the range of acceptance or tightening tolerance, 100% yield can be achieved.

13.4 DESIGNING NONLINEAR CIRCUITS USING THE HARMONIC BALANCE METHOD

The use of nonlinear components such as bipolar transistors, GaAs FETs, and microwave diodes makes it necessary to predict large signal-handling performance. The traditional tools to do this were the SPICE approach and Volterra series expansion.

The SPICE program is a program operating solely in the time domain. SPICE is an outstanding workhorse for dc analysis as a function of bias and temperature and transient analysis. The drawbacks of SPICE are (1) the lack of an optimizer; (2) the lack of distributed elements such as tee junctions, crosses, and others; and (3) the slow execution speed related to the time-domain approach.

Another approach that has been tried is Volterra series expansion. This approach is a simulation where the actual computation time is somewhat independent of the values of the components used in a circuit. However, once the number of harmonics goes up, Volterra series expansion also becomes very time consuming. The Volterra series can be regarded as a nonlinear generalization of the familiar convolution integral. The Volterra series also has the limitation that the degree of nonlinearity must be mild, as the representation otherwise requires an intractably large number of details for adequate modeling.

The recently developed harmonic balance method avoids many of the time-consuming mathematical approaches mentioned previously. This method is a hybrid time- and frequency-domain approach which allows all the advantages of a time-domain device model, combined with the strength of the steady-state frequency-domain technique, to be presented in the lumped and distributed circuit elements in which the device is embedded. The time-domain model can be completely general, thus bypassing complicated determination of coefficients by curve fitting over different bias levels.

As introduced originally, the harmonic balance method is a "single-tone" method that cannot handle the more general case of nonlinearities such as mixers. To handle

the multitone aspect, a modified harmonic balance method has been created and multidimensional Fourier transforms have been implemented. A variety of attempts have been made at accurate modeling of the FET including work by Madjar and Rosenbaum, Curtice, Sussman-Fort, and many others.

13.4.1 Splitting the Linear and Nonlinear Portion

The key concept in the harmonic balance method is to take advantage of a linear program such as Super-Compact that handles all the microwave components accurately. The microstrip and stripline discontinuities are of greatest interest. This calculation is done in the frequency domain and thus is fast and efficient. An interface is required which then hands over the information to the nonlinear portion of the program, which uses the harmonic balance method, being computed in the time domain.

Figure 13.14 shows a complete FET model which is separated into an external portion, the parasitics, and the nonlinear model. If we assume that all elements marked with a Z are distributed elements, it becomes obvious that we need a microwave program that handles the transmission lines, a portion that can handle the lumped elements, and a program that can handle the nonlinearities. Figure 13.15 shows the separation between the frequency-domain and time-domain portions.

13.4.2 How Does the Program Work?

For a fixed circuit topology (analysis case), the frequency domain is passed through only once; the admittance matrix of the linear subnetwork is computed and stored for subsequent use. Figure 13.16 shows the harmonic balance flowchart. In the time-domain path, the state-variable harmonics are first used to compute the corresponding time-domain waveforms. As mentioned earlier, these are fed to nonlinear device equipment to produce the time-domain device port voltages and currents. Voltage and current harmonics are then described by one- or two-dimensional fast Fourier transforms (FFTs) for the cases of single-tone and two-tone excitation, respectively. The voltage harmonics are used to generate "linear" current harmonics via the linear subnetwork admittance matrix. The two sets of current harmonics are finally compared to produce individual harmonic balance errors and a combined (global) harmonic balance error to be used in a convergence test.

In well-conditioned cases (e.g., FET circuits), a standard Newton–Raphson iteration may be used successfully as an update mechanism even though no starting-point information is available (i.e., if zero initial values are assumed for all harmonics). In such cases the harmonic balance errors are used via a simple perturbation mechanism to generate a Jacobian matrix. The latter is then inverted and applied to the error vector to generate the updated harmonic vectors. The algorithm is fast and accurate.

For circuits containing strongly nonlinear devices such as microwave diodes, a simple Newton iteration may sometimes fail to converge. To overcome this difficulty, Microwave Harmonica incorporates a second iteration scheme based on a variable metric algorithm (quasi-Newton iteration), which is slower although considerably more robust than the regular Newton method.

In ill-conditioned cases, the quasi-Newton iteration may be used to approach the required solution. After this has been done to a satisfactory extent, automatic switchover to Newton iteration takes place, so that the approach solution can quickly be refined to any desired accuracy.
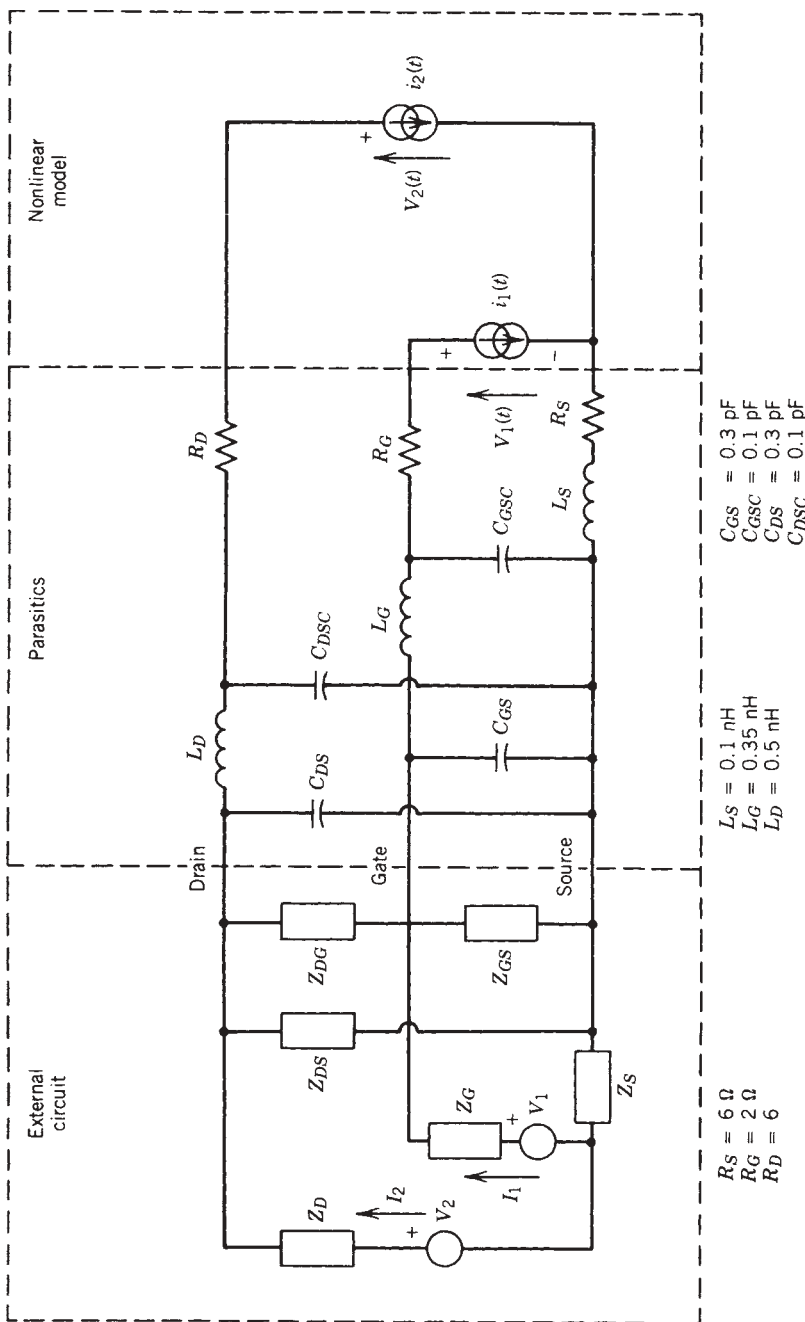
FIGURE 13.14 Complete FET model showing nonlinear/linear circuit, external circuit, and parasitics used to model NEC-72089.

$$R_S = 6\ \Omega$$
$$R_G = 2\ \Omega$$
$$R_D = 6$$

$$L_S = 0.1\ \text{nH}$$
$$L_G = 0.35\ \text{nH}$$
$$L_D = 0.5\ \text{nH}$$

$$C_{GS} = 0.3\ \text{pF}$$
$$C_{GSC} = 0.1\ \text{pF}$$
$$C_{DS} = 0.3\ \text{pF}$$
$$C_{DSC} = 0.1\ \text{pF}$$

Standard Harmonic Balance
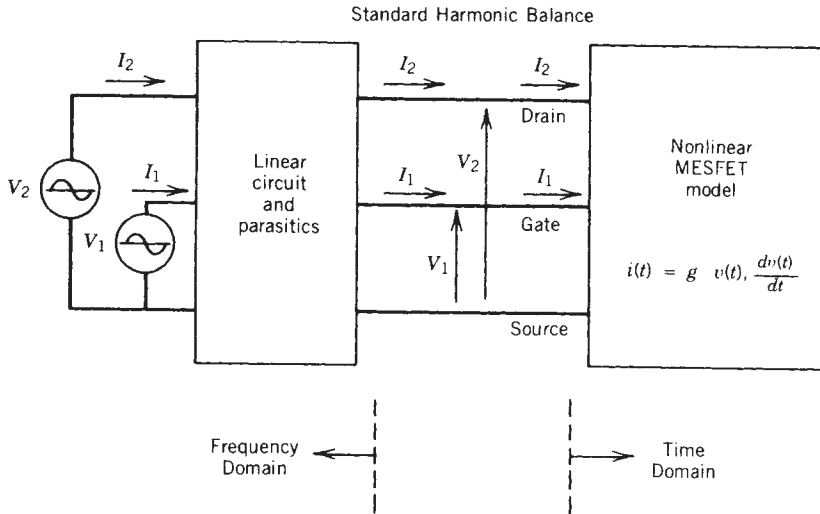
FIGURE 13.15 Partitioned MESFET circuit. Applied gate and drain voltages and relevant terminal voltages and currents are indicated.
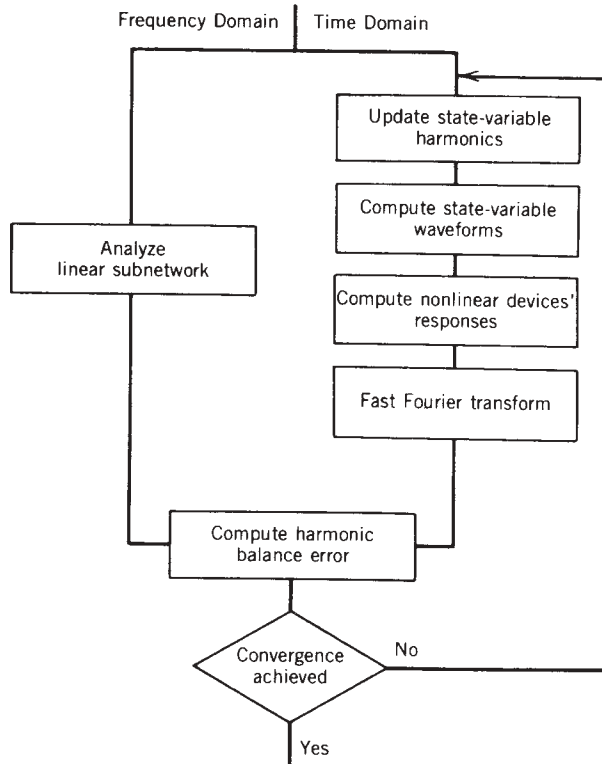
FIGURE 13.16 Flowchart of harmonic balance analysis.
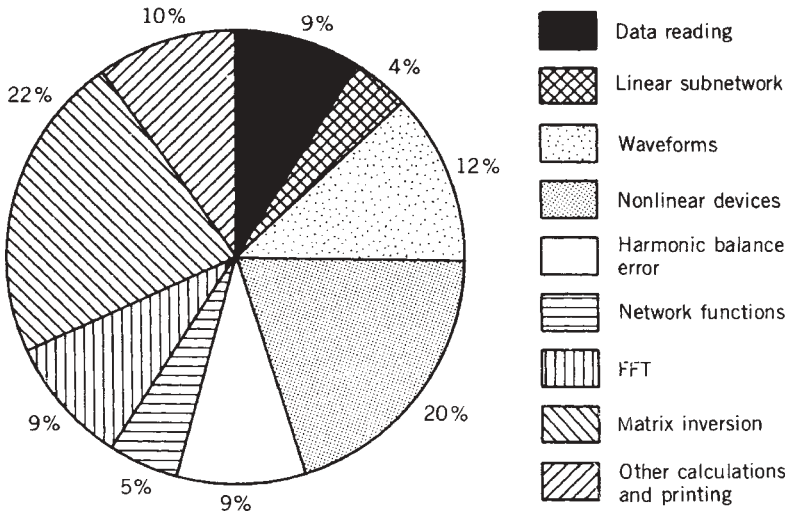
FIGURE 13.17 Analysis of a single-ended FET mixer. Overall computation time 12.9 s (VAX 8800).

Timing information pertaining to the analysis of a single-ended FET mixer is given in Figure 13.17. When circuit optimization is requested, the algorithm flowchart is modified. Harmonic balance errors are computed in the same way, but now the variable circuit parameters are also updated and the linear subnetwork admittance is computed at each iteration. An objective function is defined as a combination of harmonic balance error and a contribution arising from the electrical specifications. Such an objective is then minimized by the variable metric algorithm until a minimum close enough to zero is reached. Circuit parameters and state-variable harmonics are updated simultaneously, thus avoiding the nesting of nonlinear analysis and circuit optimization loops. Microwave Harmonica is a general tool using the harmonic balance method for microwave. The harmonic balance method is a generic mathematical approach and its use in a commercial CAD software is a first. Today the program of interest is Ansoft's Designer.

We mentioned earlier that there are cases where we mix linear and nonlinear components, and as the number of active devices and frequency points increase, the overall speed requirement and program size become an issue. At Compact Software we are looking at both PC-based and mainframe-based versions. In the case of the mainframe, we wanted to make sure that all mainframes that support Fortran 77 can handle the software and that it can be run on the largest machine (or rather, the fastest).

Figure 13.18 shows a plot diagram by which either a VAX or a Cray computer can be addressed. In the PC environment, a nice graphics interface has been developed to provide output information from the simulator. Figure 13.19 shows the FET curves, Figure 13.20 shows the output waveforms as a function of time, and Figure 13.21 shows the output level as a function of the input level for different harmonics.

Library Functions The program has a large library of components, both idealized and microstrip.
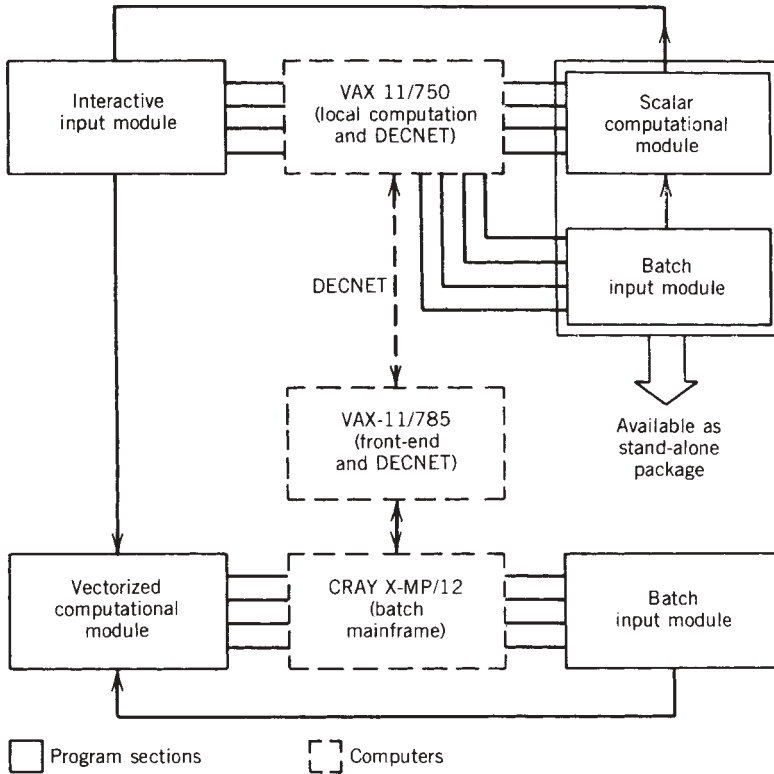
FIGURE 13.18   Block diagram of the software package and a typical computer system used to run it.
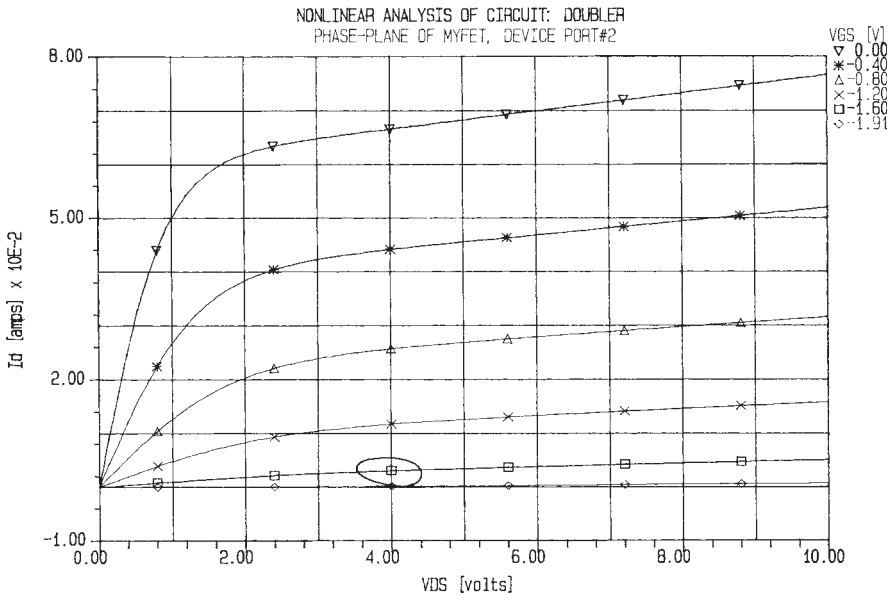
FIGURE 13.19   FET curves.
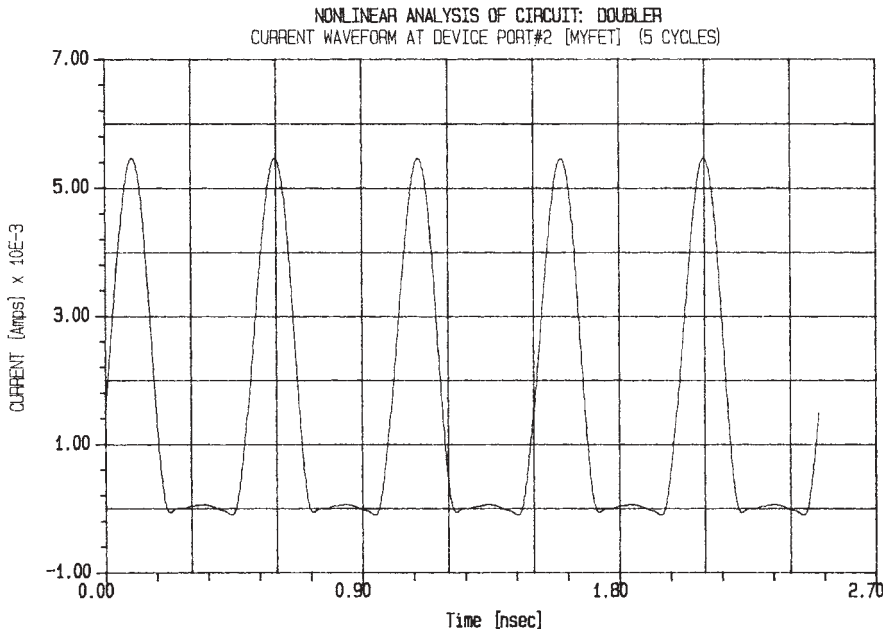
FIGURE 13.20   Output waveforms as a function of time.
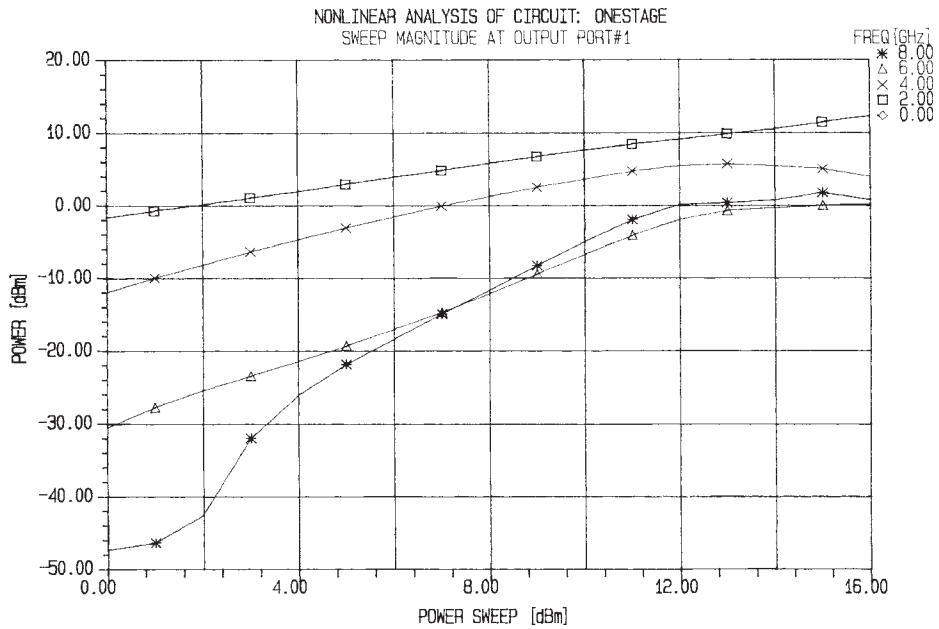
FIGURE 13.21   Output level as a function of input level for different harmonics.

Idealized Components

Series-connected *RLC* one-port
Parallel-connected *RLC* one-port
Two- or three-port transformer
Voltage-dependent voltage source (including delay)
Current-dependent voltage source (including delay)
Voltage-dependent current source (including delay)
Current-dependent current source (including delay)
Loss-free TEM line section
Short-circuited loss-free TEM line stub
Open-circuited loss-free TEM line stub
Loss-free symmetric TEM coupled-line section

Microstrip Components

Fringing capacitance of microstrip open end
Parasitics of microstrip impedance step
Right-angle microstrip bend
Compensated right-angle microstrip bend
Microstrip tee junction
Microstrip cross junction
Uniform microstrip section, lossy and dispersive
Short-circuited microstrip stub, lossy and dispersive
Open-circuited microstrip stub, lossy and dispersive, including open-end correction
Symmetric coupled-microstrip section, lossy and dispersive
Array of coupled microstrip lines of unequal widths and spacings, lossy and dispersive, using a simplified implementation of the spectral-domain approach
Rectangular microstrip resonator
Uniform microstrip section coupled to dielectric resonator

All microstrip components are described by state-of-the-art models. They are defined by means of geometrical data such as microstrip widths and lengths and share a number of parameters related to their fabrication technology. These parameters, which may be input separately, include substrate thickness, dielectric constant, loss tangent, and roughness. Their values are taken into account in the calculations.

In addition, the program accepts any number of "measured" (i.e., a priori known) linear components described by a frequency-dependent impedance, admittance, or scattering matrix. Interpolation of input data is carried out by the program automatically whenever necessary. Finally, users can input any set of arbitrarily self-defined models to create their own technology-dependent libraries.

The description of the linear subnetwork comprises both the RF and bias circuits, including all free sources, in a unique circuit file. Any physical or electrical parameter may be selected as a variable to be optimized. A unique feature of this package is that

the bias source voltages are also optimizable, so that the user can ask the program to choose the best bias conditions for the nonlinear devices.

The specification of design goals marks one of the essential differences between linear and nonlinear optimization. In the linear case, a network function is simply an algebraic consequence of the scattering parameters. On the other hand, to compute the performance of a nonlinear network, the actual steady-state regime must be completely known since the network functions can be obtained only from the voltage and current harmonics at the circuit ports. This increased complication is handled completely by the program; it requires no special efforts by the user. A menu of optimizable network functions is available. This includes all of the most common performance indexes of nonlinear circuits:

1. The output power from a given port at any harmonic
2. The spectral purity of the output signal at a specified harmonic from a given port
3. The return loss at any port connected with a free RF source
4. The power transfer efficiency from the dc bias sources to the output signal at a given port and harmonic
5. The transducer gain between given input and output ports at specified harmonics
6. The power-added efficiency between given input and output ports

Any of these functions can be specified arbitrarily or simply monitored throughout the optimization. The program associated with each function identifies a set of operations on voltage and current harmonics at the relevant network ports, which is utilized to compute the required function automatically.

13.4.3 Examples

In conventional CAD programs, analysis and optimization were centered around a variation of components used to match active devices. Since these devices are assumed to be linear and/or memoryless, optimization was independent of the level of operation. Microwave Harmonica takes into consideration nonlinear modeling and thus deals with the problem of optimizing the circuit not only as a function of frequency but also as a function of drive level. This required the development of totally new optimization techniques. A typical example is provided by nonlinear circuits having multiple operating points, such as the frequency divider, whose hysteresis cycle is displayed in Figure 13.22. At an input power level P, this circuit will have three operating points, a, b, and c. Analyzing the circuit starting from zero harmonics will lead to point a. Constraining the analysis properly makes sure that all possible operating points can always be found in a short number of turns.

Another important application is the active microstrip frequency multiplier shown in Figure 13.23. The harmonic balance analysis provides information about the magnitude of the drain voltage harmonics. The correct solution is found after approximately 70 iterations. Figures 13.24 and 13.25 show the magnitudes and phases of these harmonics, illustrating the fact that their proper values are reached after approximately 70 iterations. The rapid convergence for both analysis and optimization can be expressed as the error function shown in Figure 13.26.
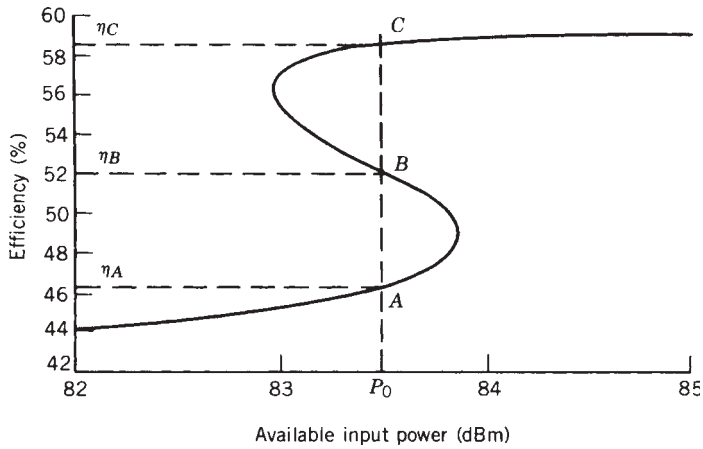
FIGURE 13.22 Hysteresis cycle of a microstrip parametric frequency divider.
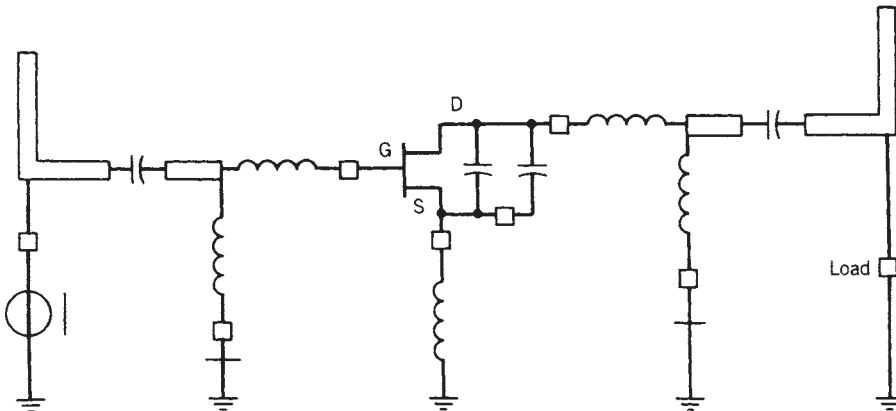
FIGURE 13.23 Schematic representation of an active microstrip frequency multiplier.

Many more applications are possible. Figure 13.27 shows a comparison of measured response versus the harmonic balance approach for a monolithic VCO. The conduction current waveforms through the source reactor of the VCO can be predicted (see Fig. 13.28). Finally, the FET harmonic mixer shown in Figure 13.29 was analyzed. The resulting drain voltage spectrum for the mixer (Fig. 13.30) provides all the necessary information about its operation.

13.5 PROGRAMMABLE MICROWAVE TUNING SYSTEM

The Programmable Microwave Tuning System, developed by the David Sarnoff Research Center, provides a unique new measurement system that performs a variety of automatic microwave tuning and device characterization procedures.
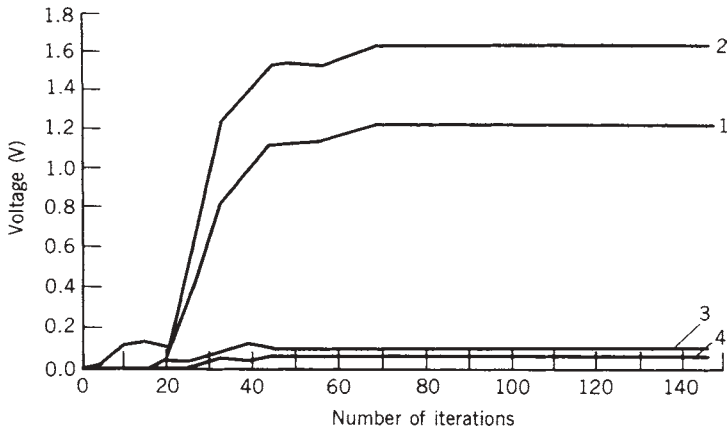
FIGURE 13.24   Harmonic balance analysis of the circuit in Figure 13.23. Magnitudes of the drain voltage harmonics versus the number of iterations.
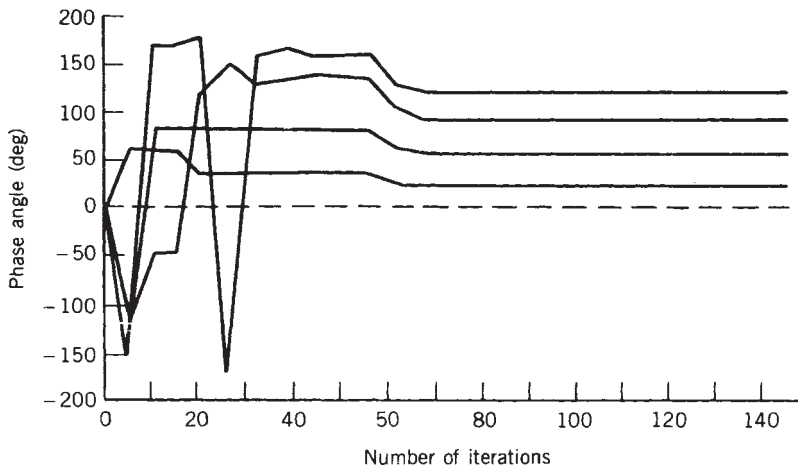
FIGURE 13.25   Harmonic balance analysis of the circuit in Figure 13.23.

13.5.1   The PMT System

The Programmable Microwave Tuner System (PMTS) is a computer-controlled state of-the-art method of dynamically testing microwave circuits under full-power conditions while automatically varying the load and/or source impedance. When used as an interface to the appropriate peripheral equipment (RF source, power meters, noise figure meter, etc.), this system greatly simplifies active-device characterization by providing accurate and repeatable measurements. When coupled with a host computer running the PMT application software, the system can be directed optimally to seek either a specific impedance point that maximizes (or minimizes) a measurable parameter (e.g., peak output power, maximum efficiency, minimum noise) or a family of impedance points that satisfy specific criteria (e.g., constant output power, constant efficiency, or a constant noise figure).
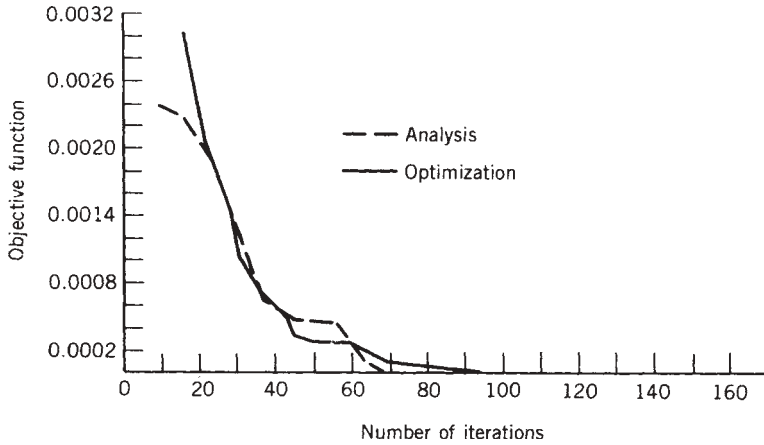
FIGURE 13.26   Dependence of the objective function on the number of iterations for an analysis and an optimization of the circuit in Figure 13.23.
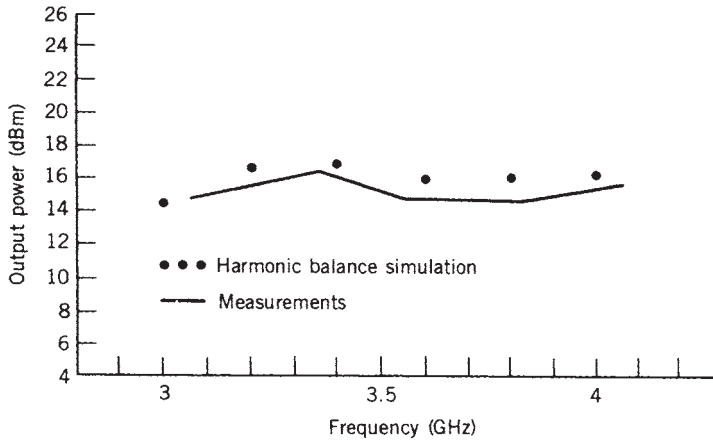
FIGURE 13.27   Output power of monolithic VCO.

The PMTS provides an arbitrary impedance to circuits and measures their responses. This is accomplished by a combination of precision hardware and software—no network analyzer is required. The PMTS software combines equivalent-circuit models and sophisticated search algorithms to characterize the load- and source-pull characteristics of a device or circuit with respect to power, efficiency, and noise figure. It obviates the need to precharacterize at discrete impedance points using a network analyzer system.

13.5.2   Tuning Techniques

Maximum power transfer between an RF source and a load is obtained when the complex-load impedance is the conjugate of the complex-source impedance. If an active device is placed between the source and load, the input and output impedances must be conjugately matched simultaneously.
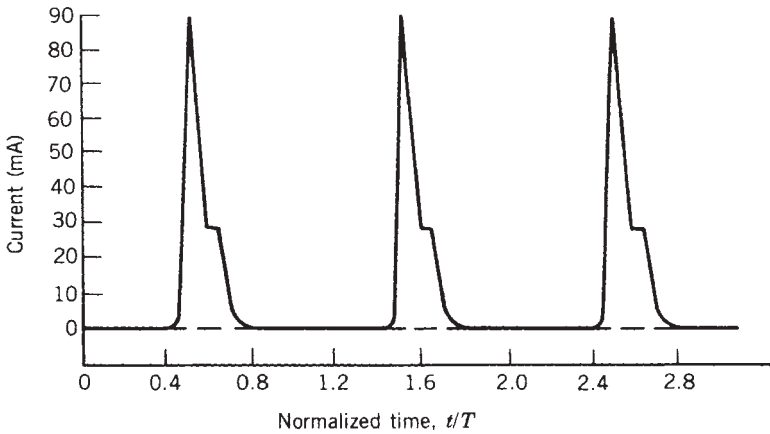
FIGURE 13.28 Conduction current waveform through the source varactor of a monolithic VCO.
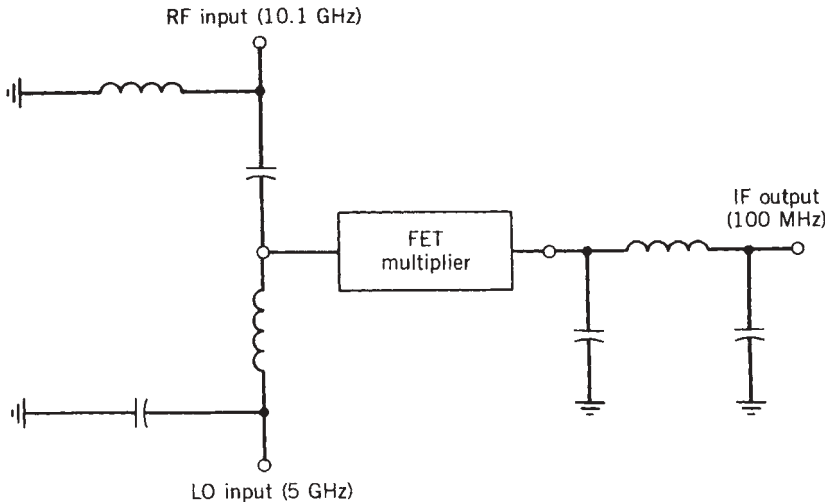
FIGURE 13.29 Schematic diagram of an FET harmonic mixer.

Before automatic vector network analyzers made impedance measurements routine, microwave engineers would place tuners before and after their circuit and simply "diddle" the tuners for maximum output power. After the tuners were adjusted properly, the impedance of each was determined by using a slotted line. This technique was repeated for other frequencies in the range of interest. In the case of linear small-signal circuits, such tuning procedures are no longer necessary. Modern CAD programs can synthesize matching networks analytically using the measured or modeled network parameters of the circuit (S, Y, or Z) parameters and the source and load impedances. Although tuners are no longer needed in the design of small-signal linear amplifiers, they are still required in the design of low-noise circuits, nonlinear circuits, and even large-signal linear circuits.
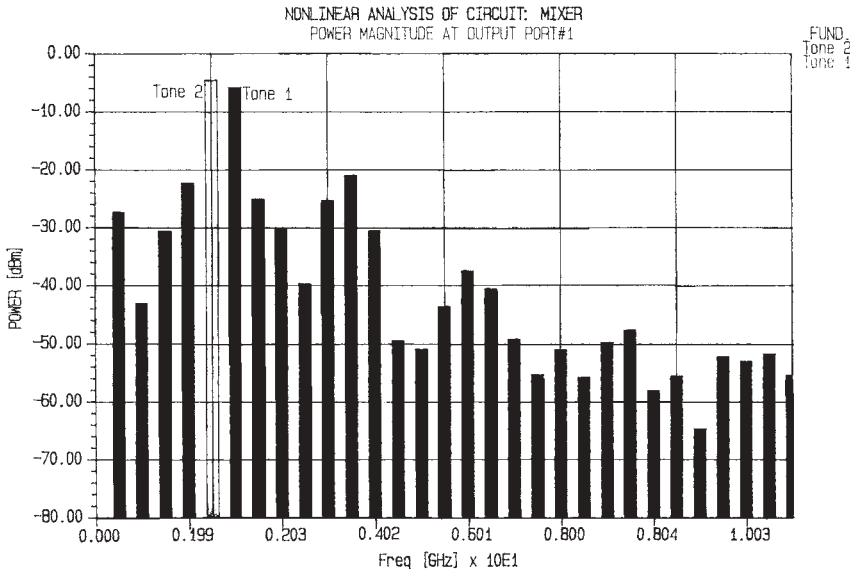
FIGURE 13.30   Drain voltage spectrum for the mixer in Figure 13.29.

When designing low-noise-amplifier matching networks, the proper impedance needed for optimum input noise match is independent of the device's network parameters. It can be determined by placing a tuner on the input of the device and adjusting the tuner for the minimum noise figure. An indirect measurement technique can also be used in which the noise figure is measured for several different known impedances at the input of the device. These data are then used to calculate the noise parameters of the device: the minimum noise figure, the source impedance for minimum noise figure, and the equivalent noise resistance. These parameters allow the circuit designer to compute the noise figure for any arbitrary source impedance.

Large-signal designs also require terminating impedances which cannot be determined from the linear network parameters. The most effective technique for determining the required matching network is to place a tuner on the output of the device and tune it for maximum (or some target) power. Information on how the output power, efficiency, and distortion vary with load impedance and frequency is usually needed to design the optimum matching network. Such load-pull data require further tuner measurements.

13.5.3   The PMTS Approach

The most apparent problem when using a manual tuner is the enormous amount of time required to obtain results. Each data point requires manual adjustment of the tuner to obtain the desired performance and then removal of the tuner and measurement of its impedance on a network analyzer. If the tuner's loss is taken into account, which should be done for accurate results, all four S parameters must be measured and the desired response (noise figure, output power, efficiency, etc.) recalculated. The results may not be correct even when this procedure for calculating loss is followed since the measured parameter cannot be corrected for tuner loss until after the tuner is
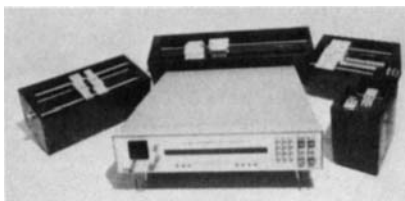
FIGURE 13.31   PMTS system hardware components.

measured. The PMT system overcomes such difficulties by incorporating the following components: (1) a family of programmable tuners, (2) a programmable tuner controller, and (3) application software that provides tuner control, optimization procedures, and data manipulation routines. Figure 13.31 shows the system hardware components.

Tuner   Tuners are available to cover the frequency range 400 MHz to 26.5 GHz. Each is built around a slotted transmission line section fitted with two low-impedance elements (slugs) riding on the center conductor. The tuners are designed to achieve a minimum VSWR of approximately 10 : 1 over an octave bandwidth. High-precision stepper motors and zero-backlash ball screw assemblies provide extremely precise slug positioning anywhere along the line. PMTS incorporates an electrical model of the tuner in the control software. Each tuner is precisely characterized over its entire bandwidth/tuning range. The characterization data are stored in a microprocessor chip within each tuner and read on demand by the tuner controller.

Programmable Tuner Controller   The PTC-8700 tuner controller provides a full-function instrument for controlling up to two programmable tuners and interacting with the host computer running the PMT application software. The front panel consists of a high-resolution alphanumeric display panel, a function/data-entry keyboard, and a joystick tuning control lever. The joystick is used for manual control of the tuner. In the automatic mode of operation, the PTC-8700 communicates with a host computer running the PMT software. System messages appear on the alphanumeric display and the front-panel keyboard provides for operator interaction. Keyboard functions include setting the operating frequency and measurement reference planes as well as setting the tuner impedance.

PMT Software   The tuners and PTC-8700 act together in accordance with commands from the PMT application software and provide any arbitrary impedance value anywhere in a particular tuner's VSWR/frequency range. As its basic function, PMT translates any desired impedance request into tuner settings and, conversely, determines the impedance corresponding to any tuner setting. In addition to controlling the tuner itself, the software can measure the gain of a device using programmable power meters, determine the noise figure using a programmable noise figure meter, measure bias voltage and currents via a data acquisition unit, and provide graphical output on a CRT or plotter.

By combining the capability to control test instrumentation along with the ability to "synthesize" an impedance accurately, a variety of high-level measurement procedures can now be performed quickly and easily. The PMTS can determine the impedance that produces the maximum output power or can determine (and plot/display) the
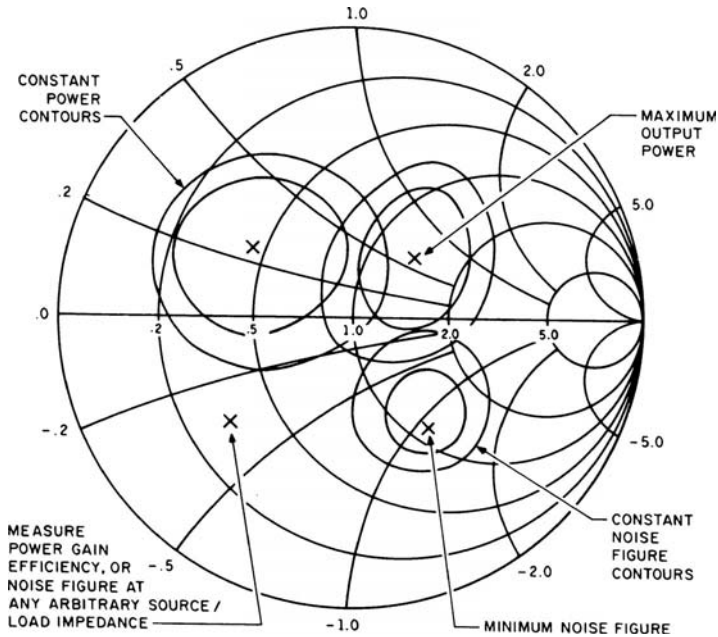
FIGURE 13.32   Graphical representation of the PMT measurement data includes constant-power and noise figure contours.

locus of all impedance points that provide a specified output power (constant-power contours). Similar functions can be performed for efficiency and noise. The PMTS determines performance contours and operating points by actually presenting the device with impedances, the selection of which is guided by the measured device response and the optimized search algorithms incorporated into PMT. Figure 13.32 shows the various types of measurement data that the PMT system can provide. Figure 13.33 depicts typical measurement system configurations for performing power measurements and noise characterization.

13.6   INTRODUCTION TO MMIC CONSIDERING LAYOUT EFFECTS

As the density of the circuits has increased, the effect of coupling has to be considered. A special program called LINMIC+ developed by Professor Jansen at the University of Duisburg can handle these cases and offers other important enhancements. LINMIC+ enables the CAD of strip-type planar MICs and MMICs and incorporates analysis, sensitivity analysis, and a stable and efficient interactive optimization procedure. It accomplishes this by making direct, automated use of a very general, rigorous field-theoretical approach to the generation of design information for a wide class of structures up to high-millimeter-wave frequencies.

Its description is based on a fast, enhanced spectral-domain technique which computes the required design data in the form of multidimensional look-up tables. In analysis and optimization, these tables are used together with a fast interpolation method. This approach constitutes a shift away from analytical models, further extending the
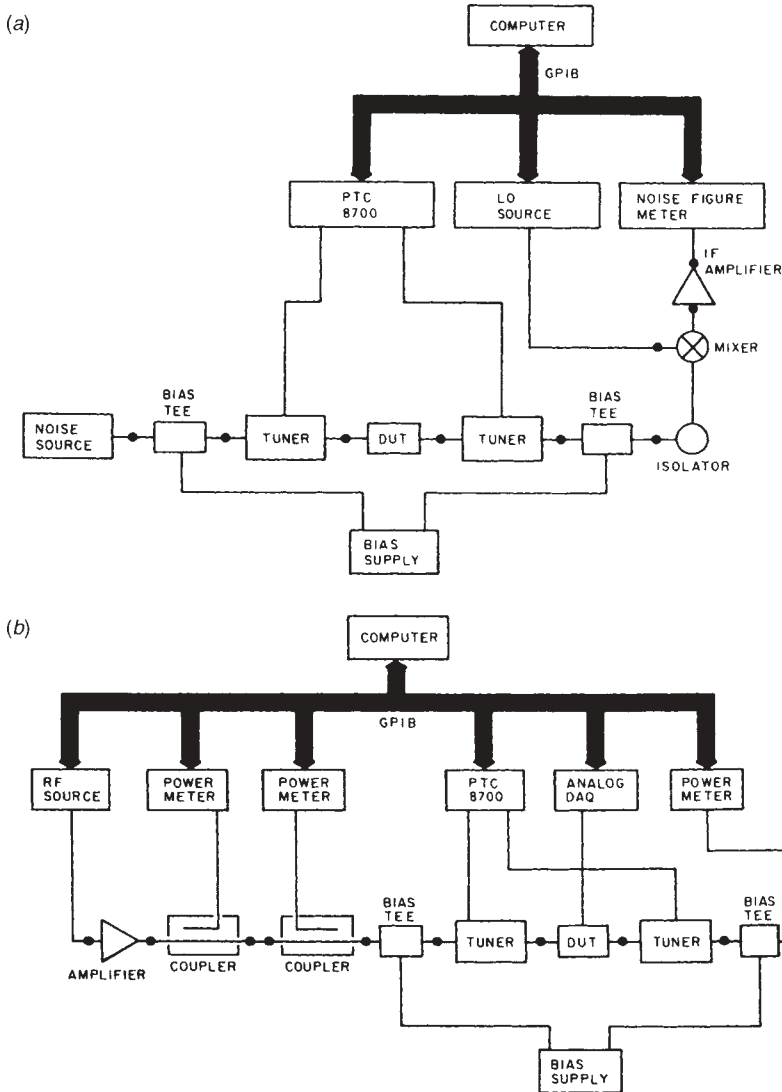
FIGURE 13.33   Block diagram of equipment configuration used for performing (*a*) power measurements and (*b*) noise characterization.

range of applicability and accuracy in circuit predictions (particularly at high frequencies). Circuit simulation and optimization in LINMIC+ are performed by using the layout's geometrical data and the electrical specifications of available commercial hybrid components; that is, the design parameters are physical quantities that are actually under the designer's control. Practical realizability of a design can be enforced by user-definable constraints. A user-controlled objective function for the design of MICs and MMICs can handle any of the complex network electrical quantities generated internally in up to nine user-selected formats (also mixed): real or imaginary, magnitude or phase. It can optimize any of these quantities to be greater, equal to, or less than

a given specification. In addition, the noise figure and stability factor can be handled. Circuit performance specifications can be defined within and far outside a band of interest. Also, interactive control of the features of the optimization algorithm allows gradual change between maximally flat and equal-ripple designs. Up to 60 parameters in a circuit can be varied during optimization.

In addition, LINMIC+ enables the automated generation and implementation of transistor models for very broadband applications from measured or data sheet S parameters. This allows for device simulation outside the frequency range of measurement.

As a consequence of its field-theoretical program, the LINMIC+ package has the potential to describe internally a variety of microwave circuit structures which could never be described by analytical models. LINMIC+ is thus applicable for microstrip, stripline, suspended substrate, and multilayer MMIC transmission line structures.

LINMIC+'s LCPACK can handle interdigital capacitors, multiturn square spiral inductors, and even planar spiral transformers and couplers at very high frequencies, on a substrate with or without passivation or second-level dielectric. Another option, named MELINE, allows for accurate characterization of a single strip meander line and parallel-coupled meander structures. Of course, whenever accurate analytical models for microwave strip structures are available, they are implemented in LINMIC+ as an alternative. A variety of models are used to describe the frequency-dependent characteristics of single and coupled microstrips (accurate at frequencies well into the millimeter-wave region). These models have been used in the major commercial CAD packages because of their high accuracy. An overall illustration of the LINMIC+ program is shown in Figure 13.34.
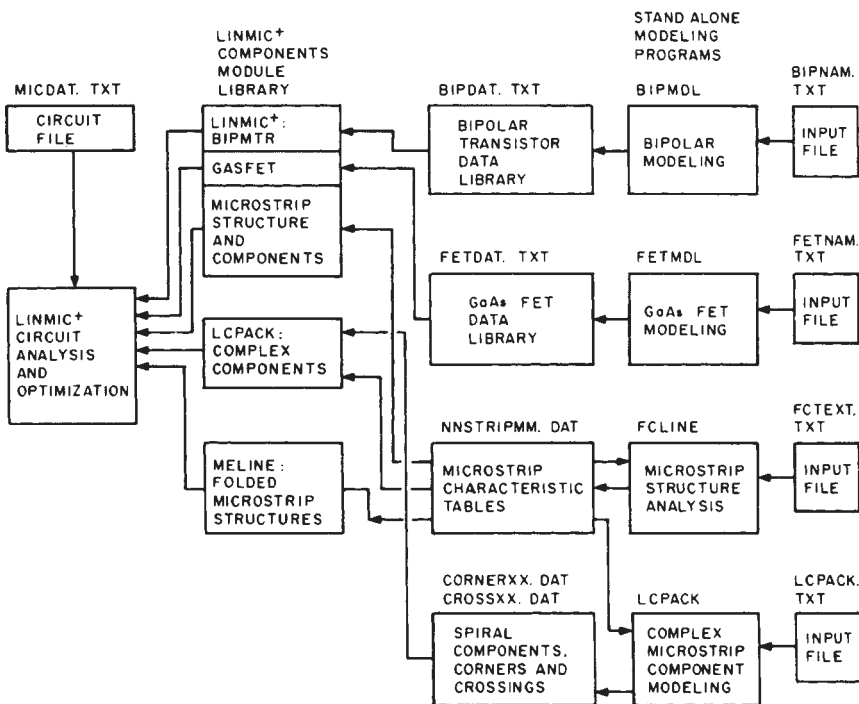
FIGURE 13.34   LINMIC+ structural elements.

13.6.1   Component and Interconnection Modules

The following elementary component modules are supplied with the LINMIC+ package:

SSTRIP	Single strip transmission lines, including microstrip and suspended substrate; up to 20 different user-definable substrate configurations/transmission media, each controlled by an integer identifier (applies to all component modules)
CSTRIP	Section of symmetrically coupled strips, four-port
MSTRIP	Analog to SSTRIP; avoids parameter recomputation
NSTRIP	Section of N multiply coupled strips, $2N$-port ($N = 3, \ldots, 10$)
CPLPRT	Coupled strip section loaded with admittances at two ports
DFLINE	User-defined strip transmission line
OPSTUB	Transmission line stub with ideal/nonideal open end
SHSTUB	Transmission line stub with ideal/nonideal short-circuited end (or via hole short)
SCSTUB	Sector-shaped radial stub structure open ended
CHBEND	Chamfered 90° strip transmission line bend
STEPLN	Symmetrical/unsymmetrical impedance step, including line section
LJUNCT	Symmetrical/unsymmetrical loaded strip-type T-junction
TJUNCT	Symmetrical/unsymmetrical T-junction three-port
UNSGAP	Unsymmetrical gap between two end-to-end coupled strips
SECTOR	Radial strip structure extruding from 90° bend, two-port
DLBCAP	Chip capacitor inserted into a gap between two strips
RSCHIP	Chip resistor mounted over a gap between two strips
BIPMTR	Bipolar microwave transistor, chip or packaged
GASFET	Gallium arsenide microwave FET, chip or packaged
RLCPRT	Ideal network elements R, L, C or any shunt or series combination of these; includes the definition of strips to contact these elements
BRANCP	Branch guide coupler, including the coupling effects between the involved parallel strips
RATRCP	Rat-race ring coupler
SLANCP	Straight, interdigitated (Lange) coupler, using four strips
FLANCP	Folded, interdigitated (Lange) coupler, using four strips
BRSDCP	Broadside-coupled stripline-type directional coupler

Note that many of the modules show the more general case. For example, NSTRIP represents a total of 48 physically different structures; RLCPRT represents 28 different configurations.

Additional interconnection operations can be performed:

COMPNT	Repeated use and linking of stored components
SUBNET	Use of subnetworks as (super) components

SNLINK	Link between ports of the current subnetwork
TNLINK	Interconnections of ports associated with different subnetworks; final linking operation in a design
METLINE	extension modules are:
SNGMEA	Folded single-strip structures
CPLMEA	Parallel folded structures coupled to each other
LCPACK	extension modules are:
INDUCT	Rectangular MIC/MMIC spiral inductors
PLTRAN	Rectangular MIC/MMIC spiral transformers
INTCAP	Interdigitated capacitors
NSLACP	Four- and six-strip interdigitated coupler configurations

The component module used for data-bank handling and black-box circuit operations is

SCFILE	Reading, using, and writing S-, Y-, or Z-parameter files for components with $1, \ldots, 4$ ports in the LINMIC+ environment (compatible with Super-Compact file format)

A conventional procedure based on the segmentation approach reduces circuits to a number of capacitors, inductors, transmissions lines, rectangular inductors, or other components. For example, a circuit with a rectangular inductor can be simulated by using one of the better mathematical expressions, such as the one developed by Ingo Wolff. These mathematical models assume, however, no underpass or air-bridge connection for inductors. LINMIC+ extends this analytic capability.

Figure 13.35 is a drawing of spiral tracks and a general structure. The underpass is used to connect the inner portion of the inductor to the outside. The inductor was built using seven turns, with a track and gap dimension of 12 μm and an inner turn on a 100×100-μm grid.

Figure 13.36 clearly illustrates the improvement in accuracy obtainable through the use of LINMIC+. The first curve (A) is a plot of the actual measured data obtained with an HP8510 network analyzer. The second curve (B) shows the predicted results of LINMIC+. The third curve (C) is the predicted curve obtained through the use of a popular PC-based software package.

Figure 13.37 is even more impressive. By looking at the input and output reflection coefficients, it becomes obvious that the measured data and those predicted by LINMIC+ are very close, while the dashed-line prediction by the PC product (Fig. 13.37) shows no difference between the input and output parameters. This apparent (and nonvalid) symmetry resulted from a disregard of the coupling between the tracks and the effect of the underpass.

Having understood this, it is even more interesting to analyze a four-stage amplifier for circuit simulation. Figure 13.38 is a Calma plot of an experimental four-stage traveling-wave amplifier which was used as a tool to verify the accuracy of the software. This Plessey amplifier was first generated on a standard simulator without taking into consideration the effect of coupling. Curve C in Figure 13.39 shows the predicted performance using the segmentation approach.

Actual measurements on an HP8510 (curve A in Fig. 13.39) show significantly different results; the magnitude of S_{21} drops much earlier than originally predicted. By using LINMIC+ and taking into consideration the coupling of the various transmission
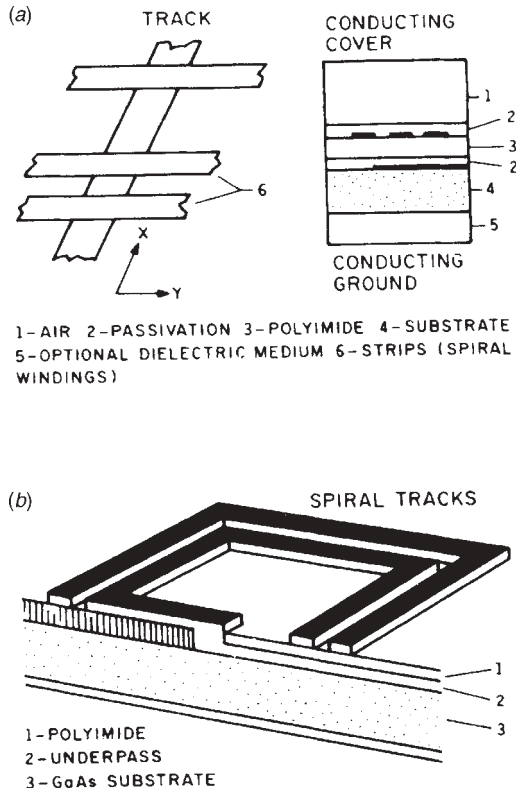
FIGURE 13.35 Spiral (inductor) tracks: (*a*) cross-sectional view illustrates multilayer composition; (*b*) underpass provides contact to inner turn.
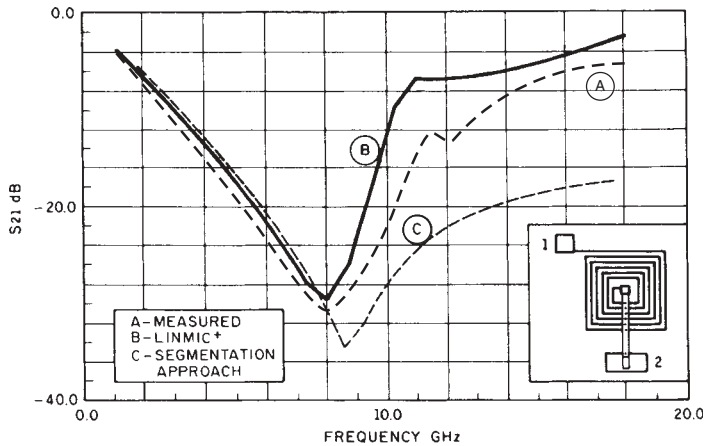
FIGURE 13.36 Multiturn inductor scattering parameter S_{21} frequency: *A*, values measured on HP-8510 analyzer; *B*, LINMIC+ predicted performance; *C*, predicted performance using the standard segmentation approach.
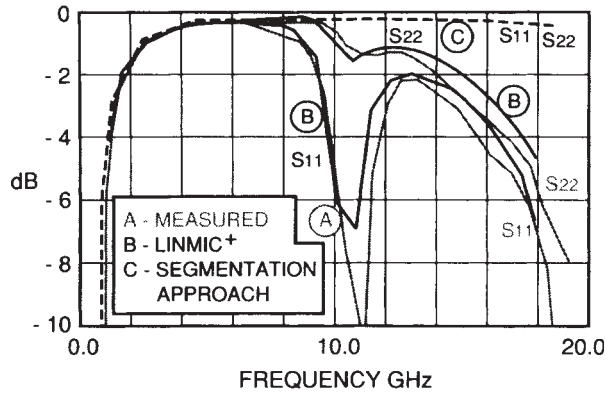
FIGURE 13.37 Multiturn inductor input and output scattering parameters S_{11} and S_{22} versus frequency: A, HP-8510 measured values; B, LINMIC+ predicted performance; C, predicted performance using the standard segmentation approach.
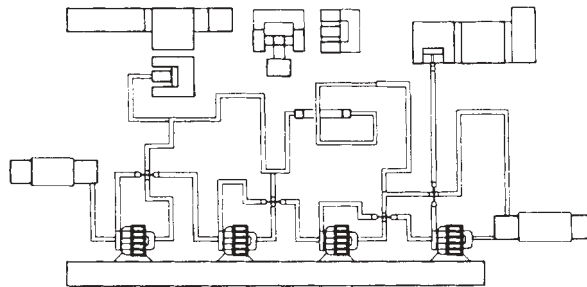
FIGURE 13.38 Calma plot of a four-stage distributed amplifier.
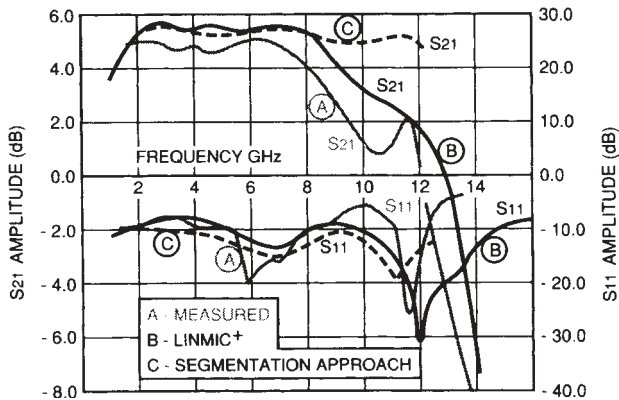
FIGURE 13.39 Multistage amplifier input and gain characterization versus frequency: A, HP-8510 measurements; B, LINMIC+ predictions; C, segmentation predictions relate to differences between measurements and LINMIC+ predictions relate to use of statistical rather than actual measured data for the FET.
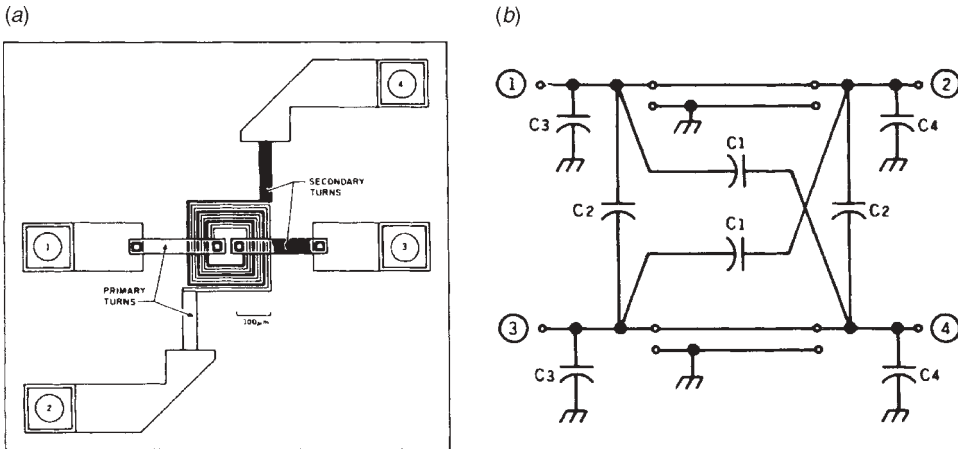
FIGURE 13.40   Transmission-line-based spiral transformer: (*a*) physical representation; (*b*) electrical equivalent circuit up to 18 GHz.

lines while using an enhanced model for the bends, the simulation prediction is very close (curve *B* in Fig. 13.39). LINMIC+ can also handle exotic structures such as the transmission-line-based spiral transformer shown in Figure 13.40. LINMIC+ is a dedicated MMIC simulator and outperforms the segmentation approach for high-density MMIC designs.

13.7   GaAs MMIC LAYOUT SOFTWARE

When used in conjunction with electrical and/or optical simulation software, graphics layout software assists the analog designer to develop GaAs MMIC and millimeter-wave circuits and optoelectronic components. One particular package, the GaS STATION, utilizes mouse-driven menu-oriented inputs to pull up a main display and up to 12 different menus. The process is initiated by choosing from a main menu up to four separate menus from the following list:

EDIT1	ARCS	TSTONE	TOGGLE
EDIT2	COMPAC	MWAVE2	SETUP
WINDOW	NODE	LAYOPS	FILE

Figure 13.41 illustrates this with a screen presentation that includes the MAIN and TOGGLE to the left and the EDIT1 and EDIT2 menus to the right of the main window.

13.7.1   Capabilities

GaS STATION is used to generate patterns. It utilizes what is known as the GDS-II data format, an industry standard, that allows for up to 64 layers (of processing) with choices from a 256-color palette. One of the powerful features of GaS STATION is that, besides using a graphics input, it can pull from geometrically defined circuit files available in several leading microwave CAD packages (e.g., the COMPAC and
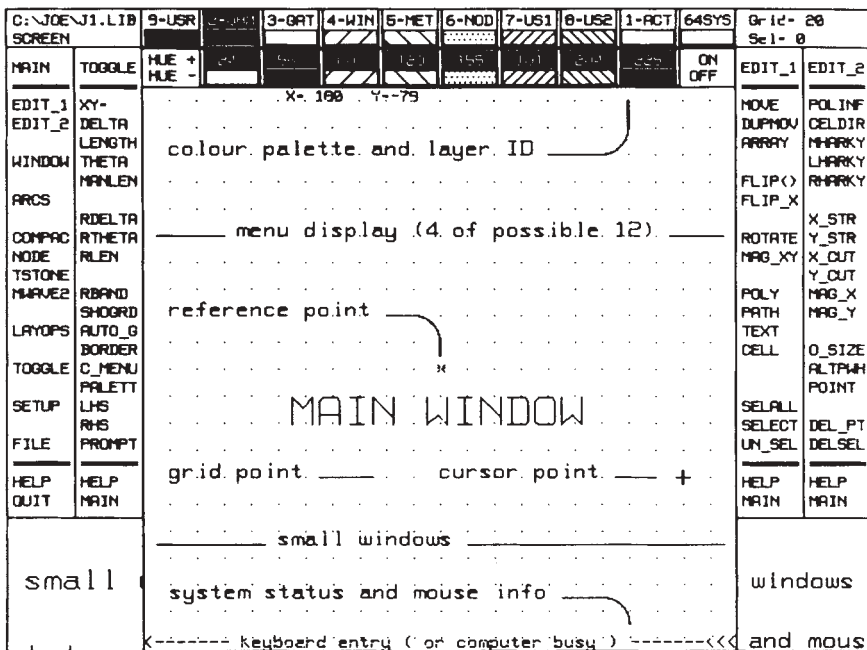
FIGURE 13.41   Maximum of four menus can be used with the main window.

TSTONE menus listed above). A node capability is built into the software to help facilitate this interaction between the electrical circuit description and the geometrical layout.

Typical shapes that can be generated, such as circles, arcs, and sinusoidal and exponential functions, are illustrated by the distributed filter section in Figure 13.42. Notice that in this case only two menus are called up to the right of the main window.

Command files can be run from GaS STATION, which enables the user to run a setup file to configure the system. Command files can also be used to store a record of the design session or, as mentioned before, to generate or run Super-Compact or Touchstone files.

13.7.2 Example

Consider the "open-end effects circuit" shown in Figure 13.43. The first half of it is delineated in the following circuit block descriptor:

```
CAP  1 0 C=1.2PF
IND  1 2 L=1NH
CAP  2 0 C=1.2PF
TRL  2 3 W=100UM P=400UM SUB1
CROS 3 4 5 6 W1=100UM W2=100UM W3=100UM W4=100UM SUB1
OST  4 W=100UM P=400UM SUB1
```

From the above, notice that a 400-μm-long, 100-μm-wide dielectric factor 1 (SUB1) transmission line was placed between nodes 2 and 3. GaS STATION users can work
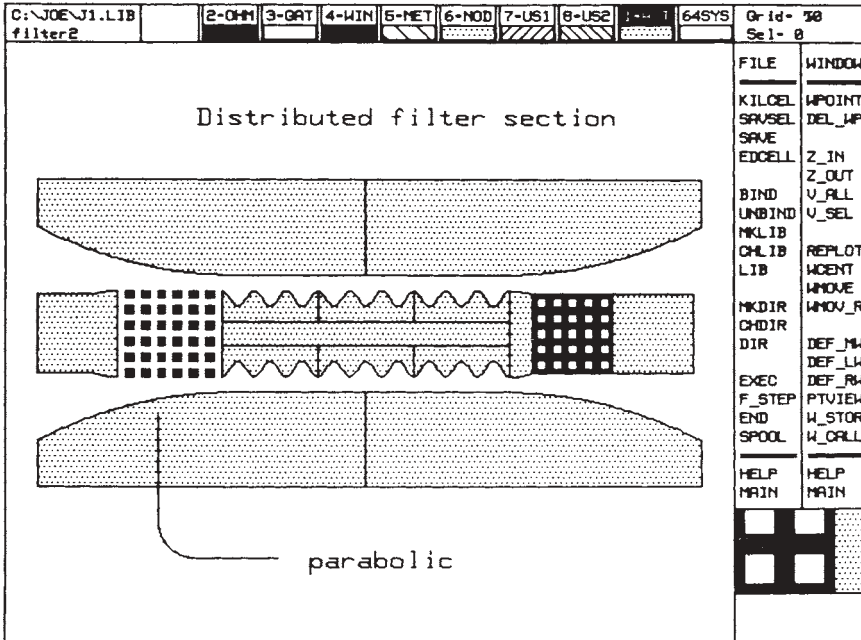
FIGURE 13.42 Distributed filter section requires parabolic shape generation.
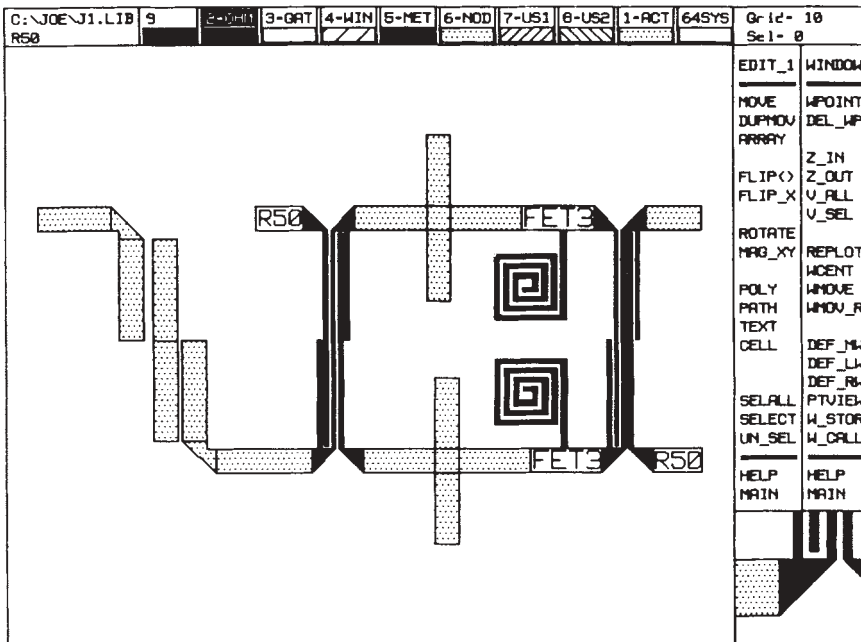
FIGURE 13.43 Open ends affect circuit.
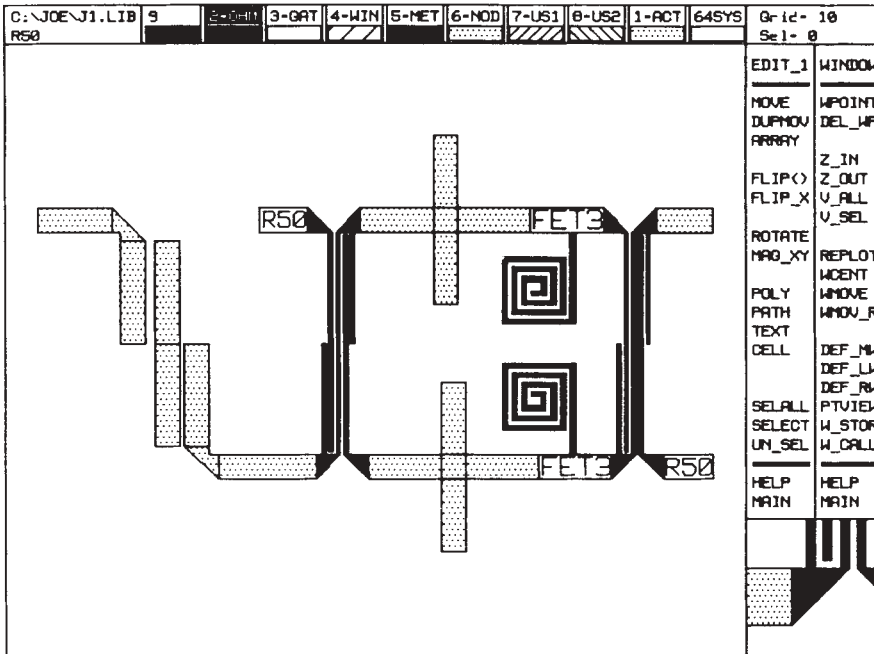
FIGURE 13.44 Circuit utilizes constant-impedance bends achievable through software commands.

with both metric and English units of measurement. In the English system the numbers can range from 0.1 to 100,000 μm, literally a ratio of 1 million to 1. Appropriately, the TOGGLE menu includes a variety of relative and absolute angle and length indicators.

Figure 13.44 indicates another useful feature available from the software's command structure. A transmission line can be Chamfered to maintain a constant impedance through a bend.

13.8   PRACTICAL DESIGN EXAMPLE

In the previous chapters we have been looking at both linear and nonlinear circuits, but in reality circuits are parts of systems. These systems incorporate various applications. In our opinion, a good example of how to integrate these things is a 4-GHz anticollision radar consisting of a pulsed transmitter and a selective receiver.

13.8.1   The Design

Figure 13.45 shows a sketch of the receiver and transmitter portion. As can be seen, the receiver consists of an antenna, a three-element input filter, and a matching circuit for the input amplifier. The output of the amplifier shows a matching circuit and a dc decoupler capacitor which feeds into one arm of a branch line coupler. The branch line coupler is also driven from a dielectric resonator oscillator. The output of the branch line coupler terminates in a video detector consisting of two diodes.
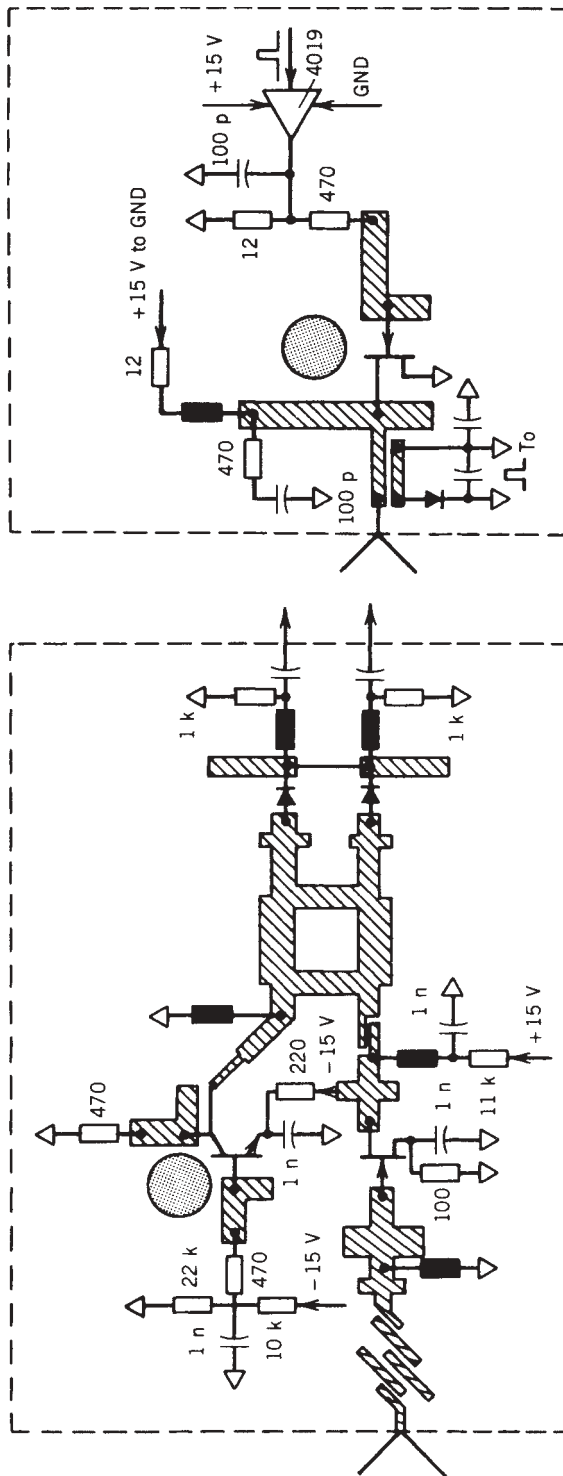
FIGURE 13.45 Sketch of a receiver and transmitter used in an anticollision radar.

The transmitter has its own antenna, and a coupler in the output monitors the power level. For reasons of overall power, the oscillator uses a FET as the active device, and the gate voltage is pulsed to turn the transistor on and off.

13.8.2 The Elements

Figure 13.46 shows the insertion losses and return losses of adjacent planar antennas at various distances (1 m, 70 cm, and 50 cm). Figure 13.47 shows the radiation diagram of a planar antenna in the E and H field with a height of 3.14 mm and a dielectric constant of 2.33. Figure 13.48 shows the pattern of a slightly different antenna with $H = 1.57$ m. Here the antenna impedance is 88 Ω, versus 52 Ω in Figure 13.47.

13.8.3 The Input Filter

The input filter was designed using common requirements for bandpass filters using parallel-coupled lines. The frequency was 4.3 GHz with 200 MHz bandwidth. The filter response is shown in Figure 13.49. Figure 13.50 shows the list of an equivalent model of a parallel-modeled resonator bandpass filter. Comparison of the CAD simulation and measurements indicates excellent tracking. The response curve shown in Figure 13.51 is very close to measurements done with the network analyzer.

13.8.4 The Dielectric Resonator

The dielectric resonator for the oscillator can be configured in several ways. Figures 13.52 to 13.54 show the resonant behavior of the dielectric resonator in
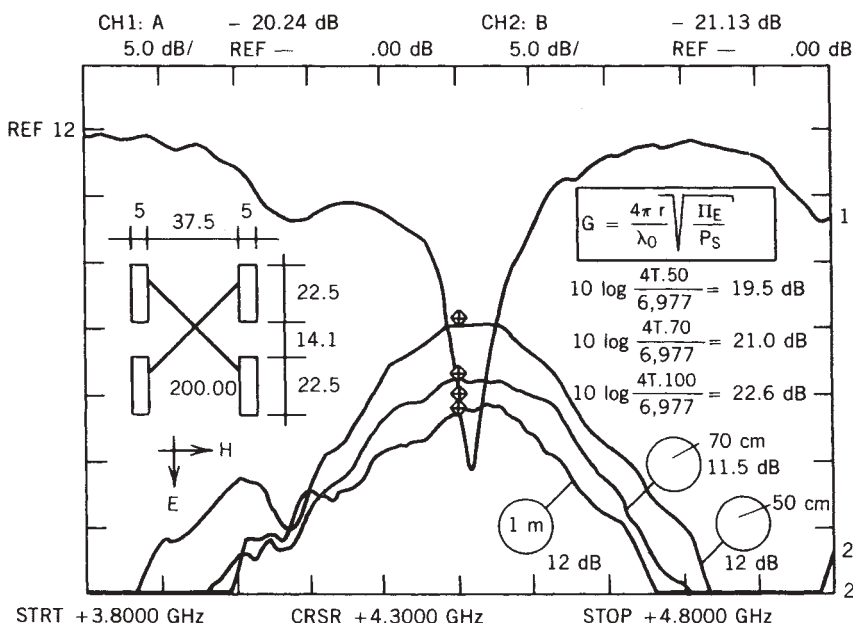
FIGURE 13.46 Insertion losses and return losses of adjacent planar antennas at different distances.
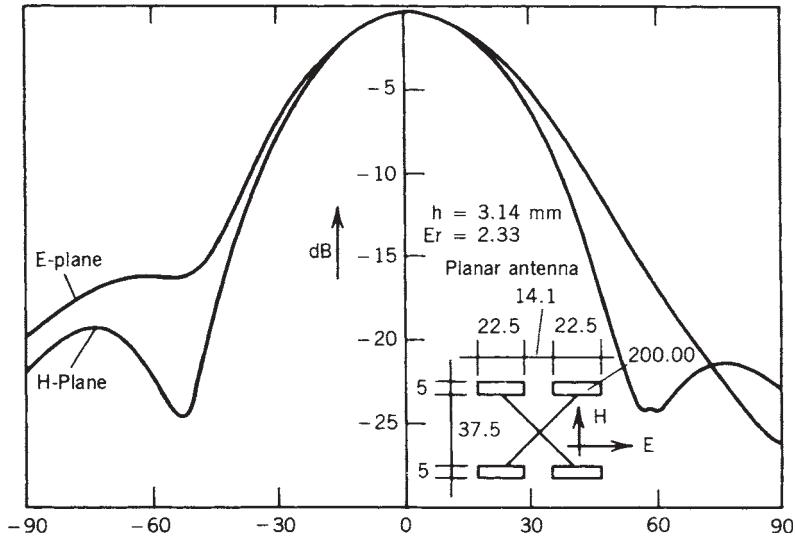
FIGURE 13.47 Radiation diagram of a planar antenna in the $E-H$ field with a height of 3.14 mm and a dielectric constant of 2.33.
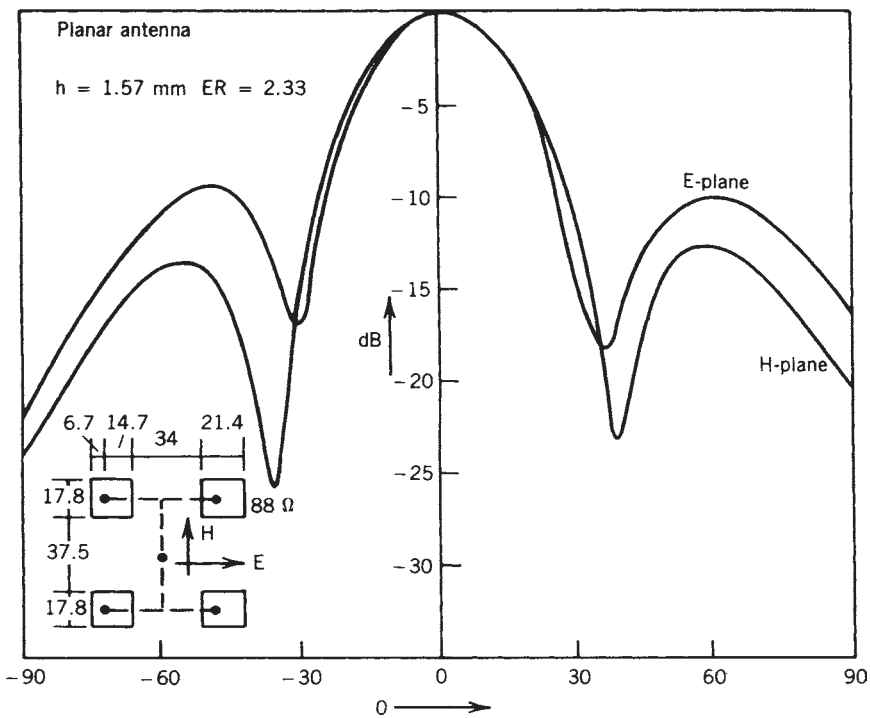
FIGURE 13.48 Pattern of a slightly different antenna with $H = 1.57$ m. Here the antenna impedance is 88 versus 52 Ω in the preceding example.
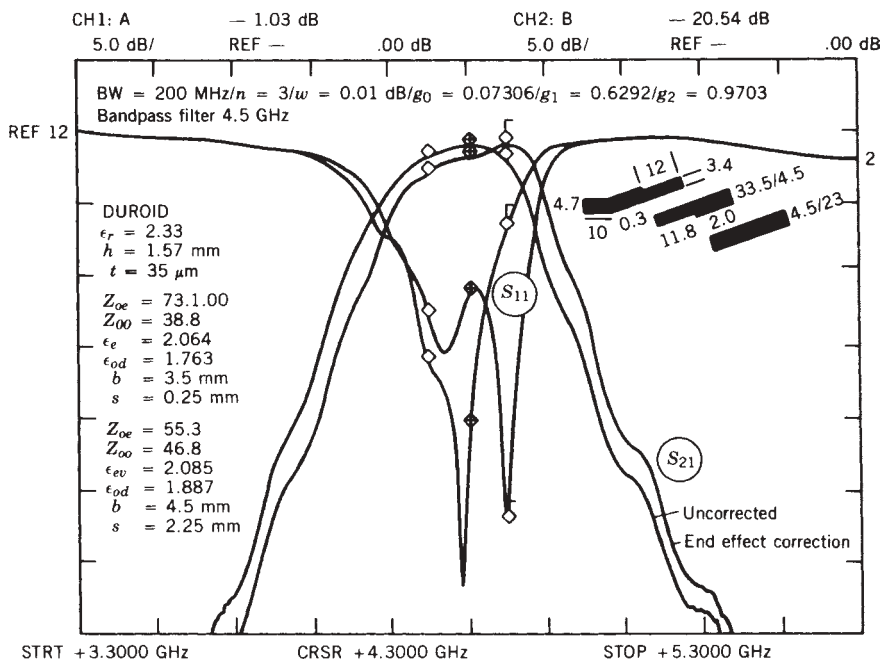
FIGURE 13.49   Structure and measured response of 4.3-GHz bandpass filter.

different configurations. A circuit simulation again provides good agreement between measurement and prediction.

13.8.5   The Branch Line Coupler

The branch line coupler has always caused a lot of interest in modeling, because it consists of a T junction and transmission lines as shown in Figure 13.55. As the device consists of four tees, it is a good test to verify the accuracy of the model. Comparison of measurement and prediction again reveals close tracking and resemblance (see Figs. 13.56 to 13.58). Typically, in CAD tools, it is important to run as many test cases as possible to verify the accuracy of the models.

13.8.6   Other Circuit Elements

The dc separation between the chain of the preamplifier and the branch line coupler also requires some verification. Although we recommend that readers use their CAD tools to model those elements, we have provided the actual measurement. Figure 13.59 shows the insertion loss and return loss for a quarter-wave coupler as shown in the original circuit.

The diode detector requires a matching circuit. Figure 13.60 shows the return loss of the HP diode HP5082-2217 for various currents through a 1-kΩ resistor at the particular mechanical configuration. The purpose of this was to determine the right matching combination. The transmitter requires a power monitor. Figure 13.61 shows insertion loss and return loss for a quarter-wave microstrip coupler as a function of frequency.

```
*********************************************************************
*                                                                   *
* EQUIVALENT MODEL OF A PARALLEL-COUPLED RESONATOR BANDPASS FILTER  *
*                                                                   *
*********************************************************************
O1:3.5MM
O2:4.4862MM
BLK
    CPL   1   2   3   4   W=O1   S=0.25MM   P=12.697MM   SUB1
    OPEN  2   W=O1   SUB1
    OPEN  4   W=O1   SUB1
    CPL   3   5   6   7   W=O2   S=2.1595MM   P=12.404MM   SUB1
    OPEN  5   W=O2       SUB1
    OPEN  7   W=O2       SUB1
A:2POR   1   6
END
BLK
    CPL   1   2   3   4   W=O1   S=0.25MM   P=11.800MM   SUB1
    OPEN  2   W=O1   SUB2
    OPEN  4   W=O1   SUB2
    CPL   3   5   6   7   W=O2   S=2.1595MM   P=11.700MM   SUB1
    OPEN  5   W=O2       SUB2
    OPEN  7   W=O2       SUB2
B:2POR   1   6
END
BLK
    A   1   6
    A   8   6
C:2POR   1   8
END
BLK
    B   1 2
    B   3 2
D: 2POR 1 3
END
FREQ
    STEP   3.3GHZ   5.3GHZ   0.1GHZ
END
OUT
    PRI   C   S
    PRI   D   S
    PRI   A   S
    PRI   B   S
END
DATA
SUB1:   MS   H=1.57MM   ER=2.33   TAND=0.001   MET1=CU   35UM
SUB2:   MS   H=1.57MM   ER=2.33
END
```

FIGURE 13.50   Super-Compact circuit description of bandpass filter shown in Figure 13.49.

13.9   CAD APPLICATIONS

The following circuit files from the application notes section of the Super-Compact PC manual serve as a good introduction to the use of linear CAD tools and demonstrate the power of modern CAD microwave tools.

APP1: Single-Stage Amplifier (Figs. 13.62, 13.63)   Application Note 1 shows a combination of several useful features in the Super-Compact PC program. The main purpose is to illustrate the design of a single-stage amplifier using microstrip. In conjunction with pure circuit analysis, the TRL program was used. Optimization techniques and the use of the DATABANK are also demonstrated. TRL is used to determine the line width of the microstrip with a certain characteristic impedance ($Z_0 = 50$ Ω in this case). This step is important since you can improve the quality factor (Q) by
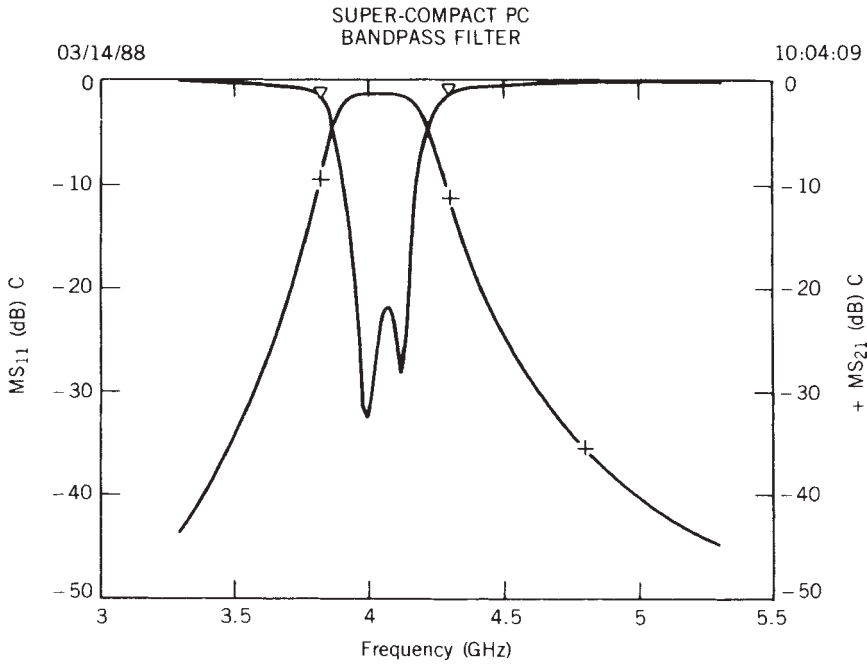
FIGURE 13.51   Calculated response of 4.3-GHz bandpass filter.
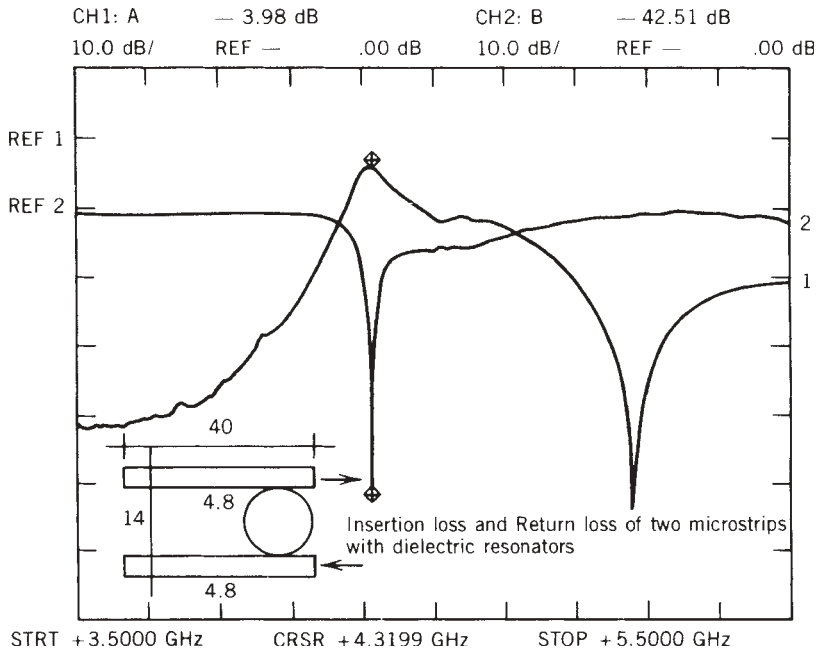
FIGURE 13.52   Insertion loss and return loss of dielectric resonator between coupled lines.
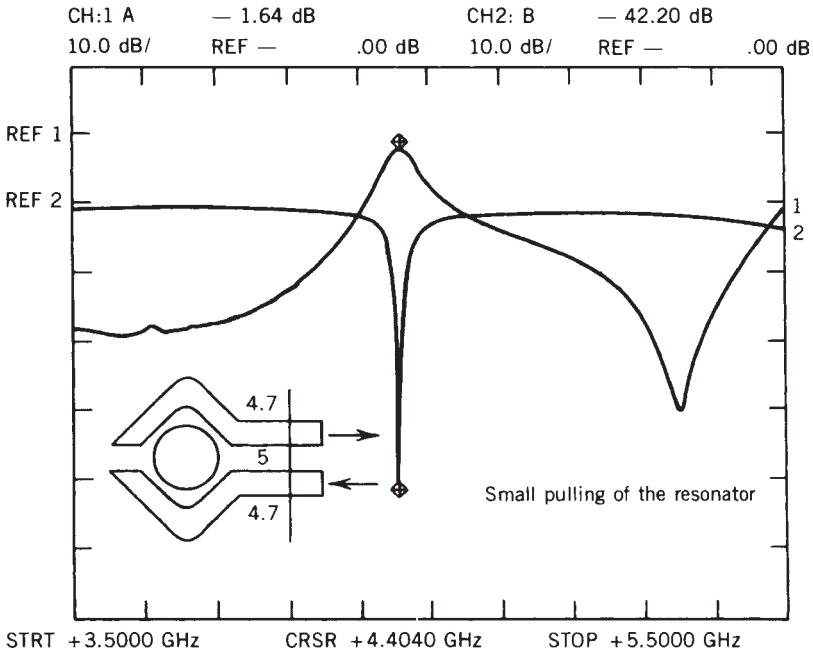
FIGURE 13.53 Insertion loss and return loss for different transmission line configurations.
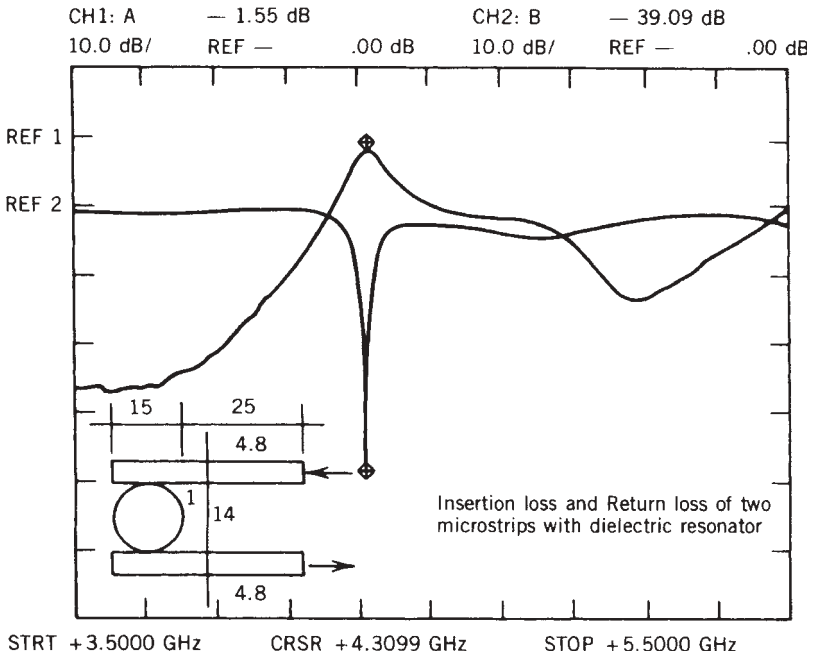
FIGURE 13.54 Insertion loss and return loss with different coupling to the resonator.

```
*   BRANCH-LINE DIRECTIONAL COUPLER (BRNLINE2.CKT)
WW: 7.6MM
LW: 14.5MM
WN: 4.7MM
LN: 9.80MM
BLK
   T:  TEE 1   5 9 W1=WN W2=WW W3=WN SUB
   WL: TRL 5   6    W=WW  P=LW   SUB
   NL: TRL 9 12     W=WN  P=LN   SUB
   T    2   6 10
   NL 10 11
   T    4   8 12
   WL   8   7
   T    3   7 11
PHYS: 4POR 1 2 3 4
END
FREQ
   STEP 3.3GHZ 5.5GHZ  0.2GHZ
   4.465GHZ
END
OUT
   PRI PHYS S
END
DATA
   SUB: MS H=1.57MM ER=2.33 MET1=CU 35UM
END
```

FIGURE 13.55   Super-Compact circuit file listing of branch line directional coupler.
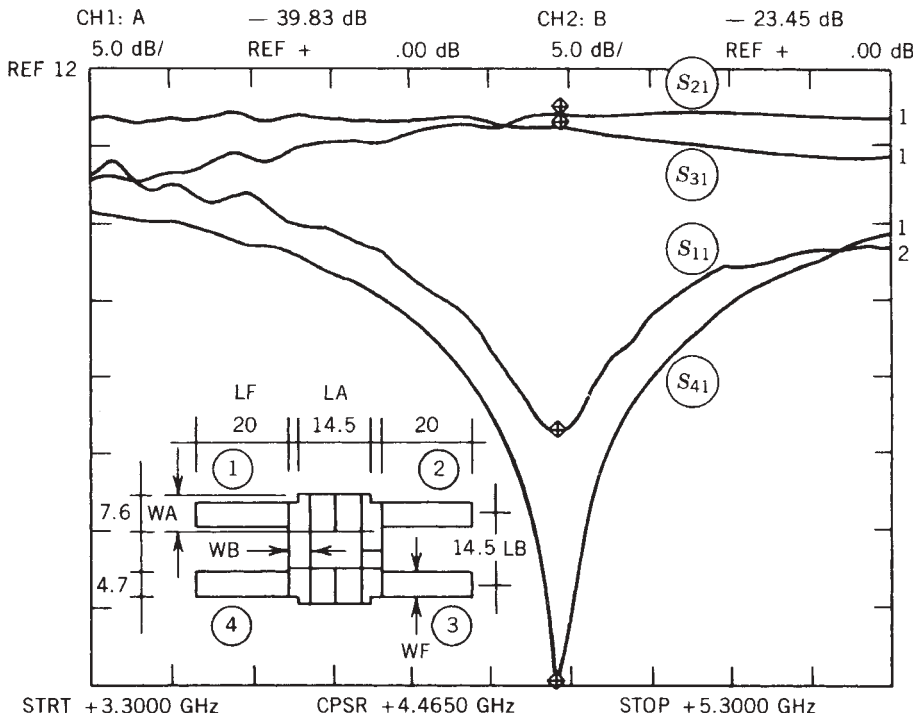
FIGURE 13.56   Measured response of branch line coupler.

SUPER-COMPACT PC
BRANCHLINE COUPLER

10:21:02
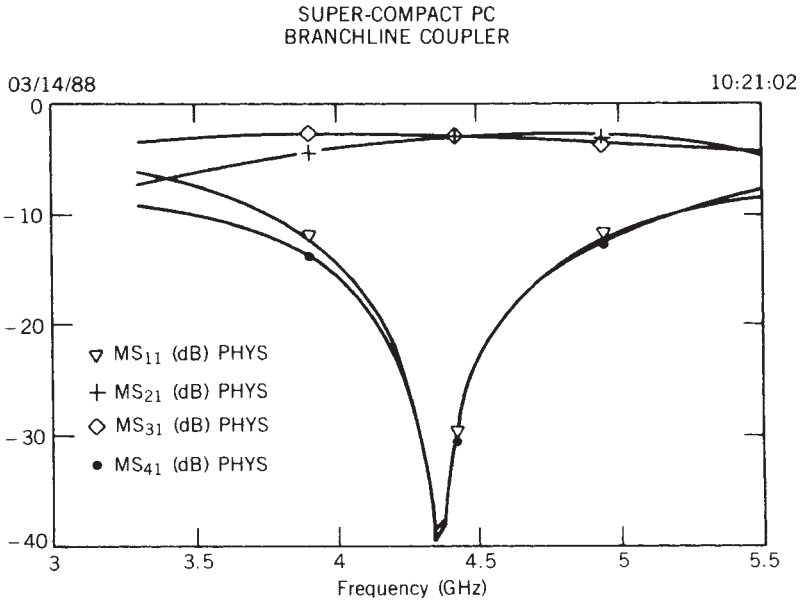
FIGURE 13.57 Calculated response of branch line coupler.

SUPER-COMPACT PC
DIRECTIONAL COUPLER

10:51:45
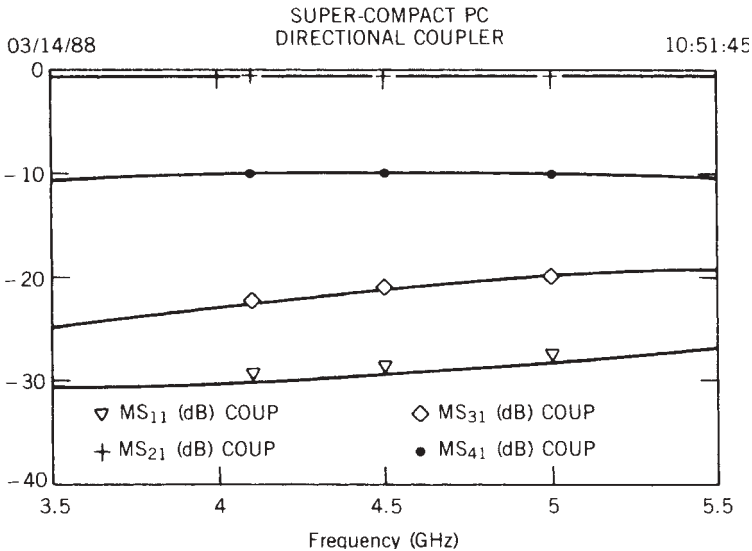
FIGURE 13.58 Coarse and response of branch line coupler.

selecting impedances around 70 Ω or you can omit discontinuities by always selecting the same impedance. Optimization is used to obtain the highest possible gain (MS21) and the lowest possible reflection (MS11) in order to meet the specifications of the circuit. Because the DATABANK contains most of the common transistor data, it comes in very handy for the user. All the available information about the device will
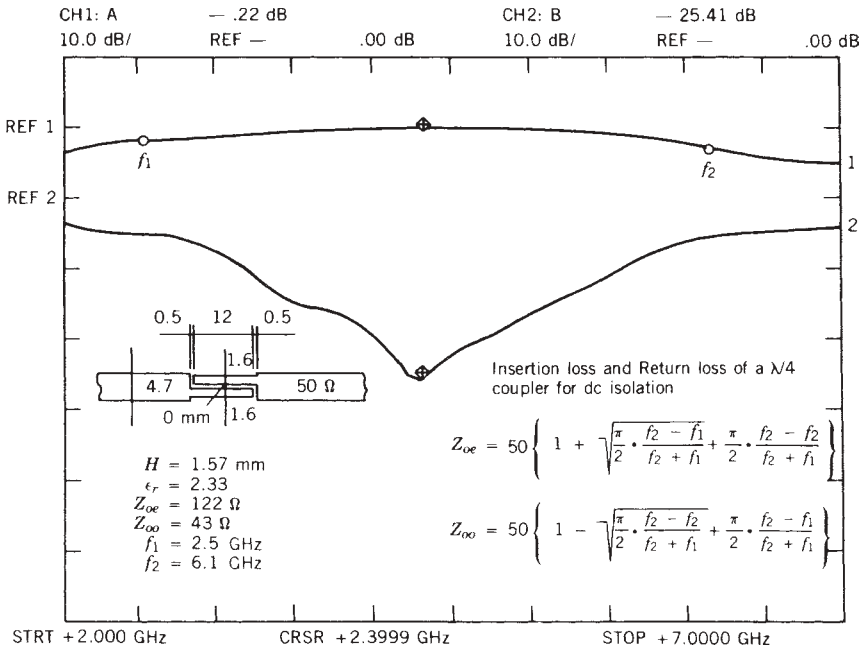
FIGURE 13.59   Insertion loss and return loss of control wavelength coupler.
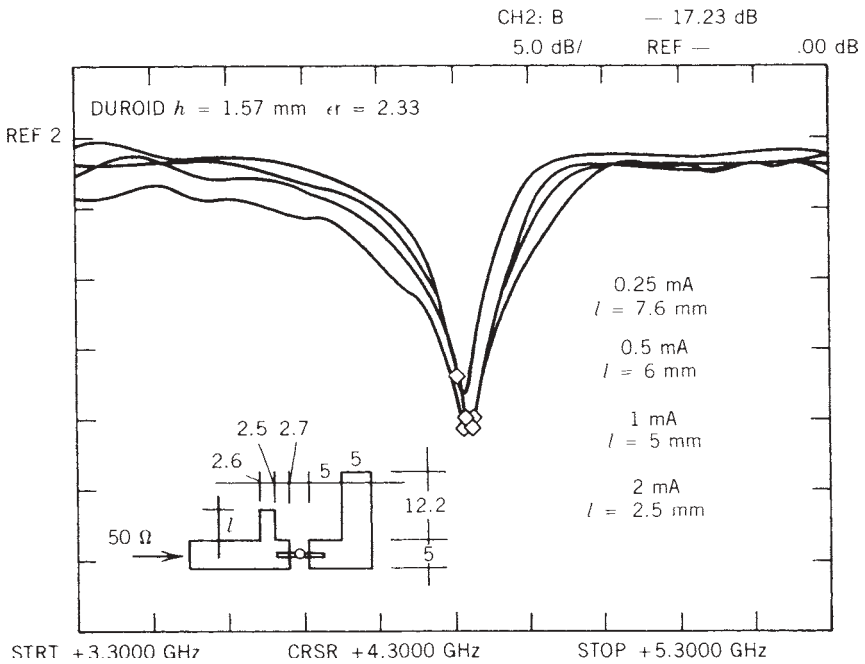
FIGURE 13.60   Return loss of HP-5082-2217 diodes for different bias.
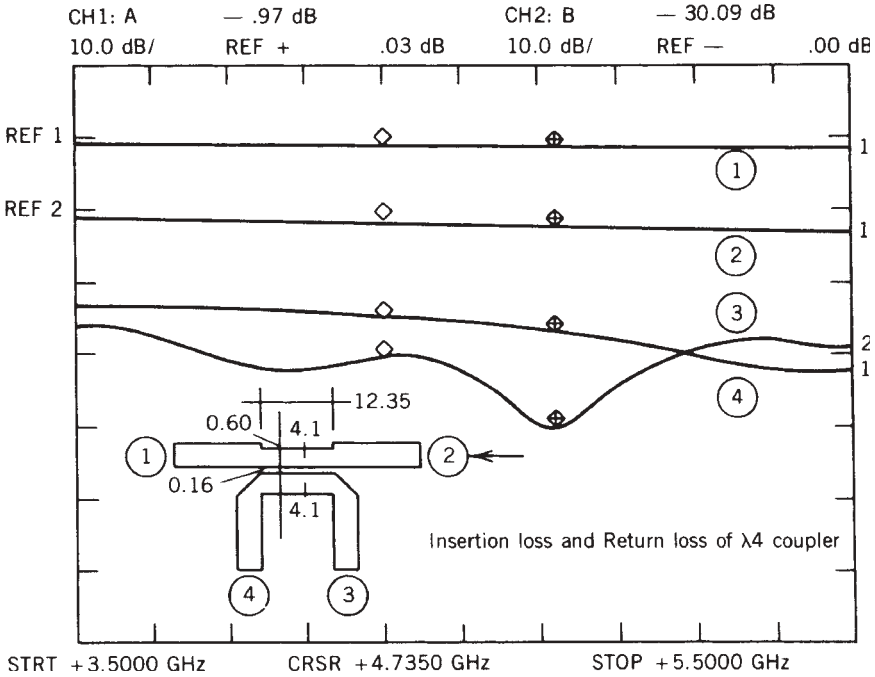
FIGURE 13.61 Insertion loss and return loss of quarter-wave coupler at the output.
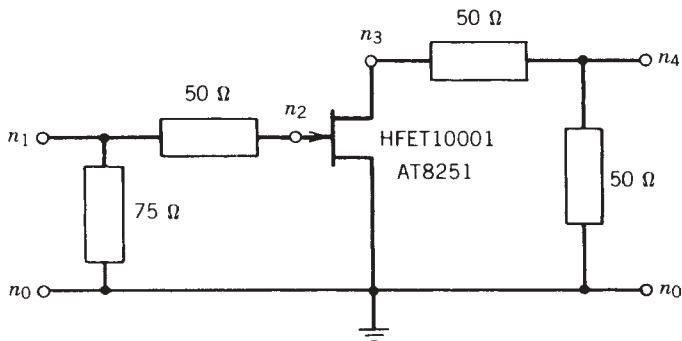
FIGURE 13.62 Schematic of single-stage amplifier.

be linked to the circuit as long as it is defined in the DATA block in the following format:

```
HAMP : HPMCC FILE=\BANK01\HPM . FLP
```

where HAMP = label of user-defined black box
    HPMCC = name of device in databank
    BANK01 = directory where databank can be found
    HPM.FLP = filename for databank
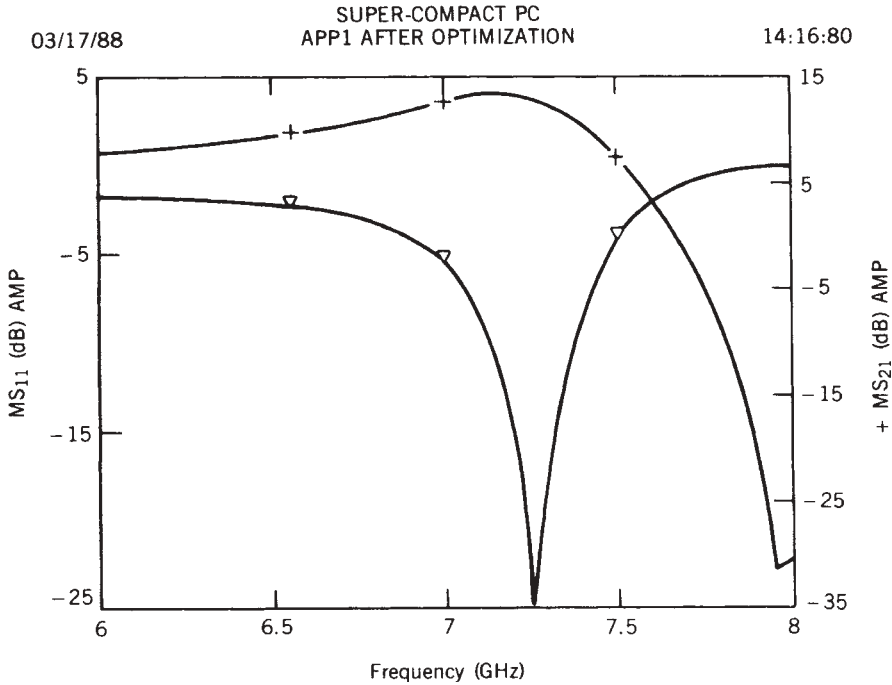
FIGURE 13.63 Frequency response of amplifier of Figure 13.62.

```
* OPTIMIZATION OF A SINGLE STAGE MICROSTRIP AMPLIFIER
*                      (APP1.CKT)
*                   BY ANTHONY W. KWAN

LAD
     TRL 1 0 W=0.221MM P=?4.97MM? SUB
     TRL 1 2 W=0.576MM P=?4.838MM? SUB
     TWO 2 3 HAMP
     TRL 3 4 W=0.576MM P=?4.838MM? SUB
     TRL 4 0 W=0.576MM P=?4.838MM? SUB

AMP : 2POR 1 4
END
FREQ
     STEP 6GHZ 8GHZ 0.1GHZ
END
OUT
   PRI AMP SK
END
OPT
   AMP
     F=7.2GHZ 7.3GHZ MS21 12DB GT
     F=7.2GHZ 7.3GHZ MS11 -15DB LT
END
DATA
```

```
    HAMP:HPMCC                 FILE=\BANK01\HPM.FLP
    SUB:MS H=.635MM ER=10.0 MET1=CU 15UM TAND=0.0001
END
```

APP2: 3-dB Branch Line Coupler (Figs. 13.64 to 13.66)   Application Note 2
shows how a physical model is optimized to an ideal electrical model. Before opti-
mization the physical model did not resonate at 10 GHz and did not have the right
values for any of the *S* parameters. Since the line width of the microstrip does not
change the frequency, the physical lengths were chosen as the parameters to be opti-
mized. After optimization the physical model characteristics came very close to the
electrical model, especially the 3 dB bandwidth. In this case the goal is to come as
close as possible to the response of the electrical network. Therefore, the complete set
of *S* parameters is optimized using only one expression.

```
* 3DB BRANCH-LINE DIRECTIONAL COUPLER (APP2.CKT)
*                   AFTER OPTIMIZATION

WW: ?1.148MM?
LW: ?2.74MM?
WN: ?0.604MM?
```


(a)
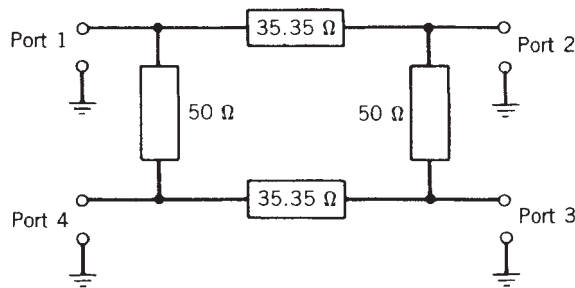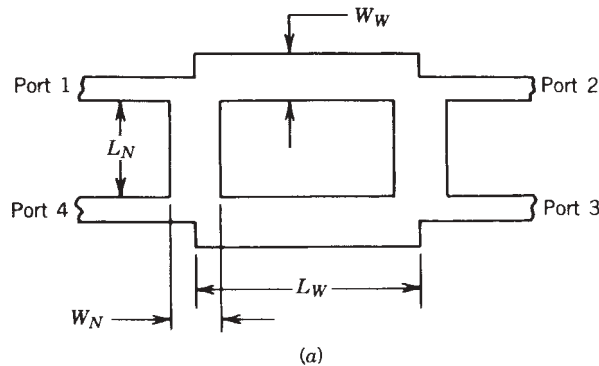
Note: All lines are λ/4 at 15 GHz

(b)

FIGURE 13.64   A 3-dB branch line coupler: (*a*) physical model; (*b*) electrical model.
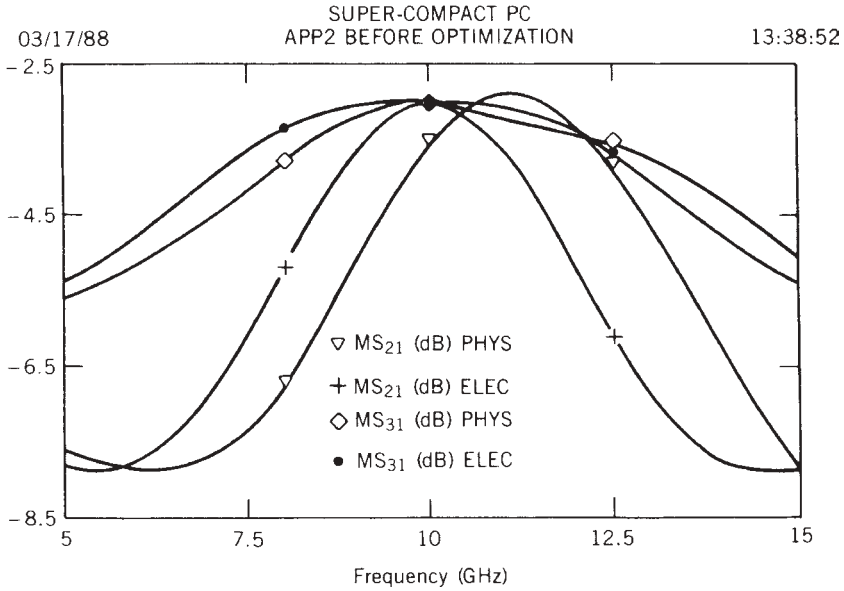
FIGURE 13.65 Frequency response of 3-dB branch line coupler before optimization.
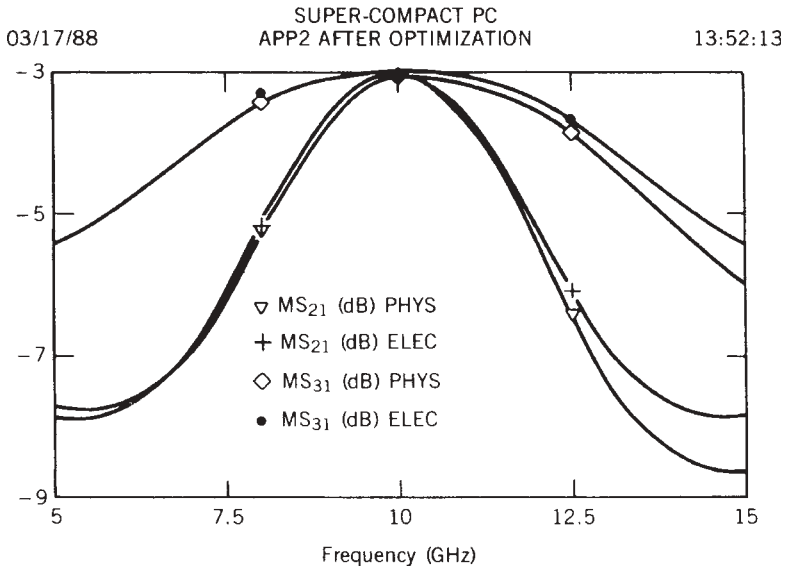
FIGURE 13.66 Frequency response of 3-dB branch line coupler after optimization.

```
LN: ?2.84MM?
BLK
  T:   TEE 1   5 9 W1=WN  W2=WW  W3=WN  SUB
  WL:  TRL 5   6 W=WW   P=LW   SUB
  NL:  TRL 9  12 W=WN   P=LN   SUB
```

```
  T    2  6 10
  NL  10  11
  T    4  8 12
  WL   8  7
  T    3  7 11
PHYS: 4POR 1 2 3 4
END
BLK
  TRL 1 2 Z=35.35 E=90 F=10GHZ
  TRL 4 3 Z=35.35 E=90 F=10GHZ
  TRL 1 4 Z=50    E=90 F=10GHZ
  TRL 2 3 Z=50    E=90 F=10GHZ
ELEC: 4POR 1 2 3 4
END
FREQ
  STEP 5GHZ 15GHZ 500MHZ
END
OUT
  PRI PHYS S
  PRI ELEC S
END
OPT
  PHYS
F=7.5GHZ 12.5GHZ S=ELEC
END
DATA
  SUB: MS H=.635MM ER=10 MET1=AU 3UM
END
```

APP3: Edge-Coupled Microstrip Filter (Figs. 13.67, 13.68)   Application Note 3 shows how to realize a microstrip filter with a center frequency of 6 GHz. The selected bandwidth is 65%. This particular bandwidth is not easy to realize using edge-coupled lines to build up the microwave filter. Nevertheless, the necessary values for the filter design are as follows:
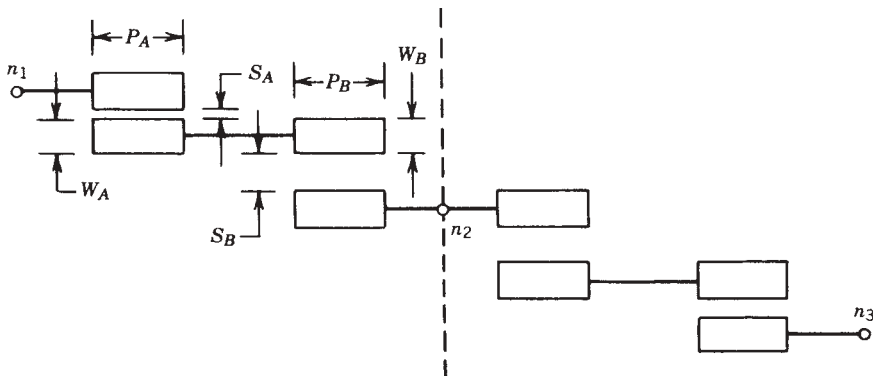
FIGURE 13.67   Edge-coupled filter.

SUPER COMPACT PC
AN EDGE COUPLED FILTER
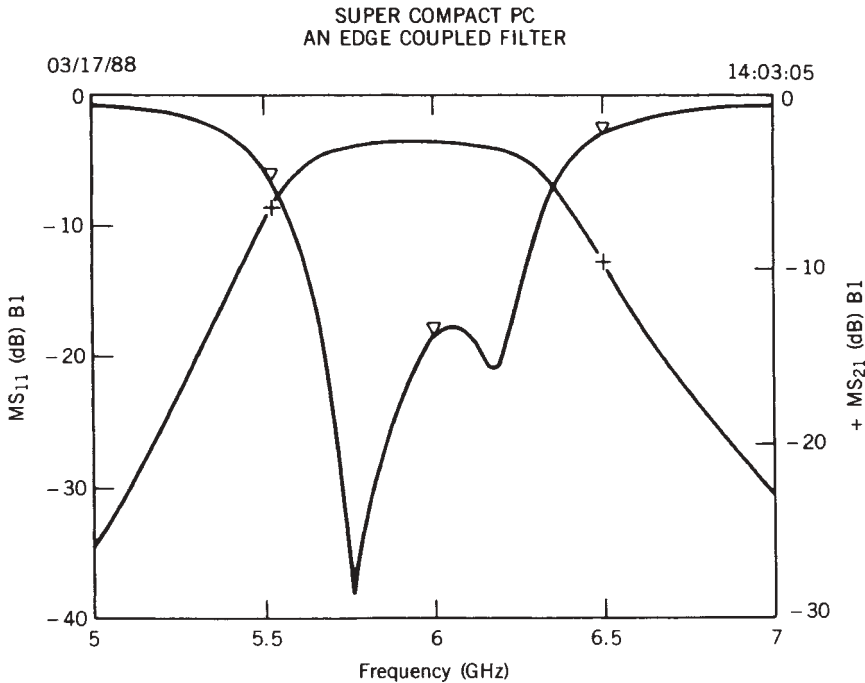
FIGURE 13.68   Couple frequency response of edge-coupled filter.

Z_{0e}	Z_{00}	Gap (mm)	Width (mm)	Length (mm)
68.834	31.1655 ± 0.0217	4.4497		
	0.0583			
50.156	36.7023	0.0877	0.0881	4.3454
50.156	36.7023	0.0877	0.0881	4.3454
68.834	31.1655 ± 0.0217	4.4497		
	0.0583			

The actual design splits the symmetrical circuit into two pieces. First, one half of the filter is defined in subcircuit $a1$. Then subcircuit $a1.$ is used and connected with itself again. The final circuit is called $b1$.

```
*Edge coupled filter with a bandwidth of 65% (APP3)
*and a center frequency of 6GHz
*using length for layout with open end effect

blk
    cpl 1 2 3 4 w=0.0583mm s=0.0217mm p=4.4281mm sub
    cpl 3 5 6 7 w=0.0881mm s=0.0877mm p=4.3177mm sub
    open  2      w=0.0583mm sub
    open  4      w=0.0583mm sub
    open  5      w=0.0881mm sub
    open  7      w=0.0881mm sub
a1:2por 1 6
```

```
end
*
blk
    a1   1 2
a1   3 2
b1:2por 1 3
end
*
freq
   step 5ghz 7ghz .1ghz
end
out
  pri b1 s
end
data
   sub : ms h=0.1mm er=12.9 met1=au 1um
end
```

APP4: End-Coupled Filter (Figs. 13.69, 13.70)   Application Note 4 shows how to apply the GAP to a narrow-band capacitive-coupled resonator filter. The 4-GHz bandpass filter has a high transmission coefficient (MS21) and low reflection coefficient (MS11). However, this type of configuration is not as common as the one shown in Application Note 3, mainly because the physical length of the filter gets too long to be built practically.

```
*CAPACITIVE END-COUPLED HALF-WAVE RESONATOR FILTER
*(APP4.CKT)
*
G1 : ?.50363MM?
G2 : ?.85663MM?
L1 : ?11.254MM?
L2 : ?4.4424MM?
L3 : ?4.3502MM?
WW1:    4.8MM
BLK
    TRL  1 2 W=WW1  P=L2 SUB2
    GAP  2 3 W=WW1  G=G1   SUB1
    TRL  3 4 W=WW1  P=L1   SUB2
    GAP  4 5 W=WW1  G=G2   SUB1
```
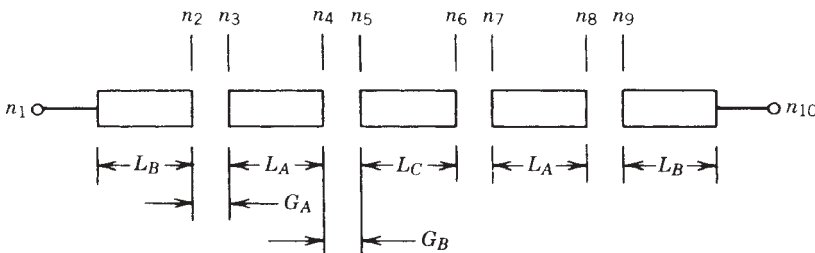

FIGURE 13.69   End-coupled filter.
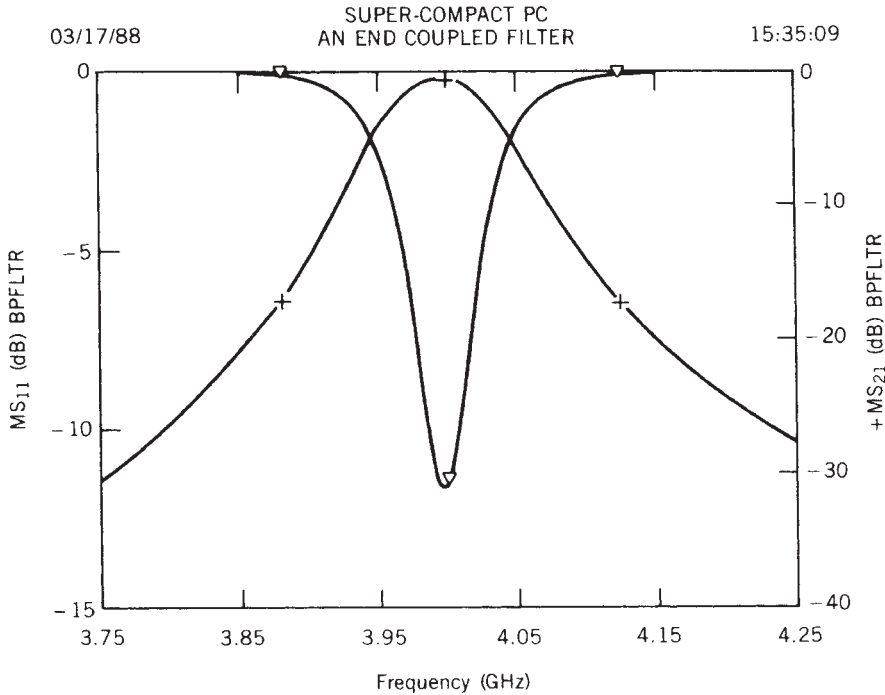
FIGURE 13.70   Frequency response of end-coupled filter.

```
      TRL   5 6 W=WW1 P=L3   SUB2
      GAP   6 7 W=WW1 G=G2   SUB1
      TRL   7 8 W=WW1  P=L1   SUB2
      GAP   8 9 W=WW1 G=G1   SUB1
      TRL   9 10   W=WW1   P=L2 SUB2
BPFLTR: 2POR 1 10
END
FREQ
    STEP 3.75GHZ 4.25GHZ 0.01GHZ
         4GHZ
END
OUT
    PRI BPFLTR SK
END
OPT
BPFLTR  F=3.98GHZ 4.02GHZ MS21 -.5DB GT
        F=4.1GHZ  5.00GHZ MS21 -15DB LT
        F=3.0GHZ  3.90GHZ MS21 -15DB LT
END
DATA
   SUB1: MS H=2.4MM ER=10.0
   SUB2: MS H=2.4MM ER=10.0 MET1=CU 35UM TAND=0.0001
END
```

APP5: Traveling-Wave Amplifier (Figs. 13.71 to 13.73) Application Note 5 shows the simulation of a traveling-wave amplifier (TWA). The distributed amplifiers provide a very flat gain slope and a bandwidth for several octaves. Today's TWAs are typically built as MMICs and the optimum number of active stages is about 4. The inductors shown compensate for the internal capacitors of the semiconductors. The active elements are simulated through simple voltage sources and the distributed transmission lines are approximated by the inductors.

```
*A TRAVELLING WAVE AMPLIFER (APP5.CKT)

L1: .5804NH
L2: .20778NH
C1: .05494PF
BLK
   CAP 1 0 C=0.25PF
   VCG 1 2 G=30MS R1=100E6 R2=100E6
```
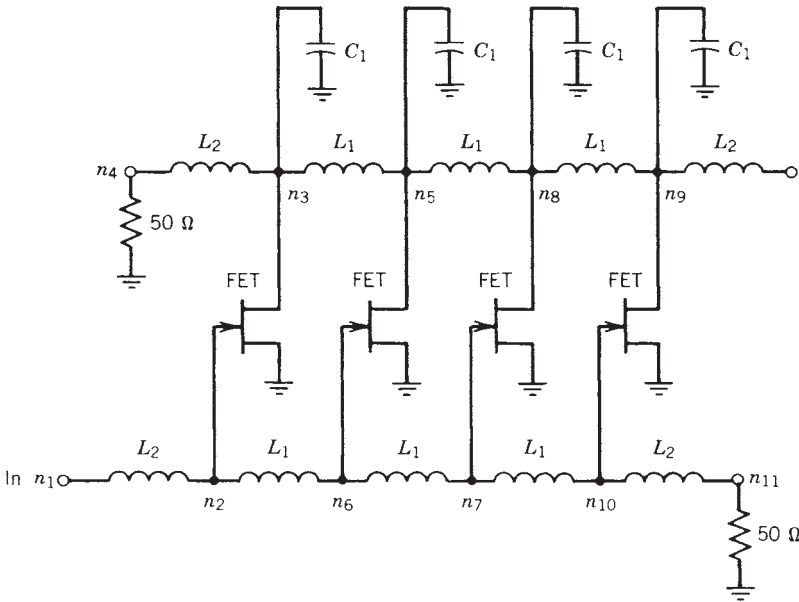

FIGURE 13.71   Traveling-wave amplifier.
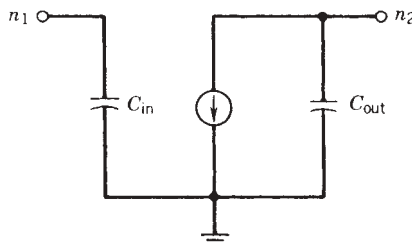
FIGURE 13.72   Equivalent FET model.
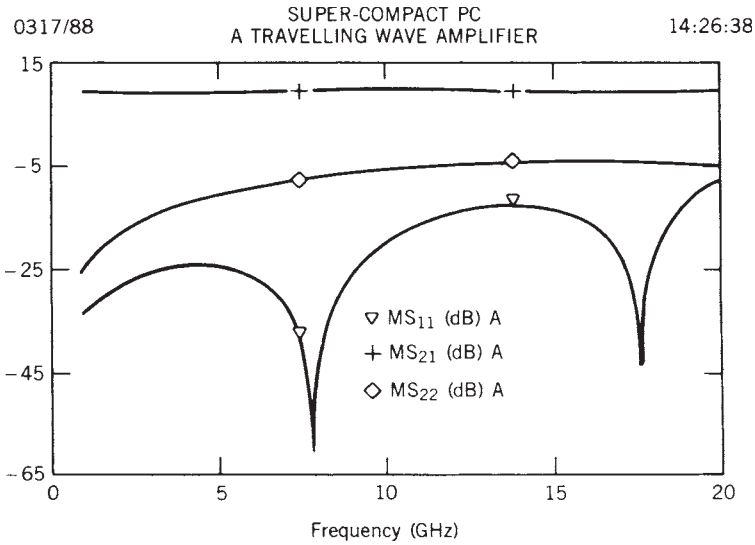
FIGURE 13.73   Frequency response of traveling-wave amplifier.

```
    CAP 2 0 C=0.025PF
FET:2POR 1 2
END
BLK
    IND 1 2   L=L2
    FET 2 3
    IND 3 4   L=L2
    RES 4 0   R=50
    CAP 3 0   C=0.225PF
    IND 2 6   L=L1
    IND 3 5   L=L1
    FET 6 5
    IND 5 8   L=L1
    CAP 5 0   C=C1
    IND 6 7   L=L1
    FET 7 8
    IND 7 10 L=L1
    CAP 8 0   C=C1
    IND 8 9   L=L1
    FET 10 9
    IND 10 11 L=L2
    RES 11 0   R=50
    CAP  9 0   C=C1
     IND 9 12   L=L2
A:2POR 1 12
END
FREQ
    STEP 1GHZ 20GHZ 0.5GHZ
END
OUT
```

```
    PRI FET S
    PRI A   S
END
```

APP6: Voltage-Controlled Oscillator (Figs. 13.74, 13.75)   Application Note 6 shows a 7.5-GHz VCO. This design takes advantage of the tweak feature of Super-Compact PC to illustrate the variation in frequency by changing the tuning diode. The capacitance, which determines the oscillating frequency, is varied to simulate the voltage change. However, as the oscillating frequency varies, the impedance (Z_{11})
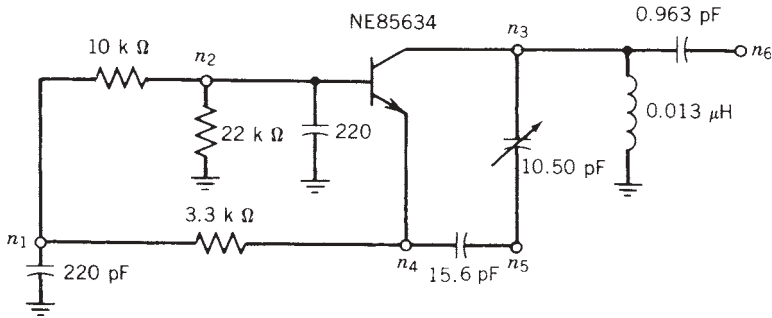
FIGURE 13.74   Voltage-controlled oscillator.
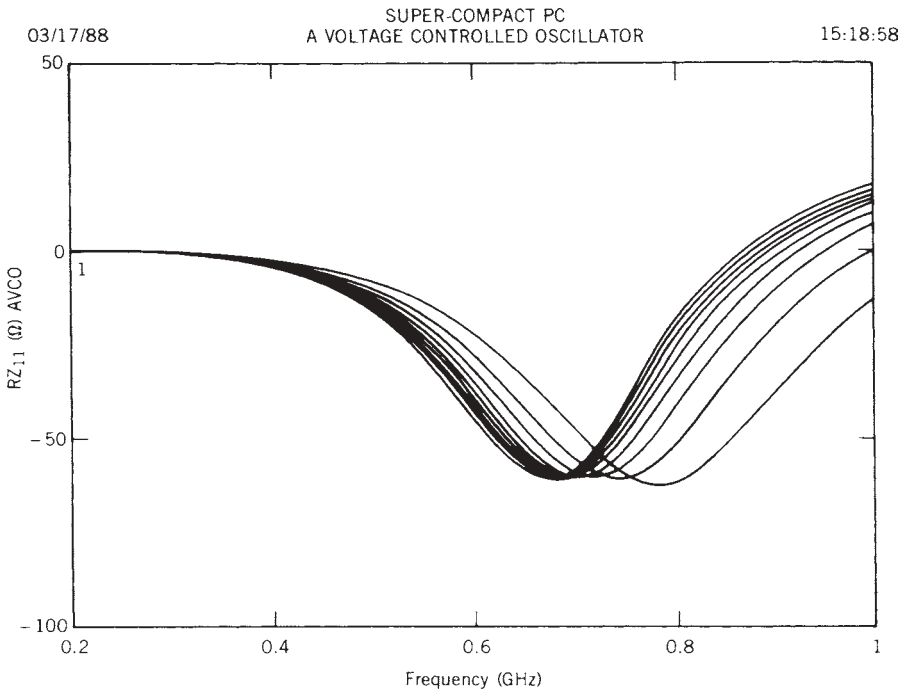
FIGURE 13.75   Optimized negative resistance for a VCO.

changes as well. Therefore, the output power will decrease if the load impedance is kept constant to 50 Ω. Seven curves are shown on the impedance plot, having initial capacitance 25 pF and final capacitance 50 pF with a step of 5 pF. The use of the databank, one feature of Super-Compact PC, is also demonstrated.

```
*                    A VCO DESIGN
*          USING THE TWEAK FEATURE OF SUPER-
*                    COMPACT PC
*                   BY ANTHONY KWAN

BLK
   RES 1 2 R=10000
   CAP 1 0 C=220PF
   RES 2 0 R=22000
   CAP 2 0 C=220PF
   TWO 2 3 4 BIPL
   RES 1 4 R=3300
   CAP 4 5 C=?15.603PF?
*THIS CAP BELOW IS BEING TWEAKED TO ADJUST THE
*OSCILLATING FREQUENCY
   CAP 3 5 C=?40.783PF?
   IND 3 0 L=?.01298UH?
   CAP 3 6 C=?.96307PF?
AVCO: 1POR 6
END
FREQ
    STEP 200MHZ 1GHZ 25MHZ

END
OUT
    PRI AVCO Z
    PRI AVCO SK
END
OPT
    AVCO F=775MHZ RZ11=-50
END
DATA
    BIPL:NECZW FILE=\BANK01\NEC.FLP
END
```

APP7: Modeling a Microwave Transistor (Figs. 13.76 to 13.80) Application Note 7 illustrates how optimization can be used to obtain a device model. The schematic diagram shows a FET model in which six components, those through which an arrow is drawn, are to be optimized. The goal of optimization is to choose values for these components such that computed S parameters for the model fit a set of measured S parameters. The model is named circuit a and is optimized subject to

$$S = Q_1$$

as specified in the OPT section.
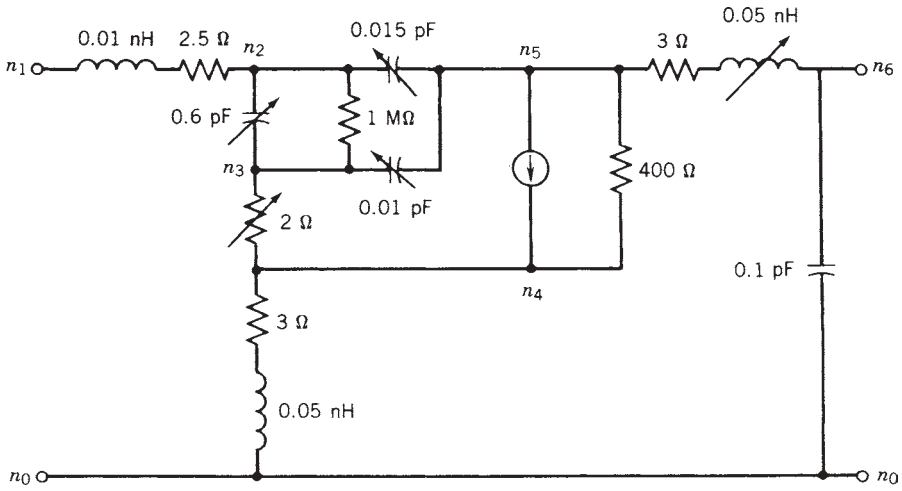
FIGURE 13.76   Equivalent circuit of a microwave transistor.
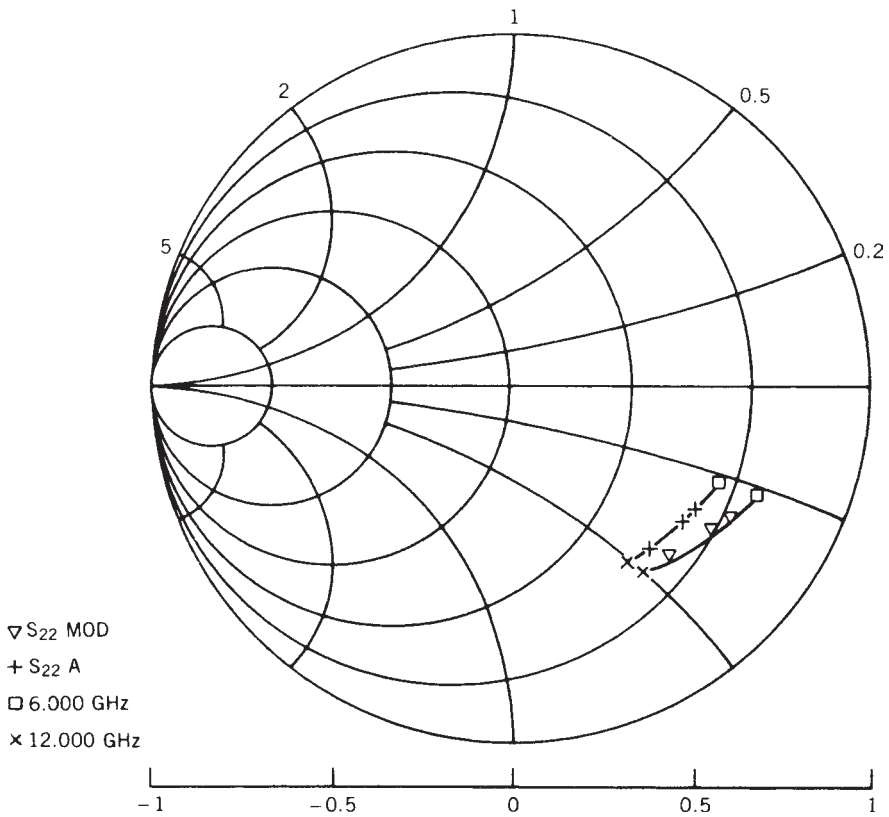
FIGURE 13.77   Frequency response of a modeled microwave transistor showing difference for S_{22}.
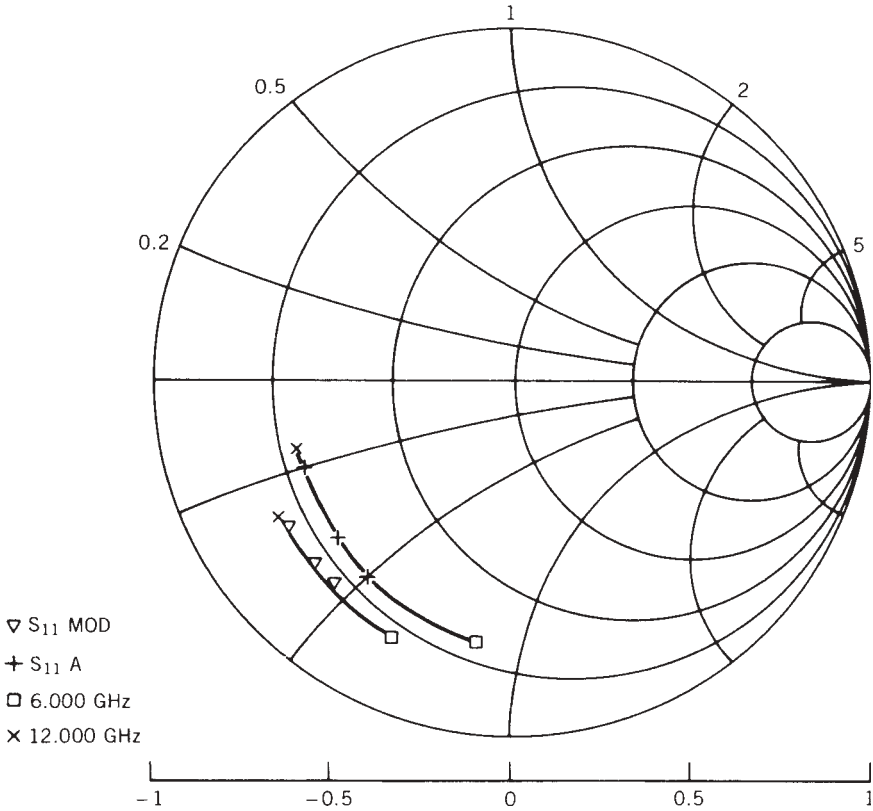
FIGURE 13.78 Frequency response of a modeled microwave transistor showing difference for S_{11}.

```
*MODELLING A MICROWAVE TRANSISTOR (APP7.CKT)

BLK
 SRL 1 2 R 2.5 L .01NH
 CAP 2 3 C ?.84279PF?
 RES 3 4 R ?3.1794?
 SRL 4 R 3 L .05NH
 CAP 2 5 C ?.01448PF?
 SRL 5 6 R 3 L ?.39433NH?
 CAP 6 C ?374.72E-9PF?
* NOTE GM IS IN MHOS
 VCG 2 5 3 4 G 0.05 R1 1E6 R2 400 F 1E18 T 5E-12
 CAP 3 5 C ?.10032PF?
MOD: 2POR 1 6
END
BLK
    TWO 1 2 Q1
A:2POR 1 2
END
FREQ
```
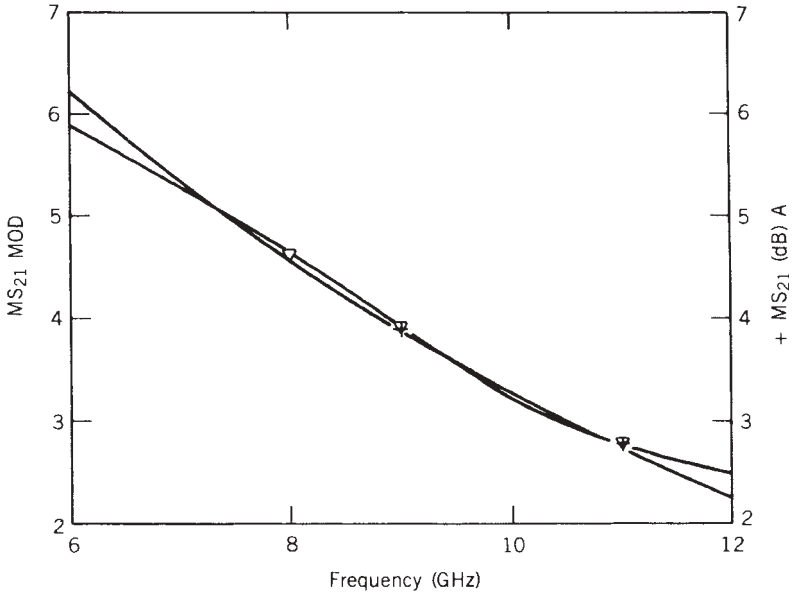
FIGURE 13.79 Frequency response of a modeled microwave transistor showing difference for S_{21}.
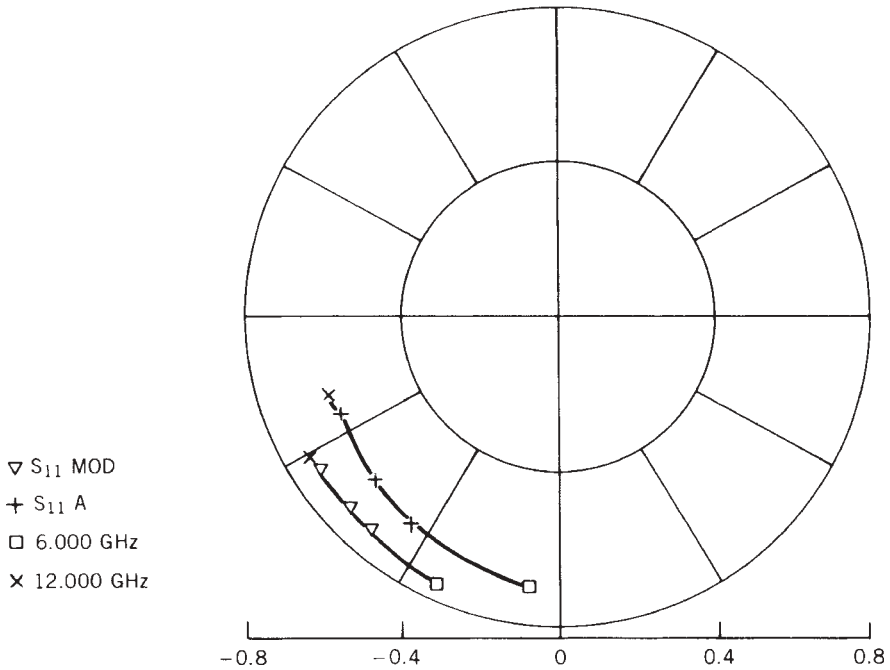
FIGURE 13.80 Frequency response of a modeled microwave transistor showing difference for S_{12}.

```
 6GHZ 7GHZ 8GHZ 9GHZ 10GHZ 11GHZ 12GHZ
END
OUT
 PRI MOD SK
 PRI A SK
END
OPT
*
* MATCH COMPUTER MODEL TO MEASURED DATA
* ORDER OF WEIGHTS IS 11, 12, 21 AND 22
*
 MOD S=Q1 W 10 10 10 10
 TERM .01
END
DATA
*  DATA FOR HPMPP WITH PARASITIC LEAD INDUCTANCES
Q1:S
 6GHZ 0.732   -96.3 1.973 99.3 0.051 69.8 0.642 -26.0
 7GHZ 0.699 -110.9 1.835 88.2 0.058 70.8 0.629 -30.3
 8GHZ 0.673 -124.4 1.708 78.4 0.066 73.2 0.618 -34.8
 9GHZ 0.644 -136.9 1.570 69.8 0.073 77.3 0.613 -39.5
10GHZ 0.622 -147.5 1.449 61.7 0.081 82.7 0.610 -44.9
11GHZ 0.616 -154.8 1.378 53.5 0.093 87.7 0.605 -51.1
12GHZ 0.623 -160.1 1.332 44.6 0.108 90.7 0.602 -58.1
```

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APPENDIX A

BIP: GUMMEL–POON BIPOLAR TRANSISTOR MODEL

TOPOLOGY OF INTRINSIC AND EXTRINSIC MODEL
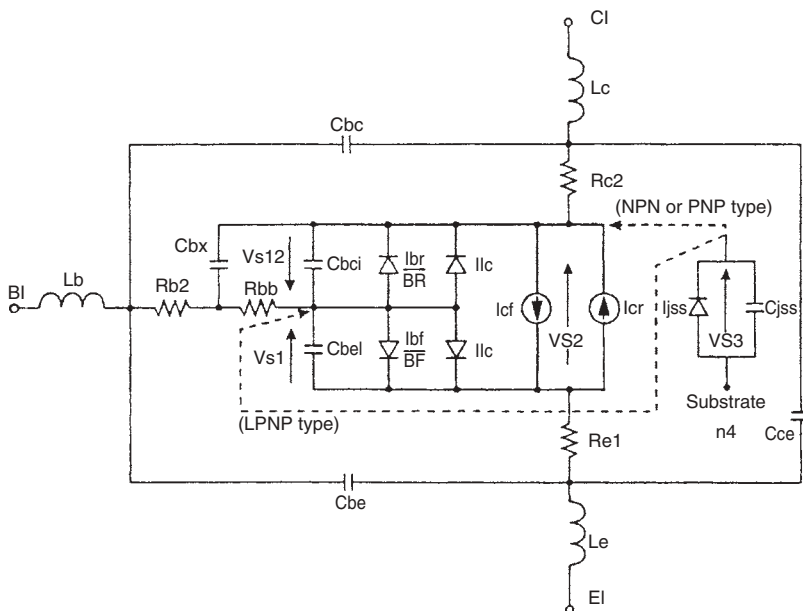
The *npn* transistor model is shown. The *pnp* transistor model has all currents and voltages in the opposite polarity.

TOPOLOGY OF PACKAGE MODEL
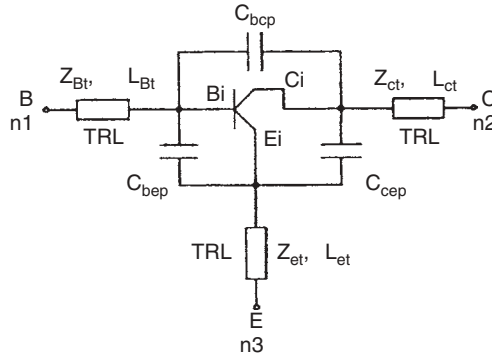
INTRINSIC MODEL KEYWORDS

Keyword	Description	Unit	Default
NPN	Model polarity	—	*npn*
PNP	Model polarity	—	*pnp*
LPNP	Selects lateral *pnp* model substrate connection	—	L_{pnp}
IS	Transport saturation current	A	1E-16
ISE	Base–emitter leakage saturation current	A	0
ISC	Base–collector leakage saturation current	A	0
BF	Ideal forward-current gain	—	100.0
BR	Ideal reverse-current gain	—	1.0
NF	Forward-current emission coefficient	—	1.0
NE	Base–emitter leakage emission coefficient	—	1.5
NR	Reverse-current emission coefficient	—	1.0
NC	Base–collector emission coefficient	—	2.0
VA	Forward Early voltage (alternate keyword: VAF)	V	inf
VB	Reverse Early voltage (alternate keyword: VAR)	V	inf
IKF	Corner for forward-beta high-current rolloff	A	inf
IKR	Corner for reverse-beta high-current rolloff	A	inf
RBM	Minimum base resistance	Ω	RB
RB	Maximum (zero-bias) base resistance	Ω	0
IRB	Current where R_{bb} falls halfway to RBM	A	inf
TF	Ideal forward transit time	s	0
TR	Ideal reverse transit time	s	0
ITF	Transit time dependency on I_c	A	0
XTF	Transit time bias dependence coefficient	—	0
VTF	Transit time bias dependence on V_{bc}	V	inf
FCC	Forward-bias depletion capacitor coefficient	—	0.5
VJE	Base–emitter built-in potential	V	0.75
MJE	Base–emitter *pn* grading factor	—	0.33
VJC	Base–collector built-in potential	V	0.75
MJC	Base–collector *pn* grading factor	—	0.33
CJC	Base–collector zero-bias capacitance	F	0.0

Keyword	Description	Unit	Default
CJE	Base–emitter zero-bias capacitance	F	0.0
XCJC	Fraction of C_{bc} connected to intrinsic R_{bb}	—	1.0
PTF	Excess phase at $1/(2\pi\ TF)$	degree	0
NKF	Exponent for high-current beta rolloff	—	0.5
UPDATE	Selects alternate base charge equation (alternate keyword: GPQ1)	—	0.0
ISS	Substrate leakage saturation current	A	0.0
NS	Substrate pn emission coefficient	—	1.0
CJS	Substrate–base/collector zero-bias capacitance	F	0.0
MJS	Substrate pn grading factor	—	0.33
VJS	Substrate junction built-in potential	V	0.75
KF	Flicker noise coefficient	—	0.0
AF	Flicker noise exponent	—	1.0
FCP	Flicker noise frequency shape factor	—	1.0
SN	Switch to turn device shot noise on or off (1 or 0)	—	1
AREA	Area multiplier	—	1.0
NOIS	Reference label to a set of noise data	—	—
NAME	Required user-specified name up to eight characters	—	—

EXTRINSIC MODEL KEYWORDS

Keyword	Description	Unit	Default
RB2	Base ohmic resistance	Ω	0
RC2	Collector ohmic resistance	Ω	0
RE1	Emitter ohmic resistance	Ω	0
CBE	Base–emitter external capacitance	F	0
CBC	Base–collector external capacitance	F	0
CCE	Collector–emitter external capacitance	F	0
LB	Base-lead inductance	H	0
LC	Collector-lead inductance	H	0
LE	Emitter-lead inductance	H	0
CBCP	Base–collector package capacitance	F	0
CBEP	Base–emitter package capacitance	F	0
CCEP	Collector–emitter package capacitance	F	0
ZBT	Base transmission line impedance	Ω	50
ZCT	Collector transmission line impedance	Ω	50
ZET	Emitter transmission line impedance	Ω	50
LBT	Base transmission line length, $\varepsilon_r = 1$	m	0
LCT	Collector transmission line length, $\varepsilon_r = 1$	m	0
LET	Emitter transmission line length, $\varepsilon_r = 1$	m	0

TEMPERATURE COEFFICIENT KEYWORDS

Keyword	Description	Unit	Default
TJ	Junction temperature	K	298
TNOM	Reference temperature	K	298
XTI	IS, ISE, and ISC temperature exponent	—	2.0
XTB	BF and BR temperature exponent	—	0
EG	Band gap voltage at 0 K	eV	1.16
TRB1	RB linear temperature coefficient (alternate keyword: ARB)	K^{-1}	0
TRB2	RB quadratic temperature coefficient (alternate keyword: BRB)	K^{-2}	0
TRM1	RBM linear temperature coefficient (alternate keyword: ARBM)	K^{-1}	0
TRM2	RBM quadratic temperature coefficient (alternate keyword: BRBM)	K^{-2}	0
TRC1	RC2 linear temperature coefficient (alternate keyword: ARC2)	K^{-1}	0
TRC2	RC2 quadratic temperature coefficient (alternate keyword: BRC2)	K^{-2}	0
TRE1	RE1 linear temperature coefficient (alternate keyword: ARE1)	K^{-1}	0
TRE2	RE1 quadratic temperature coefficient (alternate keyword: BRE1)	K^{-2}	0

DEVICE EQUATIONS

The following equations are used for the model:

$$V_{s1} = \text{intrinsic base–emitter voltage state variable}$$

$$V_{s12} = \text{intrinsic base–collector voltage}$$

$$V_{bx} = \text{extrinsic base–intrinsic collector voltage}$$

$$V_{s2} = \text{intrinsic collector–emitter voltage state variable}$$

$$V_{s3} = \text{voltage across substrate junction}$$

$$V_t = kTJ/q \text{ (thermal voltage)}$$

$$k = \text{Boltzmann's constant}$$

$$q = \text{electron charge}$$

$$T_J = \text{analysis temperature (kelvins)}$$

Conduction Currents

$$I_b = \text{base current} = \frac{I_{bf}}{\text{BF}} + I_{ie} + \frac{I_{br}}{\text{BR}} + I_{ic}$$

$$I_c = \text{collector current} = \frac{I_{bf}}{K_{qb}} - \frac{I_{br}}{K_{qb}} - \frac{I_{br}}{\text{BR}} - I_{ic}$$

$$I_{bf} = \text{forward diffusion current} = \text{IS}\left[\exp\left(\frac{V_{s1}}{\text{NF } V_t}\right) - 1\right]$$

$$I_{ie} = \text{nonideal base–emitter current} = \text{ISE}\left[\exp\left(\frac{V_{s1}}{\text{NE } V_t}\right) - 1\right]$$

$$I_{br} = \text{reverse diffusion current} = \text{IS}\left[\exp\left(\frac{V_{s12}}{\text{NR } V_t}\right) - 1\right]$$

$$I_{ic} = \text{nonideal base–collector current} = \text{ISC}\left[\exp\left(\frac{V_{s12}}{\text{NC } V_t}\right) - 1\right]$$

$$I_{cf} = \frac{I_{bf}}{K_{qb}}$$

$$I_{cr} = \frac{I_{br}}{K_{qb}}$$

$$I_{jss} = \text{substrate current} = \text{ISS}\left[\exp\left(\frac{V_{s3}}{\text{NS } V_t}\right) - 1\right]$$

$$K_{qb} = \text{base charge factor} = \frac{K_{q1}}{2}[1 + (1 + 4K_{q2})^{\text{NKF}}]$$

$$K_{q1} = \begin{cases} \dfrac{1}{1 - V_{s12}/\text{VA} - V_{s1}/\text{VB}} & \text{UPDATE} = 0 \quad \text{or} \quad \dfrac{V_{s12}}{VA} + \dfrac{V_{s1}}{VB} \leq 0 \\[3mm] \dfrac{1}{1 + V_{s12}/\text{VA} + V_{s1}/\text{VB}} & \text{otherwise} \end{cases}$$

$$K_{q2} = \frac{I_{bf}}{\text{IKF}} + \frac{I_{br}}{\text{IKR}}$$

$$R_{bb} = \begin{cases} \text{RBM} + \dfrac{\text{RB} - \text{RBM}}{K_{qb}} & \text{IRB} = \infty \ (\text{default}) \\[3mm] \text{RBM} + 3(\text{RB} - \text{RBM})\dfrac{\tan(x) - x}{x\tan^2(x)} & \text{IRB} > 0 \end{cases}$$

where

$$x = \frac{\sqrt{1 + 144 I_b/\text{IRB}\pi^2} - 1}{(24/\pi^2)\sqrt{I_b/\text{IRB}}}$$

Capacitances

$$C_{bei} = \text{base–emitter capacitance} = C_{bet} + C_{bej}$$

$$C_{bet} = \text{transmit time capacitance} = \frac{\partial}{\partial V_{s1}}\left(t_f \frac{I_{bf}}{K_{qb}}\right)$$

$$t_f = \text{effective TF} = \text{TF}\left[1 + \text{XTF } x^2 \exp\left[\frac{V_{s12}}{1.44\text{VTF}}\right]\right]$$

where $x = I_{bf}/I_{bf} + \text{ITF}$.

$$C_{bej} = \begin{cases} \text{CJE}\left(1 - \dfrac{V_{s1}}{\text{VJE}}\right)^{-\text{MJE}} & V_{s1} \leq \text{FCC} \times \text{VJE} \\[2ex] \text{CJE}(1 - \text{FCC})^{-(1+\text{MJE})} \\[1ex] \times \left(1 - \text{FCC}(1 + \text{MJE}) + \text{MJE}\dfrac{V_{s1}}{\text{VJE}}\right) & V_{s1} > \text{FCC} \times \text{VJE} \end{cases}$$

$C_{bci} = \text{base–collector capacitance} = C_{bct} + \text{XCJC } C_{bcj}$

$C_{bct} = \text{transit time capacitance} = \text{TR } G_{bc}$

$G_{bc} = \text{base–collector conductance} = \dfrac{\partial I_{br}}{\partial V_{s12}}$

$$C_{bcj} = \begin{cases} \text{CJC}\left(1 - \dfrac{V_{s12}}{\text{VJC}}\right)^{-\text{MJC}} & V_{s12} \leq \text{FCC} \times \text{VJC} \\[2ex] \text{CJC}(1 - \text{FCC})^{-(1+\text{MJC})} \\[1ex] \times \left(1 - \text{FCC}(1 + \text{MJC}) + \text{MJC}\dfrac{V_{s12}}{\text{VJC}}\right) & V_{s12} > \text{FCC} \times \text{VJC} \end{cases}$$

$C_{bx} = \text{extrinsic base–intrinsic collector capacitance} = (1 - \text{XCJC})C_{bxj}$

$$C_{bxj} = \begin{cases} \text{CJC}\left(1 - \dfrac{V_{bx}}{\text{VJC}}\right)^{-\text{MJC}} & V_{bx} \leq \text{FCC} \times \text{VJC} \\[2ex] \text{CJC}(1 - \text{FCC})^{-(1+\text{MJC})} \\[1ex] \times \left(1 - \text{FCC}(1 + \text{MJC}) + \text{MJC}\dfrac{V_{bx}}{\text{VJC}}\right) & V_{bx} > \text{FCC} \times \text{VJC} \end{cases}$$

$$C_{jss} = \text{substrate capacitance} = \begin{cases} \text{CJS}\left(1 - \dfrac{V_{s3}}{\text{VJS}}\right)^{-\text{MJS}} & V_{s3} \leq 0 \\[2ex] \text{CJS}\left(1 + \text{MJS}\dfrac{V_{s3}}{\text{VJS}}\right) & V_{s3} > 0 \end{cases}$$

AREA EFFECTS

$$\begin{aligned} I_{bf} &= \text{AREA} \times I_{bf} & I_{br} &= \text{AREA} \times I_{br} \\ I_{ie} &= \text{AREA} \times I_{ie} & I_{ic} &= \text{AREA} \times I_{ic} \\ I_{cf} &= \text{AREA} \times I_{cf} & I_{cr} &= \text{AREA} \times I_{cr} \\ C_{bc} &= \text{AREA} \times C_{bc} & C_{be} &= \text{AREA} \times C_{be} \\ C_{bx} &= \text{AREA} \times C_{bx} & R_{bb} &= \frac{R_{bb}}{\text{AREA}} \end{aligned}$$

$$RB2 = \frac{RB2}{AREA} \quad RC2 = \frac{RC2}{AREA}$$

$$RE1 = \frac{RE1}{AREA} \quad I_{jss} = AREA \times I_{jss}$$

$$C_{jss} = AREA \times C_{jss}$$

TEMPERATURE EFFECTS

Define $\Delta t = TJ - TNOM$; $tn = TJ/TNOM$.

$$IS(TJ) = IS \exp\left[\frac{(tn-1)EG}{V_t}\right] tn^{XTI/NF}$$

$$ISE(TJ) = ISE \exp\left[\frac{(tn-1)EG}{V_t}\right] tn^{XTI/NE}$$

$$ISC(TJ) = ISC \exp\left[\frac{(tn-1)EG}{V_t}\right] tn^{XTI/NC}$$

$$ISS(TJ) = ISS \exp\left[\frac{(tn-1)EG}{V_t}\right] tn^{XTI/NS}$$

$$\beta(TJ) = \beta\, tn^{XTB}$$

where β is BF or BR.

$$V_{bi}(TJ) = V_{bi}tn - 3V_t \ln(tn) - tn\, EGap(TNOM) + EGap(TJ)$$

where V_{bi} is VJE, VJC, or VJS.

$$EGap(TJ) = EG - 0.000702\frac{TJ^2}{TJ + 1108}$$

$$C_j(TJ) = C_j\left[1 + M_j\left(0.0004\,\Delta t + 1 - \frac{V_{bi}(TJ)}{V_{bi}}\right)\right]$$

where C_j, M_j, and V_{bi} are (CJE, MJE, and VJE), (CJC, MJC, and VJC), and (CSS, MJS and VJS), respectively.

$$R(TJ) = R(1 + AR\,\Delta t + BR\,\Delta t^2)$$

where R is RB, RBM, RC2, or RE1; AR refers to the linear temperature coefficient, for example, ARB; and BR refers to the quadratic temperature coefficient, for example, BRB.

APPENDIX B

LEVEL 3 MOSFET

$$I_{DS} = \beta \left(V_{GS} - V_{\text{TH}} - \frac{1 + F_B}{2} V_{DS} \right) V_{DS} \tag{B.1}$$

where

$$\beta = \mu_{\text{eff}} C_{ox} \frac{W}{L_{\text{eff}}} \tag{B.2}$$

$$\mu_s = \frac{UO}{1 + \theta(V_{GS} - V_{\text{TH}})} \tag{B.3}$$

$$\mu_{\text{eff}} = \frac{\mu_o}{1 + \dfrac{\mu_s}{V_{\text{max}} L_{\text{eff}}} V_{DS}} \tag{B.4}$$

The threshold voltage is defined by

$$V_{\text{TH}} = V_{FB} + \phi - \sigma V_{DS} + \gamma F_S \sqrt{\phi - V_{BS}} + F_N(\phi - V_{BS}) \tag{B.5}$$

where

$$\sigma = \eta \frac{8.15 \times 10^{-22}}{C_{ox} L_{\text{eff}}^3} \tag{B.6}$$

$$F_S = 1 - \frac{X_J}{L_{\text{eff}}} \left[\frac{LD + W_C}{X_J} \sqrt{1 - \left(\frac{W_P / X_J}{1 + W_P / X_J} \right)^2} - \frac{LD}{X_J} \right] \tag{B.7}$$

$$F_N = \Delta \frac{\pi \varepsilon_{\text{Si}}}{2C_{ox}W} \tag{B.8}$$

$$F_B = \frac{\gamma F_S}{4\sqrt{\phi - V_{BS}}} + F_N \tag{B.9}$$

$$W_P = X_d\sqrt{\phi - V_{BS}}$$
$$\frac{W_C}{X_J} = d_0 + d_1\frac{W_P}{X_J} + d_2\left(\frac{W_P}{X_J}\right)^2 \tag{B.10}$$

$$d_0 = 0.0631353 \qquad d_1 = 0.8013292 \qquad d_2 = -0.01110777$$

The saturation model is based on velocity-limited carrier flow:

$$V_{D,\text{SAT}} = \frac{V_{GS} - V_{\text{TH}}}{1 + F_B} + \frac{V_{\max}L_{\text{eff}}}{\mu_s} - \sqrt{\left(\frac{V_{GS} - V_{\text{TH}}}{1 + F_B}\right)^2 + \left(\frac{V_{\max}L_{\text{eff}}}{\mu_s}\right)^2} \tag{B.11}$$

$$\Delta L = X_d\left[\sqrt{\left(\frac{E_P X_d}{2}\right)^2 + \kappa(V_{DS} - V_{D,\text{SAT}})} - \frac{E_P X_d}{2}\right] \tag{B.12}$$

where

$$E_P = \frac{I_{D,\text{SAT}}}{G_{D,\text{SAT}}L_{\text{eff}}}$$

CAPACITANCE MODEL

The gate capacitances defined by the Meyer model, C_{GS}, C_{GD}, and C_{GB}, are listed below for the three main regions of operation of a MOSFET. In the cutoff region, $V_{GS} \le V_{\text{TH}}$, all three capacitances are constant:

$$C_{GB} = C_{OX} + \text{CGBO } L_{\text{eff}}$$
$$C_{GS} = \text{CGSO } W \tag{B.13}$$
$$C_{GD} = \text{CGDO } W$$

In saturation, $V_{\text{TH}} < V_{GS} \le V_{\text{TH}} + V_{DS}$, the expressions are

$$C_{GB} = \text{CGBO } L_{\text{eff}}$$
$$C_{GS} = \frac{2}{3}C_{OX} + \text{CGSO } W \tag{B.14}$$
$$C_{GD} = \text{CGDO } W$$

In linear operation, $V_{GS} > V_{\text{TH}} + V_{DS}$,

$$C_{GB} = \text{CGBO } L_{\text{eff}}$$
$$C_{GS} = C_{OX}\left\{1 - \left[\frac{V_{GS} - V_{DS} - V_{ON}}{2(V_{GS} - V_{ON}) - V_{DS}}\right]^2\right\} + \text{CGSO } W \tag{B.15}$$

$$C_{GD} = C_{OX}\left\{1 - \left[\frac{V_{GS} - V_{ON}}{2(V_{GS} - V_{ON}) - V_{DS}}\right]^2\right\} + \text{CGDO } W$$

where

$$C_{OX} = C_{ox} W L_{\text{eff}}$$

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{T_{OX}}$$

The charge conservation model derives asymmetrical capacitances according to the following definitions:

$$Q_{\text{chan}} = Q_D + Q_S = -(Q_G + Q_B) \tag{B.16}$$

$$Q_D = \text{XQC}Q_{\text{chan}} \tag{B.17}$$

$$C_{xy} = \frac{\partial Q_x}{\partial V_y} \neq \frac{\partial Q_y}{\partial V_x} = C_{yx} \tag{B.18}$$

TEMPERATURE MODEL

In addition to I_S, ϕ_J, and C_J, which have the temperature dependence described for the diode, the intrinsic concentration n_i and the mobility are adjusted for temperature:

$$n_i(T) = n_i(300)\left(\frac{T}{300}\right)^{1.5}\exp\left[\frac{q}{2k}\left(\frac{1.16 \text{ eV}}{300 \text{ K}} - \frac{E_g}{T}\right)\right] \tag{B.19}$$

$$n_i(300) = 1.45 \times 10^{10} \text{ m}^{-3}$$

$$\mu(T) = \mu(300)\left(\frac{300}{T}\right)^{1.5} \tag{B.20}$$

NOISE MODEL

The noise contributed by the drain–source current is

$$\overline{i_{ds}^2} = \frac{8kT_{gm}}{3}\Delta f + \frac{\text{KF } I_{DS}^{\text{AF}}}{f C_{ox} L_{\text{eff}}^2}\Delta f \tag{B.21}$$

APPENDIX C

NOISE PARAMETERS OF GaAs MESFETs

Figure C.1 shows the noise model of a FET with a noise source at the input and the output:

$$\overline{i_d^2} = 4kTg_m P \ \Delta f$$

$$\overline{i_g^2} = \frac{4kT(wC_{gs})^2 R}{g_m} \Delta f$$

$$\overline{i_g i_d^\bullet} = -jwC_{gs} 4kTC \sqrt{PR} \ \Delta f$$

$$S(i_d) = \frac{\overline{i_d^2}}{\Delta f} = \left\langle |\overline{i_d^2}| \right\rangle = 4kTg_m P$$
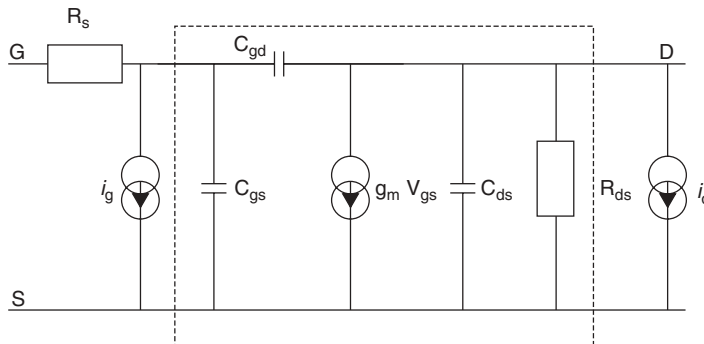
FIGURE C.1   Intrinsic FET and noise.

$$S(i_g) = \frac{\overline{i_g^2}}{\Delta f} = \left\langle \overline{|i_g^2|} \right\rangle = \frac{4kT(wC_{gs})^2 R}{g_m}$$

$$S(i_g i_d^\bullet) = \left\langle \overline{|i_g i_d^\bullet|} \right\rangle = -jwC_{gs} 4kTC\sqrt{PR}$$

where P, R, and C are FET noise coefficients.

Noise parameters are calculated as follows (Fig. C.2):

$$[Y]_{tr} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$$

$$[C_Y] = [N]_{\text{noise matrix}} = \begin{bmatrix} \overline{i_g i_g^\bullet} & \overline{i_g i_d^\bullet} \\ \overline{i_d i_g^\bullet} & \overline{i_d i_d^\bullet} \end{bmatrix}$$

$$[C_Y]_{tr} = 4kT \begin{bmatrix} \dfrac{w^2 c_{gs}^2 R}{g_m} & -jwc_{gs} C\sqrt{PR} \\ jwc_{gs} C\sqrt{PR} & g_m P \end{bmatrix}$$

A noise transformation from the output to the input can be done for simplification to calculate the noise parameters (Fig. C.3):

$$[C_a]_{tr} = \begin{bmatrix} \overline{e_n e_n^\bullet} & \overline{e_n i_n^\bullet} \\ \overline{i_n e_n^\bullet} & \overline{i_n i_n^\bullet} \end{bmatrix}$$

$$[C_a]_{tr} = [T][C_Y]_{tr}[T]^+$$
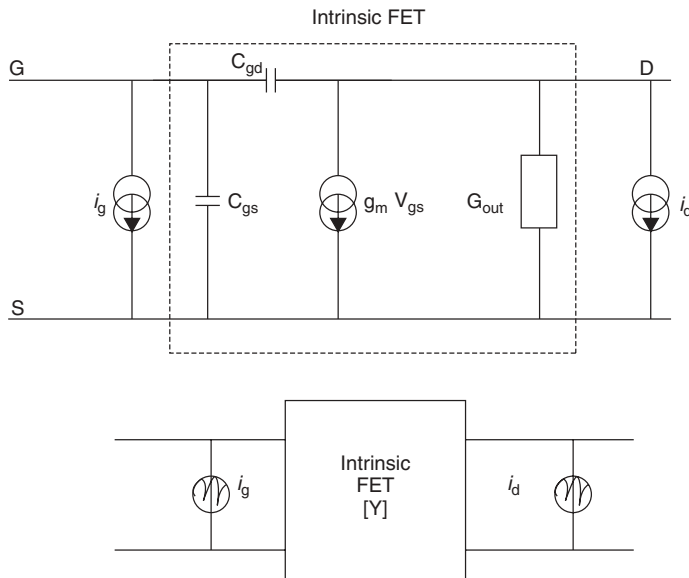
FIGURE C.2   Y parameter of Intrinsic FET and noise current sources.
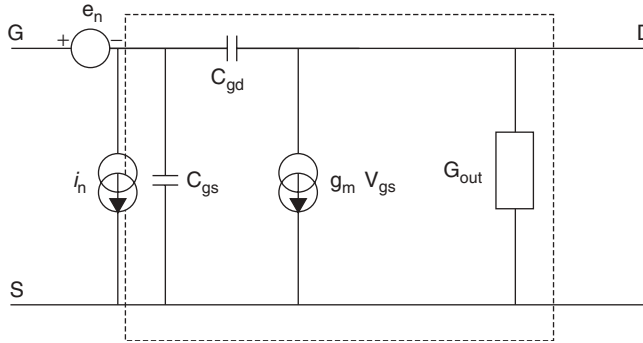
FIGURE C.3   Intrinsic FET with noise sources at input.

$$[T] = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix}$$

$$[C_a]_{tr} = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix} [C_Y]_{tr} \begin{bmatrix} 0 & 1 \\ B_{CS}^{\bullet} & D_{CS}^{\bullet} \end{bmatrix}$$

The following shows the calculations:

$$[ABCD]_{FET} = \begin{bmatrix} A_{CS} & B_{CS} \\ C_{CS} & D_{CS} \end{bmatrix} = \begin{bmatrix} 1 & R_s \\ 0 & 1 \end{bmatrix}$$

$$\times \begin{bmatrix} 1 & 0 \\ sc_{gs} & 1 \end{bmatrix} \begin{bmatrix} \dfrac{sc_{gd}}{sc_{gd} - g_m} & \dfrac{1}{sc_{gd} - g_m} \\ \dfrac{g_m sc_{gd}}{sc_{gd} - g_m} & \dfrac{sc_{gd}}{sc_{gd} - g_m} \end{bmatrix} \begin{bmatrix} 1 & 0 \\ g_{ds} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sc_{ds} & 1 \end{bmatrix}$$

$$= \begin{bmatrix} 1 & R_s \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \dfrac{sc_{gd}}{sc_{gd} - g_m} & \dfrac{1}{sc_{gd} - g_m} \\ \dfrac{sc_{gd}(g_m + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} & \dfrac{sc_{gd} + g_{ds} + sc_{gs} + sc_{ds}}{sc_{gd} - g_m} \end{bmatrix}$$

$$= \begin{bmatrix} \dfrac{sc_{gd}}{sc_{gd} - g_m} & \dfrac{1}{sc_{gd} - g_m} \\ + \left(\dfrac{\begin{matrix} R_s sc_{gd}(g_m + g_{ds}) \\ + sc_{gs} + sc_{ds}) \end{matrix}}{sc_{gd} - g_m} \right) & + \left(\dfrac{\begin{matrix} R_s(sc_{gd} + g_{ds}) \\ + sc_{gs} + sc_{ds}) \end{matrix}}{sc_{gd} - g_m} \right) \\ \dfrac{sc_{gd}(g_m + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} & \dfrac{sc_{gd} + g_{ds} + sc_{gs} + sc_{ds}}{sc_{gd} - g_m} \end{bmatrix}$$

$$[C_Y]_{FET} = 4kT \begin{bmatrix} \dfrac{w^2 c_{gs}^2 R}{g_m} & -jwc_{gs}C\sqrt{PR} \\ jwc_{gs}C\sqrt{PR} & g_m P \end{bmatrix}$$

$$[C_a]_{\text{FET}} = [T][C_Y]_{\text{tr}}[T]^+$$

$$= \begin{bmatrix} 0 & \dfrac{1}{sc_{gd} - g_m} + \dfrac{R_s(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \\[3mm] 1 & \dfrac{sc_{gd} + g_{ds} + sc_{gs} + sc_{ds}}{sc_{gd} - g_m} \end{bmatrix}$$

$$\times\, 4kT \begin{bmatrix} \dfrac{w^2 c_{gs}^2 R}{g_m} & -jwc_{gs}C\sqrt{PR} \\[3mm] jwc_{gs}C\sqrt{PR} & g_m P \end{bmatrix} \times K_1$$

$$K_1 = \begin{bmatrix} 0 & 1 \\[3mm] \left(\dfrac{\dfrac{1}{sc_{gd}-g_m}}{+\dfrac{R_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}} \right)^{\!\bullet} & \left(\dfrac{sc_{gd}+g_{ds}+sc_{gs}+sc_{ds}}{sc_{gd}-g_m} \right)^{\!\bullet} \end{bmatrix}$$

$$= 4kT \begin{bmatrix} \dfrac{sc_{gs}C\sqrt{PR}}{sc_{gd}-g_m} + \left(\dfrac{sc_{gs}R_sC\sqrt{PR}(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m} \right) & \dfrac{g_m P}{sc_{gd}-g_m} + \left(\dfrac{g_m P R_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m} \right) \\[6mm] \dfrac{w^2 c_{gs}^2 R}{g_m} + \left(\dfrac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})sc_{gs}C\sqrt{PR}}{sc_{gd}-g_m} \right) & -jwc_{gs}C\sqrt{PR} + \left(\dfrac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})g_m P}{sc_{gd}-g_m} \right) \end{bmatrix} \times K_2$$

$$K_2 = \begin{bmatrix} 0 & 1 \\[3mm] \left(\dfrac{\dfrac{1}{sc_{gd}-g_m}}{+\dfrac{R_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}} \right)^{\!\bullet} & \left(\dfrac{sc_{gd}+g_{ds}+sc_{gs}+sc_{ds}}{sc_{gd}-g_m} \right)^{\!\bullet} \end{bmatrix}$$

$$[C_a]_{\text{FET}} = \begin{bmatrix} C_{uu}^\bullet & C_{ui}^\bullet \\ C_{u^\bullet i} & C_{ii}^\bullet \end{bmatrix} = \begin{bmatrix} R_n & \dfrac{F_{\min}-1}{2} - R_n Y_{\text{opt}}^\bullet \\[3mm] \dfrac{F_{\min}-1}{2} - R_n Y_{\text{opt}} & R_n |Y_{\text{opt}}|^2 \end{bmatrix}$$

$$C_{uu\bullet} = 4kT \left[\left(\frac{g_m P}{sc_{gd} - g_m} + \frac{g_m P R_s (sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right) \right.$$

$$\left. \times \left(\frac{1}{sc_{gd} - g_m} + \frac{R_s (sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right)^{\bullet} \right]$$

$$C_{ui\bullet} = 4kT \left(\frac{sc_{gs} C \sqrt{PR}}{sc_{gd} - g_m} + \frac{sc_{gs} R_s C \sqrt{PR}(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right) + A_1$$

$$A_1 = \left[\left(\frac{g_m P}{sc_{gd} - g_m} + \frac{g_m P R_s (sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right) \right.$$

$$\left. \times \left(\frac{(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right)^{\bullet} \right]$$

$$C_{u\bullet i} = 4kT \left[\left(-jwc_{gs} C \sqrt{PR} + \frac{(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})g_m P}{sc_{gd} - g_m} \right) \right.$$

$$\left. \times \left(\frac{1}{sc_{gd} - g_m} + \frac{R_s (sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})}{sc_{gd} - g_m} \right)^{\bullet} \right]$$

$$C_{ii\bullet} = 4kT \left[\left(\frac{w^2 c_{gs}^2 R}{g_m} + \frac{(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})sc_{gs} C \sqrt{PR}}{sc_{gd} - g_m} \right) + B_1 \right]$$

$$B_1 = \left(-jwc_{gs} C \sqrt{PR} + \frac{(sc_{gd} + g_{ds} + sc_{gs} + sc_{ds})g_m P}{sc_{gd} - g_m} \right)$$

$$\times \left(\frac{sc_{gd} + g_{ds} + sc_{gs} + sc_{ds}}{sc_{gd} - g_m} \right)^{\bullet};$$

and finally

$$R_n = \frac{C_{uu\bullet}}{2kT}$$

$$F_{\min} = 1 + \frac{C_{ui\bullet} + C_{uu\bullet} Y_{\text{opt}}}{kT}$$

$$Y_{\text{opt}} = \sqrt{\frac{C_{ii\bullet}}{C_{uu\bullet}} - \left[\text{Im} \left(\frac{C_{ui\bullet}}{C_{uu\bullet}} \right) \right]^2} + j \, \text{Im} \left(\frac{C_{ui\bullet}}{C_{uu\bullet}} \right)$$

$$\Gamma_{\text{opt}} = \frac{Z_{\text{opt}} - Z_0}{Z_{\text{opt}} + Z_0}, \Gamma_{\text{opt}} = \frac{Y_{\text{opt}} - Y_0}{Y_{\text{opt}} + Y_0}$$

$$F = F_{\min} + \frac{R_n}{G_g}[(G_{\text{opt}} - G_g)^2 + (B_{\text{opt}} - B_G)^2]$$

$$Y_{\text{opt}} = G_{\text{opt}} + j B_{\text{opt}}$$
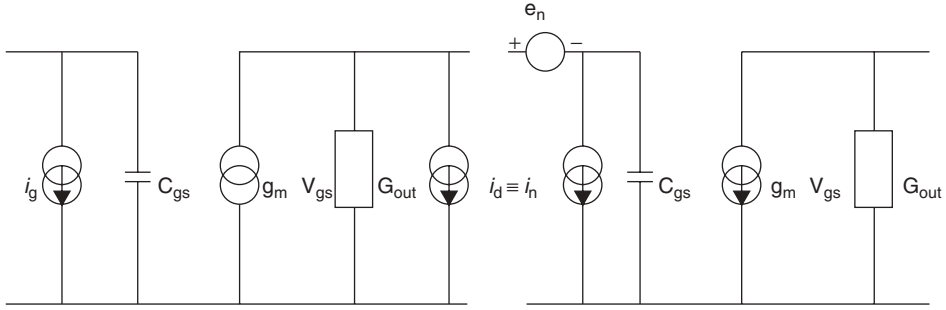
FIGURE C.4 Simplified FET and noise sources.

Neglecting gate leakage current I_{gd} (without C_{gd}), we will use the following models and matrix transformation to get a simplified C_a (Fig. C.4):

$$[C_a]_{tr} = \begin{bmatrix} \overline{e_n e_n^{\bullet}} & \overline{e_n i_n^{\bullet}} \\ \overline{i_n e_n^{\bullet}} & \overline{i_n i_n^{\bullet}} \end{bmatrix} = [T][C_Y]_{FET}[T]^+$$

$$[T] = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix}_{FET}$$

$$[C_a]_{FET} = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix} [C_Y]_{tr} \begin{bmatrix} 0 & 1 \\ B_{CS}^{\bullet} & D_{CS}^{\bullet} \end{bmatrix}$$

$$[C_a]_{tr} = \begin{bmatrix} \overline{e_n e_n^{\bullet}} & \overline{e_n i_n^{\bullet}} \\ \overline{i_n e_n^{\bullet}} & \overline{i_n i_n^{\bullet}} \end{bmatrix}$$

$$[C_a]_{FET} = [T][C_Y]_{FET}[T]^+$$

The transformation matrix T comes from the $ABCD$ matrix of the intrinsic FET:

$$[Y]_{FET} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} sc_{gs} & 0 \\ g_m & G_{out} \end{bmatrix}$$

$$ABCD]_{FET} = \begin{bmatrix} A_{CS} & B_{CS} \\ C_{CS} & D_{CS} \end{bmatrix} = \begin{bmatrix} -\dfrac{y_{22}}{y_{11}} & \dfrac{1}{-y_{21}} \\ \dfrac{\Delta}{y_{21}} & \dfrac{y_{11}}{y_{21}} \end{bmatrix} = \begin{bmatrix} -\dfrac{G_{out}}{g_m} & \dfrac{1}{-g_m} \\ \dfrac{sc_{gs}G_{out}}{-g_m} & \dfrac{sc_{gs}}{-g_m} \end{bmatrix}$$

$$[T] = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{1}{-g_m} \\ 1 & \dfrac{sc_{gs}}{-g_m} \end{bmatrix}$$

$$[T]^+ = \begin{bmatrix} 0 & 1 \\ B_{CS}^{\bullet} & D_{CS}^{\bullet} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ \dfrac{1}{-g_m} & \dfrac{sc_{gs}}{-g_m} \end{bmatrix}$$

$$[C_a]_{\text{FET}} = [T][C_Y]_{\text{FET}}[T]^+$$

$$= \begin{bmatrix} 0 & \dfrac{1}{-g_m} \\ 1 & \dfrac{sc_{gs}}{-g_m} \end{bmatrix} \times 4kT \begin{bmatrix} \dfrac{w^2 c_{gs}^2 R}{g_m} & -jwc_{gs}C\sqrt{PR} \\ jwc_{gs}C\sqrt{PR} & g_m P \end{bmatrix}$$

$$\times \begin{bmatrix} 0 & 1 \\ \dfrac{1}{-g_m} & \dfrac{sc_{gs}}{-g_m} \end{bmatrix}$$

$$= \dfrac{4kT}{g_m} \begin{bmatrix} P & -jwc_{gs}(P + C\sqrt{PR}) \\ jwc_{gs}(P + C\sqrt{PR}) & w^2 c_{gs}^2 (P + R + 2C\sqrt{PR}) \end{bmatrix}$$

$$[C_a]_{\text{tr}} = \begin{bmatrix} C_{uu^\bullet} & C_{ui^\bullet} \\ C_{u^\bullet i} & C_{ii^\bullet} \end{bmatrix} = 4kT \begin{bmatrix} R_n & \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}}^\bullet \\ \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}} & R_n |Y_{\text{opt}}|^2 \end{bmatrix}$$

and again we obtain

$$R_n = \dfrac{C_{uu^\bullet}}{4kT} = \dfrac{P}{g_m}$$

$$Y_{\text{opt}} = \sqrt{\dfrac{C_{ii^\bullet}}{C_{uu^\bullet}} - \left[\text{Im} \left(\dfrac{C_{ui^\bullet}}{C_{uu^\bullet}} \right) \right]^2} + j\, \text{Im} \left(\dfrac{C_{ui^\bullet}}{C_{uu^\bullet}} \right)$$

$$= G_{\text{opt}} + jB_{\text{opt}}$$

$$G_{\text{opt}} = \dfrac{wc_{gs}}{P} \sqrt{PR(1 - C^2)}$$

$$B_{\text{opt}} = -wc_{gs} \left(1 + C\sqrt{\dfrac{R}{P}} \right)$$

$$F_{\min} = 1 + \dfrac{C_{ui^\bullet} + C_{uu^\bullet} Y_{\text{opt}}}{kT} = 1 + \dfrac{2wc_{gs}}{g_m} \sqrt{PR(1 - C^2)}$$

Now, let us calculate the influence of C_{gd}, R_g, and R_s on the noise parameters:

$$[C_a]_{\text{FET}} = \begin{bmatrix} \overline{e_n e_n^\bullet} & \overline{e_n i_n^\bullet} \\ \overline{i_n e_n^\bullet} & \overline{i_n i_n^\bullet} \end{bmatrix} = \begin{bmatrix} C_{uu^\bullet} & C_{ui^\bullet} \\ C_{u^\bullet i} & C_{ii^\bullet} \end{bmatrix}$$

$$C_{uu^\bullet} = \left| \dfrac{g_m}{g_m - jwc_{gd}} \right|^2 \left(\dfrac{P + R - 2C_r\sqrt{RP}}{g_m} \right) + (R_s + R_{gs})$$

$$C_{ui^\bullet} = \left| \dfrac{g_m}{g_m - jwc_{gd}} \right|^2 \left[\left(\dfrac{w^2 c_{gs}^2 c_{gd}^2}{g_m^2} + \dfrac{jwc_{gd}}{g_m} \right) \right.$$

$$\left. \times (R - C\sqrt{RP}) + \dfrac{-jwc_{gs}}{g_m}(P - C^*\sqrt{RP}) \right]$$

$$C_{u \bullet i} = \left\{ \left| \frac{g_m}{g_m - jwc_{gd}} \right|^2 \left[\left(\frac{w^2 c_{gs}^2 c_{gd}^2}{g_m^2} + \frac{jwc_{gd}}{g_m} \right) \right. \right.$$

$$\left. \left. \times (R - C\sqrt{RP}) + \frac{-jwc_{gs}}{g_m}(P - C^*\sqrt{RP}) \right] \right\}^*$$

$$C_{ii \bullet} = \left| \frac{g_m}{g_m - jwc_{gd}} \right|^2 \left\{ \left| \frac{w^2 c_{gs}^2 c_{gd}^2}{g_m^2} - \frac{jwc_{gd}}{g_m} \right|^2 \frac{R}{g_m} + \left| \frac{jwc_{gs}}{g_m} \right|^2 \right.$$

$$\left. \times P g_m + 2Re\left[\left(\frac{w^2 c_{gs}^2 c_{gd}^2}{g_m^2} + \frac{jwc_{gd}}{g_m} \right) \left(\frac{jwc_{gs}}{g_m} \right) C\sqrt{RP} \right] \right\}$$

where

$$\frac{R}{g_m} = \overline{e_n e_n^\bullet} \qquad P g_m = \overline{i_n i_n^\bullet}$$

$$C = \frac{\overline{|e_n i_n^\bullet|}}{\sqrt{(\overline{e_n e_n^\bullet})(\overline{i_n i_n^\bullet})}} = \frac{\overline{|e_n i_n^\bullet|}}{\sqrt{|e_n^2||i_n^2|}}$$

$$[C_a]_{\text{FET}} = \begin{bmatrix} C_{uu\bullet} & C_{ui\bullet} \\ C_{u\bullet i} & C_{ii\bullet} \end{bmatrix} = \begin{bmatrix} R_n & \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}}^\bullet \\ \dfrac{F_{\min} - 1}{2} - R_n Y_{\text{opt}} & R_n |Y_{\text{opt}}|^2 \end{bmatrix} ;$$

The new results are

$$R_n = C_{uu\bullet}$$

$$Y_{\text{opt}} = \sqrt{\frac{C_{ii\bullet}}{C_{uu\bullet}} - \left[\text{Im}\left(\frac{C_{ui\bullet}}{C_{ii\bullet}} \right) \right]^2} + j\, \text{Im}\left(\frac{C_{ui\bullet}}{C_{uu\bullet}} \right)$$

$$Z_{\text{opt}} = \sqrt{\frac{C_{uu\bullet}}{C_{ii\bullet}} - \left(\frac{\text{Im } C_{ui\bullet}}{C_{ii\bullet}} \right)^2} - j\left(\frac{\text{Im } C_{ui\bullet}}{C_{ii\bullet}} \right)$$

$$Y_{\text{opt}} = G_{\text{opt}} + j B_{\text{opt}}$$

$$F_{\min} = 1 + 2[\text{Re}(C_{ui\bullet}) + C_{ii\bullet}\text{Re}(Z_{\text{opt}})]$$

$$= 1 + 2\left[\left(\frac{w^2 c_{gs}^2}{g_m^2} \right)(R_{gs} + R_s) P g_m \right.$$

$$\left. + \sqrt{\frac{w^4 c_{gs}^4}{g_m^4}(R_{gs} + R_s)^2 P^2 g_m^2 + \left(\frac{w^2 c_{gs}^2}{g_m^2} \right)[PR(1 - C^2) - P g_m R_{gs}]} \right]$$

$$R_n = \left| \frac{g_m}{g_m - jwc_{gd}} \right|^2 \left(\frac{P + R - 2C_r\sqrt{RP}}{g_m} \right)(R_{gs} + R_s)$$

$$R_{\text{opt}} = \frac{1}{wc_{gs}} \sqrt{\frac{g_m(R_s + R_{gs}) + R(1 - C_r^2)}{P} + w^2 c_{gs}^2 (R_s + R_{gs})^2}$$

$$X_{\text{opt}} = \frac{1}{wc_{gs}} \left(1 - C_r\sqrt{\frac{R}{P}}\right)$$

We will now introduce a minimum noise temperature $T_{\min}$ and modify the noise parameters previously derived. This equation will now have *temperature dependence* factors.

Figures C.5*a* and *b* present the familiar two-port noise representation of the intrinsic FET in admittance and *ABCD* matrix form. The admittance representation of the noise parameter of the intrinsic FET is expressed as

$$G_1 = \frac{\overline{|i_g^2|}}{4kT_0\Delta f} \qquad G_2 = \frac{\overline{|i_d^2|}}{4kT_0\Delta f} \qquad C_r = \frac{\overline{|i_g i_d^\bullet|}}{\sqrt{|i_d^2||i_g^2|}}$$

where $k = 1.38 \times 10^{-23}$ is Boltzmann's constant, T_0 is the standard temperature of 290 K, and Δf is the incremental bandwidth.

The *ABCD* matrix representation and the corresponding noise parameters are

$$R_n = \frac{\overline{|e_n^2|}}{4kT_0\Delta f} \qquad g_n = \frac{\overline{|i_n^2|}}{4kT_0\Delta f}$$

$$C_r = \frac{\overline{|e_n i_n^\bullet|}}{\sqrt{|e_n^2||i_n^2|}} \qquad N = R_{\text{opt}} g_n$$

where g_n is noise conductance.

The expression for noise temperature T_n and a noise measure M of a two-port driven by generator impedance Z_g is expressed as

$$T_n = T_{\min} + T_0 \frac{g_n}{R_g} |Z_g - Z_{\text{opt}}|^2$$

$$= T_{\min} + NT_0 \frac{|Z_g - Z_{\text{opt}}|^2}{R_g R_{\text{opt}}}$$
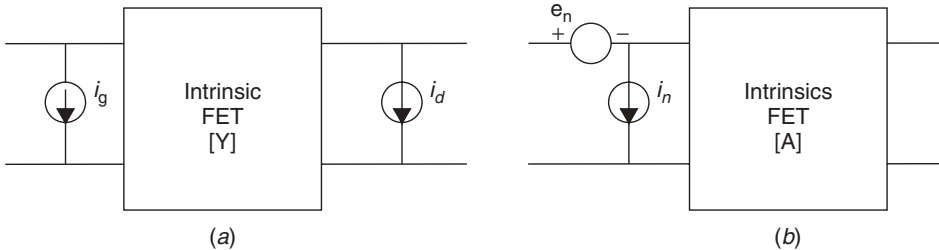
FIGURE C.5 Noise representation in linear two-port: (*a*) current noise source at input and output; (*b*) current and voltage noise source at input.

$$= T_{\min} + 4NT_0 \frac{|T_g - T_{\mathrm{opt}}|^2}{1 - |T_{\mathrm{opt}}|^2)(1 - |T_g|^2}$$

$$T_{\mathrm{opt}} = \frac{Z_{\mathrm{opt}} - Z_0}{Z_{\mathrm{opt}} + Z_0} \qquad M = \frac{T_n}{T_0} \left(\frac{1}{1 - 1/G_a} \right)$$

where Z_0 is the reference impedance and G_a is the available gain.

An extrinsic FET is shown in Figure C.6 with parasitic resistances which contributes thermal noise, and their influence can be calculated with the knowledge of the ambient temperature T_a:

$$G_1 = \frac{T_g}{T_0} \frac{r_{gs}(wC_{gs})^2}{1 + w^2 C_{gs}^2 r_{gs}^2} \qquad G_2 = \frac{T_g}{T_0} \frac{g_m^2 r_{gs}}{1 + w^2 C_{gs}^2 r_{gs}^2} + \frac{T_d}{T_0} g_{gs}$$

$$C_{r_c} = C_r \frac{\overline{|i_g i_d^{\bullet}|}}{\sqrt{|i_d^2||i_g^2|}} = \frac{-jwg_m C_{gs} r_{gs}}{1 + w^2 C_{gs}^2 r_{gs}^2} \frac{T_g}{T_0}$$

The noise properties of the intrinsic FET are treated by assigning equivalent temperatures T_g and T_d to r_{gs} and g_{ds}. No correlation is assumed between the noise sources represented by the equivalent temperatures T_g and T_d in Figure C.7.

The modified noise parameters are expressed as

$$Z_{\mathrm{opt}} = R_{\mathrm{opt}} + j X_{\mathrm{opt}}$$

$$R_{\mathrm{opt}} = \sqrt{\left(\frac{f_T}{f} \right)^2 \frac{r_{gs}}{r_{ds}} \frac{T_g}{T_d} + r_{gs}^2}$$

$$X_{\mathrm{opt}} = \frac{1}{wC_{gs}}$$

FIGURE C.6   Extrinsic FET.

FIGURE C.7   Intrinsic FET with assigned equivalent temperature.

$$T_{\min} = 2\frac{f}{f_T}\sqrt{r_{gs}g_{ds}T_gT_d + \left(\frac{f_T}{f}\right)^2 r_{gs}^2 g_{ds}^2 T_d^2 + 2\left(\frac{f_T}{f}\right)^2 r_{gs}g_{ds}T_d}$$

$$T_{\min} = (F_{\min} - 1)T_0$$

$$g_n = \left(\frac{f_T}{f}\right)^2 \frac{g_{ds}T_d}{T_0} \qquad f_T = \frac{g_m}{2\pi C_{gs}}$$

$$\frac{4NT_0}{T_{\min}} = \frac{2}{1 + r_{gs}/R_{opt}}$$

$$R_n = \frac{T_g}{T_0}r_{gs} + \frac{T_d}{T_0}\frac{g_{ds}}{g_m^2}(1 + w^2 C_{gs}^2 r_{gs}^2)$$

$$C_r = C\sqrt{R_n g_n} = \frac{T_d}{T_0}\frac{g_{ds}}{g_m^2}(w^2 C_{gs}^2 r_{gs} + jwC_{gs})$$

With reasonable approximation, the expression of noise parameters becomes much simpler. (The values from the calculation are typically less than 5% by introducing the following approximation). If

$$\frac{f}{f_T} \le \sqrt{\frac{r_{gs}}{r_{ds}}\frac{T_g}{T_d}} \qquad R_{opt} \ge r_{gs}$$

then

$$R_{opt} \cong \left(\frac{f_T}{f}\right)\sqrt{\frac{r_{gs}}{r_{ds}}\frac{T_g}{T_d}}$$

$$X_{opt} = \frac{1}{wC_{gs}}$$

$$T_{\min} = 2\frac{f}{f_T}\sqrt{r_{gs}g_{ds}T_gT_d}$$

$$g_n = \left(\frac{f_T}{f}\right)^2 \frac{g_{ds}T_d}{T_0}$$

$$f_T = \frac{g_m}{2\pi C_{gs}}$$

$$\frac{4NT_0}{T_{\min}} \cong 2$$

For example, us assume a linear FET model with the following intrinsic parameters:

$$r_{gs} = 2.5 \ \Omega \qquad r_{ds} = 400 \ \Omega \qquad C_{gs} = 0.28 \ \text{pF} \qquad C_{ds} = 0.067 \ \text{pF}$$
$$C_{gd} = 0.042 \ \text{pF} \qquad g_m = 57 \ \text{mS} \qquad f = 8.5 \ \text{GHz}$$

Then the temperature-dependent noise parameters for intrinsic FET are calculated to be

1. $T_0 = 290$ K, $T_a = 297$ K, $T_g = 304$ K, $T_d = 5514$ K, $V_{ds} = 2$ V, $I_{ds} = 10$ mA.
2. $T_0 = 290$ K, $T_a = 12.5$ K, $T_g = 14.5$ K, $T_d = 1406$ K, $V_{ds} = 2$ V, $I_{ds} = 5$ mA

Example 1: $T_a = 297$ K, $T_g = 304$ K, $T_d = 5514$ K, $V_{ds} = 2$ V, $I_{ds} = 10$ mA:

$$f_T = \frac{g_m}{2\pi C_{gs}} = 32.39 \ \text{GHz}$$

$$R_{\text{opt}} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{r_{gs}}{g_{ds}} \frac{T_g}{T_d} + r_{gs}^2} = 28.42 \ \Omega$$

$$X_{\text{opt}} = \frac{1}{w C_{gs}} = 66.91 \ \Omega$$

$$T_{\min} = 2\frac{f}{f_T}\sqrt{r_{gs} g_{ds} T_g T_d + \left(\frac{f_T}{f}\right)^2 r_{gs}^2 g_{ds}^2 T_d^2} + 2\left(\frac{f_T}{f}\right)^2 r_{gs} g_{ds} T_d = 58.74 \ \text{K}$$

$$g_n = \left(\frac{f_T}{f}\right)^2 \frac{g_{ds} T_d}{T_0} = 3.27 \ \text{mS}$$

$$F_{\min} = \frac{T_{\min}}{T_0} + 1 = \frac{58.7}{290} + 1 = 1.59 \ \text{dB}$$

$$R_n = \frac{T_g r_{gs}}{T_0} + \frac{g_{ds} T_d}{T_0 g_m^2}(1 + w^2 r_{gs}^2 c_{gs}^2) = 17.27 \ \Omega$$

Example 2: $T_a = 12.5$ K, $T_g = 14.5$ K, $T_d = 1406$ K, $V_{ds} = 2$ V, $I_{ds} = 5$ mA:

$$f_T = \frac{g_m}{2\pi C_{gs}} = 32.39 \ \text{GHz}$$

$$R_{\text{opt}} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{r_{gs}}{g_{ds}} \frac{T_g}{T_d} + r_{gs}^2} = 12.34 \ \Omega$$

$$X_{\text{opt}} = \frac{1}{w C_{gs}} = 66.9 \ \Omega$$

$$T_{\min} = 2\frac{f}{f_T}\sqrt{r_{gs}g_{ds}T_g T_d + \left(\frac{f_T}{f}\right)^2 r_{gs}^2 g_{ds}^2 T_d^2} + 2\left(\frac{f_T}{f}\right)^2 r_{gs}g_{ds}T_d = 7.4 \text{ K}$$

$$g_n = \left(\frac{f_T}{f}\right)^2 \frac{g_{ds}T_d}{T_0} = 0.87 \text{ mS}$$

$$F_{\min} = \frac{T_{\min}}{T_0} + 1 = \frac{7.4}{290} + 1 = 0.21 \text{ dB}$$

$$R_n = \frac{T_g r_{gs}}{T_0} + \frac{g_{ds}T_d}{T_0 g_m^2}(1 + w^2 r_{gs}^2 c_{gs}^2) = 3.86 \text{ }\Omega$$

These final results are consistent with results published by Pucel and Pospiezalski.
The following values for P, R, and C are typical [10.69]:

$$P = \begin{cases} 0.67 & \text{JFETs} \\ 1.2 & \text{MESFETs} \end{cases} \qquad R = \begin{cases} 0.2 & \text{JFET} \\ 0.4 & \text{MESFET} \end{cases} \qquad C = \begin{cases} 0.4 & \text{JFET} \\ 0.6\text{--}0.9 & \text{MESFET} \\ 0.9 & \text{HEMT} \end{cases}$$

APPENDIX D

DERIVATIONS FOR UNILATERAL GAIN SECTION

From Figure 8.6, the derivations of S_{12} and S_{21} are shown below:

$$S_{12} = \frac{b_1}{a_2} = C\,\underline{/0^\circ} + (T\,\underline{/-90^\circ})(\sqrt{G_{maR}}\,\underline{/\theta_2})(1\,\underline{/\phi})(T\,\underline{/-90^\circ})$$

$$+ (T\,\underline{/-90^\circ})(\sqrt{G_{maR}}\,\underline{/\theta_2})(1\,\underline{/\phi})[(C\,\underline{/0^\circ})(\sqrt{G_{maR}}\,\underline{/\theta_2})(1\,\underline{/\phi})]^1(T\,\underline{/-90^\circ})$$

$$+ (T\,\underline{/-90^\circ})(\sqrt{G_{maR}}\,\underline{/\theta_2})(1\,\underline{/\phi})[(C\,\underline{/0^\circ})(\sqrt{G_{maR}}\,\underline{/\theta_2})(1\,\underline{/\phi})]^2(T\,\underline{/-90^\circ}) + \cdots$$

$$+ (T\,\underline{/-90^\circ})(\sqrt{G_{maR}}\,\underline{/\theta_2})(1\,\underline{/\phi})[(C\,\underline{/0^\circ})(\sqrt{G_{maR}}\,\underline{/\theta_2})(1\,\underline{/\phi})]^n(T\,\underline{/-90^\circ})$$

$$= C\,\underline{/0^\circ} + \sum_{n=0}^{\infty} (T\,\underline{/-90^\circ})(\sqrt{G_{maR}}\,\underline{/\theta_2})(1\,\underline{/\phi})$$

$$\times \left[(C\,\underline{/0^\circ})(\sqrt{G_{maR}}\,\underline{/\theta_2})(1\,\underline{/\phi})\right]^n (T\,\underline{/-90^\circ})$$

$$= C\,\underline{/0^\circ} + \frac{T^2\sqrt{G_{maR}}\,\underline{/(-180^\circ + \phi + \theta_2)}}{1 - C\sqrt{G_{maR}}\,\underline{/(\phi + \theta_2)}} = \frac{C\,\underline{/0^\circ} - \sqrt{G_{maR}}\,\underline{/(\phi + \theta_2)}}{1 - C\sqrt{G_{maR}}\,\underline{/(\phi + \theta_2)}} \quad \text{(D.1)}$$

$$S_{21} = \frac{b_2}{a_1} = C\,\underline{/0^\circ} + (T\,\underline{/-90^\circ})(\sqrt{G_{ma}}\,\underline{/\theta_1})(1\,\underline{/\phi})(T\,\underline{/-90^\circ})$$

$$+ (T\,\underline{/-90^\circ})(\sqrt{G_{ma}}\,\underline{/\theta_1})(1\,\underline{/\phi})[(C\,\underline{/0^\circ})(\sqrt{G_{ma}}\,\underline{/\theta_1})(1\,\underline{/\phi})]^1(T\,\underline{/-90^\circ})$$

$$+ (T\,\underline{/-90^\circ})(\sqrt{G_{ma}}\,\underline{/\theta_1})(1\,\underline{/\phi})[(C\,\underline{/0^\circ})(\sqrt{G_{ma}}\,\underline{/\theta_1})(1\,\underline{/\phi})]^2(T\,\underline{/-90^\circ}) + \cdots$$

$$+ (T\,\underline{/-90^\circ})(\sqrt{G_{ma}}\,\underline{/\theta_1})(1\,\underline{/\phi})[(C\,\underline{/0^\circ})(\sqrt{G_{ma}}\,\underline{/\theta_1})(1\,\underline{/\phi})]^n(T\,\underline{/-90^\circ})$$

$$= C \underline{/0^\circ} + \sum_{n=0}^{\infty} (T \underline{/-90^\circ})(\sqrt{G_{ma}} \underline{/\theta_1})(1 \underline{/\phi})$$

$$\times \left[(C \underline{/0^\circ})(\sqrt{G_{ma}} \underline{/\theta_1})(1 \underline{/\phi}) \right]^n (T \underline{/-90^\circ})$$

$$= C \underline{/0^\circ} + \frac{T^2 \sqrt{G_{ma}} \underline{/(-180^\circ + \phi + \theta_1)}}{1 - C\sqrt{G_{ma}} \underline{/(\phi + \theta_1)}} = \frac{C \underline{/0^\circ} - \sqrt{G_{ma}} \underline{/(\phi + \theta_1)}}{1 - C\sqrt{G_{ma}} \underline{/(\phi + \theta_1)}} \quad \text{(D.2)}$$

where (D.1) and (D.2) use $1 + x + x^2 + x^3 + \cdots = 1/(1 - x)$, $x < 1$, which means

$$C\sqrt{G_{ma}} \underline{/(\phi + \theta_1)} < 1 \quad \text{(D.3)}$$

The derivation of unilateralization is shown as follows (Fig. 8.6): Let $\phi + \theta_2 = \theta_6$, $a = C$, $b = \sqrt{G_{maR}} < 1$, $S_{12} = f(\theta_6)$, and $|S_{12}| = g(\theta_6)$. $\Rightarrow f(\theta) = (a - be^{j\theta_6})/(1 - abe^{j\theta_6})$. Then

$$g(\theta_6) = |f(\theta_6)| = \left| \frac{a - be^{j\theta_6}}{1 - abe^{j\theta_6}} \right| = \left| \frac{(a - b\cos\theta_6) - jb\sin\theta_6}{(1 - ab\cos\theta_6) - jab\sin\theta_6} \right|$$

$$= \frac{|(a - b\cos\theta_6) - jb\sin\theta_6|}{|(1 - ab\cos\theta_6) - jab\sin\theta_6|}$$

$$= \left(\frac{(a - b\cos\theta_6)^2 + b^2\sin^2\theta_6}{(1 - ab\cos\theta_6)^2 + a^2b^2\sin^2\theta_6} \right)^{1/2} = \left(\frac{a^2 - 2ab\cos\theta_6 + b^2}{1 - 2ab\cos\theta_6 + a^2b^2} \right)^{1/2} \quad \text{(D.4)}$$

Let

$$|S_{12}| = g(\theta_6) = 0 \Rightarrow a^2 - 2ab\cos\theta_6 + b^2 = 0 \Rightarrow a = b(\cos\theta_6 \pm j\sin\theta_6) \quad \text{(D.5)}$$

Because $a = C$, which is a positive real number, a must equal b and $\theta_6 = \phi + \theta_2 = 0^\circ$. Therefore, $S_{12} = 0$ only if $\theta_6 = \phi + \theta_2 = 0^\circ$ and $C = \sqrt{G_{maR}}$, which states the coupling factor is the reverse G_{ma}.

The derivation of the maximum absolute value of S_{21} is shown below. Let $\phi + \theta_1 = \theta_5$, $a = C$, $b = \sqrt{G_{ma}} > 1$, $S_{21} = f(\theta_5)$, and $|S_{21}| = g(\theta_5)$. $\Rightarrow f(\theta) = (a - be^{j\theta_5})/(1 - abe^{j\theta_5})$. Then

$$g(\theta_5) = |f(\theta_5)| = \left(\frac{a^2 - 2ab\cos\theta_5 + b^2}{1 - 2ab\cos\theta_5 + a^2b^2} \right)^{1/2}$$

$$1 > a > 0, b > 1, \text{ and } ab > 0 \quad \text{(D.6)}$$

$$g'(\theta_5) = \frac{ab\sin\theta_5(1 + a^2b^2 - a^2 - b^2)}{(a^2 + b^2 - 2ab\cos\theta_5)(1 + a^2b^2 - 2ab\cos\theta_5)^{3/2}}$$

$$g'(\theta_5) = 0 \text{ only if } \sin\theta_5 = 0^\circ \text{ or } 180^\circ \quad \text{(D.7)}$$

$$g''(0^\circ) = \frac{2ab(1 - a^2)(1 - b^2)}{(a - b)^2(1 - ab)^3} \qquad g''(0^\circ) < 0 \text{ only if } ab < 1 \quad \text{(D.8)}$$

$$g''(180^\circ) = \frac{-2ab(1 - a^2)(1 - b^2)}{(a + b)^2(1 + ab)^3} \qquad g''(180^\circ) \text{ is always more than zero}$$

Let $g(0°)$ be the maximum point for $g'(0°) = 0$ and $g''(0°) < 0$. So S_{21} reaches a maximum magnitude when $\theta_5 = \phi + \theta_1 = 0°$. Therefore,

$$|S_{21}|_{\max} = \left| \frac{C - \sqrt{G_{ma}}}{1 - C\sqrt{G_{ma}}} \right| = \frac{\sqrt{G_{ma}} - C}{1 - C\sqrt{G_{ma}}} = \sqrt{U} \qquad \text{(D.9)}$$

$$S_{21} = \frac{C - \sqrt{G_{ma}}}{1 - C\sqrt{G_{ma}}} = -\frac{\sqrt{G_{ma}} - C}{1 - C\sqrt{G_{ma}}} = -\sqrt{U}$$

$$\text{if } \theta_5 = \phi + \theta_1 = 0° \qquad \text{(D.10)}$$

APPENDIX E

VECTOR REPRESENTATION OF TWO-TONE INTERMODULATION PRODUCTS

INTRODUCTION

An amplifying device is said to be linear if its output is an exact replica of its input, except for gain and time delay. However, in most solid-state devices, some (usually small) amount of distortion is unavoidable. It therefore becomes necessary to establish a yardstick by which such distortion can be measured. A commonly used scheme is when two equal-amplitude sinusoidal signals close in frequency are applied; the result is intermodulation products at nearby frequencies.

In classical power series analysis [E.1], a two-tone input signal given by

$$v_{\text{in}} = E \cos \omega_1 t + E \cos \omega_2 t \tag{E.1}$$

is applied. The resulting output is

$$v_{\text{out}} = v_{\text{in}} k_1 + v_{\text{in}}^2 k_2 + v_{\text{in}}^3 k_3 + v_{\text{in}}^4 k_4 + v_{\text{in}}^5 k_5 + \cdots \tag{E.2}$$

From these equations, the various intermodulation products can be derived. This power series scheme is of limited value when applied to real-world amplifiers because it can only account for AM-to-AM distortion products. For real-world amplifiers, not only AM-to-AM distortion but also AM-to-PM distortion products occur.

To accommodate both effects, a formulation is required that includes both AM and PM distortion products. This makes it possible to view the various intermodulation products as vectors in the complex plane. We begin by inquiring what form such a scheme would take.

SINGLE-TONE ANALYSIS

Consider the case of a nonlinear transconductance device as represented schematically in Figure E.1. It has three ports: a bias port where a dc voltage V_{dc} is applied, an input port where the RF signal is applied, and an output port where the resultant RF signals are produced. The output port is terminated by linear impedance Z_0. The voltage v_{in} is the signal that is applied at the input port, and i_0 is the resultant current at the output port. The current i_b is the bias current. The total current that flows through the device is $i_b - i_0$. Around the device, a diplexer is designed that separates the dc and any low-frequency component to the bias port, whereas the RF signals are directed to the output port. For the single-tone case, a sufficiently high input signal could cause the bias current i_b to change. A series impedance inserted in the bias port will cause the bias of the device to change, modifying its performance. This "bias-induced" component provides a mechanism for memory effects, where the bias could be dependent on past history. For the two-tone case, this bias-induced products could modulate the bias of the device, producing, among other things, unequal intermodulation sidebands. A simplified model for this effect will be discussed later, but for now, back to the single-tone case.

Let

$$v_{in} = V \cos \omega t \tag{E.3}$$

be the applied voltage at the input port. We wish to derive the resultant output voltage v_0.

The convention used here is for complex numbers to be set boldface. From the single-tone expansion of the Volterra series analysis [E.2] of Eq. (E.64) in a later section, the output at the fundamental frequency is

$$v_0|_{fund} = \text{Re} \left[\sum_{n=0,2,4,\dots}^{\infty} V^n \mathbf{G}_{n+1} V \, e^{j\omega t} \right] \tag{E.4}$$

where $\mathbf{G}_{n+1} = \mathbf{H}_{n+1} \mathbf{Z}_0$.
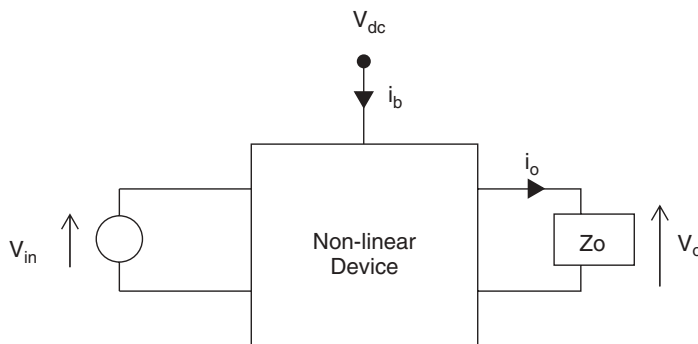
FIGURE E.1   Block Diagram.

This can be separated into a linear term and a distortion term:

$$V_0|_{\text{fund}} = \text{Re}\left[\left(\underbrace{\mathbf{G}_1}_{\text{small-signal gain}} + \underbrace{\sum_{n=2,4,6,\ldots}^{\infty} V^n \mathbf{G}_{n+1}}_{\text{distortion term}}\right) V e^{j\omega t}\right] \qquad (\text{E.5})$$

The important feature that Eq. (E.5) establishes is that the gain, which assumes the small-signal value $\mathbf{G}_1$ for V small, will vary as a function of even powers of V.

Let $\mathbf{G}_L$ be defined as the large-signal gain

$$\mathbf{G}_L = \mathbf{G}_1 + \sum_{n=2,4,6,\ldots}^{\infty} V^n \mathbf{G}_{n+1} \qquad (\text{E.6})$$

The large-signal gain can be represented as a vector in the complex plane that converges to the small-signal gain as V decreases. The distortion vector will in general produce AM and PM perturbations to the gain. This is depicted in Figure E.2.

If the distortion vector causes the gain to decrease in magnitude as is shown in this example, the distortion is said to be compressive, whereas if the gain is increased, expansion results. In fact, the distortion could have different regions of expansive and compressive behavior.

For small distortions, the distortion vector can be decomposed into two orthogonal components: (1) the part that is parallel to the small-signal gain vector, called the in-phase part, and (2) the part that is perpendicular to the gain vector, called the quadrature part. The distortion vector is the vector sum of these two components. (The units of both the in-phase and quadrature components are volts per volts.)
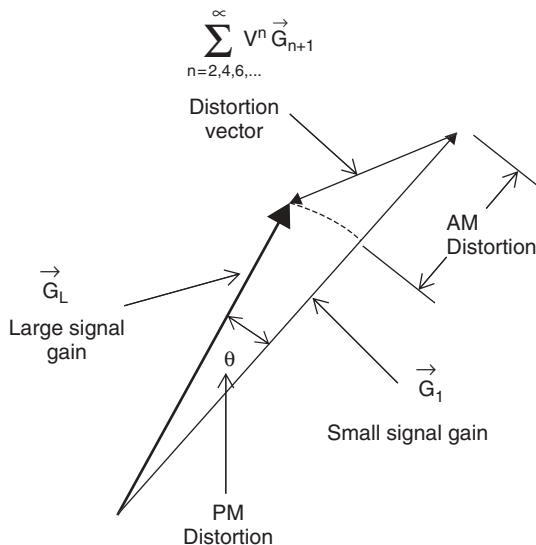
FIGURE E.2 Gain phasor in complex plane.
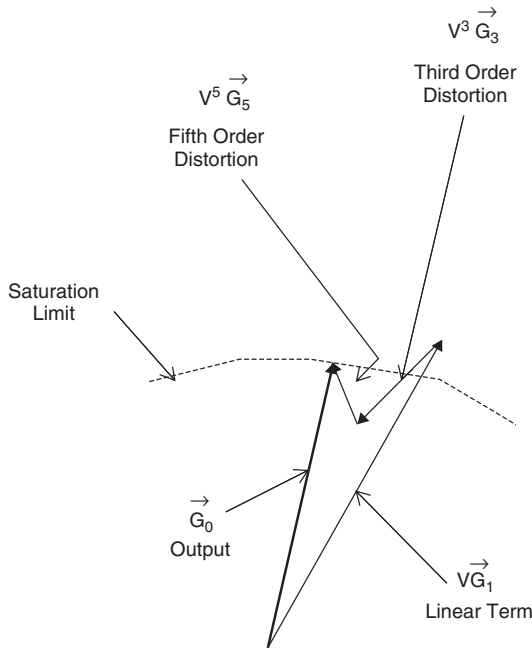
FIGURE E.3   Signal phasor in complex plane.

The output power of FET-based devices typically saturates to a constant level, even if the input power is further increased. This can be understood if the in-phase part of each successive higher (odd-order) product has alternating compressive and expansive behavior. This requirement will be assumed in the following example to illustrate the relationship of these vectors to each other. Limiting the distortion of Eq. (E.5) to fifth-order products, we have

$$V_0 = \mathrm{Re}\left[\left(\underbrace{\mathbf{G}_1 V}_{\text{linear term}} + \underbrace{V^3 \mathbf{G}_3}_{\text{third-order distortion}} + \underbrace{V^5 \mathbf{G}_5}_{\text{fifth-order distoriton}}\right) e^{j\omega t}\right] \qquad (E.7)$$

This effect can be viewed as phasors of the signal vector V_0 as shown in Figure E.3.

In this example, the third-order contribution is compressive whereas the fifth-order contribution is expansive, making them generally point in opposite directions. This example will be used in the next section on two-tone, third-order intermodulation distortion products.

TWO-TONE ANALYSIS

We embark on the two-tone analysis by starting with the single-tone representation of Eq. (E.3):

$$v_{\text{in}} = V \cos \omega_0 t \qquad (E.8)$$

Here, the voltage magnitude V, previously assumed to be constant, will now be allowed to slowly vary with time. More specifically, V takes the form

$$V = 2E \cos \omega_m t \tag{E.9}$$

where $\omega_m \ll \omega_0$, so that Eq. (E.8) becomes

$$v_{\text{in}} = 2E \cos \omega_m t \cos \omega_0 t \tag{E.10}$$

This is the double-sideband suppressed carrier output of a product detector, a commonly used modulation technique. Without any loss of generality, we can assume that $\omega_2 > \omega_1$.

Letting

$$\omega_m = \frac{\omega_2 - \omega_1}{2} \qquad \omega_0 = \frac{\omega_2 + \omega_1}{2} \tag{E.11}$$

Eq. (E.10) becomes

$$v_{\text{in}} = E \cos \omega_1 t + E \cos \omega_2 t \tag{E.12}$$

Equations (E.10) and (E.12) are two different but equivalent mathematical expressions for the two-tone signals. Figure E.4a shows the time-domain representation of this signal, best represented by Eq. (E.10). It is viewed as a signal with periodicity corresponding to frequency ω_0 with envelope $2E \cos(\omega_m t)$. The peak envelope power $(2E)$ is 6 dB higher than the single-tone power (E) whereas the average power is 3 dB higher. It may seem curious that whereas the time-domain behavior shows a modulated signal oscillating at frequency ω_0, there is no spectral component at this frequency. This is the "suppressed" carrier that undergoes a $180°$ phase shift for every zero crossing of the envelope. Were it not for this phase shift, a substantial component would appear.

Equation (E.12) clearly shows the spectral composition of this signal. The frequency-domain representation is shown in Figure E.4b and represents what would be seen on a spectrum analyzer.

A third representation is the modulation domain. Here, the suppressed carrier is viewed as being modulated by a pair of oppositely rotating vectors.

Define the modulation vector $\mathbf{V}_{\text{in}}$ to be

$$\mathbf{V}_{\text{in}} = E e^{j\omega_m t} + E e^{-j\omega_m t} \tag{E.13}$$

so that

$$\mathbf{V}_{\text{in}} e^{j\omega t} = (E e^{j\omega_m t} + E e^{-j\omega_m t}) e^{j\omega_0 t} \tag{E.14}$$

and

$$v_{\text{in}} = \text{Re}(\mathbf{V}_m e^{j\omega_0 t}) \tag{E.15}$$

The vectors $\mathbf{V}_{\text{in}}$ can be shown to be a pair of oppositely rotating vectors in the complex plane as per Goldman [E.3]. This is illustrated in Figure E.4c. The vector sum falls on the real axis and defines the envelope of the two-tone signals as a function of time.
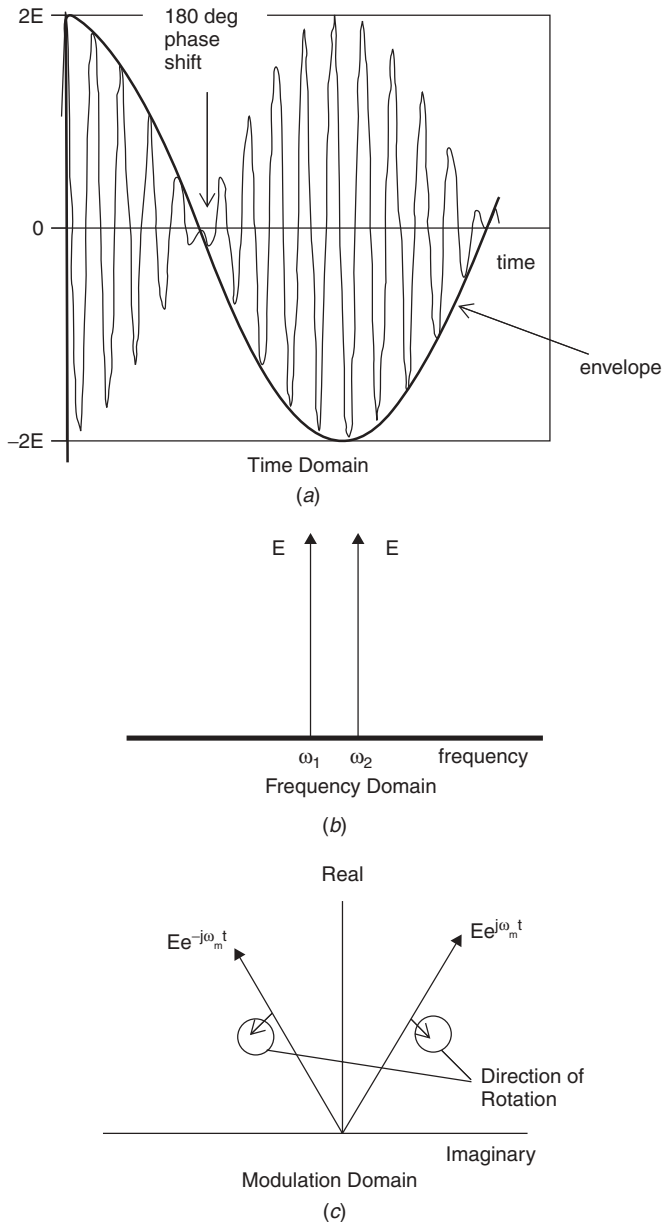
FIGURE E.4   Two-tone representation: (*a*) time domain; (*b*) frequency domain; (*c*) modulation domain.

We now consider the nonlinear effects. Returning to Eq. (E.5),

$$v_0 = \text{Re}\left[\left(\mathbf{G}_1 + \sum_{n=2,4,6,\ldots}^{\infty} V^n \mathbf{G}_{n+1}\right) V e^{j\omega_0 t}\right] \tag{E.16}$$

Reindexing,

$$V_0 = \text{Re}\left[\left(\mathbf{G}_1 V + \sum_{n=3,5,7,\ldots}^{\infty} V^n \mathbf{G}_n\right) e^{j\omega_0 t}\right] \tag{E.17}$$

Substituting Eq. (E.9) in Eq. (E.17), we have

$$V_0 = \text{Re}\left[\left(\mathbf{G}_1 (2E\cos\omega_m t) + \sum_{n=3,5,7,\ldots}^{\infty} (2E\cos\omega_m t)^n \mathbf{G}_n\right) e^{j\omega_0 t}\right] \tag{E.18}$$

It is now possible to derive all intermodulation products. For now, we will limit our attention to the first- and third-order products, although, as we shall later see, higher order products are easily derived.

But from

$$\cos^n \omega t = \left(\frac{1}{2}\right)^n (e^{j\omega t} + e^{-j\omega t})^n = \left(\frac{1}{2}\right)^n \sum_{m=0}^{n} C_m^n e^{j(n-2m)\omega t} \tag{E.19}$$

where the binomial coefficient C_m^n (sometimes called the combination of n things taken m at a time) is

$$C_m^n = \frac{n!}{m!(n-m)!} \tag{E.20}$$

it can be shown that

$$\cos^n \omega t = \begin{cases} \dfrac{1}{2^{n-1}} \displaystyle\sum_{m=0,1,2,\ldots}^{(n-1)/2} C_m^n \cos(n-2m)\omega t & \text{if } n \text{ is odd} \\[4mm] \dfrac{1}{2^{n-1}} \displaystyle\sum_{m=0,1,2,\ldots}^{n/2-1} C_m^n \cos(n-2m)\omega t + \dfrac{1}{2^n} \dfrac{n!}{[(n/2!)]^2} & \text{if } n \text{ is even} \end{cases} \tag{E.21}$$

The last two terms are

$$\cos^n \omega t = \begin{cases} \cdots + \dfrac{1}{2^{n-1}} \dfrac{n!}{\left(\dfrac{n+3}{2}!\right)\left(\dfrac{n-3}{2}!\right)} \cos 3\omega t \\[6mm] + \dfrac{1}{2^{n-1}} \dfrac{n!}{\left(\dfrac{n+1}{2}!\right)\left(\dfrac{n-1}{2}!\right)} \cos \omega t \qquad \text{if } n \text{ is odd} \\[6mm] \cdots + \dfrac{1}{2^{n-1}} \dfrac{n!}{\left(\dfrac{n+2}{2}!\right)\left(\dfrac{n-2}{2}!\right)} \cos 2\omega t \\[6mm] + \dfrac{1}{2^n} \dfrac{n!}{\left(\dfrac{n}{2}!\right)^2} \qquad \text{if } n \text{ is even} \end{cases} \tag{E.22}$$

Substituting the n odd case of the above equation in Eq. (E.18),

$$V_0 = \text{Re}\left[\left(\underbrace{\mathbf{G}_1 2E \cos \omega_m t}_{\text{linear term}} + \sum_{n=3,5,7,\ldots}^{\infty} (2E)^n \mathbf{G}_n\right.\right.$$
$$\left.\left.\times \left(\underbrace{\frac{1}{2^{n-1}} \frac{n! \cos 3\omega_m t}{\frac{n+3}{2}! \frac{n-3}{2}!}}_{\text{third-order distortion products}} + \underbrace{\frac{1}{2^{n-1}} \frac{n! \cos \omega_m t}{\frac{n+1}{2}! \frac{n-1}{2}!}}_{\text{first-order distortion products}}\right)\right) e^{j\omega_0 t}\right] \quad \text{(E.23)}$$

Further limiting our attention to contributions from the third-order nonlinearities, Eq. (E.23) becomes

$$V_0 = \text{Re}\left[\underbrace{(\mathbf{G}_1 2E \cos \omega_m t + 2E^3 \mathbf{G}_3(\cos 3\omega_m t + 3\cos \omega_m t))}_{\text{envelope}} e^{j\omega_0 t}\right] \quad \text{(E.24)}$$

We find that the contribution to the first-order product is stronger than to the third-order product. The first-order contribution is 20 log(3) or 9.5 dB higher than the third-order product. However, this product is largely obscured by the linear term and would be difficult to isolate on a spectrum analyzer. If the linear term is canceled as is the case in certain predistortion or feed-forward schemes, the first-order product would still be the strongest signal seen.

Figure E.5 shows the signal in the time domain, with the undistorted envelope also plotted for reference. The distortion displayed is the AM part. The PM part is difficult to ascertain because it requires a display of the variance of the zero crossings of the RF waveform from the undistorted signal. The total distortion product is larger than the AM part seen here, because the PM part is not taken into account.

This example shows the distortion to be compressive, although expansion is also possible. The compression is mostly due to the third-order contributions to the first-order product, which in this case accounts for 75% of the compression with only 25% due to contributions to the third-order product.

From Eq. (E.24) we have

$$\begin{aligned}
v_0 &= \text{Re}\{\lfloor \mathbf{G}_1 E (e^{j\omega_m t} + e^{-j\omega_m t}) + \mathbf{G}_3 E^3 \\
&\quad \times [(e^{j3\omega_m t} + e^{-j3\omega_m t}) + 3(e^{j\omega_m t} + e^{-j\omega_m t})]\rfloor e^{j\omega_0 t}\} \\
&= \text{Re}[\mathbf{G}_1 E (e^{j\omega_1 t} + e^{j\omega_2 t}) + \mathbf{G}_3 E^3 \\
&\quad \times [(e^{j(2\omega_1 - \omega_2)t} + e^{j(2\omega_2 - \omega_1)t}) + 3(e^{j\omega_1 t} + e^{j\omega_2 t})]]
\end{aligned} \quad \text{(E.25)}$$

Equation (E.25) identifies the various spectral components. In Figure E.6, the components in the frequency domain are displayed. Here, the total distortion products (i.e.,
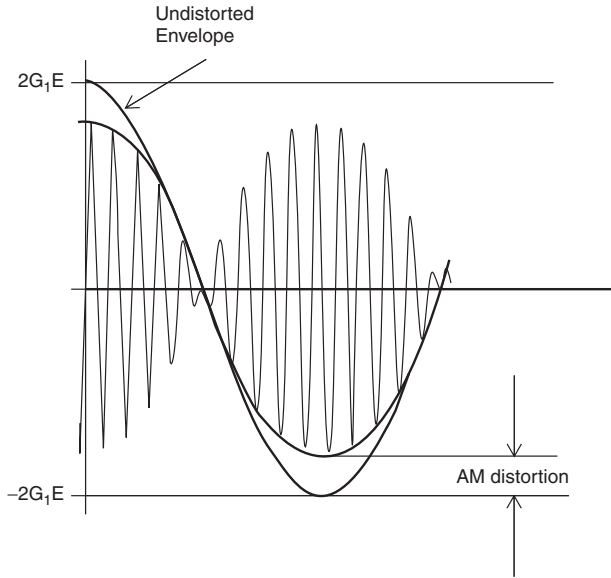
FIGURE E.5   Time-domain representation.
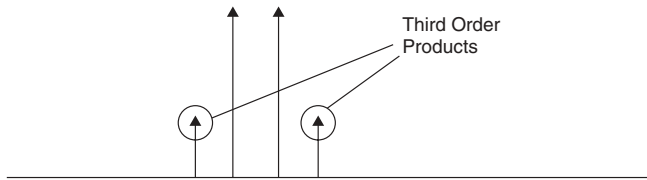
FIGURE E.6   Frequency-domain representation.

both the AM and PM parts) are seen. How much of it is AM and how much is PM cannot be determined, however.

From Eq. (E.23),

$$
V_0 = \mathrm{Re} \left[\left(\underbrace{\mathbf{G}_1 2E \cos \omega_m t}_{\text{linear term}} + \sum\nolimits_{n=3,5,7,\ldots}^{\infty} \right. \right.
$$
$$
\left. \left. \times\, 2 \left(\underbrace{\mathbf{IMD}_3 \cos 3\omega_m t}_{\text{third-order distortion products}} + \underbrace{\mathbf{IMD}_1 \cos \omega_m t}_{\text{first-order distortion products}} \right) \right) e^{j\omega_0 t} \right] \quad \text{(E.26)}
$$

where

$$
\mathbf{IMD}_3 = \sum_{n=3,5,7,\ldots}^{\infty} \mathbf{G}_n \frac{n!\,E^n}{\dfrac{n+3}{2}!\,\dfrac{n-3}{2}!} \quad \text{(E.27)}
$$

and

$$\mathbf{IMD}_1 = \sum_{n=3,5,7,\ldots}^{\infty} \mathbf{G}_n \frac{n! E^n}{\dfrac{n+1}{2}! \dfrac{n-1}{2}!} \tag{E.28}$$

The third-order intermodulation products have contributions from all odd-order terms. Limiting to the third- and fifth-order contributions, we have

$$\mathbf{IMD}_3 = \left[\underbrace{\mathbf{G}_3 E^3}_{\text{third order}} + \underbrace{5\mathbf{G}_5 E^5}_{\text{fifth order}} \right] \tag{E.29}$$

At the lower drive levels where the third-order contribution is dominant, this product will increase 3 dB per 1-dB increase of input power. As the drive increases, it is possible for the faster growing fifth-order contribution to overtake and become dominant. At these levels, the third-order product will increase 5 dB per 1 dB. What happens at the point where both contributions are approximately equal in magnitude depends on the relative direction of both contributions to each other. One possible scenario is where the third-order contribution is compressive and the fifth-order is expansive, causing these vectors to be generally pointing in opposite directions. The presence of the fifth-order contribution will cause the third-order product to decrease in magnitude over what would otherwise be the case. At this point, the presence of the fifth-order contribution improves the linearity.

In general, the pth-order distortion product is

$$\mathbf{IMD}_p = \sum_{n=p,p+2,\ldots}^{\infty} \mathbf{G}_n \frac{n! E^n}{\dfrac{n+p}{2}! \dfrac{n-p}{2}!} \qquad p \text{ odd} \tag{E.30}$$

The complete intermodulation phasor is

$$\mathbf{V}_0 = \sum_{p=1,3,5,\ldots}^{\infty} \mathbf{IMD}_p (e^{jp\omega_m t} + e^{-jp\omega_m t}) \tag{E.31}$$

The complete output signal is

$$v_0 = \text{Re} \left[\sum_{p=1,3,5,\ldots}^{\infty} \sum_{n=p,p+2,\ldots}^{\infty} \mathbf{G}_n \frac{n! E^n}{\dfrac{n+p}{2}! \dfrac{n-p}{2}!} \right.$$

$$\left. \times \left(e^{j[(1+p)/2]\omega_1 t + j[(1-p)/2]\omega_2 t} + e^{j[(1-p)/2]\omega_1 t + j[(1+p)/2]\omega_2 t} \right) \right] \tag{E.32}$$

Each term represents the nth-order contribution to the pth-order product. Both n and p are odd integers, and n must be greater or equal to p. The first-order contribution to the first-order product is the linear term; all others are nonlinear.

BIAS-INDUCED DISTORTION

This section is concerned with distortion products that result from modulation of the bias voltage. The modulation is caused by even-order nonlinearities resulting in bias current being a function of drive level. This comes about because each $\mathbf{G}_n$ term is a function of bias voltage. The resultant distortion vectors, when added to the (odd-order) distortion products of the previous section, can give rise to two surprising effects: (1) unequal distortion products and (2) the distortion products being a function of frequency separation. This can be viewed as distortion of the envelope, giving rise to possible memory effects, as contrasted to odd-order distortion of the previous section where the RF waveform itself is distorted. Inasmuch as these effects add considerable complexity to the analysis, only the lowest order effect will be discussed.

There is a sense that the odd-order nonlinearities can be considered to be the "memoryless" part of the nonlinearity since they do not affect the bias, whereas the even-order nonlinearities are the part that could give rise to memory effects, since they do affect the bias. The circuit is shown in Figure E.7. This is similar to Figure E.1, except for the inclusion of a linear impedance $\mathbf{Z}_b$ installed in the bias port. As indicated earlier, any dc and low-frequency current will be directed through this impedance. Only even-order nonlinearities produce such terms:

$$I_R(V_{dc} + \Delta V_a) = \underbrace{I_R(V_{dc})}_{dc\ term} + \sum_{n=2,4,6,...}^{\infty} V^n D_n(\omega) \tag{E.33}$$

In the two-tone case, where from Eq. (E.9)

$$V = 2E \cos \omega_m t \tag{E.34}$$

is substituted in Eq. (E.64), the result is

$$i_b|_{low\ freq} = \sum_{n=2,4,6,...}^{\infty} D_n(\omega) 2^n E^n \cos^n \omega_m t \tag{E.35}$$
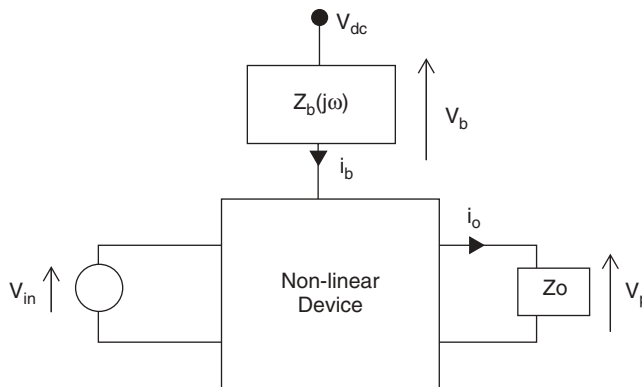
FIGURE E.7   Nonlinear device with bias circuit.

We limit this analysis to the last two terms of the n even case of Eq. (E.22). Thus

$$i_b|_{\text{low freq}} = \sum_{n=2,4,6,\ldots}^{\infty} D_n(\omega) E^n \left[\frac{2n!}{\left(\frac{n+2}{2}!\right)\left(\frac{n-2}{2}!\right)} \cos 2\omega_m t + \frac{n!}{\left(\frac{n}{2}!\right)^2} \right] \quad \text{(E.36)}$$

Further limiting to only second-order contributions,

$$i_b|_{\text{low freq}} = 2D_2(\omega) E^2 (\cos 2\omega_m t + 1) \quad \text{(E.37)}$$

The voltage that is generated across the impedance $\mathbf{Z}_b$ is

$$V_b = [2D_2(\omega) E^2][|\mathbf{Z}_b(j2\omega_m)| \cos(2\omega_m t + \theta_{Zb}) + \mathbf{Z}_b(0)] \quad \text{(E.38)}$$

where

$$\theta_{Zb} = \arctan\left[\frac{\text{Im } \mathbf{Z}_b(j2\omega_m)}{\text{Re } \mathbf{Z}_b(j2\omega_m)} \right] \quad \text{(E.39)}$$

This voltage will modulate the bias of the device, which in turn can produce bias-induced distortion products. For example, the small-signal gain, being bias dependent, can be expanded:

$$\mathbf{G}_1(\mathbf{V}_{\text{dc}} + \mathbf{V}_b) = \underbrace{\mathbf{G}_1(\mathbf{V}_{\text{dc}})}_{\text{linear term}} + \underbrace{V_b \frac{d\mathbf{G}_1}{dV}}_{\text{bias-induced term}} \quad \text{(E.40)}$$

The resultant bias-induced distortion product is

$$\begin{aligned} v_0|_{\text{bias induced}} &= \text{Re}\left[\left(V_b \frac{d\mathbf{G}_1}{dV} \right) 2E \cos \omega_m t \; e^{j\omega_0 t} \right] \\ &= \text{Re}\left[\left(2D_2(\omega) E^2 (|\mathbf{Z}_b(j2\omega_m)| \cos(2\omega_m t + \theta_{Zb}) + \mathbf{Z}_b(0)) \frac{d\mathbf{G}_1}{dV} \right) \right. \\ &\quad \left. \times 2E \cos \omega_m t \; e^{j\omega_0 t} \right] \end{aligned} \quad \text{(E.41)}$$

Assuming zero dc resistance of the bias circuit,

$$\begin{aligned} v_0|_{\text{bias induced}} &= \text{Re}\left[\left\{ 2D_2(\omega) E^2 [|\mathbf{Z}_b(j2\omega_m)| \cos(2\omega_m t + \theta_{Zb})] \frac{d\mathbf{G}_1}{dV} \right\} 2E \cos \omega_m t e^{j\omega_0 t} \right] \\ &= \text{Re}\left[\left\{ 2D_2(\omega) E^2 \frac{d\mathbf{G}_1}{dV} |\mathbf{Z}_b(j2\omega_m)| \right. \right. \\ &\quad \left. \left. \times [\cos(3\omega_m t + \theta_{Zb}) + \cos(\omega_m t + \theta_{Zb})] \right\} e^{j\omega_0 t} \right] \\ &= \text{Re}\left[\left\{ 2D_2(\omega) E^2 \frac{d\mathbf{G}_1}{dV} |\mathbf{Z}_b(j2\omega_m)| \left[e^{j(3\omega_m t + \theta_{Zb})} + e^{-j(3\omega_m t + \theta_{Zb})} \right. \right. \right. \\ &\quad \left. \left. \left. + (e^{j(\omega_m t + \theta_{Zb})} + e^{-j(\omega_m t + \theta_{Zb})}) \right] \right\} e^{j\omega_0 t} \right] \end{aligned} \quad \text{(E.42)}$$

These products have first- and third-order contributions. Separating them by frequency,

$$v_0|_{\text{bias induced}} = \text{Re}\lfloor(\textbf{BIP}_{+3}e^{j3\omega_m t} + \textbf{BIP}_{-3}e^{-j3\omega_m t} + \textbf{BIP}_{+1}e^{j\omega_m t} + \textbf{BIP}_{-1}e^{-j\omega_m t})e^{j\omega_0 t}\rfloor$$
(E.43)

where

$$\textbf{BIP}_{+3} = \text{Re}[D_2(\omega)](E^3)\frac{d\textbf{G}_1}{dV}\textbf{Z}_b(j2\omega_m)$$
(E.44)

$$\textbf{BIP}_{-3} = \text{Re}[D_2(\omega)](E^3)\frac{d\textbf{G}_1}{dV}\textbf{Z}_b^*(j2\omega_m)$$
(E.45)

$$\textbf{BIP}_{+1} = \text{Re}[D_2(\omega)](E^3)\frac{d\textbf{G}_1}{dV}\textbf{Z}_b(j2\omega_m)$$
(E.46)

$$\textbf{BIP}_{-1} = \text{Re}[D_2(\omega)](E^3)\frac{d\textbf{G}_1}{dV}\textbf{Z}_b^*(j2\omega_m)$$
(E.47)

We call the bias-induced products (BIPs) of Eqs. (E.44) and (E.46) the *upper distortion product* and the products of Eqs. (E.45) and (E.47) the *lower distortion product*. Unless the bias circuit is resistive, the upper and lower third-order contributions of Eqs. (E.44) and (E.46), respectively, will be pointing in different directions. This is unlike the intermodulation products, where the upper and lower products are equal and there was no need to differentiate between them. When IMD vectors are summed with BIP vectors, the results will have differing upper and lower magnitudes.

The total distortion products, in consideration of Eqs. (E.25) and (E.43), are given as

$$v_0|_{\text{total product}} = \text{Re}\lfloor(\textbf{TP}_{+3}e^{j3\omega_m t} + \textbf{TP}_{-3}e^{-j3\omega_m t} + \textbf{TP}_{+1}e^{j\omega_m t} + \textbf{TP}_{-1}e^{-j\omega_m t})e^{j\omega_0 t}\rfloor$$
(E.48)

where

$$\textbf{TP}_{+3} = E^3\left[\textbf{G}_3 + \text{Re}[D_2(\omega)]\frac{d\textbf{G}_1}{dV}\textbf{Z}_b(j2\omega_m)\right]$$
(E.49)

$$\textbf{TP}_{-3} = E^3\left[\textbf{G}_3 + \text{Re}[D_2(\omega)]\frac{d\textbf{G}_1}{dV}\textbf{Z}_b^*(j2\omega_m)\right]$$
(E.50)

$$\textbf{TP}_{+1} = E^3\left[3\textbf{G}_3 + \text{Re}[D_2(\omega)]\frac{d\textbf{G}_1}{dV}\textbf{Z}_b(j2\omega_m)\right]$$
(E.51)

$$\textbf{TP}_{-1} = E^3\left[3\textbf{G}_3 + \text{Re}[D_2(\omega)]\frac{d\textbf{G}_1}{dV}\textbf{Z}_b^*(j2\omega_m)\right]$$
(E.52)

Unless $\textbf{Z}_b^*$ is real, the magnitudes of the upper and lower distortion products will be unequal.

Note that the second-order nonlinearities produce products that vary as E^3, exactly as do third-order intermodulation products. This is true in general; bias-induced products vary as E raised to an odd power—the same as intermodulation products.

To summarize, bias-induced products as described above depend on several factors: (1) even-order nonlinearities responsible for current "drive-up", producing an ac when driven by a two-tone signal; (2) bias circuit that converts this ac to modulation voltage that modulates the bias voltage of the device; and (3) change of gain as a function

of bias voltage. If the bias circuit has a reactive component, unequal upper and lower distortion products could occur.

One final note: Proper analysis of bias-induced effects could result in an iterative process, since the dc change will rebias each G_N term to a different value. They may also be affected by more than one bias terminal, as is the case for most two-terminal devices. This leads to a substantially more complex situation than the scenario presented here. Nevertheless, it is hoped that this simplified model provides a useful picture of the processes involved.

SUMMARY

A complex power series characterization scheme is presented from which two-tone products are derived. This makes it possible to exhibit these products as phasors (or vectors) in the complex plane.

This suggests a procedure where the two-tone products can be predicted from the single-tone measurements. First, we consider the single-tone AM-to-AM and AM-to-PM distortion data taken with a vector network analyzer. From these data, the $\mathbf{G}_n$ terms are derived that best fit the following equation:

$$v_0 = \mathrm{Re}\left[\left(\mathbf{G}_1 V + \sum_{n=3,5,7,\ldots}^{\infty} V^n \mathbf{G}_n\right) e^{j\omega t}\right] \qquad (E.53)$$

Knowing the $\mathbf{G}_n$ terms, with input signal given by

$$v_{\mathrm{in}} = E\cos\omega_1 t + E\cos\omega_2 t \qquad (E.54)$$

the two-tone products can be calculated from the equation

$$v_0 = \mathrm{Re}\left[\sum_{p=1,3,5,\ldots}^{\infty}\sum_{n=p,p+2,\ldots}^{\infty} \mathbf{G}_n \frac{n!E^n}{\dfrac{n+p}{2}!\dfrac{n-p}{2}!}\right.$$
$$\left. \times \left(e^{j[(1+p)/2]\omega_1 t + j[(1-p)/2]\omega_2 t} + e^{j[(1-p)/2]\omega_1 t + j[(1+p)/2]\omega_2 t}\right)\right] \qquad (E.55)$$

The coefficients of the first- and third-order products are shown in the following format:

$$v_0 = \mathrm{Re}\lfloor (A_1 E\mathbf{G}_1 + A_3 E^3\mathbf{G}_3 + A_5 E^5\mathbf{G}_5 + \cdots)(e^{j\omega_1 t} + e^{j\omega_2 t})\rfloor$$
$$+ \mathrm{Re}[(B_3 E\mathbf{G}_3 + B_5 E^5\mathbf{G}_5 + B_7 E^7\mathbf{G}_7 + \cdots)(e^{j2\omega_1 t - j\omega_2 t} + e^{j2\omega_2 t - j\omega_1 t})] \quad (E.56)$$

The coefficients A_i and B_i up to the 17th order are as follows:

i	**1**	**3**	**5**	**7**	**9**	**11**	**13**	**15**	**17**
A_i	1	3	10	35	126	462	1716	6435	24310
B_i	None	1	5	21	84	330	1287	5005	19448

SINGLE-TONE VOLTERRA SERIES EXPANSION

This section develops the Volterra series equations of a nonlinear transconductance device when driven by a single-tone (sinusoidal) signal. This generally follows the formulation of Stephen Maas [E.5]. Let

$$V_{dc} + \Delta V_a(t) \tag{E.57}$$

be the applied voltage of such a device. This has a dc part V_{dc} and a time-varying part $\Delta V_a(t)$, where V_{dc} can be thought as the "bias" of the device. The time-varying component is

$$\Delta V_a(t) = \frac{V}{2}[\exp(j\omega t) + \exp(-j\omega t)] \tag{E.58}$$

The output is then

$$
\begin{aligned}
I_R(V_{dc} + \Delta V_a) = \underbrace{I_R(V_{dc})}_{\text{dc term}} &+ \frac{V}{2}[\mathbf{K}_1(\omega)\exp(j\omega t) + \mathbf{K}_1(-\omega)\exp(-j\omega t)] \\
&+ \left(\frac{V}{2}\right)^2 [\mathbf{K}_2(\omega, \omega)\exp(j2\omega t) + \mathbf{K}_2(\omega, -\omega) \\
&+ \mathbf{K}_2(-\omega, \omega) + \mathbf{K}_2(-\omega, -\omega)\exp(-j2\omega t)] \\
&+ \left(\frac{V}{2}\right)^3 [\mathbf{K}_3(\omega, \omega, \omega)\exp(j3\omega t) + \mathbf{K}_3(\omega, \omega, -\omega)\exp(j\omega t) + \cdots] \\
&+ \cdots \\
&+ \left(\frac{V}{2}\right)^n \left\{ \sum \mathbf{K}_n(\omega_1, \omega_2, \ldots, \omega_n) \right. \\
&\times \left. \exp[j(\omega_1 + \omega_2 +, \cdots + \omega_n)t] + \cdots \right\} + \cdots + \cdots
\end{aligned}
\tag{E.59}
$$

where

> Each $\mathbf{K}_n(\omega_1, \omega_2, \ldots, \omega_n)$ is the multidimensional Fourier transform of the nth-order nonlinear impulse response. This impulse response, when convolved with the input signal, will yield the output signal in the time domain.
>
> In the single-tone case, each ω_i equals either $+\omega$ or $-\omega$.

$$\mathbf{K}_n(\omega_1, \omega_2, \ldots, \omega_n) = \mathbf{K}_n^*(-\omega_1, -\omega_2, \ldots, -\omega_n)$$

Of the summation $\sum \mathbf{K}_n(\omega_1, \omega_2, \ldots, \omega_n) \exp[j(\omega_1 + \omega_2 + \cdots + \omega_n)t]$ the following is true:

> The summation is made with all possible combinations of $(\omega_1, \omega_2, \ldots, \omega_n)$. One way to ensure all terms are collected is to start at $(\omega, \omega, \ldots, \omega)$ and progress in a binary fashion to $(-\omega, -\omega, \ldots, -\omega)$.
>
> The summation contains 2^n terms.
>
> Each term has a conjugate match; therefore the sum is real.

Each K_n will yield terms at frequency ω, $(n-2)\omega$, $(n-4)\omega$, ..., the last term being a frequency ω if n is odd and at dc if n is even.

Fundamental Term

The component at the fundamental frequency ω is

$$I_0|_{\text{fundamental}} = \frac{V}{2}[\mathbf{H}_1^+(\omega)\exp(j\omega t) + \mathbf{H}_1^-(-\omega)\exp(-j\omega t)]$$

$$+ \left(\frac{V}{2}\right)^3 [\mathbf{H}_3^+(\omega)\exp(j\omega t) + \mathbf{H}_3^-(-\omega)\exp(-j\omega t)]$$

$$+ \left(\frac{V}{2}\right)^5 [\mathbf{H}_5^+(\omega)\exp(j\omega t) + \mathbf{H}_5^-(-\omega)\exp(-j\omega t)]$$

$$+ \ldots \tag{E.60}$$

where

$$\mathbf{H}_n^+(\omega) = \sum \mathbf{K}_n(\omega_1, \omega_2, \ldots, \omega_n) \qquad n \text{ odd} \tag{E.61}$$

where the summation (for n odd) is made over all possible combinations of ω such that the number of positive ω exceeds the number of negative ω by exactly 1. There are $n!/\{[(n-1)/2]![(n+1)/2]!\}$ such terms. Similarly

$$\mathbf{H}_n^-(\omega) = \sum \mathbf{K}_n(\omega_1, \omega_2, \ldots, \omega_n) \qquad n \text{ odd} \tag{E.62}$$

where the summation (n odd) is made over all possible combinations of ω such that the number of negative ω exceeds the number of positive ω by exactly 1. There are $n!/\{[(n-1)/2]![(n+1)/2]!\}$ such terms. Define

$$\mathbf{H}_n(\omega) = \frac{1}{2^{n-1}}\mathbf{H}_n^+(\omega) \tag{E.63}$$

so that

$$I_0|_{\text{fundamental}} = \text{Re}\left[\sum_{i=1,3,5\ldots}^{\infty} V^i \mathbf{H}_i(\omega)e^{(j\omega)}\right] \tag{E.64}$$

dc Term

The dc term of Eq. (E.59) is

$$I_R(V_{\text{dc}} + \Delta V_a) = \underbrace{I_R(V_{\text{dc}})}_{\text{dc term}} + \left(\frac{V}{2}\right)^2 [\mathbf{K}_2(\omega, -\omega) + \mathbf{K}_2(-\omega, \omega)]$$

$$+ \left(\frac{V}{2}\right)^4 [\mathbf{K}_4(\omega, \omega, -\omega, -\omega) + \mathbf{K}_4(\omega, -\omega, \omega, -\omega)$$

$$+ \mathbf{K}_4(\omega, -\omega, -\omega, \omega) + \mathbf{K}_4(-\omega, \omega, \omega, -\omega)$$

$$+ \mathbf{K}_4(-\omega, \omega, -\omega, \omega) + \mathbf{K}_4(-\omega, -\omega, \omega, \omega)]$$

$$+ \cdots$$

$$+ \left(\frac{V}{2}\right)^n \left[\sum \mathbf{K}_n(\omega_1, \omega_2, \ldots, \omega_n)\right]$$

$$+ \cdots \tag{E.65}$$

where the summation (for n even) is made over all possible combinations of ω_i where the number of positive ω exactly equals the number of negative ω. There are $n!/[(n/2)!]^2$ such terms. Define

$$D_n(\omega) = \left(\frac{1}{2}\right)^n \sum \mathbf{K}_n(\omega_1, \omega_2, \ldots, \omega_n) \qquad n \text{ even} \tag{E.66}$$

where the summation (for n even) is made over all possible combinations of ω_i where the number of positive ω exactly equals the number of negative ω. Here, again, the summation is real. Equation (E.65) can be written as

$$I_R(V_{\mathrm{dc}} + \Delta V_a) = \underbrace{I_R(V_{\mathrm{dc}})}_{\text{dc term}} + \sum_{n=2,4,6,\ldots}^{\infty} V^n D_n(\omega) \tag{E.67}$$

NONLINEAR PARALLEL RC NETWORK

Finally, the specific example consisting of a parallel combination of a nonlinear resistor and a nonlinear capacitor, as shown in Figure E.8 will be analyzed. It is driven by a dc voltage in series with a finite set of sinusoidals. We wish to derive the current that results. This would be the sum of the current flowing through each element. That is,

$$I_0 = I_R + I_C \tag{E.68}$$

where I_R is the current generated by the resistor and I_C is the current generated by the capacitor. Let

$$V_{\mathrm{dc}} + \Delta V_a(t) \tag{E.69}$$
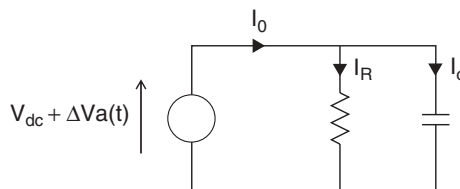
FIGURE E.8   Schematic diagram.

be the applied voltage. This has a dc part V_{dc} and a time-varying part $\Delta V_a(t)$, where V_{dc} can be thought to be the dc "bias" of the device. The time-varying component is

$$\Delta V_a(t) = V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t) + V_3 \cos(\omega_3 t) + \cdots + V_n \cos(\omega_n t)$$

$$= \sum_{i=1,2,3\ldots}^{n} V_i \cos(\omega_i t)$$

$$= \operatorname{Re}\left(\sum_{i=1,2,3\ldots}^{n} V_i e^{j\omega_i t}\right) \tag{E.70}$$

We first deal with the resistor. The instantaneous current through it is a function of the instantaneous voltage across it. The Taylor series expansion around V_{dc} is

$$I_R(V_{dc} + \Delta V_a) = \underbrace{I_R(V_{dc})}_{\text{dc term}} + \frac{\Delta V_a}{1!}\frac{dI_R}{dV} + \frac{\Delta V_a^2}{2!}\frac{d^2 I_R}{dV^2} + \frac{\Delta V_a^3}{3!}\frac{d^3 I_R}{dV^3} + \cdots$$

$$= \underbrace{I_R(V_{dc})}_{\text{dc term}} + \Delta V_a \left(\frac{1}{1!}\frac{dI_R}{dV} + \frac{\Delta V_a^1}{2!}\frac{d^2 I_R}{dV^2} + \frac{\Delta V_a^2}{3!}\frac{d^3 I_R}{dV^3} + \cdots\right) \tag{E.71}$$

Equation (E.71) can be written as

$$I_R(V_{dc} + \Delta V_a) = I_R(V_{dc}) + \operatorname{Re}\left(\sum_{i=1}^{n} V_i e^{j\omega_i t} \sum_{p=1}^{\infty} \frac{\Delta V_a^{p-1}}{p!}\frac{d^p I_R}{dV^p}\right) \tag{E.72}$$

The reason for this unorthodox form will become apparent later. We next turn our attention to the nonlinear capacitor.

Usually, for fixed capacitors, the charge Q that accumulates on its plates is linearly proportional to the voltage applied, the proportionally constant being the capacitance C. That is,

$$Q = CV \tag{E.73}$$

In this case, the charge is not linear with voltage. We can expand the charge-versus-voltage relationship about V_{dc} in a Taylor series expansion as follows:

$$Q(V_{dc} + \Delta V_a) = Q(V_{dc}) + \frac{\Delta V_a}{1!}\frac{dQ}{dV} + \frac{\Delta V_a^2}{2!}\frac{d^2 Q}{dV^2} + \frac{\Delta V_a^3}{3!}\frac{d^3 Q}{dV^3} + \cdots \tag{E.74}$$

The time derivative of charge yields the dynamic current. Hence from Eq. (E.74)

$$I_c = \frac{d(\Delta V_a)}{dt}\left(\frac{1}{0!}\frac{dQ}{dV} + \frac{\Delta V_a}{1!}\frac{d^2 Q}{dV^2} + \frac{\Delta V_a^2}{2!}\frac{d^3 Q}{dV^3} + \cdots\right) \tag{E.75}$$

From Eq. (E.70),

$$\frac{d(\Delta V_a)}{dt} = \operatorname{Re}\left(\sum_{i=1}^{n} j\omega_i V_i e^{j\omega_i t}\right) \tag{E.76}$$

Substituting Eq. (E.76) in Eq. (E.75) yields

$$I_c = \text{Re}\left[V_1 e^{j\omega_1 t}\left(j\omega_1 \frac{dQ}{dV} + j\omega_1 \frac{\Delta V_a}{1!}\frac{d^2 Q}{dV^2} + j\omega_1 \frac{\Delta V_a^2}{2!}\frac{d^3 Q}{dV^3} + \cdots \right) \right.$$

$$+ V_2 e^{j\omega_2 t}\left(j\omega_2 \frac{dQ}{dV} + j\omega_2 \frac{\Delta V_a}{1!}\frac{d^2 Q}{dV^2} + j\omega_2 \frac{\Delta V_a^2}{2!}\frac{d^3 Q}{dV^3} + \cdots \right)$$

$$+ \ldots$$

$$\left. + V_n e^{j\omega_n t}\left(j\omega_n \frac{dQ}{dV} + j\omega_n \frac{\Delta V_a}{1!}\frac{d^2 Q}{dV^2} + j\omega_n \frac{\Delta V_a^2}{2!}\frac{d^3 Q}{dV^3} + \cdots \right) \right] \quad (\text{E.77})$$

or more concisely

$$I_c = \text{Re}\left\{ \sum_{i=1}^{n} V_i e^{j\omega_i t}\left[\sum_{p=1}^{\infty} (\Delta V_a)^{p-1}\frac{j\omega_i}{(p-1)!}\frac{d^p Q}{dV^p} \right] \right\} \quad (\text{E.78})$$

The total current, in consideration of Eq. (E.68), (E.72), and (E.78), is then

$$I_0 = I_R(V_{dc}) + \text{Re}\left[\sum_{i=1}^{n} V_i e^{j\omega_i t}\sum_{p=1}^{\infty}(\Delta V_a)^{p-1}\frac{1}{p!}\frac{d^p I_R}{dV^p} \right]$$

$$+ \text{Re}\left\{ \sum_{i=1}^{n} V_i e^{j\omega_i t}\left[\sum_{p=1}^{\infty}(\Delta V_a)^{p-1}\frac{j\omega_i}{(p-1)!}\frac{d^p Q}{dV^p} \right] \right\} \quad (\text{E.79})$$

If we let

$$\mathbf{K}_p(j\omega_i) = \frac{1}{p!}\frac{d^p I_R}{dV^p} + \frac{j\omega_i}{(p-1)!}\frac{d^p Q}{dV^p} \quad (\text{E.80})$$

Equation (E.79) can then be put in the concise form

$$I_0 = I_R(V_{dc}) + \text{Re}\left[\sum_{i=1}^{n} V_i e^{j\omega_i t}\sum_{p=1}^{\infty}(\Delta V_a)^{p-1}\mathbf{K}_p(j\omega_i) \right] \quad (\text{E.81})$$

For better viewing the above equation is expanded:

$$I_0 = I_R(V_{dc}) + \text{Re}\{ V_1 e^{j\omega_1 t}\lfloor \mathbf{K}_1(j\omega_1) + \Delta V_a \mathbf{K}_2(j\omega_1) + \Delta V_a^2 \mathbf{K}_3(\omega_1) + \cdots \rfloor$$

$$+ V_2 e^{j\omega_2 t}[\mathbf{K}_1(j\omega_2) + \Delta V_a \mathbf{K}_2(j\omega_2) + \Delta V_a^2 \mathbf{K}_3(j\omega_1) + \cdots]$$

$$+ \cdots$$

$$+ V_n e^{j\omega_n t}[\mathbf{K}_1(j\omega_n) + \Delta V_a \mathbf{K}_2(j\omega_n) + \Delta V_a^2 \mathbf{K}_3(j\omega_1) + \cdots]\} \quad (\text{E.82})$$

For the single-tone case, where

$$\Delta V_a = V\cos\omega t \quad (\text{E.83})$$

the output current is

$$I_0 = I_R(V_{dc}) + \text{Re}\left\{\left[\sum_{p=1}^{\infty}(V\cos\omega t)^{p-1}\mathbf{K}_p(j\omega)\right]Ve^{j\omega t}\right\}$$

$$= I_R(V_{dc}) + \text{Re}\{[\mathbf{K}_1 + \mathbf{K}_2 V\cos\omega t + \mathbf{K}_3(V\cos\omega t)^2 + \cdots]Ve^{j\omega t}\} \quad \text{(E.84)}$$

From the above equation and with the aid of Eq. (E.21) the single tone expression of Eq. (E.4) can be derived. This is left to the reader.

ACKNOWLEDGMENTS

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APPENDIX F

PASSIVE MICROWAVE ELEMENTS

INTRODUCTION

The rapid expansion of microwave utilization derives principally from advances in two major areas: microwave semiconductors and the technology of microwave integrated circuits. The passive microwave elements technology has made use of the achievements in semiconductor fabrication and also has new branches, such as monolithic elements (discussed in Section F.4) and lumped elements (which are especially suitable for monolithic MICs and are discussed in Section F.1).

Since the analysis of transmission, such as microstrip lines and CPW is becoming more accurate and effective, CAD plays a more and more important role in microwave technology. The new analysis and modeling methods are given where we introduce the distributed elements (Section F.2) and discontinuities (Section F.3).

In the final section (Section F.5) we introduce several special-purpose elements. Dielectric resonators as an example, have been widely used in recent years, since the development of the dielectric resonator with high Q-factor.

The theory and design of passive microwave elements have been reported in numerous articles widely scattered in the technical literature, but there is no single comprehensive description available. This appendix is intended to fill that gap.

F.1 LUMPED ELEMENTS

The lumped elements can be used for definition in the microwave band if the sizes of lumped elements can be made much smaller than the wavelength. Computer-aided design of circuits using lumped elements requires complete and accurate characterization

of thin film lumped elements of microwave frequency. Differences between distributed and lumped elements with MIC circuits are primarily to provide physical support and isolation between the various elements, whereas for MICs using distributed elements, most of the energy is stored or propagates within the substrate.

Resistor (Thin Film, etc.)
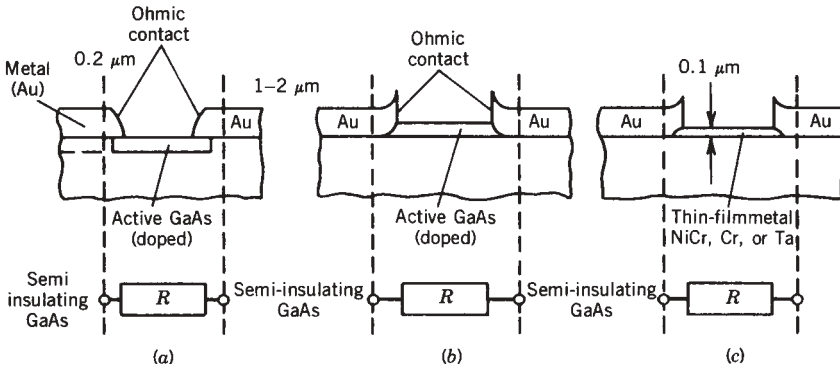
FIGURE F.1   Resistor types for GaAs MMICs: (*a*) implanted semiconductor resistor (surface resistance, $R_F > 20 \ \Omega$); (*b*) mesa semiconductor resistance ($R_F > 3 \ \Omega$); (*c*) vapor deposited or sputtered thin-film resistance ($3 \ \Omega \ R_F < 100 \ \Omega$).

Description: Resistors can be produced as semiconductor resistors (Fig. F. 1*a*, *b*) or as thin-film resistors with resistive layers of NiCrTa or Cr.

References: F.1, pp. 70–71
F.2, pp. 108–121

Capacitor (Thin Film, etc.)
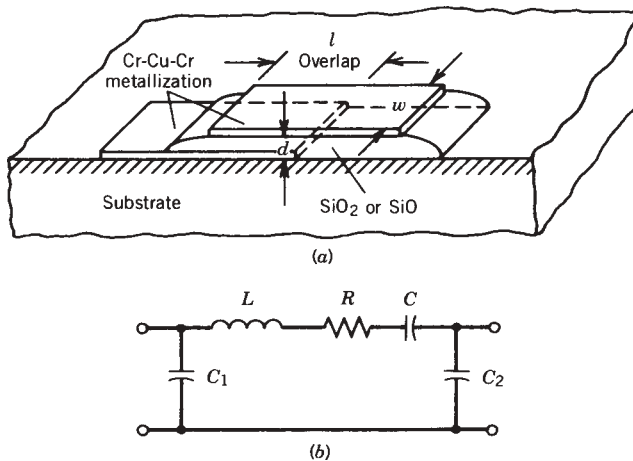
FIGURE F.2   (a) Configuration of an overlay capacitor; (b) Equivalent circuit for the capacitor in (a).

Description: With the dielectric layer (or insulator layer) between the two metal plates, we have a metal dielectric-metal capacitor.

Parameters: Overlap l, width of the top and bottom plates for capacitor W, and thickness of dielectric or insular layer d.

Equivalent Circuit: R represents losses in the capacitor; parasitics are represented by a series inductance and fringing capacitance C_1 and C_2 due to the ground. C, the capacitor, is much bigger than C_1 or C_2.

References: F.3, pp. 216–217
F.2, pp. 118–121

Bond Wire
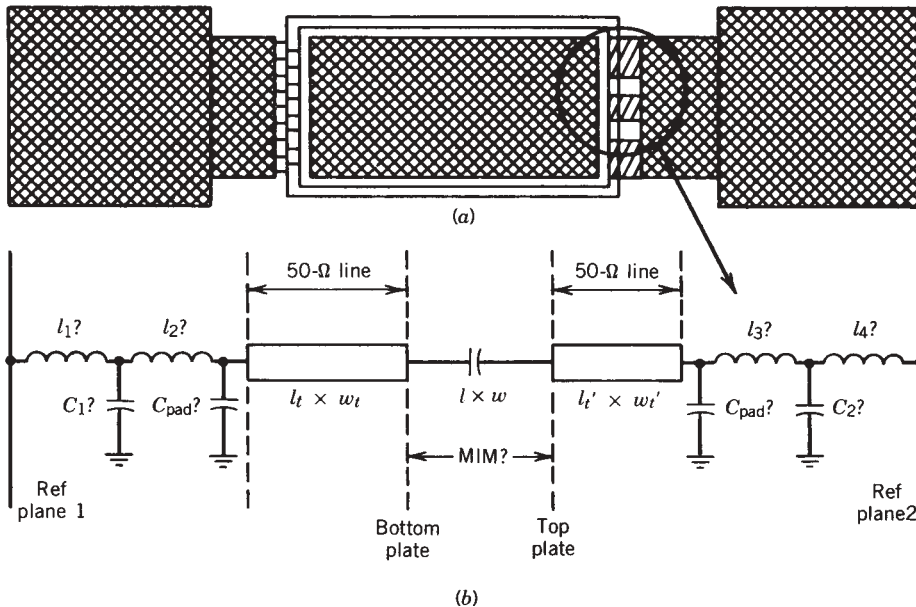
FIGURE F.3 Schematic of the circuit which includes bond wires. The elements shown with '?' are optimized. **MIM** has the distributed model incorporated in it. $(l_1 + l_2)$, $(l_3 + l_4)$ are the total inductances for the bond wires.

Description: The bond wires in Fig. F.3*a* have the equivalent circuit shown in Fig. F.3*b*. The analysis method is transmission-line theory.

Parameters: Length and width of the bond wires are required.

Equivalent Circuit: L1, L2, L3, and L4 are the inductors for the bond wires, C_1 C_2, and C_{pad} are the capacitors for the bond wires.

Reference: F.5.

Diodes (Beam Lead, etc)

Description: The beam-lead diode connected to two ends of microstrip exists in a form that can be built into MICs.
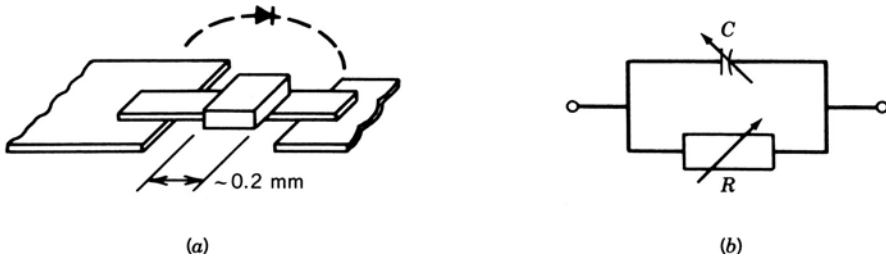
FIGURE F.4   Hybrid elements: (*a*) diode chip; (*b*) equivalent circuit.

Equivalent Circuit: The variables C and R depend on the working condition of the diode, such as the bias voltage.

Reference: F.1, pp. 56–57

F.2   DISTRIBUTED ELEMENTS

Transmission Lines
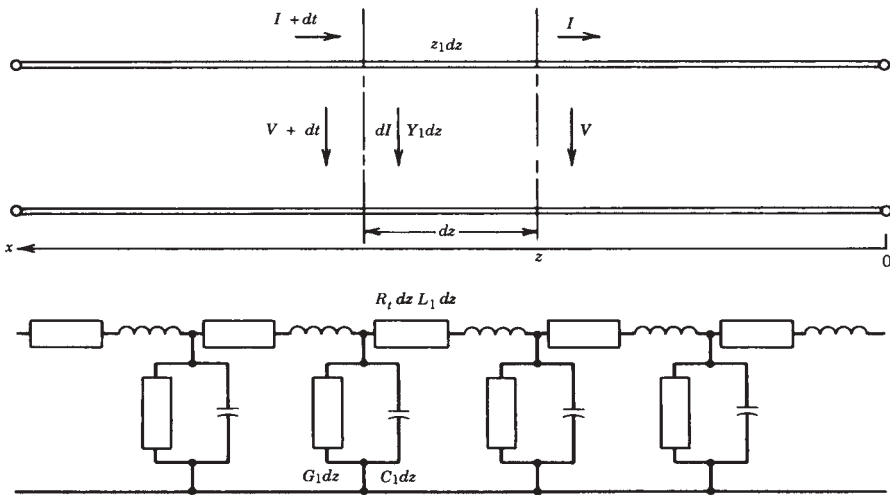
FIGURE F.5   Transmission line and its equivalent circuit.

The transmission line and its equivalent circuit are shown here. The three transmission-line examples are microstrip line, coplanar waveguide, and grounded coplanar waveguide, which are discussed below.

Microstrip Line   *Structure Parameters: W* is the width of the microstrip, h is the thickness of the dielectric layer, ε_r is the dielectric permittivity, and T is the thickness of the microstrip.

Brief Description: Microstrip line is the most popular of these transmission structures, due mainly to the fact that the mode of propagation on microstrip is almost TEM.
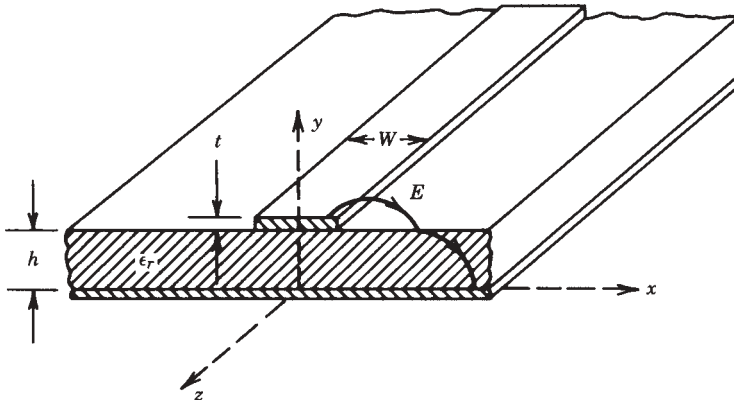
FIGURE F.6   Microstrip configuration.

Methods of Solution

1. *Quasi-static analysis*. This method can be used assuming that the mode of wave propagation in microstrip is pure TEM.
2. *Microstrip dispersion model*. As the non-TEM behavior causes the effective dielectric constant ε_{re} and impedance Zo of the microstrip to be functions of frequency, semiempirical techniques are used which take into account the non-TEM nature.
3. *Exact evaluation of ε_{re} and Zo_n; full-wave analysis of the microstrip*. One has to introduce time-varying electric and magnetic fields and solve the wave equation. Instead of evaluating the capacitance in quasi-static analysis, one has to determine the propagation constant.

Reference: F.6, pp. 4–5, 20, 43

Coplanar Waveguide (CPWC)
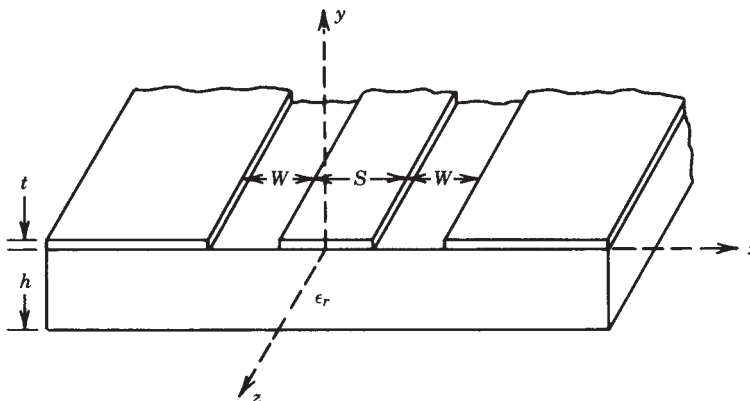
FIGURE F.7   Coplanar waveguide.

Parameters: Coplanar waveguide (all the conductors are in the same plane) consists of a center strip with two ground planes located parallel to and in the plane of the strip, and with W in between, the width of the center strip is S and the thickness of the conductor and dielectric layer (with ε_r) are t and h separately.

Methods: Coplanar lines have been studied using *quasi-static approximation* as well as *full-wave analysis*. A quasi-static analysis of these transmission lines was carried out using conformal mapping and with the assumption that the dielectric substrate is thick enough to be considered infinite. For commonly used thicknesses this assumption is valid for large values of the dielectric constant. A modification of the method studied takes the finite thickness of the dielectric substrate into consideration. The effect of enclosure on the characteristics of CPW has been determined using the finite difference method. A full-wave analysis of coplanar lines which provides information regarding the frequency dependence of phase velocity and characteristic impedance has been carried out by using Galerkin's method in the spectral domain by the variational method and by nonuniform discretization of integral equations.

Reference: F.6, p. 260

Grounded Coplanar Waveguide (GCPW)
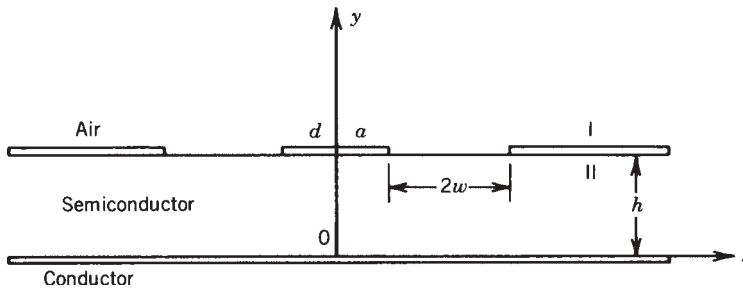
FIGURE F.8   Grounded coplanar waveguide.

Parameters: The difference between grounded coplanar waveguide and coplanar waveguide is the extra conductor plane under the dielectric layer.

Methods: As one kind of coplanar lines, GCPW can be studied using quasi-static approximation as well as full-wave analysis. The spectral domain method [F.7] has been proved to be an effective method.

Reference: F.7

Coupled Lines

Description: A coupled-line configuration consists of two transmission lines parallel to each other and in close proximity. Because of the coupling of support, there are two different modes of propagation; that is, they share their own characteristic impedances.

Parameters: The configuration for the coupled lines is shown in Fig. F.9, with the parameters labeled in the figure.

Methods

1. *Even- and odd-mode method*. Valid for description of symmetrical coupled lines. Wave propagation along a coupled line is expressed in terms of two modes,
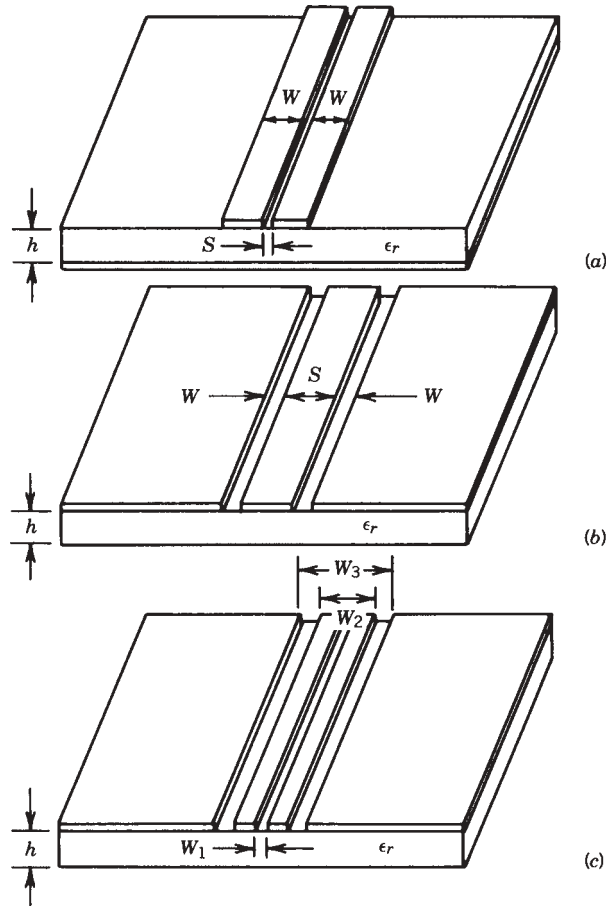
FIGURE F.9   Configurations of (*a*) coupled microstrip lines; (*b*) coupled slotlines; and (*c*) coupled coplanar waveguides.

corresponding to an even or an odd symmetry about a plane which can, therefore, be replaced by a magnetic or electric wall for the purpose of analysis.

2. *Coupled-mode approach*. This method is quite general and is applicable to asymmetric coupled lines. Also, the wave propagation is expressed in terms of the modes of propagation on individual uncoupled lines modified by the coupling because of mutual capacitances and inductances.

3. *Graph transformation technique*. This technique uses Richard's transformation and allows the coupled-line structures to be treated in exactly the same manner as lumped networks.

4. *Congruent transformation technique*. This approach is powerful for establishing coupled-line properties when there are large number of lines coupled together.

Reference: F.6, pp. 303–305

Waveguides (Coax, Rectangular)
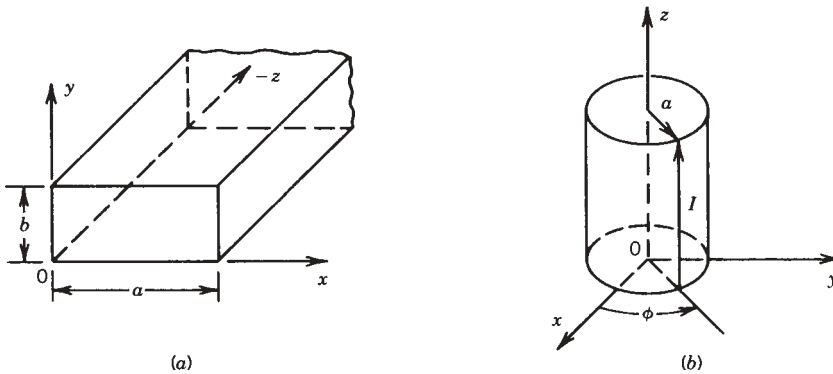
FIGURE F.10   Coordinates of a rectangular guide and a coax guide.

Description: In general, a waveguide consists of a hollow metallic tube of a rectangular or circular shape used to guide an electromagnetic wave. Waveguides are used principally at frequencies in the microwave range; inconveniently large guides would be required to transmit radio-frequency power at longer wavelengths. At frequency range X band from 8.00 to 12.0 GHz, for example, the U.S. standard rectangular waveguide WR-90 has an inner width of 2.286 cm (0.9 in.) and an inner height of 1.016 cm (0.4 in.); but its outside dimensions are 2.54 cm (1 in.) wide and 1.27 cm (0.5 in.) high.

In waveguides the electric and magnetic fields are confined to the space within the guides. Thus no power is lost through radiation, and even the dielectric loss is negligible, since the guides are normally air-filled. However, there is some power loss as heat in the walls of the guides, but the loss is very small.

It is possible to propagate several modes of electromagnetic waves within a waveguide. These modes correspond to solutions of Maxwell's equations for the particular waveguides. A given waveguide has a definite cutoff frequency for each allowed mode. If the frequency of the impressed signal is above the cutoff frequency for a given mode, the electromagnetic energy can be transmitted through the guide for that particular mode without attenuation. Otherwise, the electromagnetic energy with a frequency below the cutoff frequency for that particular mode will be attenuated to a negligible value in a relatively short distance. *The dominant mode in a particular guide is the mode having the lowest cutoff frequency.* It is advisable to choose the dimensions of a guide in such a way that for a given input signal, only the energy of the dominant mode can be transmitted through the guide.

Method

1. The desired waveguide quotients are written in the form of either rectangular or cylindrical coordinate systems suitable to the problem at hand.
2. Apply the boundary condition.
3. Get the partial differential equation and solve them by proper method (mathematical methods).

Reference: F.8, pp. 104–105

Taper
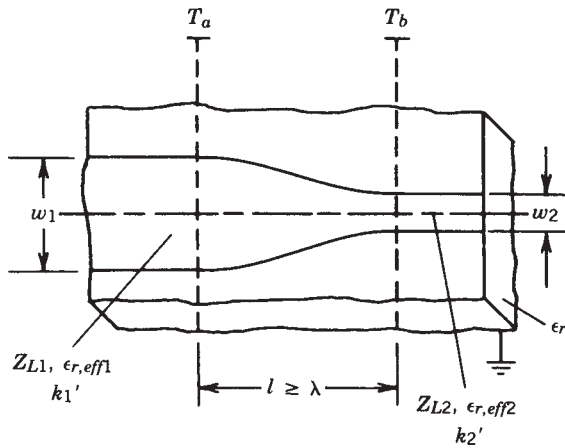
FIGURE F.11   Taper.

Description: The taper with the conductor width W_1 and W_2 has the effect that S_{11} and S_{22} can be maintained as low as required by choice of shape and length.

Method: The planar waveguide model, including high-order modes, can be used to analyze the the structure.

Reference: F.1, pp. 281–282

Air Bridge and Via
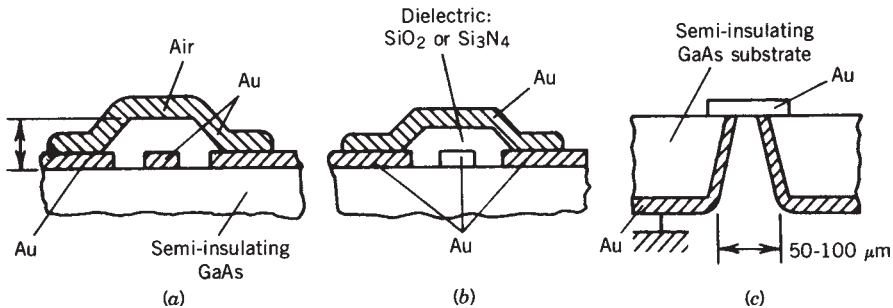
FIGURE F.12   Connecting elements for MMICs: (a) air bridge ("via"); (b) dielectric bridge; (c) ground through contact (via hole ground, "via hole").

Description: Connectors are important components for MMICs. To connect separated metallized areas, low-capacitance air bridges (air bridges, via) or dielectric bridges, or ground through contact (via a hole ground "via hole") are used. The dimensions and parameters are labeled in Fig. F.12.

Reference: F.1, pp. 70–71

Wrap
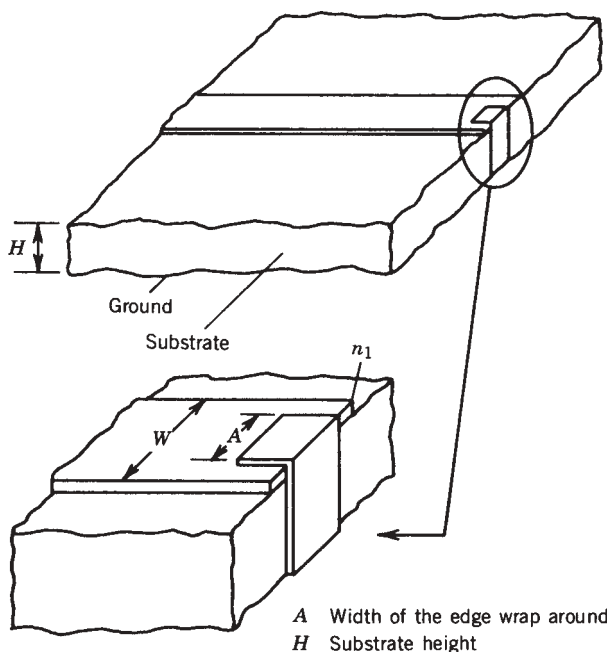
FIGURE F.13   Wrap.

Description: Wrap around ground in microstrip.
Equivalent circuit: Wrap can be modeled by a parallel inductor and a resistor.
Reference: F.1, p. 306
F.9, pp. 4–136

Coupler (Lange, Rat-Race, Branch-Line)

Description: There are two kinds of couplers. Directional couplers and hybrid couplers (such as rat-race and branch-line)
Analysis Method: Even- and odd-mode theory can be used to analyze the couplers even though the couplers are not symmetrical in structure.
References: F.1, p. 14
F.2, pp. 154–162, 383–390
F.10, pp. 171–176
F.11, pp. 775–842

F.3   DISCONTINUITIES

The microstrip or other planar transmission-line discontinuities can be analyzed by the quasi-static or full-wave method. The latter will be more accurate.

The following analysis methods are discussed in detail and in two categories: quasistatic and full-wave analysis. These methods are applicable for such discontinuities as
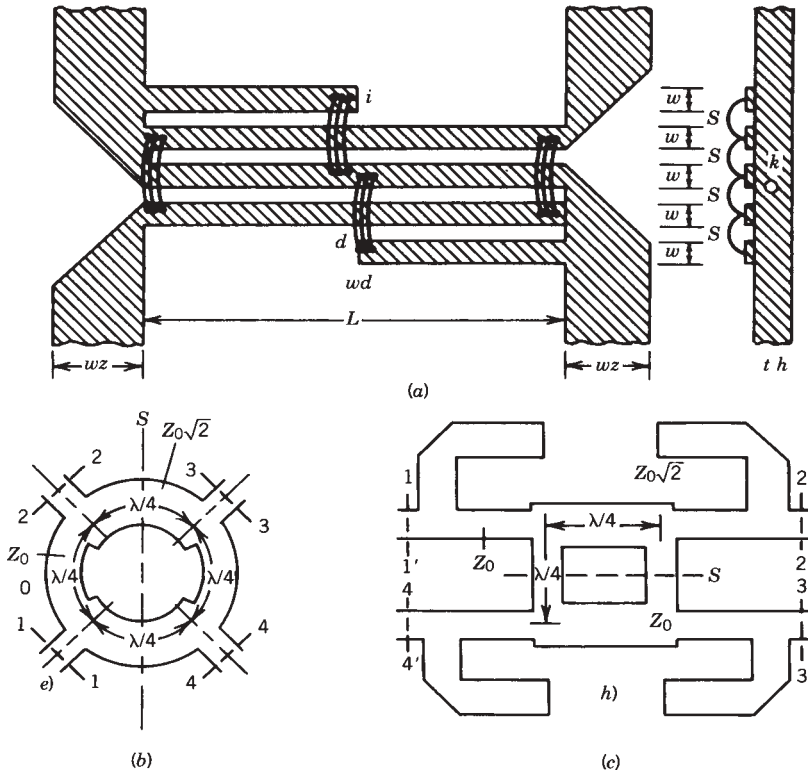
FIGURE F.14   Couplers.

gap step, bend, tee, cross, slit, and open. After the discussion of methods, the equivalent models for each case (gap, step, etc.) are given.

Methods

1. *Quasi-static analysis.* This involves calculations of static capacitances and low-frequency inductances. The equivalent circuit is derived from these results. To consider the dispersion, a waveguide-type dynamic analysis taking dispersion into account is carried out.

   To calculate the capacitances, the following methods are effective: (a) matrix version method, (b) variational method, (c) Galerkin's method in the spectral domain, and (d) use of line sources with charge reversal.

   To calculate inductances using the quasi-static method, we may use the fundamental Maxwell equations and get the inductances expression in closed form.

2. *Fullwave analysis.* Based on the planar waveguide model, the Galerkin method in FTD and the contour integral method can be used.

References: F.1, pp. 189–202
F.2, pp. 31–47
F.6, pp. 107–193
F.12, pp. 43–60

Gap
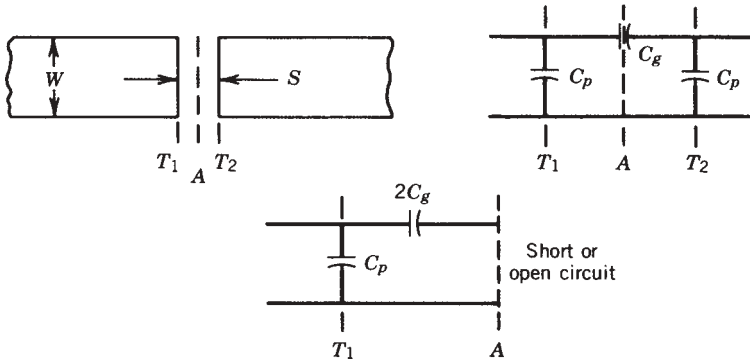
FIGURE F.15   Representation of a gap in microstrip and its equivalent circuit.

Step
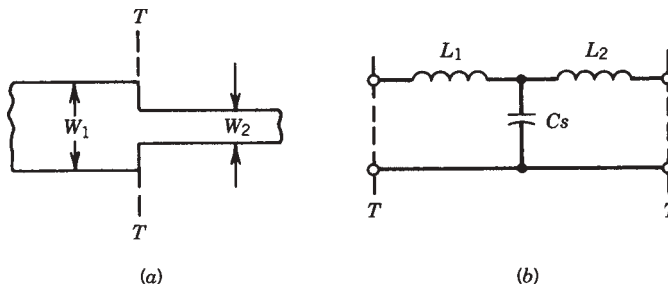
FIGURE F.16   A microstrip step discontinuity and the equivalent circuit.

Bend
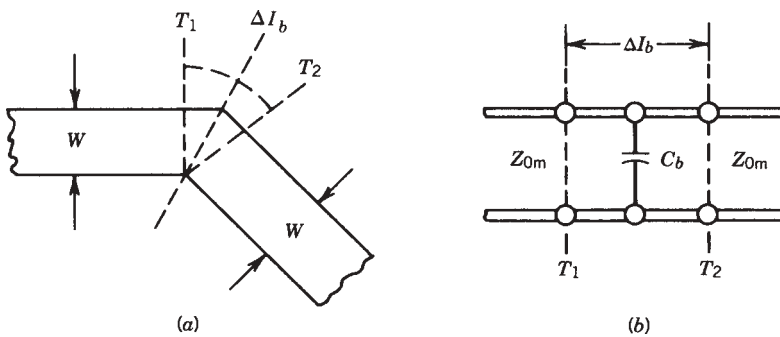
FIGURE F.17   Geometry and equivalent circuit of a microstrip bend.

Tee

(a)   *(b)*
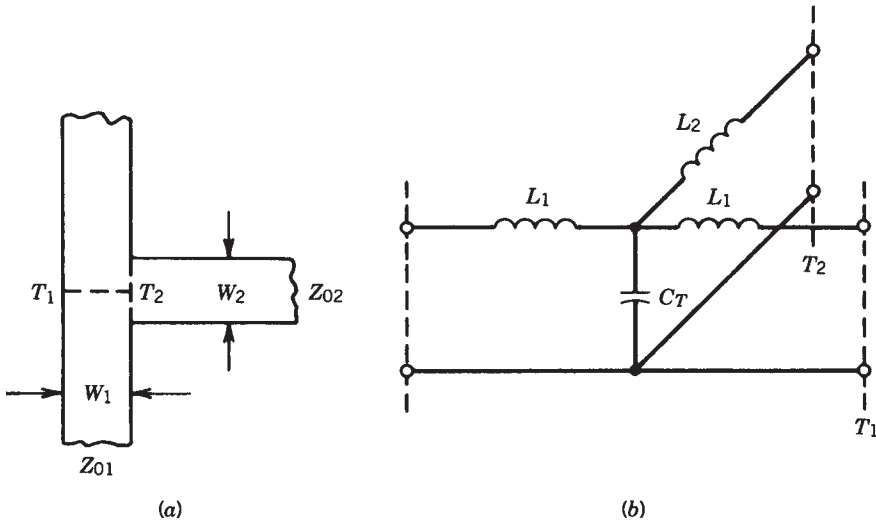
FIGURE F.18   Geometry and equivalent circuit of a microstrip tee junction.

Cross

(a)   *(b)*
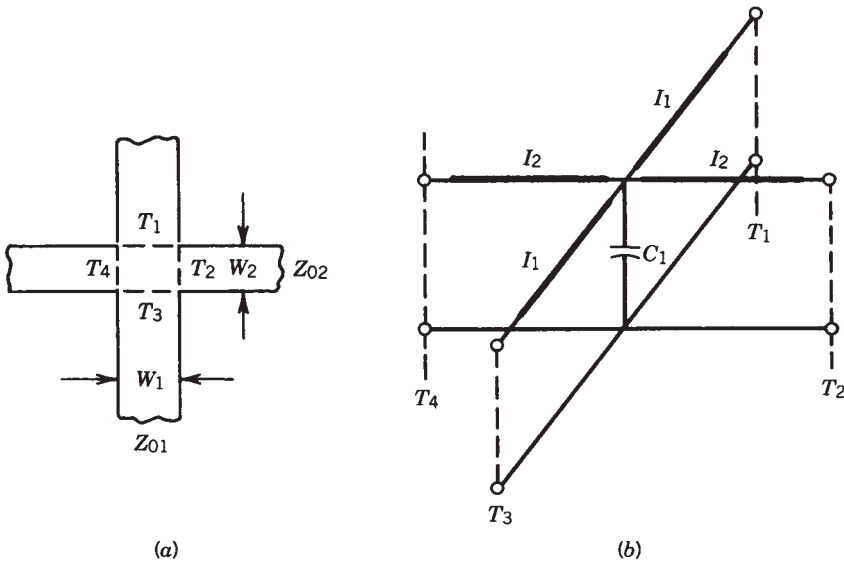
FIGURE F.19   Geometry and equivalent circuit of a microstrip cross junction.

Slit

<div align="center">(a)</div>

<div align="center">(b)</div>
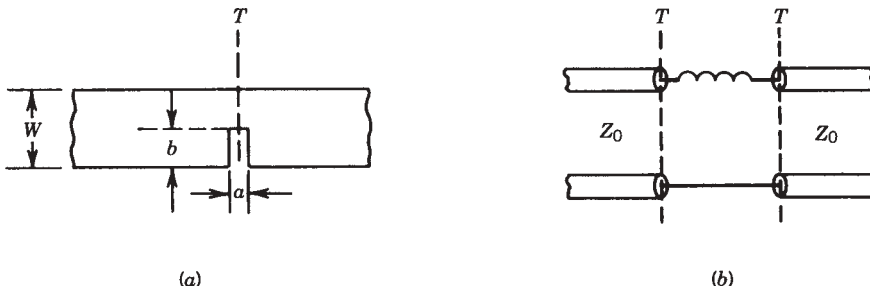
FIGURE F.20   Geometry and equivalent circuit of a microstrip slit.

Open

<div align="center">(a)</div>

<div align="center">(b)</div>
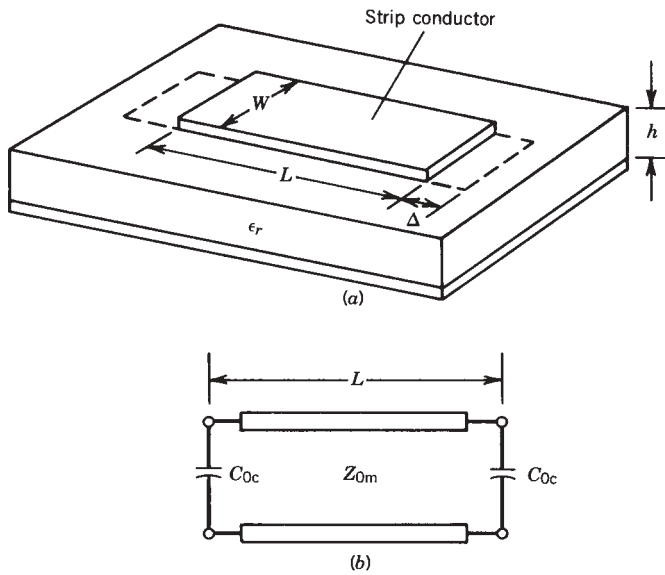
FIGURE F.21   Configuration for calculation of microstrip open-end capacitance and its equivalent circuit.

F.4   MONOLITHIC ELEMENTS

Interdigital Capacitor

Methods: The capacitance between two sets of digits in interdigital structure is found by using the capacitance formula for the odd mode in coupled microstrip lines, with the ground plane spacing tending to an infinitely large value.

   References: F.2, pp. 383–390

            F.3, p. 217
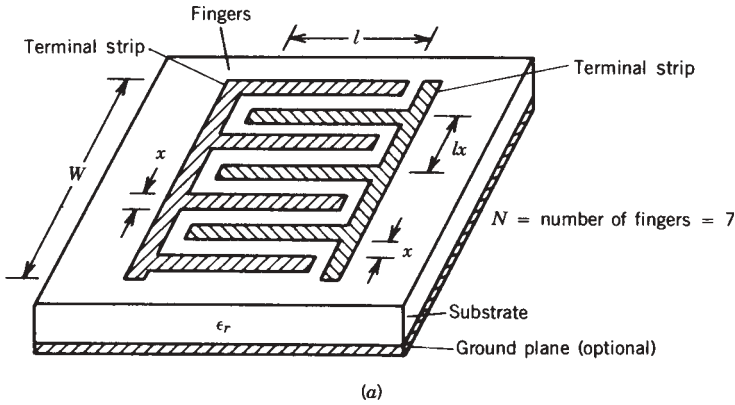
FIGURE F.22   (*a*) Configuration of an interdigital capacitor.
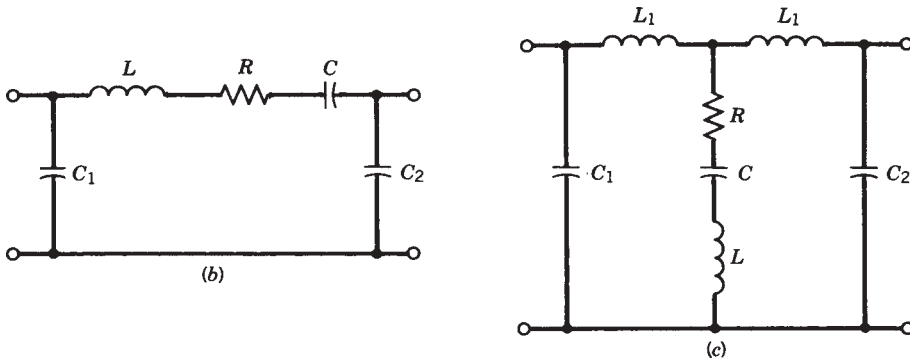
FIGURE F.22   (*b*) Equivalent circuit for series mounting; (*c*) Equivalent circuit for shunt mounting.

Interdigital Rectangular and Spiral Inductor

Description: The equivalent circuit for the spiral configuration does not consist of an inductance alone. There are associated parasitics in the form of self-capacitance and interturn capacitance, C_0, as well as the shunt fringing capacitances C_1 and C_2 due to the effects of ground. The equivalent circuit for a spiral inductor, including parasitics, is shown in Fig. F.23*b*. The series resistance R accounts for the loss. The typical range of values for parasitic elements for a spiral with diameter in the range 1.0 to 5.0 mm on an alumina substrate are as follows: C_0 is nearly 0.15 pF, C_1 ranges from 0.1 to 0.2 pF, C_2 ranges from 0.05 to 0.1 pF, and Q at 4 GHz ranges from 80 to 100.

   References: F.3, p. 211
               F.10, p. 160

Thin-Film Capacitor

See "Capacitor" in Section D.1.
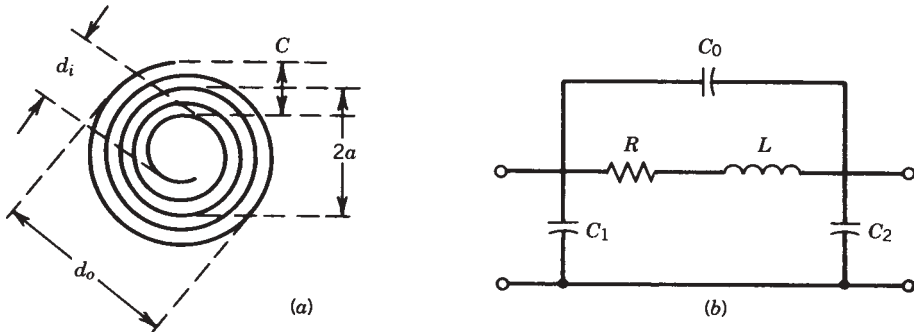
FIGURE F.23   (*a*) Configuration of a spiral inductor; (*b*) Equivalent circuit for a spiral inductor.
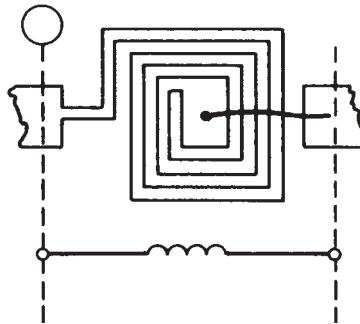
FIGURE F.24   Interdigital rectangular inductor layout and the equivalent circuit.

Thin-Film Resistor

See "Resistor" in Section F.1.
   Reference: F.2, pp. 253–260, 326–347

Interdigital transformer

Reference: F.15; F.16

Underpass/Overpass

See "Air Bridge and Via in Section F.2."

F.5   SPECIAL-PURPOSE ELEMENTS

Yig (Yttrium Iron Garnet, Y3Fe6012)

Description: It has a very high unload resonator Q-factor Q_0 up to 110,000 and can be used at its ferromagnetic resonance as a resonator to tune oscillators and filers. The resonant frequency of the YIG element can be linearly changed over a wide range,
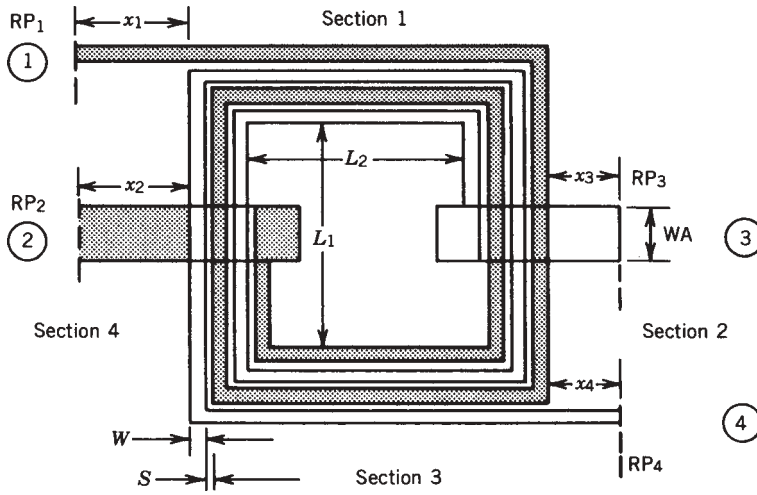
FIGURE F.25 Geometry parameters for the module PLTRAN describing the general transformer geometry.
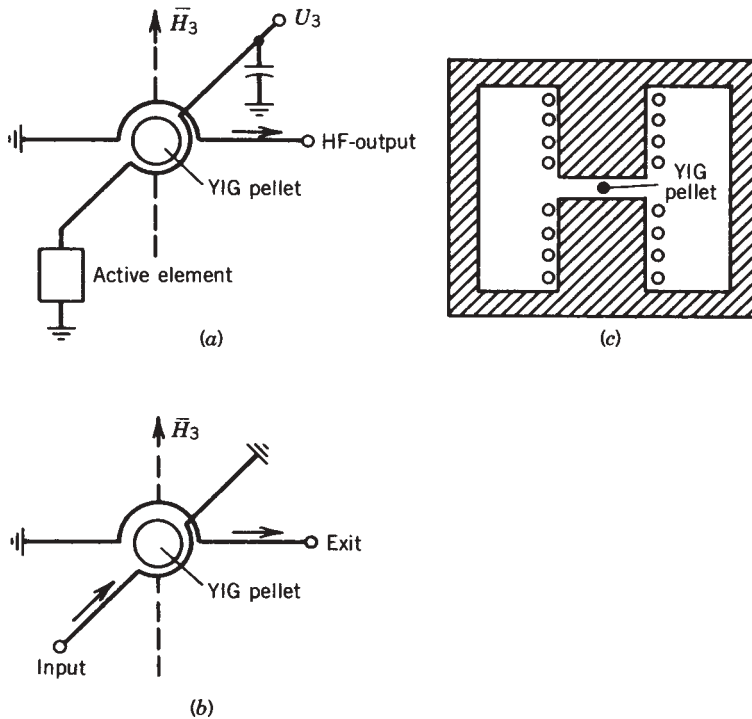
FIGURE F.26 (*a*) Diagram of a YIG band-pass filter; (*b*) YIG-tuned oscillator; (*c*) magnetic circuit for premagnetization.

by intensity of the magnetic bias field, and therefore, the element can be used to electrically tune oscillators and filters.

Reference: F.10, p. 212

Dielectric Resonator

$$Le = 1/\omega_0$$
$$Ce = 1/\omega_0$$
$$Re = a_0$$
k : turn ratio

(a)   (b)
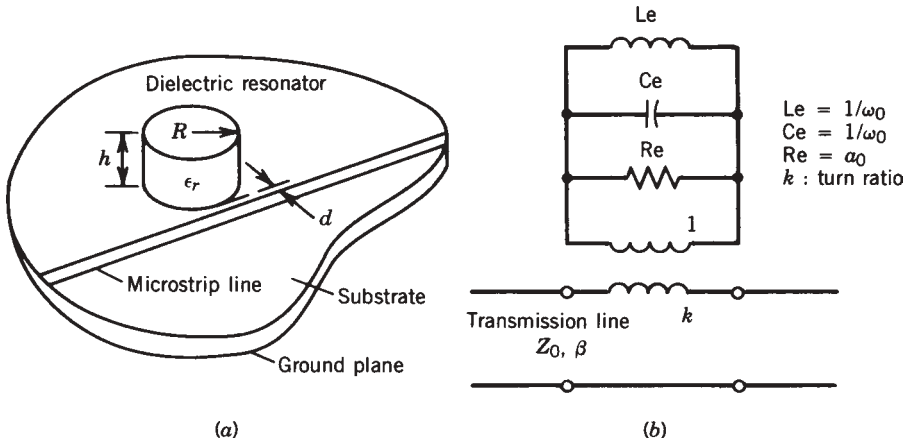
FIGURE F.27

Description: Dielectric resonators, offering high-Q cavity performance in microwave integrated circuits, are widely used in filter-stabilized oscillators, discriminators, and so on. In Fig. F.27, a dielectric resonator is placed beside the transmission line, and the equivalent circuit is shown.

Methods: Fundamental electromagnetic theory, other methods in reference book.

Reference: F.13

Gyrator
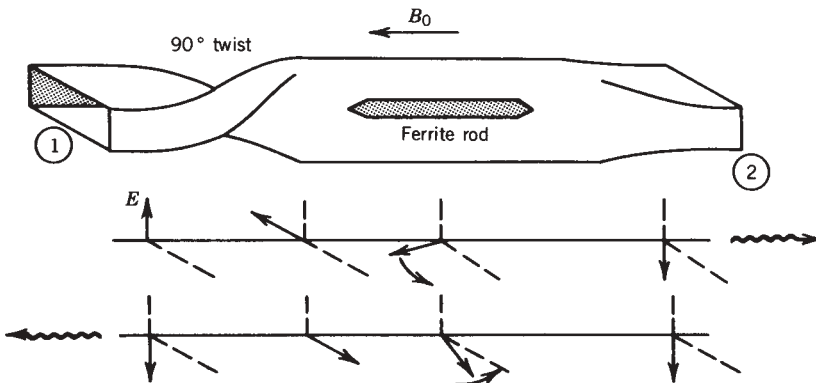
FIGURE F.28   A microwave gyrator.

Description: A gyrator is defined as a two-port device that has a relative difference in phase shift of 180° for transmission from port 1 to port 2 as compared with the phase shift for transmission from port 2 to port 1. *A gyrator may be obtained by employing the nonreciprocal property of Faraday rotation.* Figure D.28 illustrates a typical microwave gyrator. It consists of a rectangular guide with a 90° twist connected to a circular guide, which in turn is connected to another rectangular guide at the other end. The two rectangular guides have the same orientation at the input ports. The circular guide contains a thin cylindrical rod of ferrite with the ends tapered to reduce reflections. A static axial magnetic field is applied so as to produce 90° Faraday rotation of the TE_{11} dominant mode in the circular guide. Consider a wave propagating from left to right. In passing through the twist the plane of polarization is rotated by 90° in a counterclockwise direction. If the ferrite produces an additional 90° of rotation, the total angle of rotation will be 180°, as indicated in Fig. 6.28. For a wave propagating from right to left, the Faraday rotation is still 90° in the same sense. However, in passing through the twist, the next 90° of rotation is in a direction to cancel the Faraday rotation. Thus, for transmission from port 2 to port 1, there is no net rotation of the plane of polarization. The 180° rotation for transmission from port 1 to port 2 is equivalent to an additional 180° of phase shift since it reverses the polarization of the field. It is apparent, then, that the device just described satisfies the definition of a gyrator.

Reference: F.14, pp. 300–301

Circulator
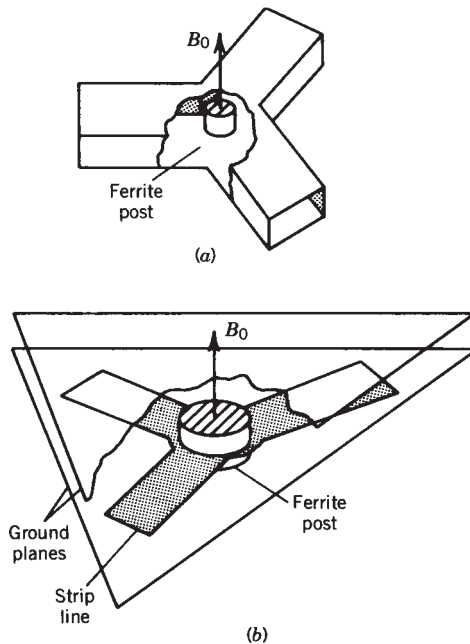
FIGURE F.29   Three-port circulators. (*a*) Waveguide version; (*b*) strip-line circulator.

Description: A circulator is a multiport device that has the property that a wave incident in port 1 is coupled into port 2 only, a wave incident in port 2 is coupled into port 3 only, and so on. The ideal circulator is also a matched device; that is, with all ports except one terminated in matched loads, the input impedance of the remaining port is equal to the characteristic impedance of its input line, and hence presents a matched load.

Reference: F.14, pp. 304–305

Isolator
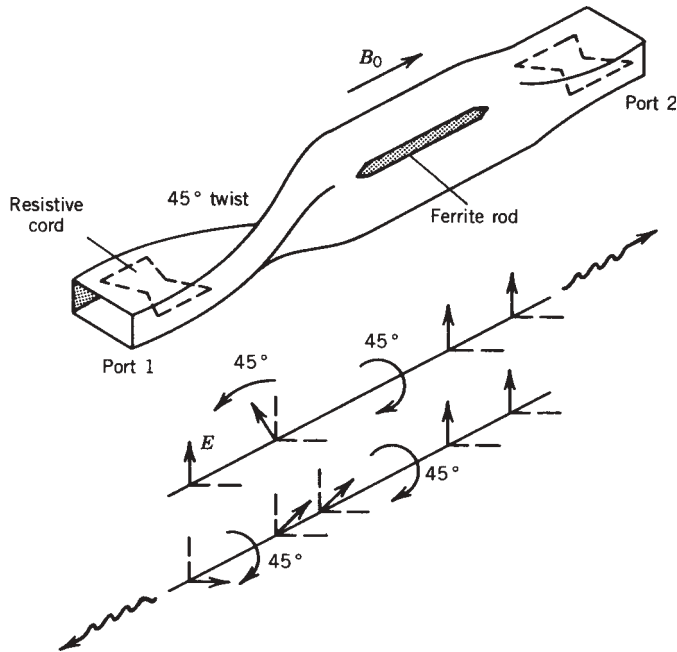
FIGURE F.30   A Faraday-rotation isolator.

Description: The isolator, or uniline, is a device that *permits unattenuated transmission from port 1 to port 2 but provides very high attenuation for transmission in the reverse direction.* The isolator is often used to couple a microwave signal generator to a load network. It has the great advantage that all the available power can be delivered to the load and yet reflections from the load do not get transmitted back to the generator output terminals. Consequently, the generator sees a matched load, and effects such as power output variation and frequency pulling (change in frequency), with variations in the load impedance, are avoided.

Reference: F.14, p. 301

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F.16   Ansoft Designer User Manual

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